J784S4X Evaluation Board

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Project : J7 EVM

TEXAS INSTRUMENTS

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Size: C | PROC141 001 J784S4XG01EVM | Rev: E4

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REVISION HISTORY #1

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	2.7	05 APR 2022	Updates shared by TI for REV E2 is done Fix for VSYS_IO_1V8 rail is updated	Mistral Design Team		
	2.8	20 APR 2022	Updated PDN SCH notes (purple font) on pgs: 26-28, 30-33, 79, 80 Updated SoC Analog SCH pg 26 filtering component values	TI		
	2.9	21 APR 2022	Updated PMIC SCH pg 30 format & power inductor values optmzd for Fsw = 4.4MHz per IPM sim results Ref clock for PCIe x2L set to SOC clock by default	Mistral Design Team		
	3.0	26 APR 2022	Updated for PCIe ref clock connection DNI'd termination for QSGMII ref clock Minor PDN SCH pg updates	Mistral Design Team		
	3.1	27 APR 2022	Updated resistor R1292 and R1293	Mistral Design Team		
E2A	3.2	20 JUN 2022	Added note for updated VCC_12V0 Enable supply DNI'd U29 and U159 (I2C buffers connected to XDS) to avoid leakage on VCC3V3_XDS Updated "EVM Bd Setting & Leo NVM Default" Table	Mistral Design Team		
	3.3	30 JUN 2022	DNI'd resistors R659 and R1122 DNI'd U29 and U159 (I2C buffers connected to XDS) to avoid leakage on VCC3V3_XDS	Mistral Design Team		
E3	3.4	06 JUL 2022	Updated sedres0 and serdes1 reference clock Changed R617 and R700 to 3k Changed VCC_12V0 enable to VSYS_3V3 Changed SW2 pin 8 pull up supply to VSYS_3V3	Mistral Design Team		
	3.5	12 JUL 2022	Updated VMON supplies connected to the SVS A and B as per PDN ver0.14d Updated sedres0 and serdes1 reference clock resistor option	Mistral Design Team		
	3.6	13 JUL 2022	Netname updated to XDS110_BUF_SELn Removed capacitor C748,C757 Updated I2C buffers used for PM_I2C connected to XDS110 to SN74CB3Q312 Provided ressitor option for VCC_12V0 buck enable supply. Enable from VSYS_IO_3V3 by default	Mistral Design Team		
	3.7	19 JUL 2022	Updated for TI review comments Changed TP166 and TP177 to TP20_SMD	Mistral Design Team		
	3.8	20 JUL 2022	Updated for TI review comments	Mistral Design Team		
	3.9	21 JUL 2022	Updated SVS part number to PPS389006004NRTERQ1	Mistral Design Team		
	4.0	26 JUL 2022	Updated PDN Updated VDD_SD_DV Enable logic DNI'd R271 and R1063	Mistral Design Team		
	4.1	29 JUL 2022	DNI'd reserved current monitors for CORE,CPU_AVS and DDR rails	Mistral Design Team		
	4.2	1 AUG 2022	DNI'd SVS monitor IC's U87 and U89	Mistral Design Team		
	4.3	9 AUG 2022	INA231 IC's are made as populate and INA226 IC's as DNI	Mistral Design Team		
	4.4	12 AUG 2022	DNI'd resistor R752 Added thermal accessories to schematic hardware page	Mistral Design Team		
	4.5	12 SEP 2022	Few SoC deCaps were replaced with GCM Series murata caps 16GB eMMC is replaced with 32GB part with MFR# MTFC32GAZAQHD-AAT C1042, C901, C1018 were replaced with 4.7uF,4V,0402 cap(GCM155D70G475ME36)	Mistral Design Team		
E4	4.6	09 NOV 2022	Replaced FL194 and FL151 with BLM31KN121SN1(4A @ 125C, Zpk = 120ohm @ 100MHz) to reduce the IR drop<1%. Enable to VDD_DDR_1V8 is derived from discrete fet and logic Added 6x new 100uF, 1210 caps on VDD_CPU Added 9x new 100uF, 1210 caps on VDD_CORE	Mistral Design Team	TI	TI

REVISION HISTORY #2

Project :		Title: REVISION HISTORY	
J7 EVM	TEXAS INSTRUMENTS	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
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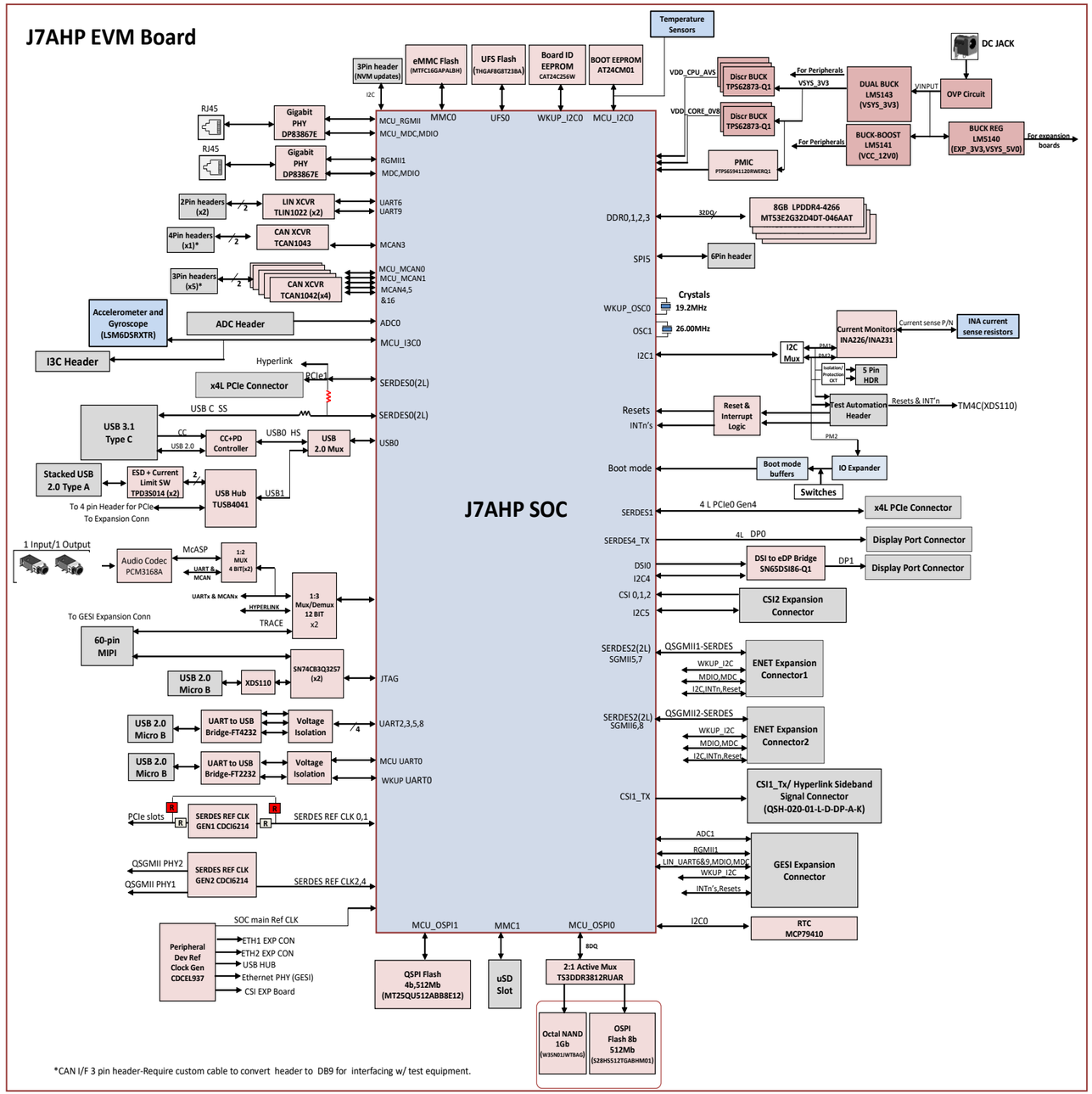
BLOCK DIAGRAM



Project : J7 EVM	TEXAS INSTRUMENTS	Title: BLOCK DIAGRAM
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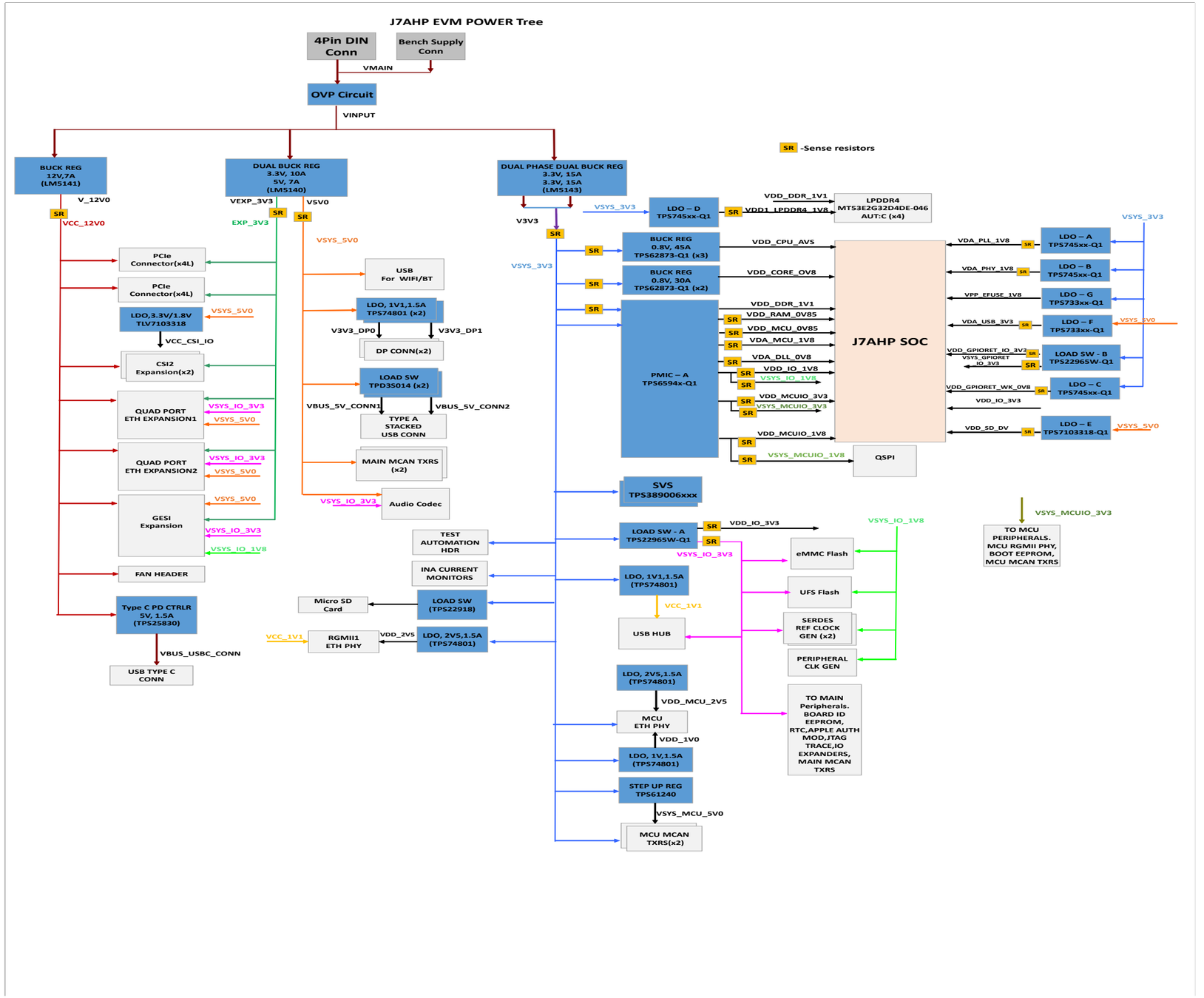
POWER FLOW DIAGRAM



Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER FLOW DIAGRAM
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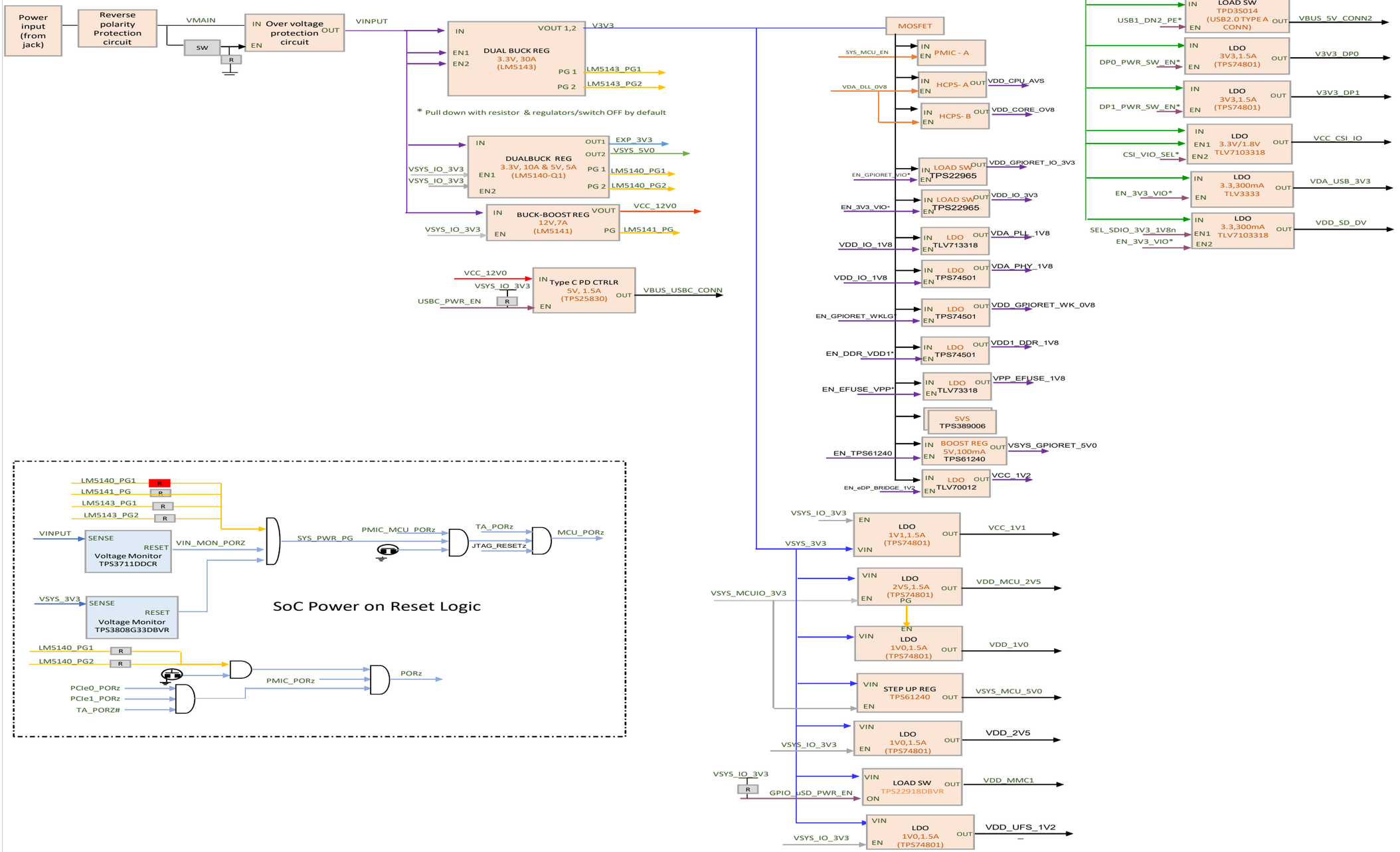
POWER SEQUENCE

J7AHP EVM Board Power Sequencing



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PDN

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 13)
HCPS-A & B, Tulip PN TPS628731Y1QWRKSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

V0.14c 6/23/2022	1. Shuffled supply rail connections to SVS-A & -B to align voltage levels to same MGMN inputs for potentially defining 1x SVS PN for -A & -B
V0.14d 6/30/2022	2. Show PG outputs from discrete bucks & LDOs as optional signals not required since SVS-A & SVS-B are providing VMON OV/UV coverage. 3. Added existing MCU power rails sourced from PMIC that have desired voltage levels to satisfy "unused" SVS-B VMGN inputs to enable 1x common PN for SVS-A & -B while avoiding false positives on MCU_PWRERP_IRQn.
V0.15 7/25/2022	4. Updated SVS-A & -B to show new common PN for use with Jacinto7 J784S4 PDN-3A scheme as shown below. Following PDN diag & PMIC NVM setting updates are needed as a result of power up & downseq bench testing: 1. PMIC NVM settings for GPIOS will need to revert from Open-Drain to Push-Pull buffer type to correctly control signaling. This works since the EN_GPIO_RETx pin (sourced from GPIOS) only interfaces to 2x low voltage FETs with Vth ~1.0 2. Add "AND" gate to control disabling of dual output LDO supplying VDD_SD_VIO. This will disable VDD_SD_DV voltage whenever EN_3V3_VIO is low as needed to remove power during low power modes (MCU Only, DDR_RET & GPIO_RET).
V0.16 7/28/2022	1. Replaced discrete "OR Gate" FET logic circuitry with 1x 8ft Configurable Multi-Function gates in 4x places
V0.17 9/2/2022	1. Update Note #9 to clarify open-drain interface is needed for automotive grade, single channel voltage translator. 2. Added "Modular PDNs support Flexible Feature Sets" table for reference 3. Removed net "H_MAIN_WKIN" connected to SoC output "PMIC_WAKEOn" since it's only needed if Main GPIO Retention low power mode is used. 4. Connect PU RonSEL_SOIO_3V3_1V8 signal to VDD_IO_3V3 supply instead of VCCA_3V3 to avoid current bleed into SOC GPIO during power up seq. A

Legend:

Power Rails (Power Rail Name)
PDN base
MCU Only/Safety Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)

Control Signals: (signals)
General cntrl & logic
(italic = SW config'd after boot)
PDN base cntrl
Func Safety
MCU Only Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option

(A) Note items
(PG) On-Chip "Pwr OK" Monitors (OV & UV)
(PGuv) On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter
High-lighted diagram changes

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FRI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:
   a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal min)
   b. MCU GPIO Retention (needs 2 indep pwr rails & 1 cntrl signals min)
   c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal min)
7. End Product Options:
   a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
   b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
   c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

Notes:
1) Functional Safety requires monitoring all "safety-critical" power rails (i.e. VSYS_3V3 input, key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VExTxxx) can be used to extend SoC's OV/UV monitoring to a live board level power rails if desired (i.e. load switch Vin = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SDCard), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) Load switches (ldsw) have been used to create VDD_MCUIO_3V3 VDD_GPIORET_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
   C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
   D) Connecting VCCA_3V3 directly to SoC 3.3V supplies is not recommended since this will leave SoC partially energized for an extent time that can negatively impact FGH reliability.

3) PMIC's GPIO_8 has been provisioned to support multiple interface signals. The PMIC PN default function sets GPIO_8 = DISABLE_WDOG function following NVM initialization. This GPIO's default function can be reassigned by system sw following SoC boot if another interface signal is needed that is not required for SoC power sequencing.
   1. Default: GPIO_8 = DISABLE_WDOG function to operate with EVM's DISABLE_WDOG signal that is latched on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq. A logic low enables normal watchdog timer operation while a logic high disables watch dog timer following a power up seq.
   2. Option1: After system SW boots, SW can reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQ/_IRQn (asserted high or low) signal. System SW must mask GPIO8 before changing GPIO8's assigned function. After selecting GPI function, SW must unmask GPI input and select whether the GPI will be either rising or falling edge sensitive. If any Main domain processing supply rail has a fault, the changing logic level on GPIO8 will set internal register bit that is monitored by PMIC's power state machine and cause a transition from Full Active state to MCU Safe state. At the board level, the WDOG_DISABLE & MAIN_PWRGRP_RGn signals are "time mux'd" onto GPIO8's input pin by using a tristate buffer with OE control connected to H_MCU_PORz_1V8. This enables WDOG_DISABLE net to set GPIO8's logic level during power up seq when H_MCU_PORz_1V8 = low since buffer is tri-stated. After power up seq, H_MCU_PORz_1V8 = high enabling buffer to drives MAIN_PWRGRP_RGn logic level into GPIO8 input.
   3. Option2: GPIO_8 = WKUP1 function can be selected by SW to operate with SoC's PMIC_PWR_ENI signal for emulator debug control of PMIC power resources (i.e. enabling VDD_CORE to activate core logic required to support JTAG signaling across the device). Combining board level WDOG_DISABLE & PMIC_POWER_ENI signals using a resistor network is possible since WDOG_DISABLE pulls logic level high when switch is closed. Afterwards, switch can be opened and PMIC_PWR_ENI signal will drive GPIO_8.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wells) low power mode requires:
   A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_GPIORET_VA_0v8 supplying MCU1 VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
      2. VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
   C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1 in (= SoC's Open-Drain PMIC_WAKE1 active low) signal connected to PMIC_GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
   D) The Open-Drain Buffer SN74LVC1G07DBVJ tri-states IO when power is OFF) connects PMIC_WAKE1 in to SOC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.

5) DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
   A) PMIC PN to assign GPIO_6 = Regulator Enable (RSEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
   B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
      2. VDD1_DDR_1V8 supplying SDRAM only
   D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.

6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, the non-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

9) A discrete FET with low VGS (EVM uses industrial temp grade FET for low Vth) or single channel, voltage translation IC (automotive Q1 grade) can support low Vth needed to ensure a logic high level output will result with an input min 0.76V (-5% supply to I). If using SN74AXC1T45-Q1, please add a discrete FETs for an open-drain interface needed to interface with "MAIN_PWRGRP_IRQn" net.
   Examples shown below:
   EVM Discrete FETs w/ low Vth
   Auto Q1, Single Ch, Voltage Translator w/ FETs for open-drain interface

10) Worst case analysis for very high thermal use cases could result in VCCA_3V3 load current in 15-18A range. This large load current range could lead to a 60~72mV voltage drop across Safety FET (Recmd PN: NVMFS4C05N) for max RDSon = 4mohm. The TPS22965-Q1 load switches have max RDSon = 27 mohm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDSon drops across Safety FET & Load Switches range from 168 ~ 330mV which exceed SoC's min voltage limit. For this reason, the Tulip buck input voltage will be moved from VCCA_3V3 to VSYS_3V3 since VDD_CPU_AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3V3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONs. If a end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDSW-B & SVS-B. Group the SoC input supplies according to be "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

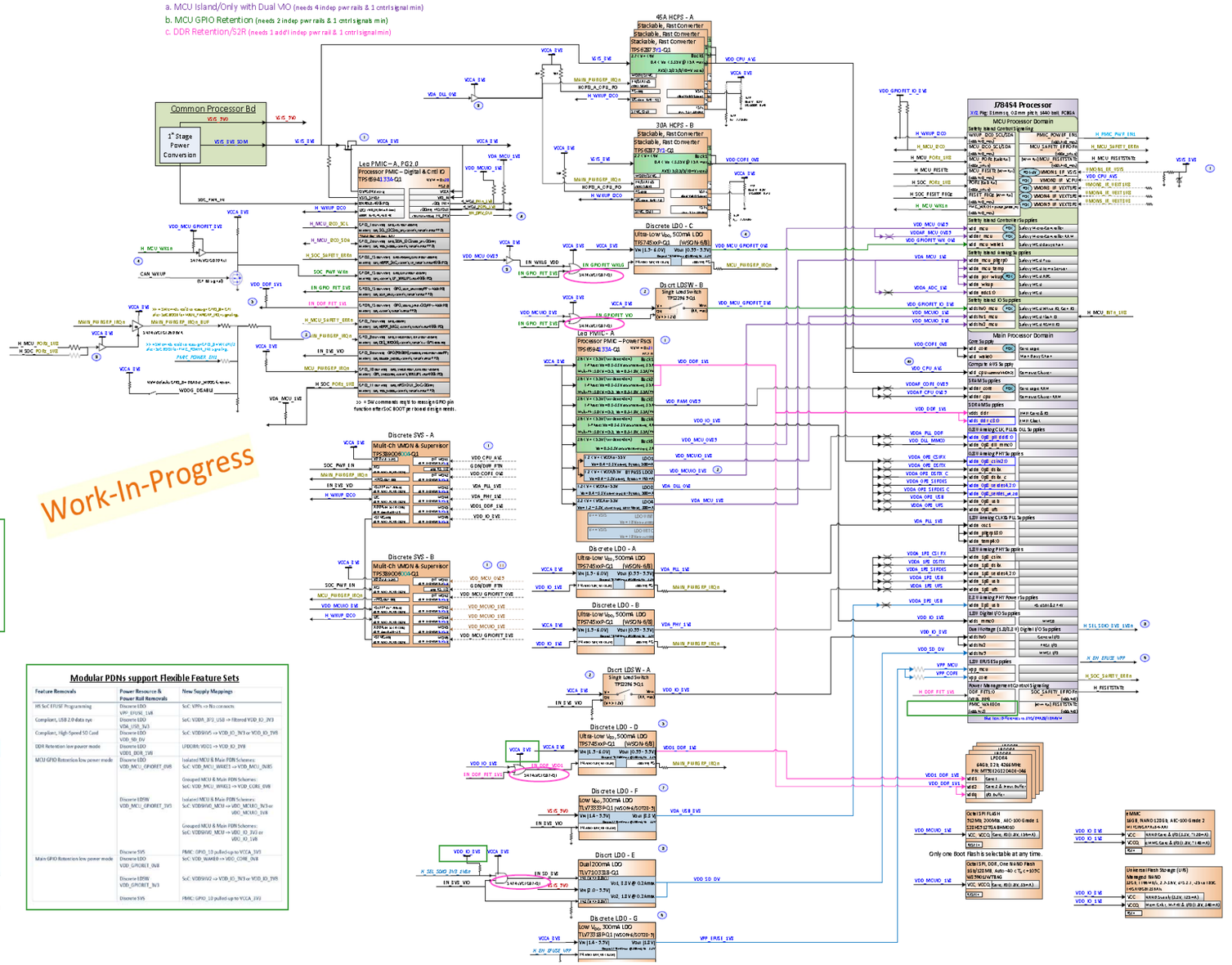
PDN Features	Isolated MCU & Main PDN Power Rails								
	VDD_MCU_0V85	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0V8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu vddar_mcu vdd_mca_wake1	vdd_core vddshv2_mcu	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_wake0	vddshv0_mcu
DDR Retention	vdd_mcu vddar_mcu vdd_mca_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mca_wake1 vdd_wake0	vddshv0_mcu vddshv2
GPIO Retention-MCU	vdd_mcu vddar_mcu	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mca_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu vddar_mcu vdd_mca_wake1	vdd_core	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_wake0	vddshv2

Notes:
1) Power rail names shown in "ALL CAPITAL LETTERS"
2) SoC input supplies shown in "all lower case letters"

Modular PDNs support Flexible Feature Sets

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC VPPn => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => Filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_3V3
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8	Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_0V8
	Discrete LDSW VDD_MCU_GPIORET_3V3	Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8	SoC: VDD_WAKE0 => VDD_CORE_0V8
	Discrete LDSW VDD_GPIORET_3V3	SoC: VDDSHV0/2 => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled up to VCCA_3V3

Work-In-Progress



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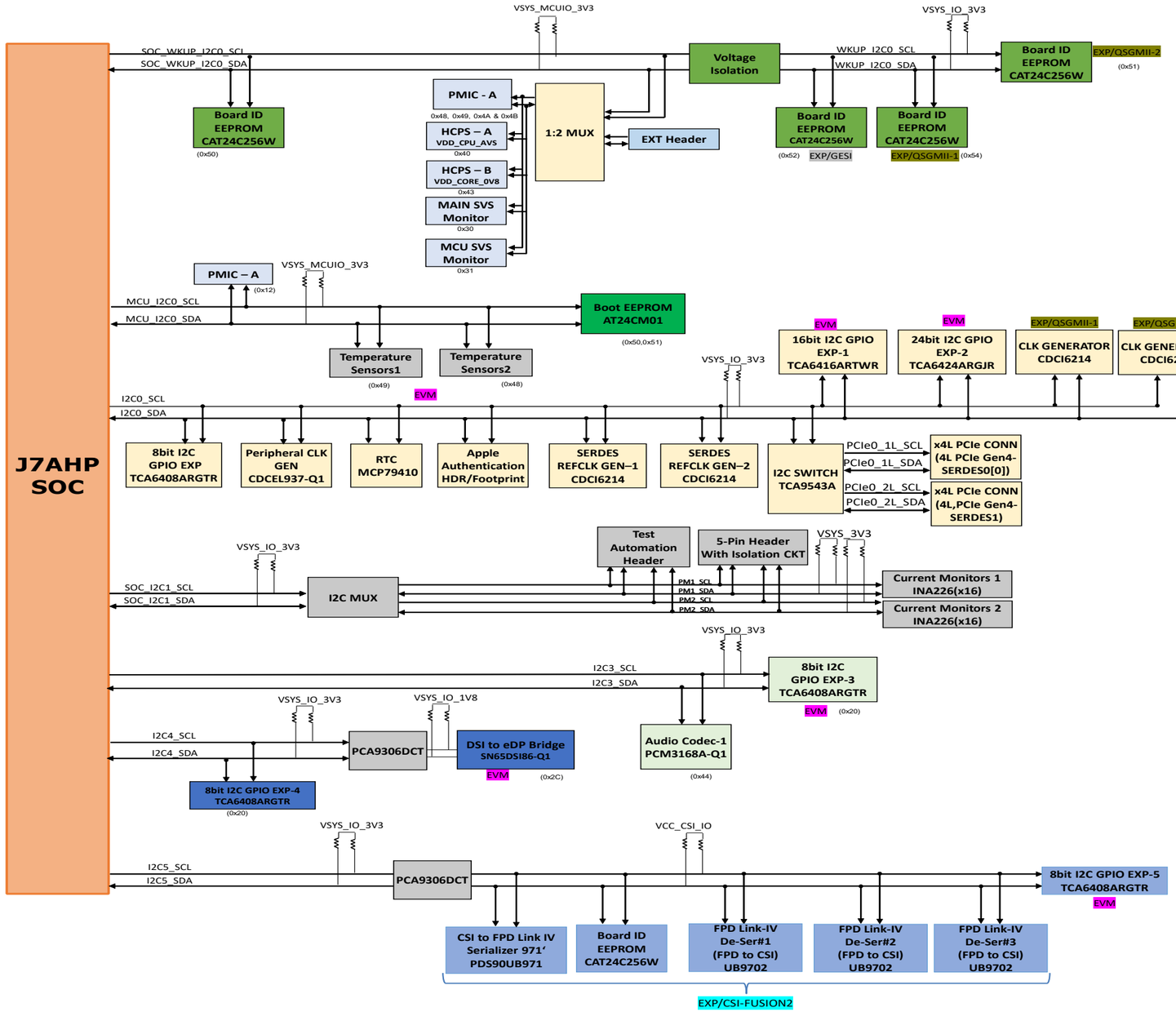
TEXAS INSTRUMENTS

I2C TREE



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I2C TABLE

Board	Interface name	Part#	Address	J7AHP Port mapping
EVM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0x54	
EXP/QSGMII -2	Board ID EEPROM	CAT24C256WI-GT3	0x51	
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EVM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
EVM	Tulip - VDD_CPU_AVS Regulator	TPS62873	0x40	
EVM	Tulip - VDD_CORE_0V8 Regulator	TPS62873	0X43	
EVM	MAIN SVS Monitor	PPS38900603NRTERQ1	0X30	
EVM	MCU SVS Monitor	PPS38900603NRTERQ1	0X31	
EVM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0
EVM	Boot EEPROM	AT24CM01	0x50, 0x51	
EVM	I2C Switch for PCIe	TCA9543APWR	0x70	Main I2C0
EVM	RTC Clock	MCP79410-I/SN	0x57,0x6F	
EVM	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM	16bit I2C GPIO EXPANDER1	TCA6424ARGJR	0x20	
EVM	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	
EVM	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	Main I2C4
EVM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM	DSI FPC Connector	<connector interface>		
EVM	I2C Switch for Automation header		0x22	Main I2C1
EVM	Current Monitors and Header		0x40 to 0x4F	
EVM	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP	8bit GPIO Expander5	TCA6408ARGTR	0x20	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x32	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	

GPIO EXPANDER MAP/TABLE

J7AHP EVM - GPIO Mapping Table						
WKUP Domain						
Net name	**J7AHP Mapping**					
	Package Signal Name	**GPIO Number**	**Input/Output**	**Default**	**State**	**Remarks**
EN_EFUSE_VPP	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active High	VPP_EFUSE LDO enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot EEPROM Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU CAN1 Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>1' - interrupt pending, '1' - normal operation)
OSPI/HYPER_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSPI1_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU CAN0 Standby
LSM6DSOX_INT/LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interupt from I3C Gyroscope sensor(*LSM6DSRX)
PM_I2C_SEL	WKUP_GPIO0_66	WKUP_GPIO0_66	Output	BOOTMODE	Active High	PM I2C Mux seletion. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA)
USBC_DIR_SOC	MCU_OSPI0_CSN1	WKUP_GPIO0_28	Input	PU	Active High	USB C direction pin
ENET1_EXP_INTB	MCU_ADC1_AIN5	WKUP_GPIO0_84	Output	PU	Active low	ENET expansion 1 Interrupt signal
ENET2_EXP_INTB	MCU_ADC1_AIN6	WKUP_GPIO0_85	Output	PU	Active Low	ENET expansion 2 Interrupt signal
I2C0_IOEXP_INT#	MCU_ADC1_AIN7	WKUP_GPIO0_86	Output	PU	Active Low	I2C0 IO expander interrupt signal
CANIO_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
MAIN_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
HYP1_RXFLCLK_MUX	MCASP0_AXR2	GPIO0_18	Input	PU	Active Low	I2C5 IO expander interrupt. Muxed with trace and Hyperlink signals
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	NA	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
CSI2_EXP_A_GPIO2(MCASP4_AXR1/TRC_DATA16_MUX)	MCAN0_RX	GPIO0_26	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
CSI2_EXP_A_GPIO4(MCASP4_AXR3/TRC_DATA5_MUX)	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
TRC_DATA0_MUX	MCAN13_TX	GPIO0_3	Input	PU	NA	Interrupt signal from DSI to eDP bridge
SOC_GPIO0_21_MUX	MCASP2_ACLKX	GPIO0_21	Input	PU	Active Low	RGMII1 INT signal
GPIO Expander - 1 Part# TCA6424ARGJR						
I2C0/0x20	P00	PCIe1_2L_MODE_SEL	Input	DIP_SEL	NA	PCIe1 4-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCIe1_4L_PERSTz	Input	PD	Active low	PCIe1 4-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCIe1_2L_RC_RSTz	Output	PD	Active low	PCIe1 4-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCIe1_2L_EP_RST_EN	Output	PD	Active low	PCIe1 4-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCIe0_4L_MODE_SEL	Input	DIP_SEL	NA	PCIe0 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCIe0_4L_PERSTz	Input	PD	Active low	PCIe0 2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCIe0_4L_RC_RSTz	Output	PD	Active low	PCIe0 2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCIe0_4L_EP_RST_EN	Output	PD	Active low	PCIe0 2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCIe1_4L_PRSNT#	Input	PU	Active High	PCIE1 4-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P11	PCIe0_4L_PRSNT#	Input	PU	Active High	PCIE0 2-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P12	CDCI1_OE1/OE4	Output	PU	Active High	PCIE 2L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P13	CDCI1_OE2/OE3	Output	PU	Active High	PCIE 1L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P14	AUDIO_MUX_SEL	Output	PU	Active High	Mux select for McASP and trace signals
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL0
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL1
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part# TCA6424ARGJR						
I2C0/0x22	P00	R_GPIO_RGMII1_RST	Output	PU	Active low	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII_RST; INFO - Not used
	P01	ENET2_I2CMUX_SEL	Output	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select USBC_MODE_SEL[1:0]: '00' = DFP, '01' = DRP, '1x' = UFP
	P05	USBC_MODE_SEL0	Output	DIP_SEL	NA	
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	R_CAN_STB	Output	PU	Active High	Standby signals for On BOARD and GESI CAN Transceiver
	P10	CTRL_PM_I2C_OE#	Output	PD	Active High	Gate drive for enable signal of PM I2C mux select
	P11	ENET2_EXP_PWRDN	Output	PU	Active low	Ethernet Expansion2 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P12	ENET2_EXP_SPARE2	Input	NA	NA	Ethernet Expansion2 Spare2 ('0' - not defined, '1' - not defined)
	P13	CDCI2_RSTZ	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P14	USB2.0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USBC, '1' - USB Hub)
	P15	CANUART_MUX_SEL0	Output	PD	Active High	Select line forboth the CANUART MUX
	P16	CANUART_MUX2_SEL1	Output	PU	Active High	Select line for CANUART MUX2
	P17	CANUART_MUX1_SEL1	Output	PU	Active High	Select line for CANUART MUX1
	P20	ENET1_EXP_PWRDN	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET1_EXP_RESETZ	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
	P22	ENET1_I2CMUX_SEL	Input	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P23	ENET1_EXP_SPARE2	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	P24	ENET2_EXP_RESETz	Output	PD	Active low	Ethernet Expansion2 Reset ('0' - device reset, '1' - normal operation)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
GPIO Expander - 4 Part# TCA6408ARGTR						
I2C40x20	P0	DP0_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	GPIO_eDP_ENABLE	Output		Active High	DSI to eDP bridge enable
GPIO Expander - 5 Part# TCA6408ARGTR						
I2C5/0x20	P0	CSI2_EXP_RSTZ	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2 Expansion Board Specific.
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2 Expansion Board Specific.
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2 Expansion Board Specific.

Project : J7 EVM

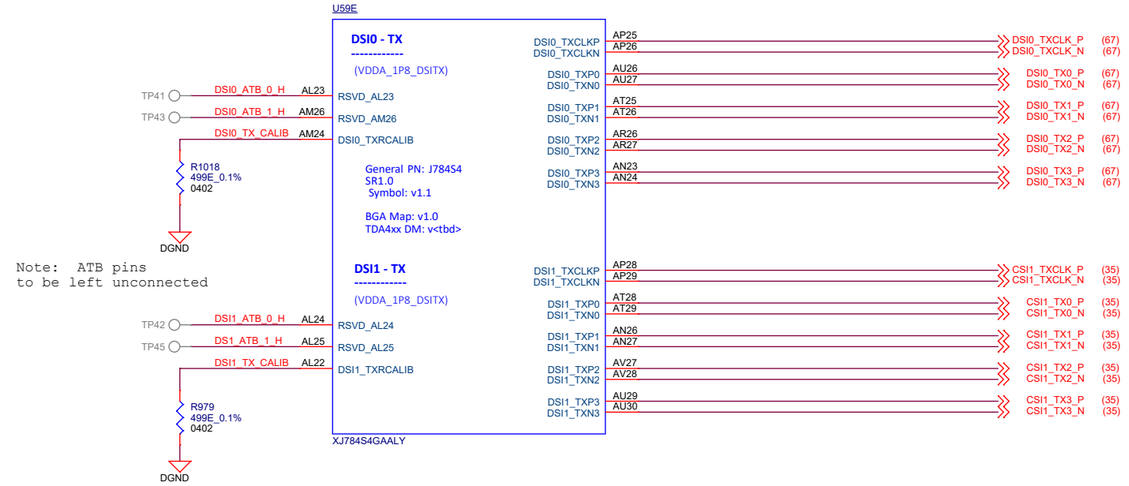
TEXAS INSTRUMENTS

Title: GPIO EXPANDER MAP/TABLE

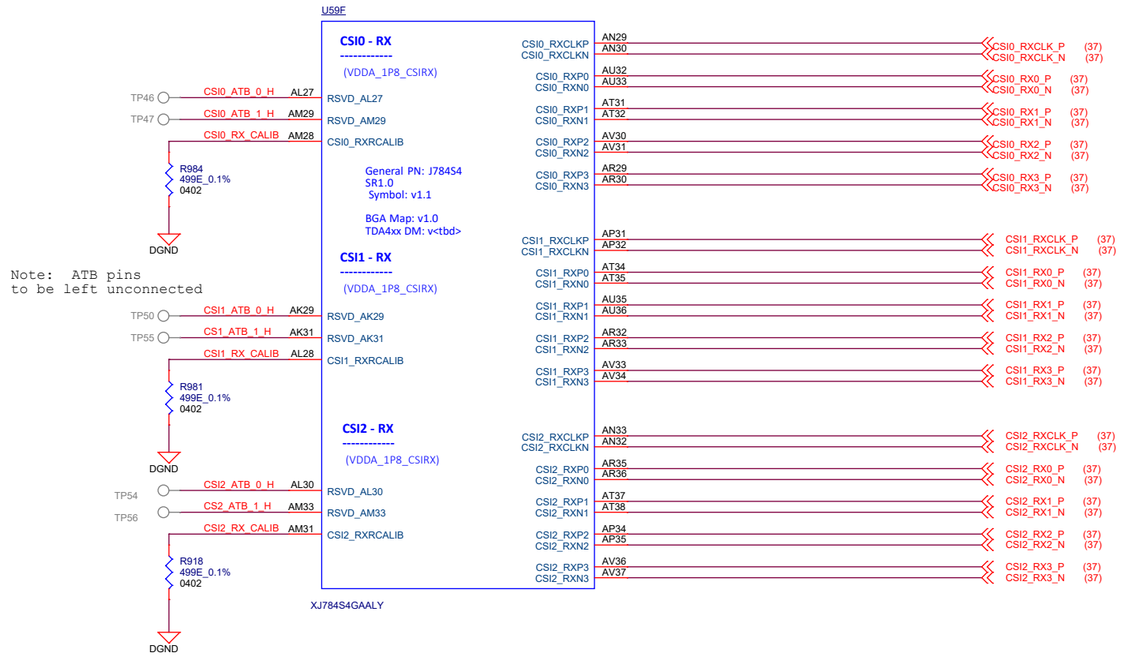
Size: C | PROC141 001 J784S4XG01EVM | Rev: E4

Date: Thursday, November 10, 2022 | Sheet 10 of 88

DSI

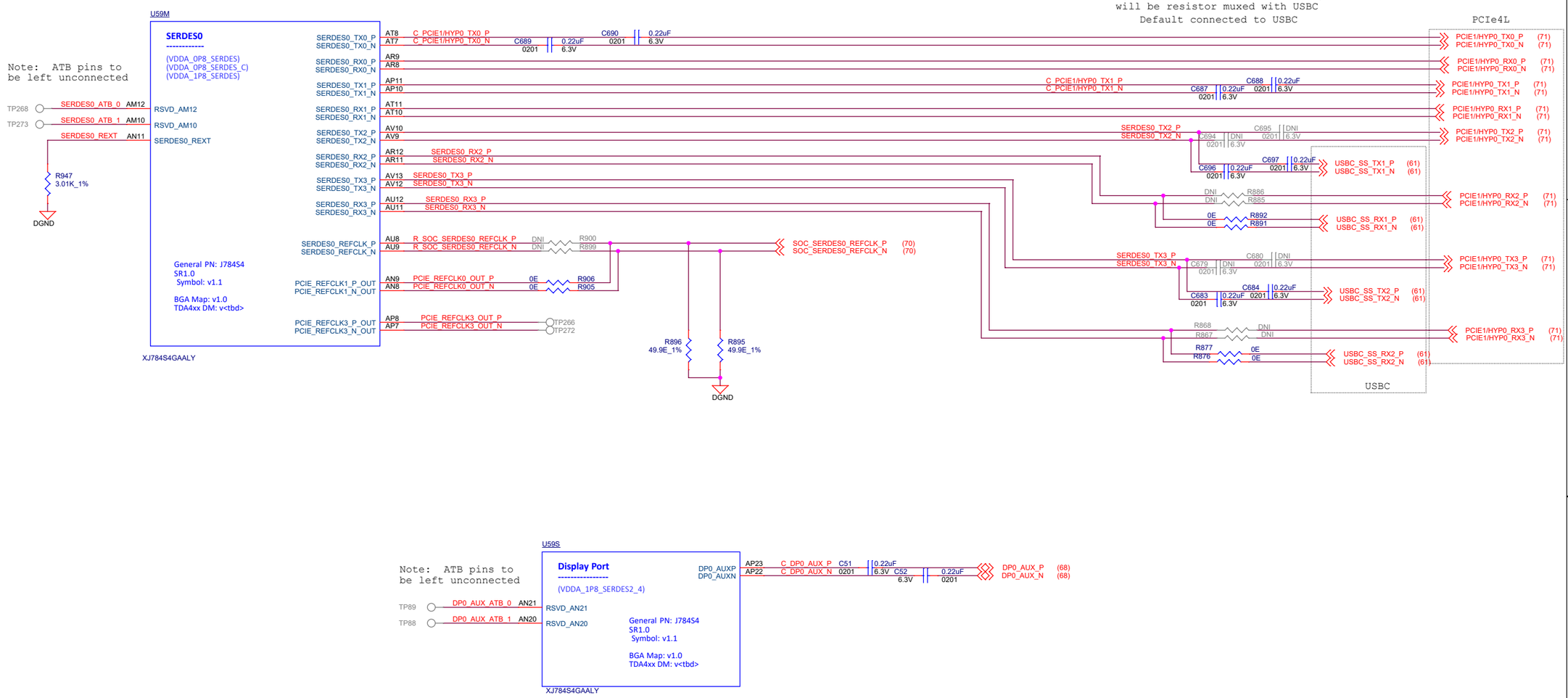


CSI



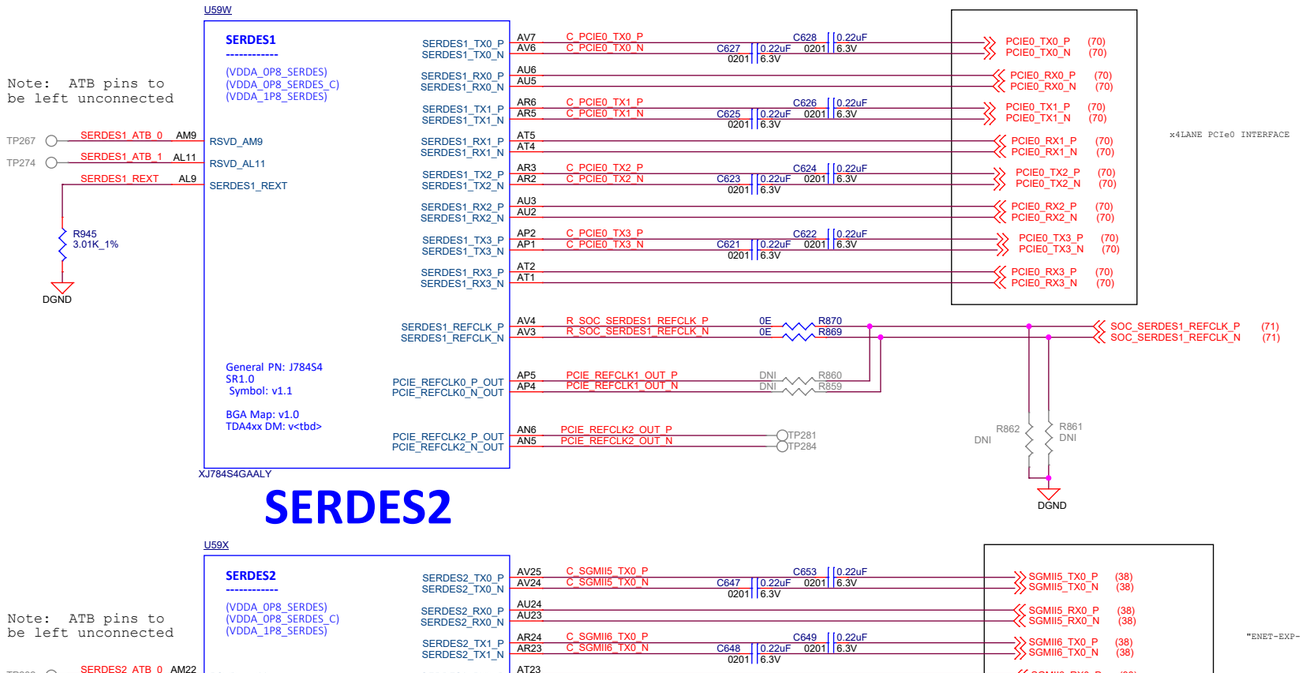
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CSI & DSI INTERFACE
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 11 of 88

SERDES0



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES INTERFACE
	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 12 of 88

SERDES1



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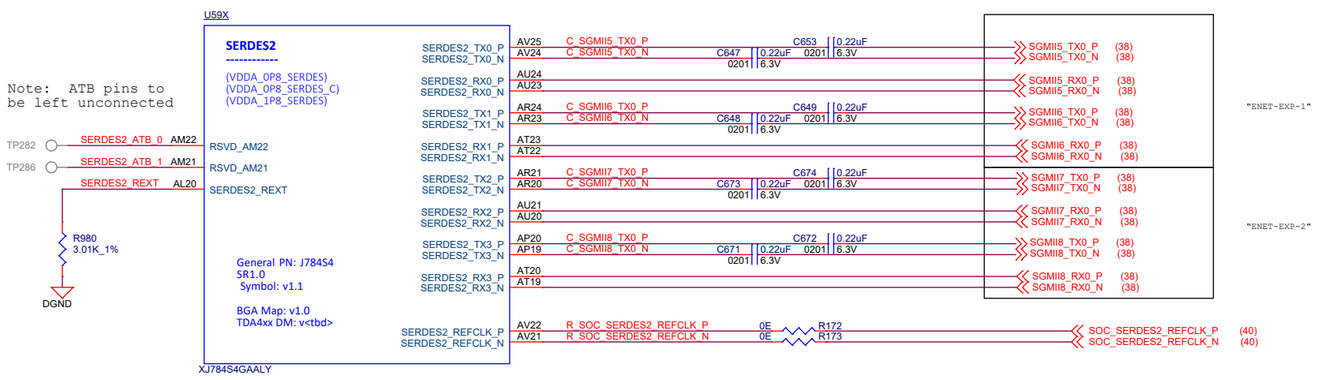

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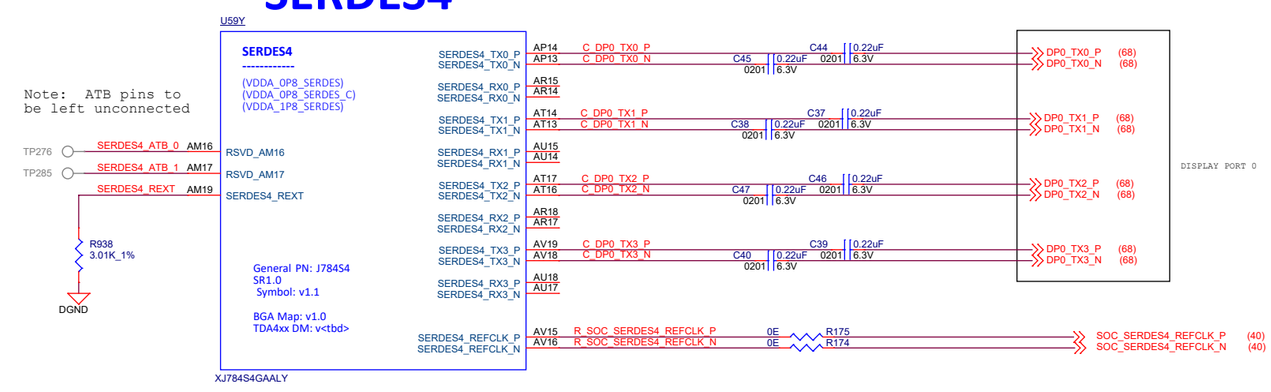
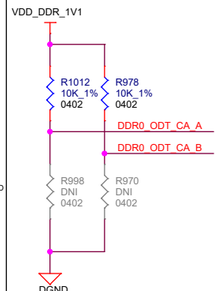
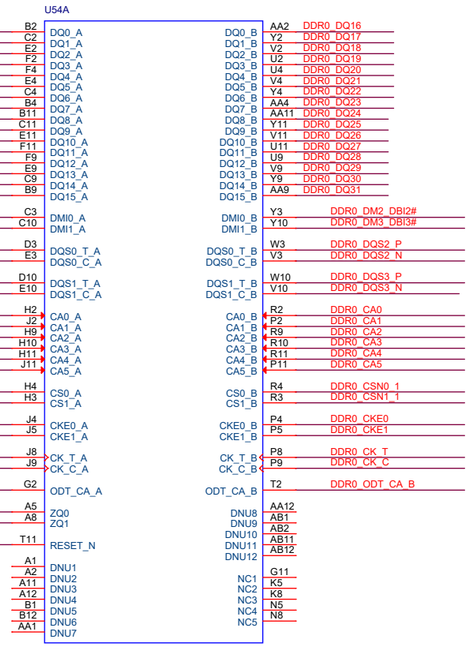
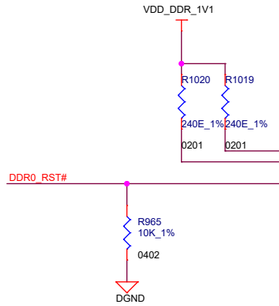


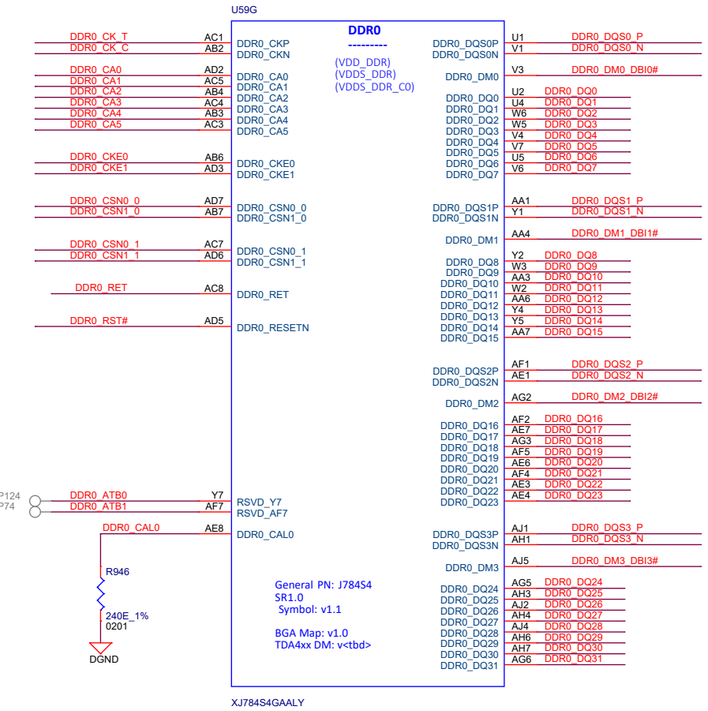
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES INTERFACE
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 13 of 88

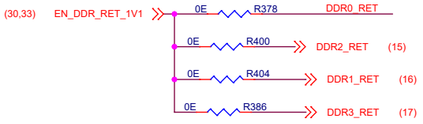
LPDDR4

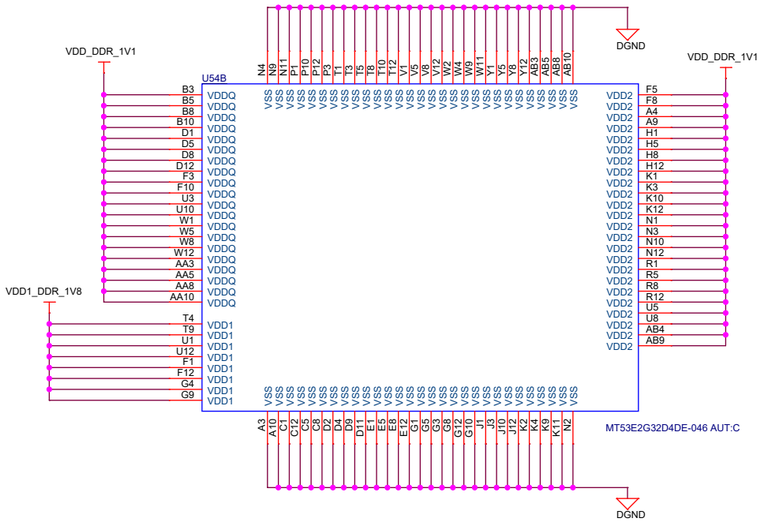


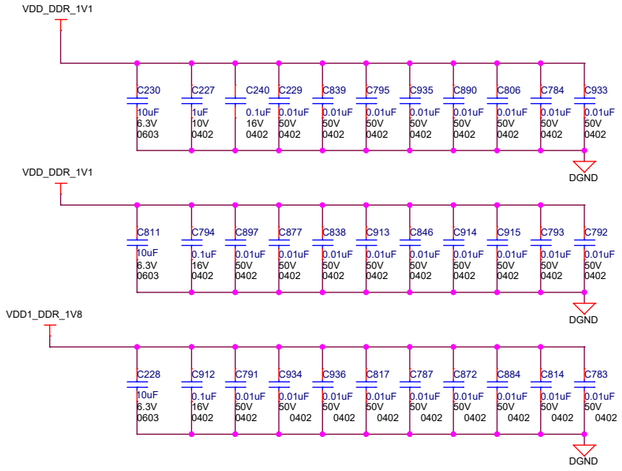






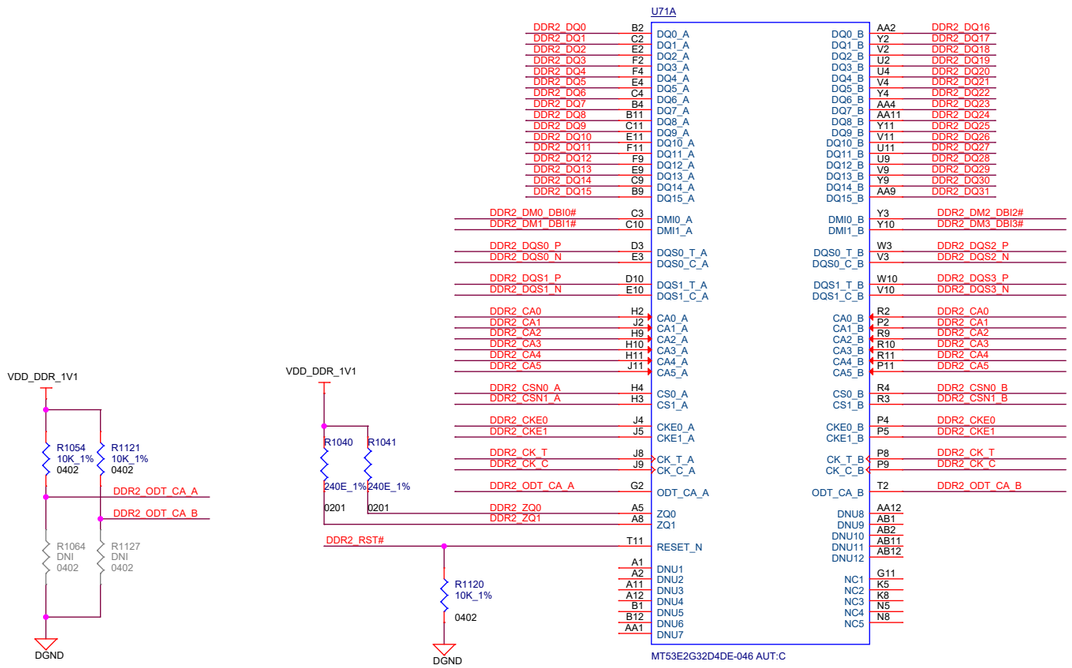


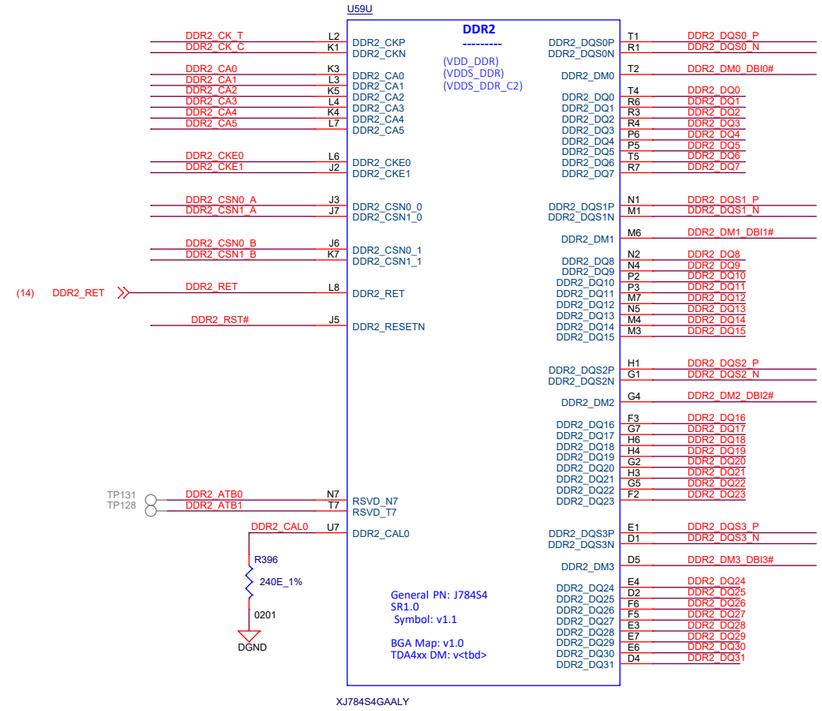


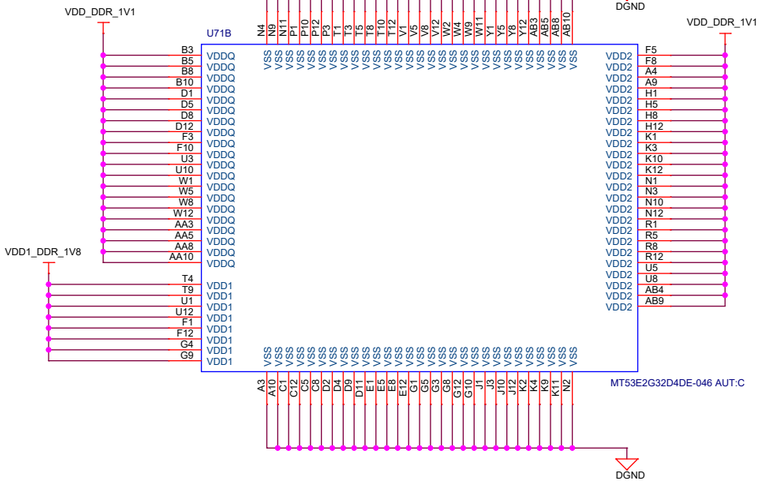


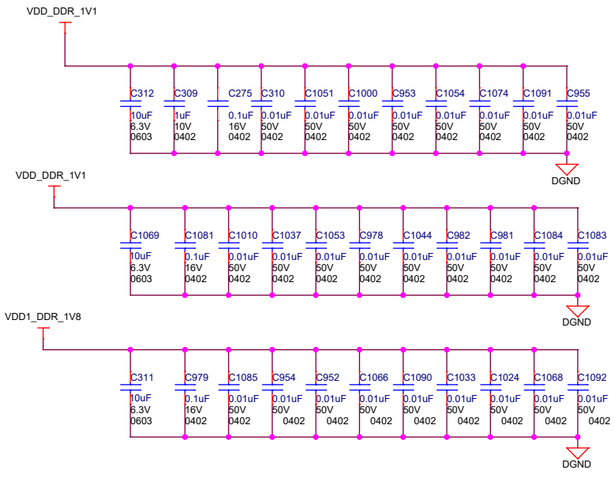
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EMIF0
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 14 of 88

LPDDR4



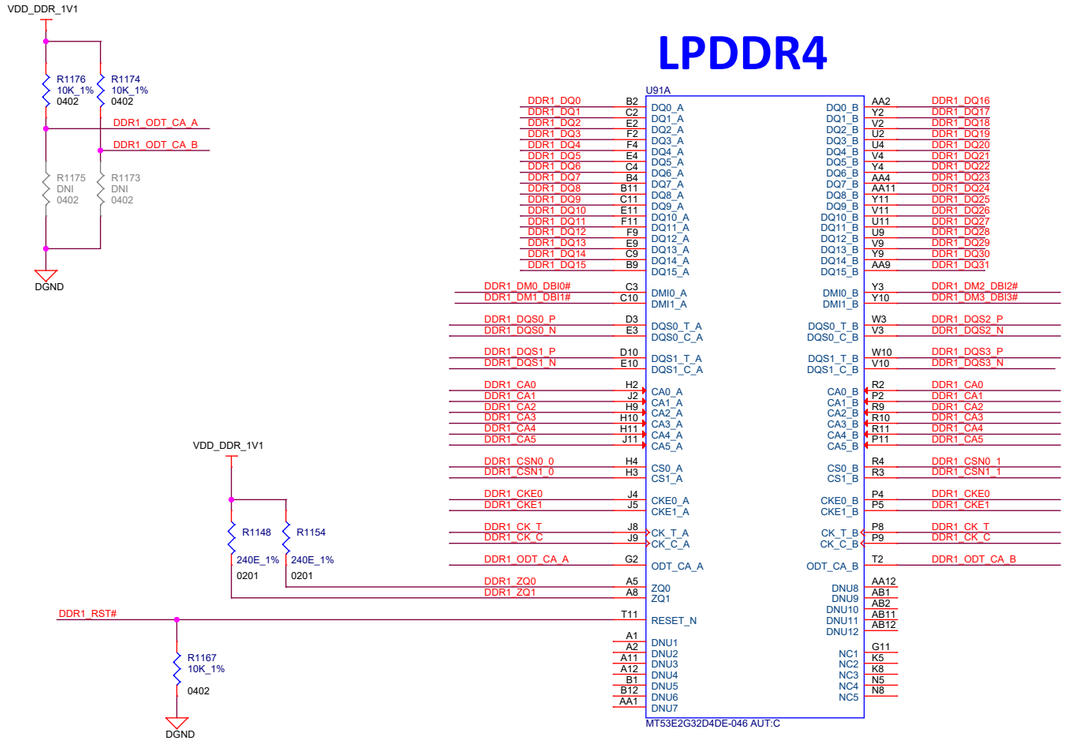


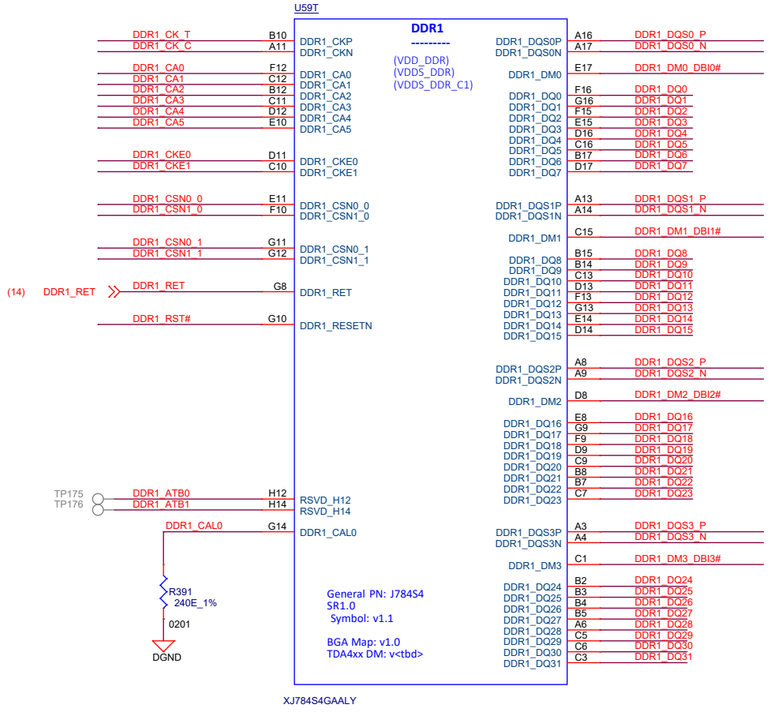




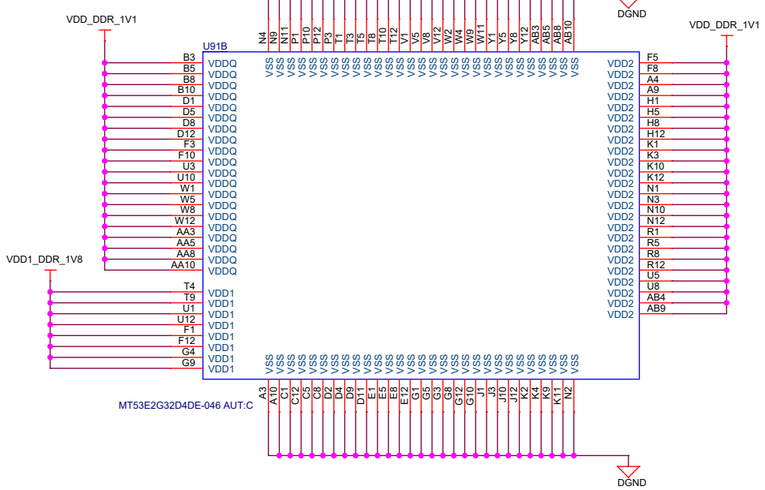
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EMIF2
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 15 of 88

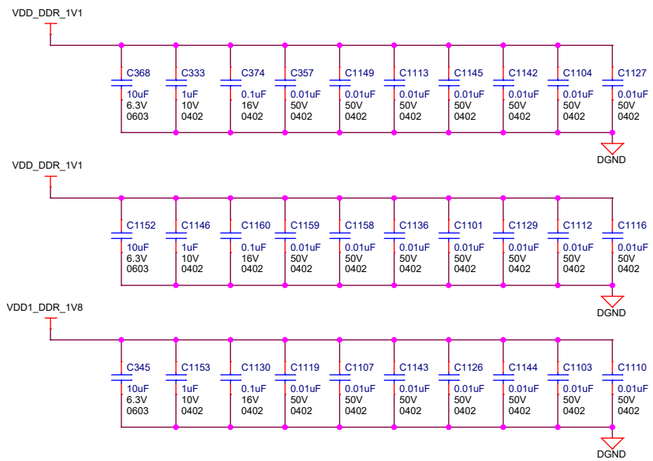
LPDDR4





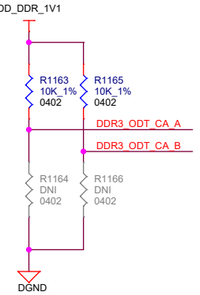
DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.

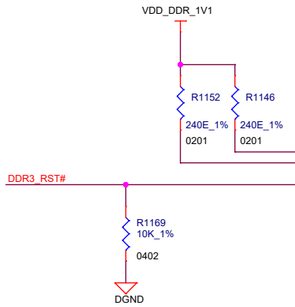


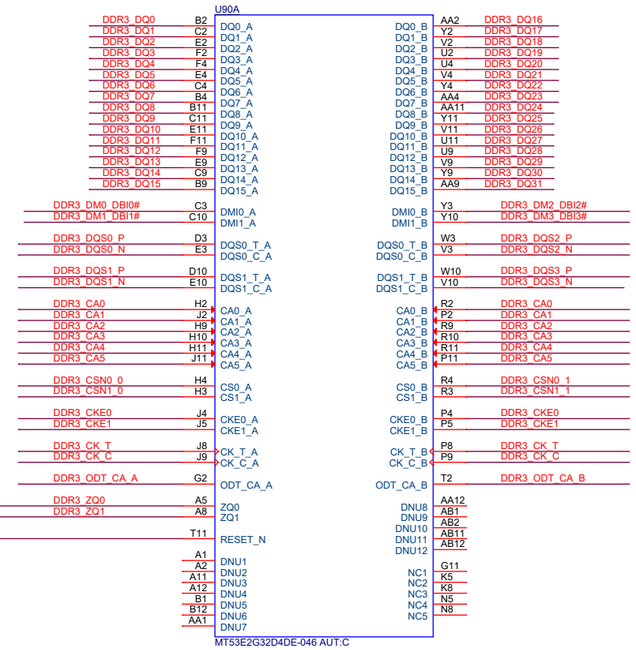


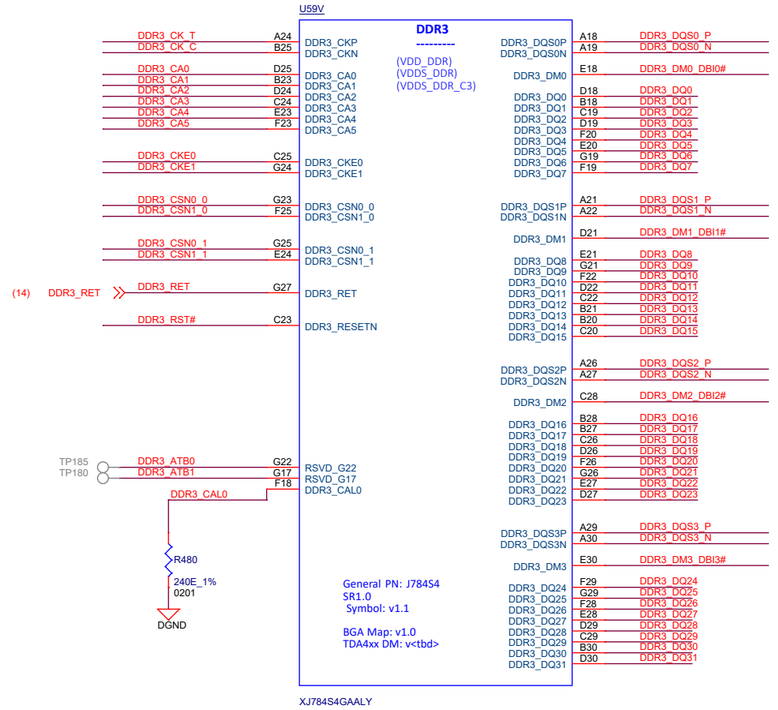
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EMIF1	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 16 of 88

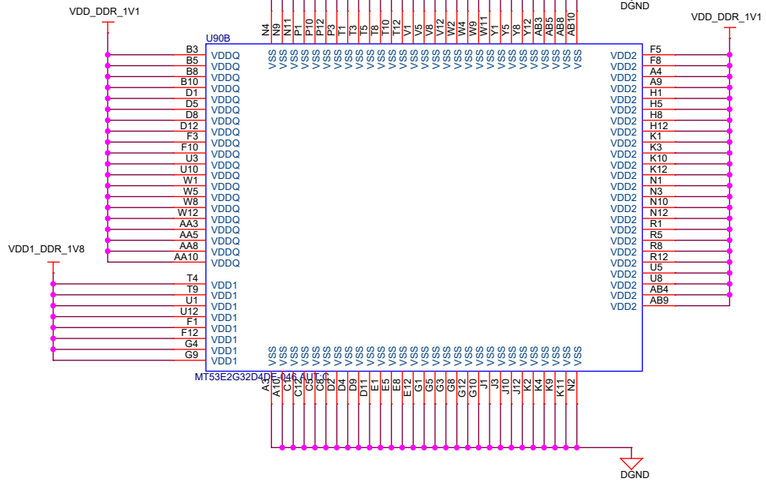
LPDDR4



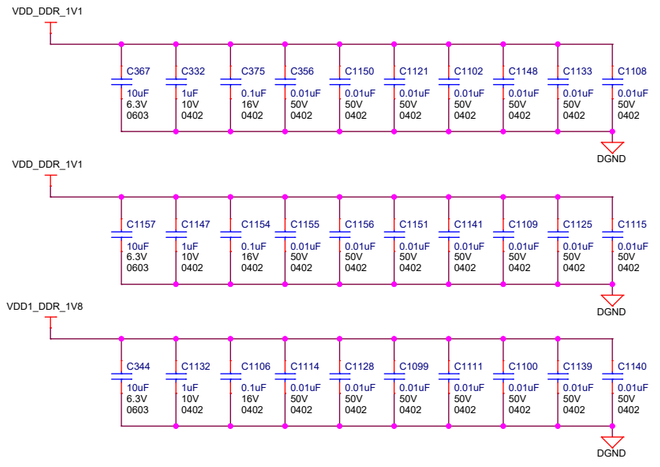








DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.



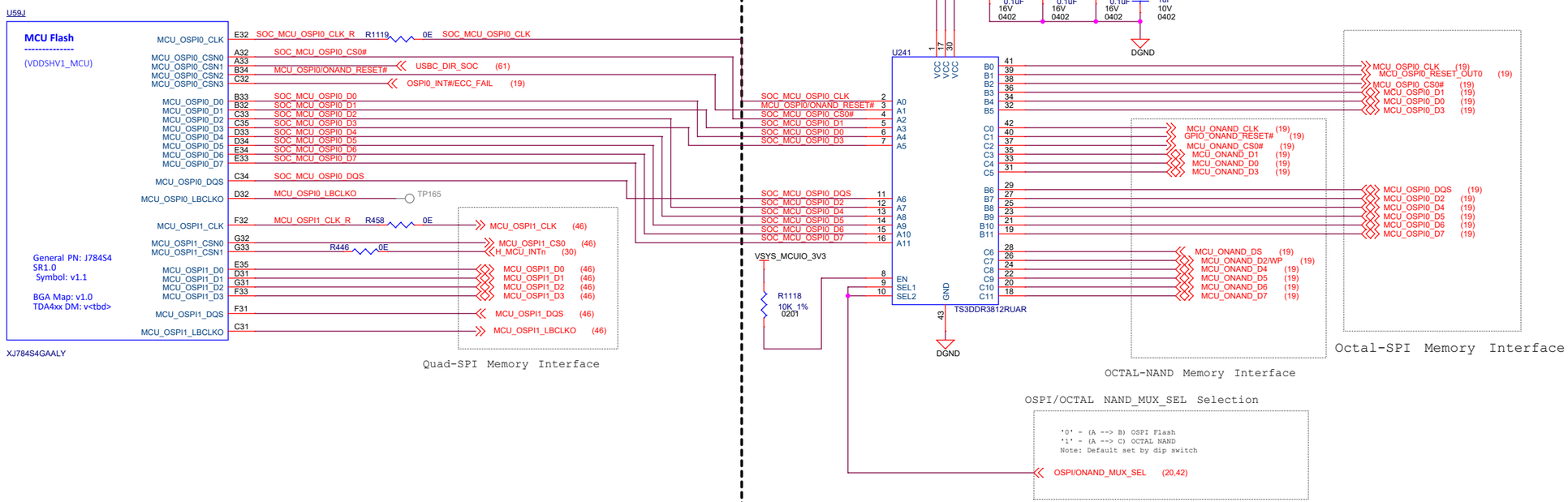
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EMIF3
	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 17 of 88

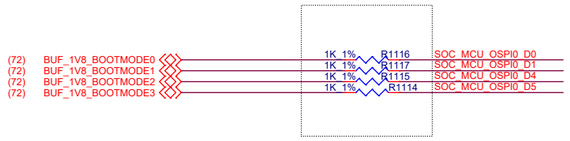
MCU FLASH

EVM development & evaluation test circuitry

(TI EVM Only)

2:1 Mux for OSPI/OCTAL NAND

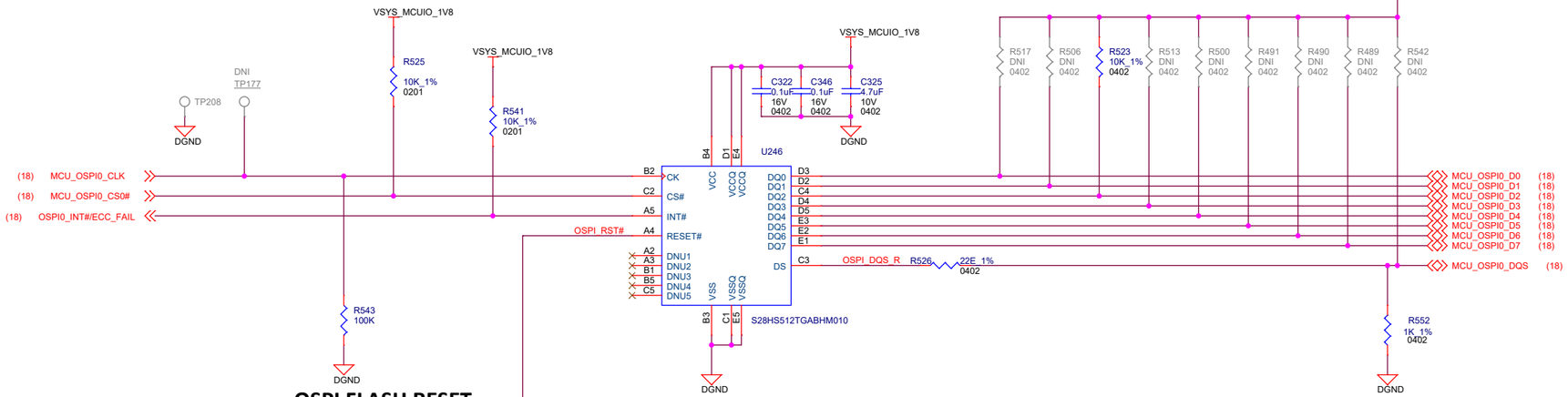




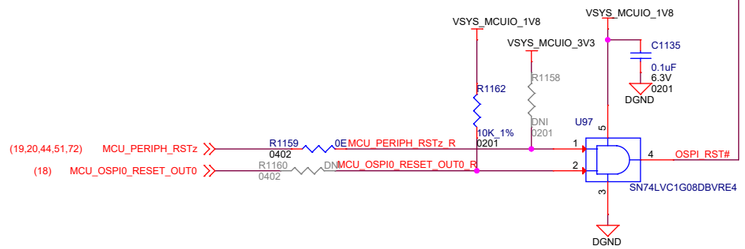
Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC MCU FLASH
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 18 of 88

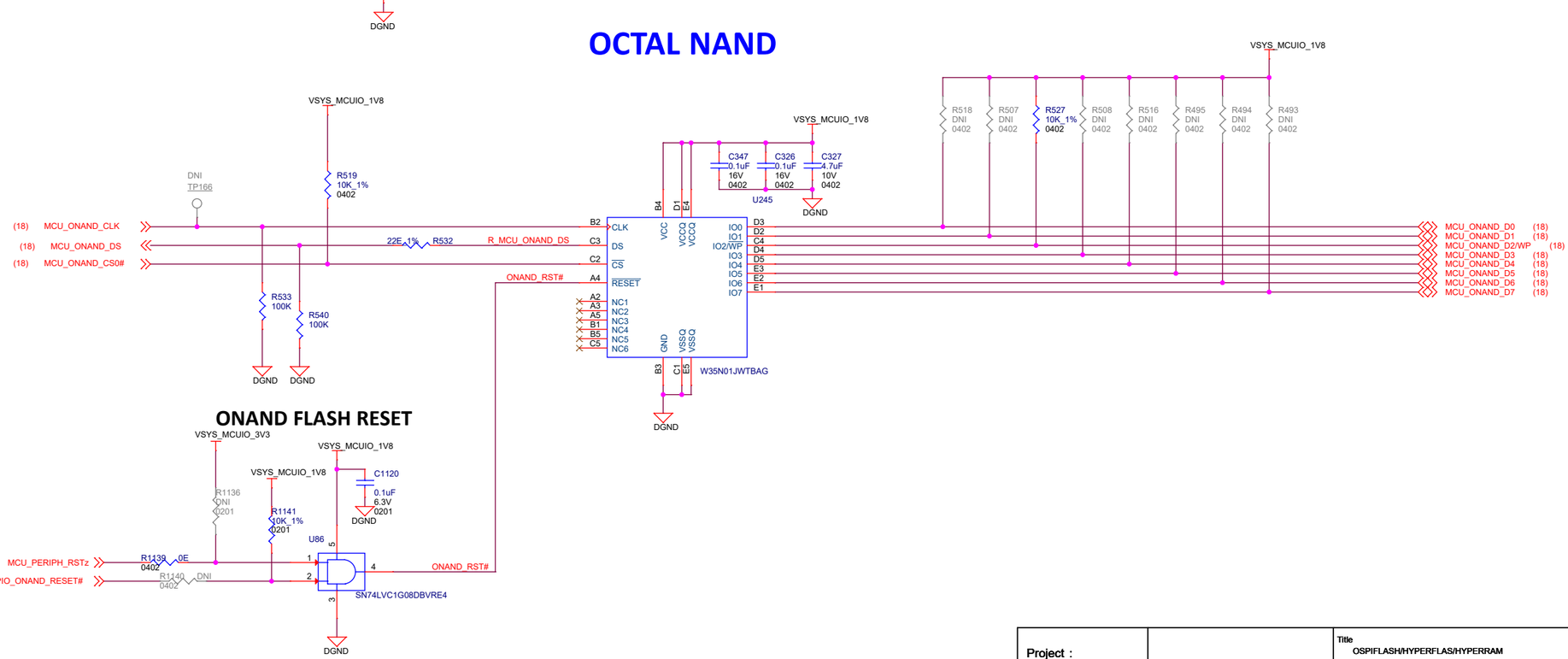
OSPI FLASH



OSPI FLASH RESET



OCTAL NAND



ONAND FLASH RESET

Project : J7 EVM	TEXAS INSTRUMENTS	Title: OSPIFLASH/HYPERFLAS/HYPERRAM	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 19 of 88

MCU & MAIN GENERAL IO, OSC CLKS

U59I

MCU General IO

(VDDSHV0_MCU)

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

XJ784S4GAALY

MCU_MCAN0_TX	K33	MCU_MCAN0_TX	(56)	
MCU_MCAN0_RX	F38	MCU_MCAN0_RX	(56)	
MCU_SPI0_CLK	G38	WKUP_GPIO0_54 R416 0402 0E	EN_EFUSE_VPP	(33)
MCU_SPI0_CS0	F37	WKUP_GPIO0_70		
MCU_SPI0_D0	H36	WKUP_GPIO0_55		
MCU_SPI0_D1	J38	WKUP_GPIO0_69	SYS_MCU_PWRDN	(42)
			MCU_CAN0_STB	(56)
WKUP_UART0_TXD	K34		WKUP_UART0_TXD	(51)
WKUP_UART0_RXD	K35		WKUP_UART0_RXD	(51)
WKUP_GPIO0_0	H38	WKUP_GPIO0_0		
WKUP_GPIO0_1	J34	WKUP_GPIO0_1	BOOT_EEPROM_WP	(50)
WKUP_GPIO0_2	J35	WKUP_GPIO0_2	MCU_CAN1_STB	(56)
WKUP_GPIO0_3	J36	WKUP_GPIO0_3	MCU_RGMII1_INT#	(62)
WKUP_GPIO0_4	H35		MCU_MCAN1_TX	(56)
WKUP_GPIO0_5	K36		MCU_MCAN1_RX	(56)
WKUP_GPIO0_6	L37	WKUP_GPIO0_6	OSPI/ONAND_MUX_SEL	(18,42)
WKUP_GPIO0_7	L36	WKUP_GPIO0_7	SYS_IRQz	(42)
		TP154		
WKUP_GPIO0_8	L35		MCU_I3C0_SCL	(23,69)
WKUP_GPIO0_9	L34		MCU_I3C0_SDA	(23,69)
WKUP_GPIO0_10	L33	R_MCU_ADC_EXT_TRIGGER		
WKUP_GPIO0_11	M38			
WKUP_GPIO0_12	J37		MCU_I3C0_SDAPULLEN	(69)
WKUP_GPIO0_13	K38		MCU_UART0_TXD	(51)
WKUP_GPIO0_14	H37		MCU_UART0_RXD	(51)
WKUP_GPIO0_15	K37		MCU_UART0_CTS#	(51)
		MCU_OBSCLK0	MCU_UART0_RTS#	(51)
		TP148		
WKUP_GPIO0_49	M33		H_MCU_WK1n	(30)
WKUP_GPIO0_56	M37	WKUP_GPIO0_56	GPIO_MCU_RGMII1_RST#	(62)
WKUP_GPIO0_57	M36	R1028 0402 DNI	LSM6DSRX_INT	(23)
		WKUP_GPIO0_57		
WKUP_GPIO0_66	N34		PM_I2C_SEL	
WKUP_GPIO0_67	M34		PM_I2C_SEL	(73)
		WKUP_LFOSC_XI		

CANIO_RET_WAKE

VSYS_VDDSHV0_MCU
R476 10K_1% 0402
SW8 7914G-1-000E
TP164
C303 0.1uF 16V 0402
D37 TPD1E10B06DPYR
DGND

VSYS_GPIORET_IO_3V3
VSYS_MCUIO_3V3
VSYS_VDDSHV0_MCU
R1128 0E
R1129 DNI

VSYS_GPIORET_IO_3V3
VSYS_IO_3V3
VSYS_VDDSHV2
R1103 DNI
R1104 0E

Low Freq Clock Selection (32K)

VSYS_MCUIO_3V3
C415 0.1uF 16V 0402
U127 SN74LVC1G126DBVR
WKUP_LFOSC_XI
WKUP_LFOSC_XI_R R613 0402 0E RTC_REF_CLK (69)
WKUP_LFOSC_XI_OE R626 0402 0E MCU_PERIPH_RSTz (19,44,51,72)
R619 DNI 0402
Note: Buffer used to isolate clock signal at reset to allow proper BOOTMODE value to be latched..

MCU BOOTMODE Control Signals

VSYS_MCUIO_3V3
R419 DNI 0402
R422 DNI 0402
R1072 DNI 0402
EN_EFUSE_VPP R414 0201 1K_1% MCU_BOOTMODE00 TP142
SYS_MCU_PWRDN R428 0201 1K_1% MCU_BOOTMODE01 TP146
MCU_CAN0_STB R1074 0201 1K_1% BUF_MCU_BOOTMODE2 (72)
R420 10K_1% 0402
R423 10K_1% 0402
R1073 DNI 0402
Note: MCU_BOOTMODE[2:0] set to '000' for 19.2MHz input frequency.

WKUP_GPIO0_0 R1065 0201 1K_1% BUF_MCU_BOOTMODE3 (72)
BOOT_EEPROM_WP R1066 0201 1K_1% BUF_MCU_BOOTMODE4 (72)
MCU_CAN1_STB R1062 0201 1K_1% BUF_MCU_BOOTMODE5 (72)
MCU_UART0_CTS# R1068 0201 1K_1% BUF_MCU_BOOTMODE6 (72)
MCU_UART0_RTS# R1069 0201 1K_1% BUF_MCU_BOOTMODE7 (72)
MCU_UART0_TXD R1070 0201 1K_1% BUF_MCU_BOOTMODE8 (72)
MCU_UART0_RXD R1071 0201 1K_1% BUF_MCU_BOOTMODE9 (72)
Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

Power-On Reset Buffers

Note: Used to align logic/levels

VSYS_IO_3V3
VDA_MCU_1V8_REG
VSYS_IO_3V3
R584 10K_1% 0402
C393 0.1uF 16V 0402
C396 0.1uF 16V 0402
U110 TXB0101DRLR
PORZ
PORZ_OE
PORZ_3V3

VSYS_MCUIO_3V3
VDA_MCU_1V8_REG
VSYS_MCUIO_3V3
R569 10K_1% 0402
C381 0.1uF 16V 0402
C382 0.1uF 16V 0402
U104 TXB0101DRLR
MCU_PORZ
MCU_PORZ_OE
MCU_PORZ_OUT
R566 1M_1%
MCU_PORZ_OUT (30,44,62)
TP197

PORZ_3V3
MCU_PORZ_OUT
U254 SN74LVC1G08DBVRE4
VSYS_IO_3V3
0.01uF C1169 50V
R1187 0402 0E
SOC_PORZ_OUT (30,36,39,44,50,59,63,70,71,72)
TP206
R1194 1M_1%

BOOTMODE Control Signals (partial)

GPIO_MCU_RGMII1_RST# R1145 0201 1K_1% BUF_3V3_BOOTMODE4 (72)
WKUP_GPIO0_57 R1142 0201 1K_1% BUF_3V3_BOOTMODE5 (72)
PM_I2C_SEL R1138 0201 1K_1% BUF_3V3_BOOTMODE6 (72)
WKUP_LFOSC_XI R1137 0201 1K_1% BUF_3V3_BOOTMODE7 (72)
Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

R_MCU_ADC_EXT_TRIGGER R1099 0201 1K_1% MCU_ADC_EXT_TRIGGER0 (69)
R1098 0201 1K_1% MCU_ADC_EXT_TRIGGER1 (36)

CONTROL & OSC

U59D

CNTRL & OSC

(VDDSHV0_MCU)
(VDDA_WKUP)
(VDDSHV0_MCU)
(VDDSHV0_MCU)
(VDDA_WKUP)
(VDDSHV0_MCU)
(VDDSHV0_MCU)
(VDDA_WKUP)
(VDDSHV0_MCU)
(VDDA_WKUP)
(VDDSHV0)
(VDDSHV0)
(VDDSHV2)
(VDDA_WKUP)
(VDDA_OSC1)

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

XJ784S4GAALY

MCU_I2C0_SCL	M35		MCU_I2C0_SCL	(30,50)
MCU_I2C0_SDA	G34		MCU_I2C0_SDA	(30,50)
MCU_PORZ	K32		MCU_PORZ	(43)
MCU_RESETZ	G36		MCU_RESETZ	(43)
MCU_RESETSTATZ	F36	MCU_RESETSTATZ	MCU_RESETSTATZ	(44)
		TP157		
		R447 10K_1%		
		DGND		
MCU_SAFETY_ERRORN	N36	MCU_SAFETY_ERRZ		
		TP315		
			MCU_SAFETY_ERRZ	(30)
PMIC_POWER_EN1	L38		PMIC_POWER_EN1	(30)
WKUP_I2C0_SCL	N33		SOC_WKUP_I2C0_SCL	(50,79)
WKUP_I2C0_SDA	N35		SOC_WKUP_I2C0_SDA	(50,79)
PORZ	P33		PORZ	(43)
RESET_REQZ	F34		RESET_REQZ	(43)
			RESETSTATZ	(36,44,72)
RESETSTATZ	AL38	RESETSTATZ		
		TP86		
		R564 10K_1%		
		DGND		
SOC_SAFETY_ERRORN	AM34		SOC_SAFETY_ERRZ	(30)
PMIC_WAKE0	AJ34		H_MAIN_WK0n	(30)
WKUP_OSC0_XI	T38	WKUP_OSC0_XI		
WKUP_OSC0_XO	U37	WKUP_OSC0_XO		
OSC1_XI	P38			
OSC1_XO	N37			

TP260
DGND

OSC1 Clock

Note: OSC1 is OPTIONAL, provides second clock frequency for SoC.

OSC1_XI
R399 0402 DNI OSC0_REFCLK (41)
R395 0402 0E
C262 0402 12pF 50V
Y5 ABM10W-26.0000MHZ-8-K1Z-T3 26.000MHz
C268 0402 12pF 50V
OSC1_XO
R402 0402 0E

WKUP_OSC0 Clock

Note: WKUP_OSC0 is required for all SoC configurations.

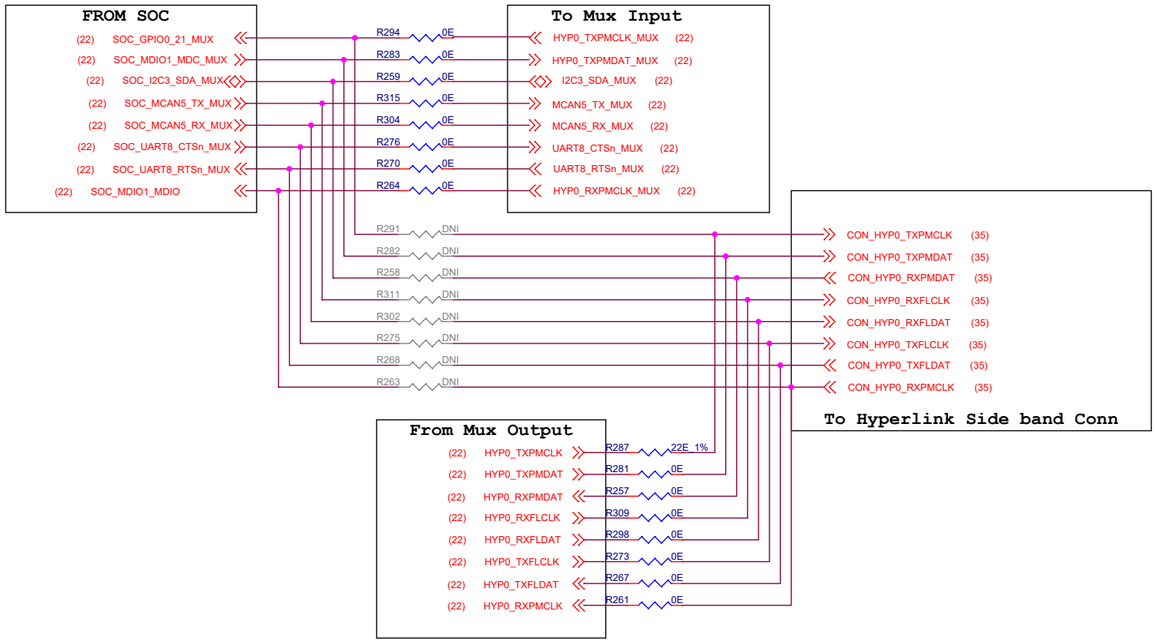
WKUP_OSC0_XI
C279 0402 12pF 50V
Y6 ABM10W-19.2000MHZ-8-K1Z-T3 19.200MHz
C270 0402 12pF 50V
WKUP_OSC0_XO

MCU I3C/I2C Pull-ups

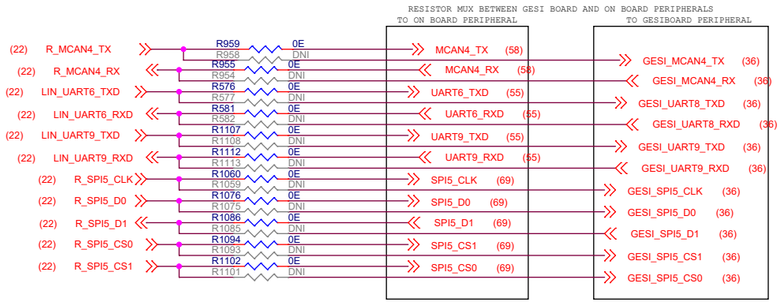
VSYS_MCUIO_3V3
R1038 10K_1% 0402
R1034 10K_1% 0402
MCU_I3C0_SCL
MCU_I3C0_SDA
SOC_WKUP_I2C0_SCL
SOC_WKUP_I2C0_SDA
R445 2.2K 0201
R478 2.2K 0201
R1149 2.2K 0201
R1150 2.2K 0201
MCU_I2C0_SCL
MCU_I2C0_SDA

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC MCU & MAIN GENERAL	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 20 of 88

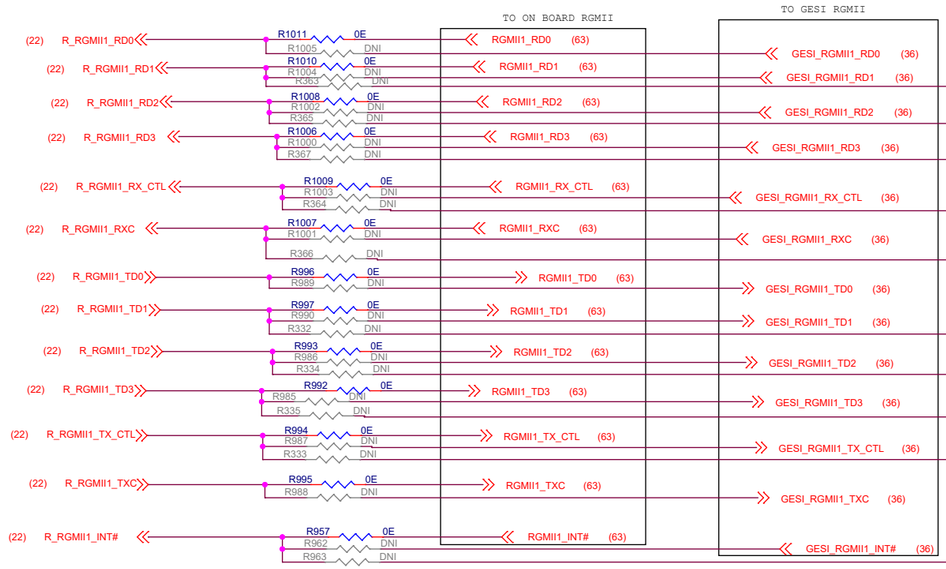
Resistor Mux option to By-pass MUX for Hyperlink sideband signals

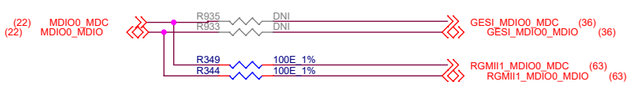


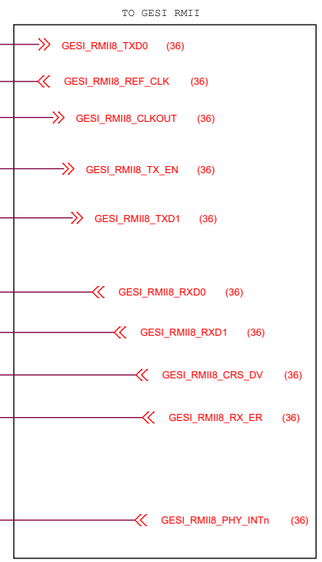
RESISTOR MUX BETWEEN GESI BOARD AND ON BOARD PERIPHERALS



RESISTOR MUX BETWEEN ON BOARD RGMII AND GESI RMII







Project : J7 EVM

Texas Instruments

Title: GENERAL IO

Size		Rev
C	PROC141 001 J784S4XG01EVM	E4
Date: Friday, May 05, 2023	Sheet 21 of 88	

GENERAL IO

U59A

General IO

(VDDSHV0)

I2C0_SCL — AN36 — I2C0_SCL (38,39,40,41,45,69,70)
I2C0_SDA — AP37 — I2C0_SDA (38,39,40,41,45,69,70)

TIMER_IO0 — AR38 — TIMER_IO0_R — 0E R292 0201 — CONN_MMC1_SDCD (47)
TIMER_IO1 — AN37 — TIMER_IO1 — 0E R310 0201 — USB0_DRVVBUS_MUX (25)

SPI0_CLK — AN38 — UART8_TXD (52)
SPI0_CS0 — AM37 — GPIO0_51 — DP0_HPD_BUF (68)
SPI0_CS1 — AP38 — UART8_RXD (52)
SPI0_D0 — AM35 — DDR3_IO_PLL_TESTOUT0P
SPI0_D1 — AM36 — DDR3_IO_PLL_REFCLK_TEST0P
0E R1251 0201 — UART2_RXD (52)
0E R1247 0201 — UART2_TXD (52)

OBSCLK0
SYSCLKOUT0 — TP93 TP81

TP293
TP295

Place Test Points close to the isolation resistors for better signal quality when probing high freq signals on test points. Length should be matched till the test point

VSYS_IO_3V3
R550 10K_1% 0201

EXTINTN — AN35 — SOC_EXTINTN (42)

ECAP0_IN_APWM_OUT — AD36 — I2C1_SCL_MUX
EXT_REFCLK1 — AJ32 — I2C1_SDA_MUX

(VDDSHV2)

MCAN0_TX — AF38 — I2C3_SCL_MUX
MCAN0_RX — AE38 — MCASP4_AXR1/TRC_DATA16_MUX

MCAN1_TX — AJ37 — UART6_TXD_MUX
MCAN1_RX — AH38 — MCASP4_AXR3/TRC_DATA5_MUX

MCAN2_TX — AC33 — UART3_RXD_MUX
MCAN2_RX — AH37 — UART3_TXD_MUX

MCAN12_TX — AG36 — UART5_TXD (52)
MCAN12_RX — AJ33 — UART5_RXD (52)

MCAN13_TX — AF33 — TRC_DATA0_MUX
MCAN13_RX — AH33 — I2C4_SDA (45,67)
I2C4_SCL (45,67)

MCAN14_TX — AG33
MCAN14_RX — AK36 — I2C5_SDA (37,45)

MCAN15_TX — AG34 — I2C5_SCL (37,45)
MCAN15_RX — AJ35 — SEL_SDIO_3V3_1V8n (33)

MCAN16_TX — AH34 — MCAN16_TX (58)
MCAN16_RX — AE33 — MCAN16_RX (58)

MCASP0_ACLKX — AK35 — SOC_MCAN5_TX_MUX (21)
SOC_MCAN5_RX_MUX (21)
MCASP0_AFSX — AK38

MCASP0_AXR0 — AF37
MCASP0_AXR1 — AG37 — SOC_UART8_CTSn_MUX (21)
MCASP0_AXR2 — AK33 — HYP1_RXFLCLK_MUX — SOC_UART8_RTSn_MUX (21)
MCASP0_AXR3 — AJ38 — MCAN3_TX_MUX
MCASP0_AXR4 — AK34 — MCAN3_RX_MUX
MCASP0_AXR5 — AG38 — MCAN4_TX_MUX
MCASP0_AXR6 — AF36 — MCAN4_RX_MUX
MCASP0_AXR7 — AE35 — R_RGMII1_TD0 (21)

MCASP0_AXR8 — AC35 — R_RGMII1_TD1 (21)
MCASP0_AXR9 — AG35 — R_RGMII1_TD2 (21)
MCASP0_AXR10 — AH36 — R_RGMII1_TD3 (21)
MCASP0_AXR11 — AF35 — R_RGMII1_TX_CTL (21)
MCASP0_AXR12 — AD34 — R_RGMII1_RD1 (21)
MCASP0_AXR13 — AJ36 — R_RGMII1_RD2 (21)
MCASP0_AXR14 — AF34 — R_RGMII1_RD3 (21)
MCASP0_AXR15 — AE34 — R_RGMII1_RX_CTL (21)

R_RGMII1_TXC — TP104
R_RGMII1_TD0 — TP103
R_RGMII1_RD0 — TP109
R_RGMII1_TD1 — TP102
R_RGMII1_TD2 — TP106
R_RGMII1_TD3 — TP107
R_RGMII1_TX_CTL — TP105
R_RGMII1_RD1 — TP110
R_RGMII1_RD2 — TP112
R_RGMII1_RD3 — TP113
R_RGMII1_RX_CTL — TP111

MCASP1_ACLKX — AC34 — R_RGMII1_RD0 (21)
MCASP1_AFSX — AD33 — MDIO0_MDIO (21)
AD38 — MDIO0_MDC (21)
MCASP1_AXR0 — AC32 — UART9_RXD_MUX
MCASP1_AXR1 — AC37 — UART9_TXD_MUX
MCASP1_AXR2 — AL33 — R_RGMII1_RXC (21)
MCASP1_AXR3 — AL34 — R_RGMII1_TXC (21)
MCASP1_AXR4

VSYS_IO_3V3
R926 2.2K 0201

MCASP2_ACLKX — AD37 — SOC_GPIO0_21_MUX (21)
MCASP2_AFSX — AE37 — SOC_MDIO1_MDC_MUX (21)
MCASP2_AXR0 — AC36 — SOC_MDIO1_MDIO — SOC_MDIO1_MDIO (21)
MCASP2_AXR1 — AE36 — SOC_I2C3_SDA_MUX (21)

GPIO0_11 — AL32 — MAIN_RET_WAKE
GPIO0_12 — AK37 — UART6_RXD_MUX

VSYS_VDDSHV2
R202 10K_1% 0402
TP39
VSYS_IO_3V3
R1292 10K_1% 0201
C160 0.1uF 16V 0402
DGND
SW3
7914G-1-000E
TPD1E10B06DPYR
D33
DGND
SOC_MDIO1_MDIO

CANIO Retension Wake:
MAIN DOMAIN

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

XJ784S4GAALY

VSYS_IO_3V3
R403 10K_1% 0402
R805 10K_1% 0402
R411 10K_1% 0402
R1025 DNI 0402
R405 DNI 0402
R1032 10K_1% 0402
DGND

FROM IO EXP
(45) CANUART_MUX1_SEL1
(45) CANUART_MUX2_SEL1
FROM IO EXP/DIP SW
(22,42,45) CANUART_MUX_SEL0
CANUART_MUX_SEL0
CANUART_MUX1_SEL1
CANUART_MUX2_SEL1
CANUART_MUX_SEL2

VSYS_IO_3V3
C1023 0.1uF 16V 0402
DGND
U227
SN74CB3Q3257PWR
TRC_DATA0_MUX — 4 1A
GPIO0_3 — 3 1B1
2 1B2
TRC_DATA0 (54)
SoC_eDP_IRQ (67)
7 2A
9 3A
12 4A
1 S
15 OE
2B1 5
2B2 6
3B1 11
3B2 10
4B1 14
4B2 13
GND 8
(22,42,45) CANUART_MUX_SEL0
R1042 10K_1% 0402
DGND

HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table

MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION	
HIGH	HIGH	LOW	A port = B1 port	(default)
HIGH	HIGH	HIGH	A port = B2 port	
HIGH	LOW	HIGH	A port = B3 port	

VSYS_IO_3V3
R328 10K_1% 0201
R327 10K_1% 0201
I2C1_SCL_MUX
I2C1_SDA_MUX

VSYS_IO_3V3
R339 10K_1% 0201
R260 10K_1% 0201
I2C3_SCL_MUX
I2C3_SDA_MUX

VSYS_IO_3V3
R303 2.2K 0201
R297 2.2K 0201
I2C0_SCL
I2C0_SDA

VSYS_IO_3V3
R809 2.2K 0201
R810 2.2K 0201
I2C4_SCL
I2C4_SDA

VSYS_IO_3V3
R1147 2.2K 0201
R1143 2.2K 0201
I2C5_SCL
I2C5_SDA

MUX1

1:3 MUX for Trace, Hyperlink and UART,MCAN

VSYS_5V0
C883 0.1uF 0402 16V
DGND

U58
VCC 17
1 of 3 MUX/DEMUX

MIPI TRC

1B1 54 — TRC_DATA2 (54)
2B1 52 — TRC_CTL (54)
3B1 50 — TRC_DATA3 (54)
4B1 47 — TRC_DATA17 (54)
5B1 45 — TRC_DATA8 (54)
6B1 43 — TRC_DATA6 (54)
7B1 41 — TRC_DATA7 (54)
8B1 39 — TRC_DATA18 (54)
9B1 36 — TRC_DATA10 (54)
10B1 34 — TRC_DATA11 (54)
11B1 32 — TRC_DATA1 (54)
12B1 30 — TRC_CLK (54)

LIN/I2C

VSYS_IO_3V3
R1280 2.2K 0201
R96 2.2K 0201
R90 2.2K 0201

1B2 53 — LIN_UART6_RXD (21)
2B2 51 — LIN_UART6_TXD (21)
3B2 48 — UART3_RXD (52)
4B2 46 — AUDIO_EXT_REFCLK1/UART3_TXD (54)
5B2 44 — LIN_UART9_RXD (21)
6B2 42 — LIN_UART9_TXD (21)
7B2 40 — MCASP0_AXR3/MCAN3_TX (54)
8B2 37 — MCASP0_AXR4/MCAN3_RX (54)
9B2 35 — GPIO0_18 — R345 0E — IOEXP5_INT# (45)
10B2 33 — I2C3_SCL (45,64)
11B2 31 — I2C1_SCL (73)
12B2 29 — I2C1_SDA (73)

UART6_RXD_MUX — 2 1A
UART6_TXD_MUX — 4 2A
UART3_TXD_MUX — 6 3A
UART3_RXD_MUX — 9 4A
UART9_RXD_MUX — 11 5A
UART9_TXD_MUX — 13 6A
MCAN3_TX_MUX — 15 7A
MCAN3_RX_MUX — 18 8A
HYP1_RXFLCLK_MUX — 21 9A
I2C3_SCL_MUX — 23 10A
I2C1_SCL_MUX — 25 11A
I2C1_SDA_MUX — 27 12A

Hyperlink1 Sideband Signals

1B3 3 — HYP1_RXFLDAT (35)
2B3 5 — HYP1_TXPMCLK (35)
3B3 7 — GPIO0_29 — TP126
4B3 10 — GPIO0_30 — TP121
5B3 12 — HYP1_RXPMCLK (35)
6B3 14 — HYP1_RXPMDAT (35)
7B3 16 — R_SPI5_CLK (21)
8B3 20 — HYP1_TXPMDAT (35)
9B3 22 — HYP1_RXFLCLK_R — R346 22E 1% — HYP1_RXFLCLK (35)
10B3 24 — R_SPI5_CS1 (21)
11B3 26 — HYP1_TXFLCLK (35)
12B3 28 — HYP1_TXFLDAT (35)

CANUART_MUX_SEL0 — 1 S0
CANUART_MUX1_SEL1 — 56 S1
CANUART_MUX_SEL2 — 55 S2

GND 8
GND 19
GND 38
GND 49

SN74CBT16214CDGGR

VSYS_5V0
C766 0.1uF 0402 16V
DGND

MUX2

U50
VCC 17
1 of 3 MUX/DEMUX

MIPI TRC

1B1 54 — GPIO0_14
2B1 52 — GPIO0_15 — TP90 TP85
3B1 50 — TRC_DATA4 (54)
4B1 47 — TRC_DATA9 (54)
5B1 45 — TRC_DATA14 (54)
6B1 43 — TRC_DATA12 (54)
7B1 41 — TRC_DATA19 (54)
8B1 39 — TRC_DATA20 (54)
9B1 36 — TRC_DATA15 (54)
10B1 34 — TRC_DATA13 (54)
11B1 32 — TRC_DATA16 (54)
12B1 30 — TRC_DATA5 (54)

MCAN & UART

VSYS_IO_3V3
R1293 2.2K 0201
VSYS_IO_3V3
R1281 2.2K 0201

1B2 53 — MCASP0_ACLKX/MCAN5_TX (54)
2B2 51 — MCASP0_AFSX/MCAN5_RX (54)
3B2 48 — GPIO0_21 — R_RGMII1_INT# (21)
4B2 46 — GPIO0_22 — ENET_EXP_MDIO1_MDC (38)
5B2 44 — UART8_CTSn (52)
6B2 42 — UART8_RTSn (52)
7B2 40 — R_MCAN4_TX (21)
8B2 37 — R_MCAN4_RX (21)
9B2 35 — GPIO0_23
10B2 33 — GPIO0_26 — CSI2_EXP_A_GPIO2 (37)
11B2 31 — GPIO0_28 — CSI2_EXP_A_GPIO4 (37)
12B2 29 — ENET_EXP_MDIO1_MDIO (38) — I2C3_SDA (45,64)

(21) MCAN5_TX_MUX — 2 1A
(21) MCAN5_RX_MUX — 4 2A
(21) HYP0_TXPMCLK_MUX — 6 3A
(21) HYP0_TXPMDAT_MUX — 9 4A
(21) UART8_CTSn_MUX — 11 5A
(21) UART8_RTSn_MUX — 13 6A
MCAN4_TX_MUX — 15 7A
MCAN4_RX_MUX — 18 8A
(21) HYP0_RXPMCLK_MUX — 21 9A
(21) I2C3_SDA_MUX — 23 10A
MCASP4_AXR1/TRC_DATA16_MUX — 25 11A
MCASP4_AXR3/TRC_DATA5_MUX — 27 12A

Hyperlink0 Sideband Signals

1B3 3 — HYP0_RXFLCLK (21)
2B3 5 — HYP0_RXFLDAT (21)
3B3 7 — HYP0_TXPMCLK (21)
4B3 10 — HYP0_TXPMDAT (21)
5B3 12 — HYP0_TXFLCLK (21)
6B3 14 — GPIO0_33 — TP290 — HYP0_TXFLDAT (21)
7B3 16 — R_SPI5_D1 (21)
8B3 20 — HYP0_RXPMCLK (21)
9B3 22 — HYP0_RXPMDAT (21)
10B3 24 — R_SPI5_CS0 (21)
11B3 26 — R_SPI5_D0 (21)
12B3 28

CANUART_MUX_SEL0 — 1 S0
CANUART_MUX2_SEL1 — 56 S1
CANUART_MUX_SEL2 — 55 S2

GND 8
GND 19
GND 38
GND 49

SN74CBT16214CDGGR

DGND

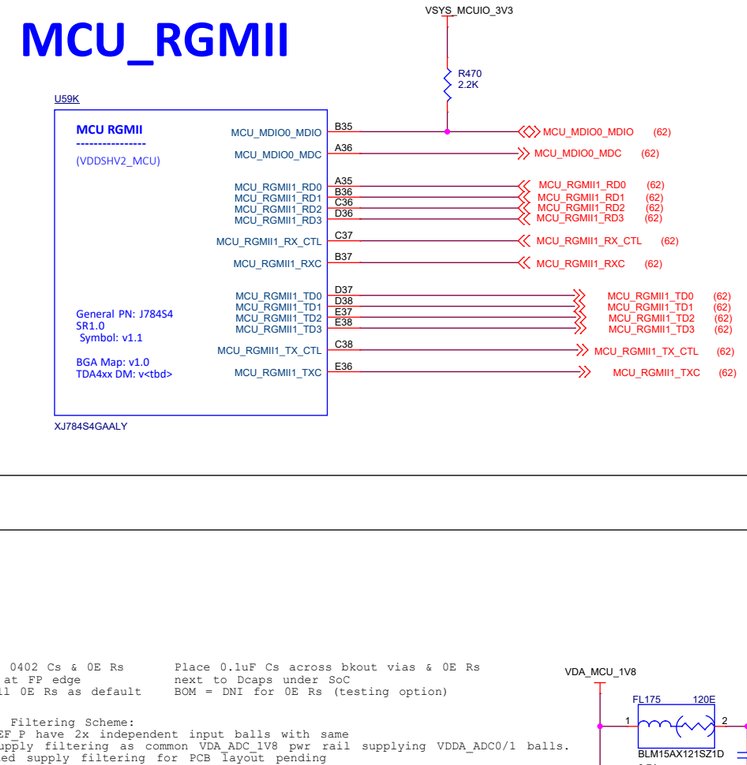
Project :
J7 EVM

TEXAS INSTRUMENTS

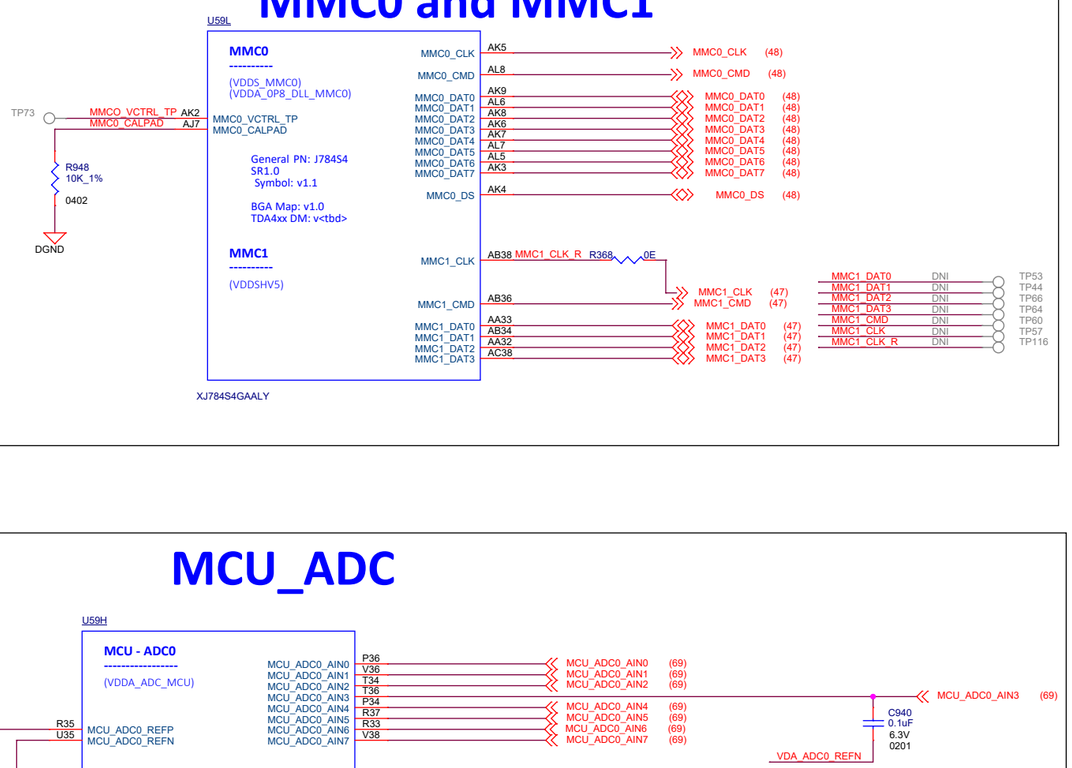
Title: GENERAL IO

Size		Rev
C	PROC141 001 J784S4XG01EVM	E4
Date: Friday, May 05, 2023	Sheet 22 of 88	

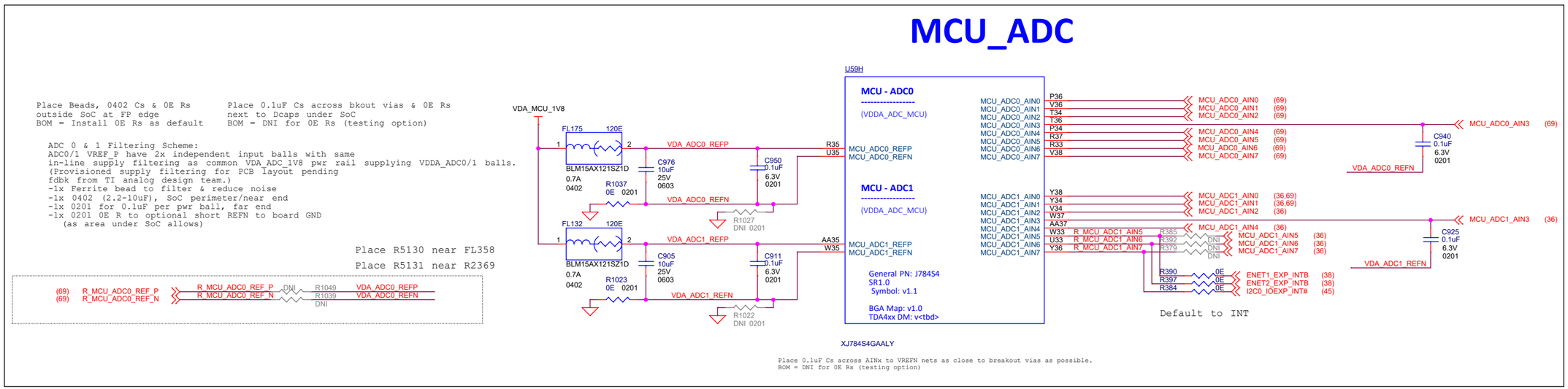
MCU_RGMII



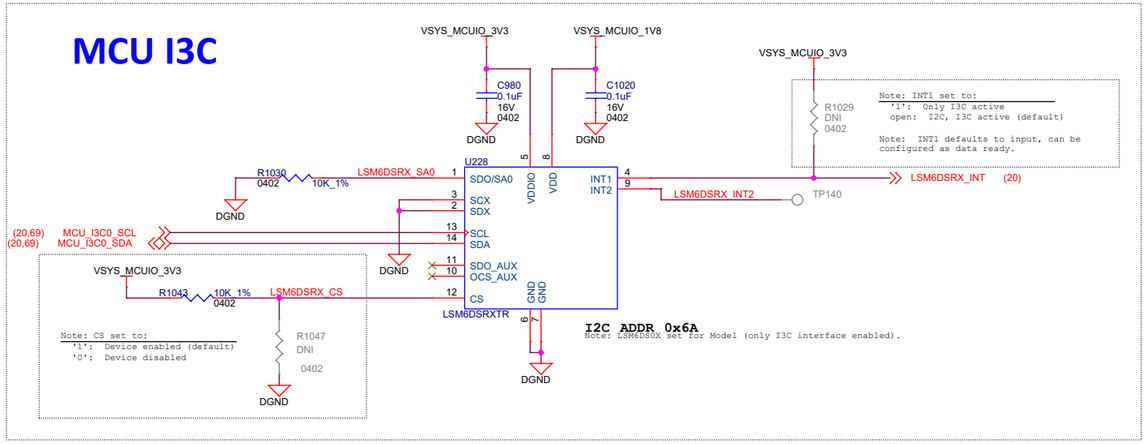
MMC0 and MMC1



MCU_ADC



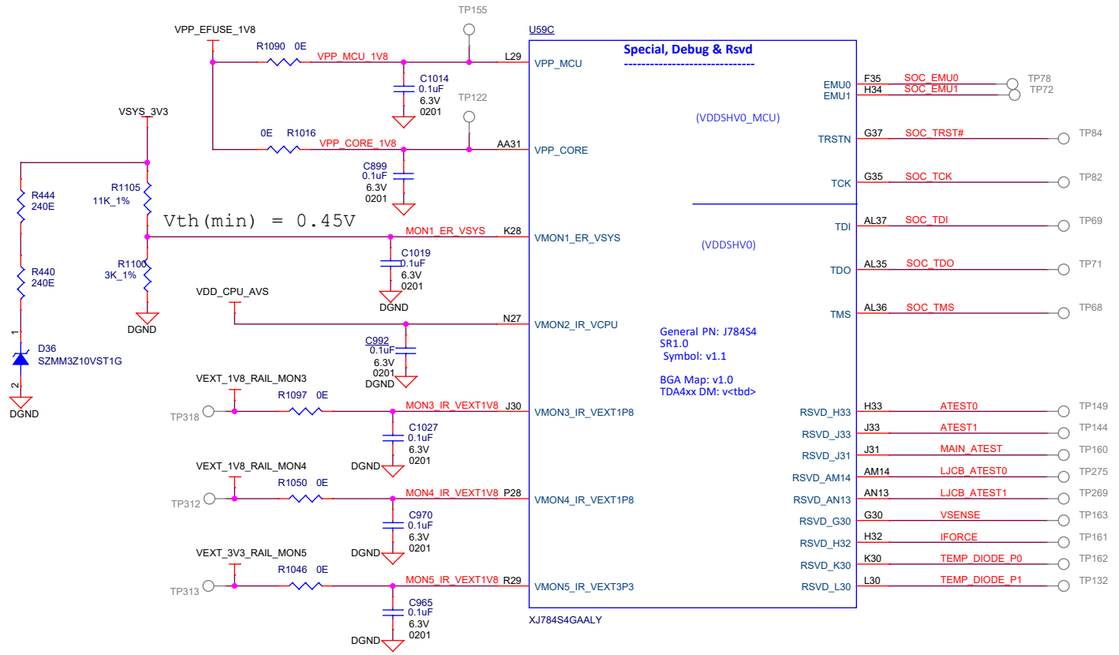
MCU I3C



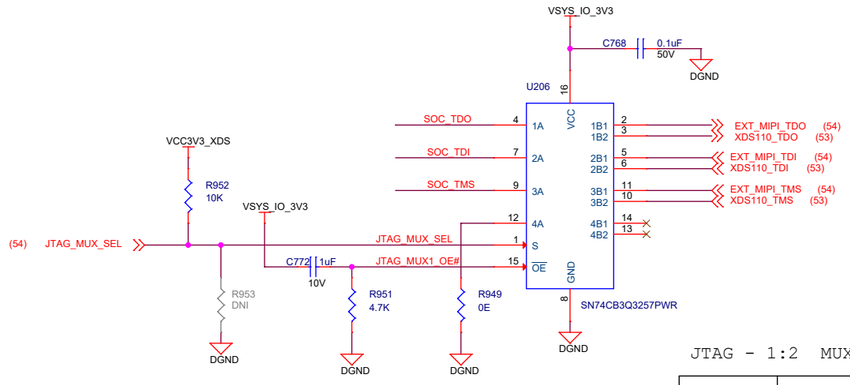
Project : J7 EVM	TEXAS INSTRUMENTS	Title: MCU RGMII & ADC	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 23 of 88

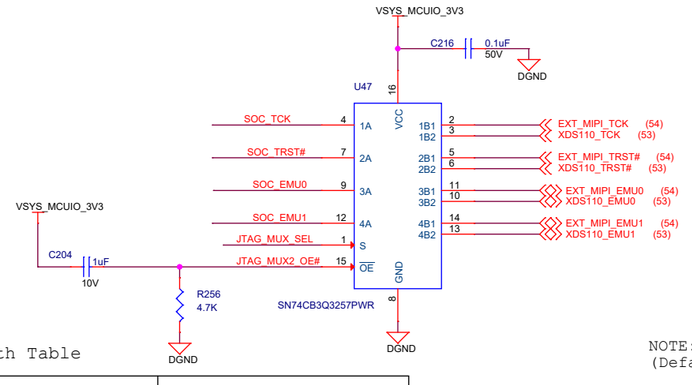
SPECIAL, DEBUG & RSVD

If monitoring VSYS_3V3, protect SoC from 1st stage fault. Alternatively, monitoring protected VCCA_3V3 requires no Zener diode.



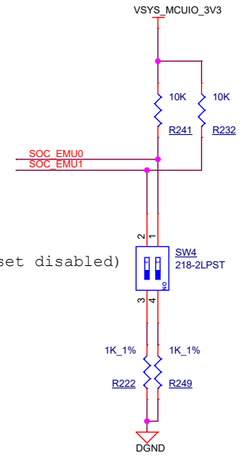
JTAG AND TRACE MUX





JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION	
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]	(default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]	
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]	
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]	



NOTE:SW4.1&2-OFF
(Default wait-in-reset disabled)

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DEBUG	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 24 of 88

USB0 2.0

By Pass USB MUX	Mount - R796,R795,R774,R775 DNI -R57,R56,R30,R29
USB MUX (Default)	Mount -R57,R56,R30,R29 DNI - R796,R795,R774,R775

USB0 2.0

U59B

USB0

(VDDA_3P3_USB)
(VDDA_1P8_USB)
(VDDA_0P8_USB)

USB0_RCALIB

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

XJ784S4GAALY

USB0_DP
USB0_DM
USB0_ID
USB0_VBUS

AP17 USB0_D_P
AP16 USB0_D_N
AN17 USB0_ID_MUX
AN15 USB0_VBUS_MUX

USB0_RCALIB AN18
R198 499E_0.1% 0402 DGND

R796 DNI
R795 DNI
Note: Option to by passive Mux.

0E R57 MUX_USB0_DATA_P
0E R56 MUX_USB0_DATA_N

R_MUX_USB0_DATA_N
R_MUX_USB0_DATA_P

VSYS_IO_3V3
C35 0.1uF 16V 0402 DGND

U12 TS3USB221ARSER

VCC 10
1D+ 1
1D- 2
2D+ 3
2D- 4
GND 5
S 9
OE 6
D+ 8
D- 7

R_USB0_DATA_P 0E R30
R_USB0_DATA_N 0E R29
R774 DNI
R775 DNI
Note: Option to by passive Mux.

USB0_DATA_P (61)
USB0_DATA_N (61)
USB2.0_MUX_SEL
USB2.0_MUX_OEn

TYPE-C

USB1_HUB_D_P (59)
USB1_HUB_D_N (59)

VSYS_IO_3V3
C585 0.1uF 16V 0402 DGND

U177 SN74CB3Q3257PWR

VCC 16
1A 4
2A 7
3A 9
4A 12
S 1
OE 15
GND 8
1B1 2
1B2 3
2B1 5
2B2 6
3B1 11
3B2 10
4B1 14
4B2 13

USB0_ID_MUX
USB0_VBUS_MUX
(22) USB0_DRVVBUS_MUX
USB2.0_MUX_SEL
USB2.0_MUX_OEn

USB0_ID (61)
USB0_VBUS_SOC
USB0_DRVVBUS (61)
USB1_ID (59)
USB1_VBUS_SOC
USB1_DRVVBUS (59)

R807 10K_1% 0402 DGND
R803 10K_1% 0402 DGND
R799 10K_1% 0402 DGND

USB HUB

USB2.0 MUX

VSYS_IO_3V3
R785 DNI 0402
(45) USB2.0_MUX_SEL
R790 10K_1% 0402 DGND

SEL	OUTPUT
LOW	A to B1 (USBC) Default
HIGH	A to B2 (USB HUB)

USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

USB0_VBUS_SOC 16.5K_1% R13 3.4K_1% R9 VBUS_USBC_CONN (61)
R14 10K_1% 0402 DGND
U3 BZX84C6V8LT1G DGND

Note: Recommended VBUS circuit for embedded Hub

USB1_VBUS_SOC 9.09K_1% R806 USB1_VBUS (59)
R804 10K_1% 0402 DGND

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC USB 2.0	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 25 of 88

ANALOG POWER 1

VDD_PHYCORE_0V8

VDA_PHY_1V8

U59N

Analog Power

XJ784S4GAALY

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

VDA_MCU_1V8

VDA_PLL_1V8

VDD_PHYCORE_0V8

VDA_PHY_1V8

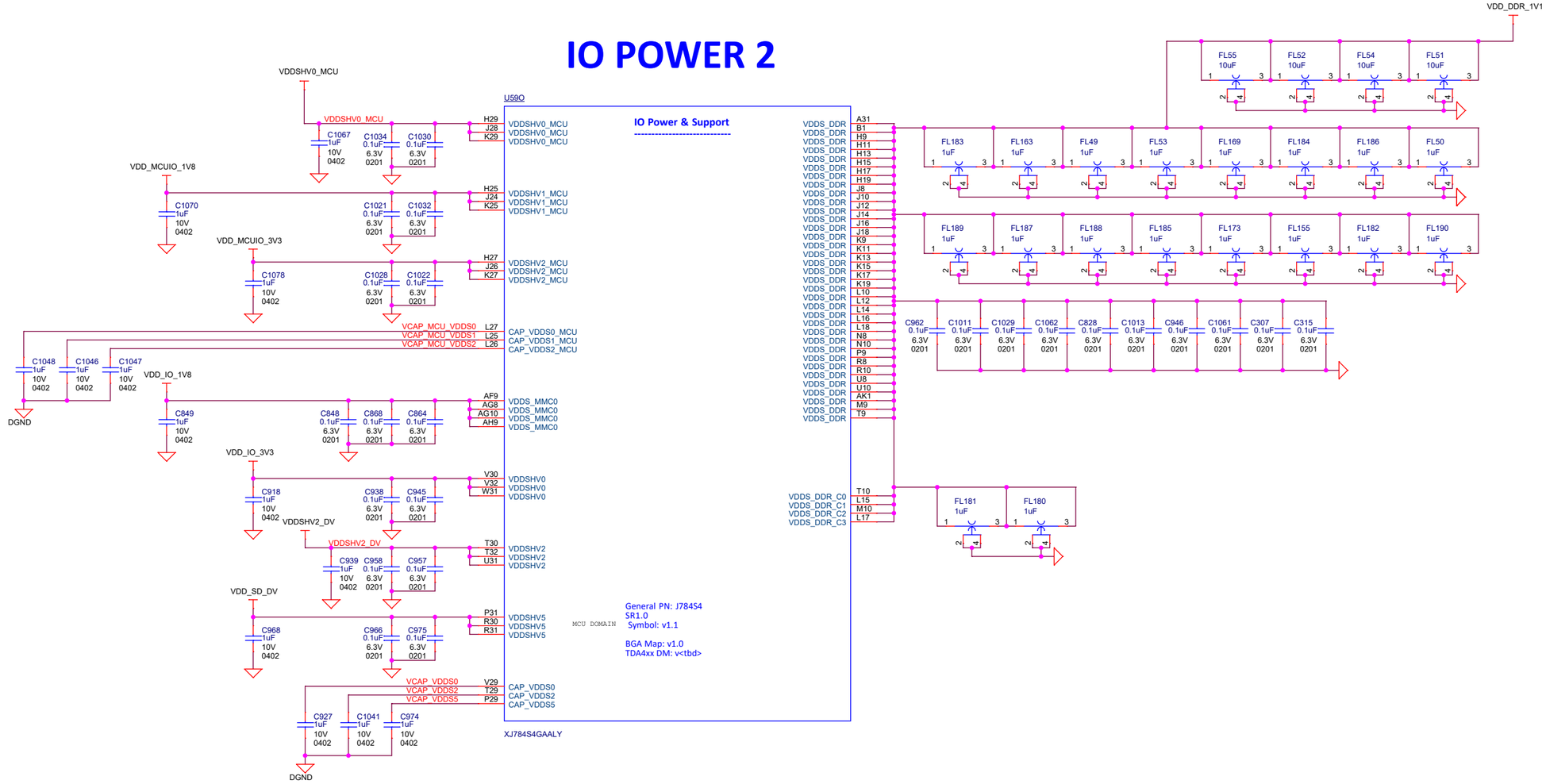
VDA_USB_3V3

VDA_DLL_0V8

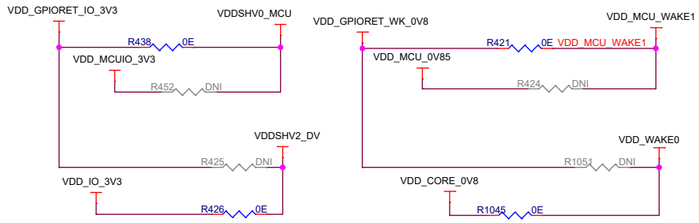
Project :	J7 EVM
Title	SOC ANALOG POWER 1
Size	C
Number	PROC141 001 J784S4XG01EVM
Rev	E4
Date:	Friday, May 05, 2023
Sheet	26 of 88

TEXAS INSTRUMENTS

IO POWER 2



EVM development & evaluation Test circuitry
EVM GPIO Retention testing option
(TI EVM Only)



MCU GPIO RETENTION mode

No MCU GPIO RETENTION mode

MAIN GPIO RETENTION mode

No MAIN GPIO RETENTION mode

Low power modes	Resistors to be Populated	Resistors to be DNI'd
No GPIO RET	R452,R424,R426,R1045	R438,R421,R425,R1051
MCU GPIO RET only	R438,R421,R426,R1045	R452,R424,R425,R1051
MAIN GPIO RET only	R452,R424,R425,R1051	R438,R421,R426,R1045
MCU & MAIN GPIO RET	R438,R421,R425,R1051	R452,R424,R426,R1045

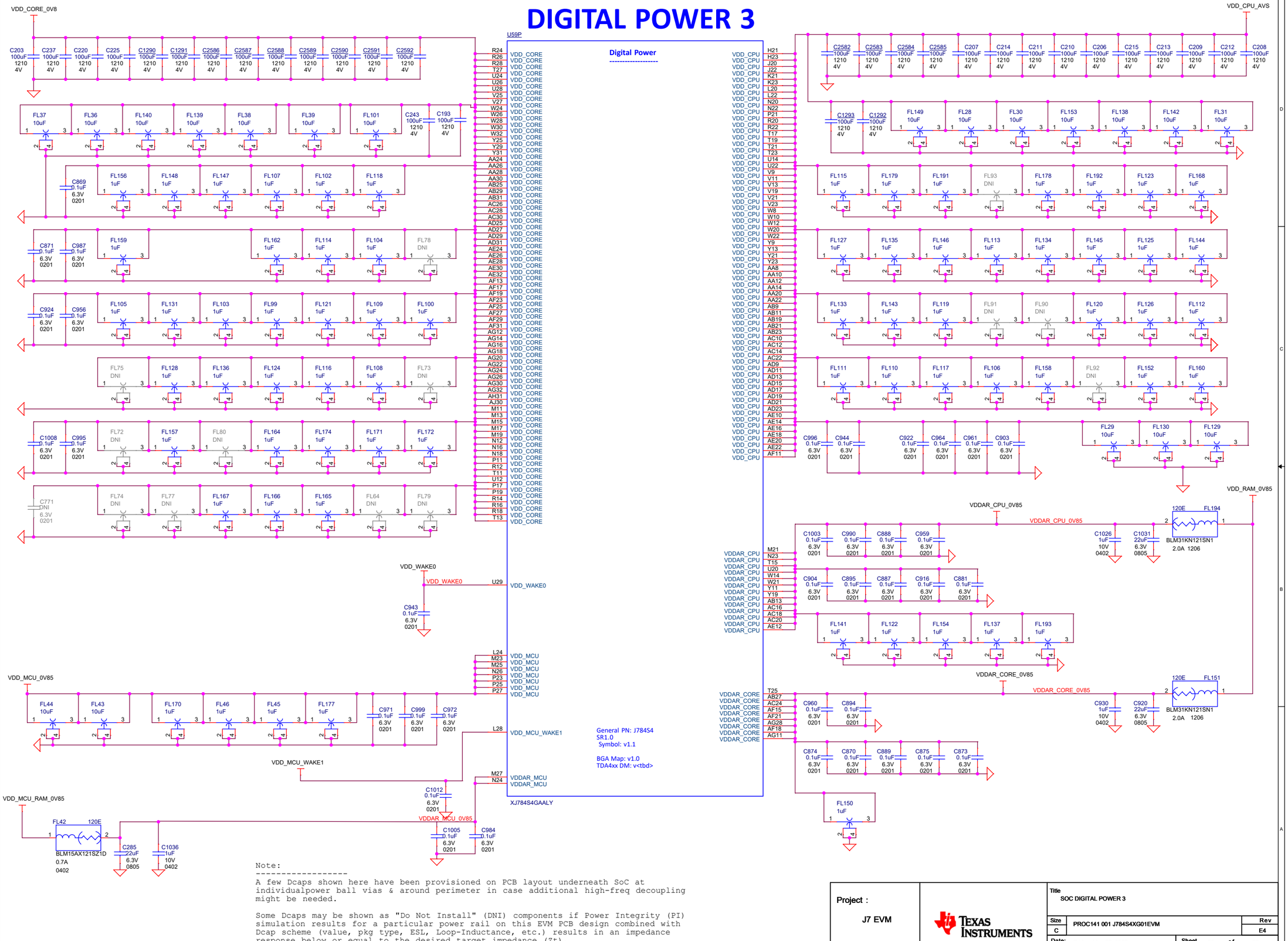
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC DIGITAL IO & SUPPORT POWER 2
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 27 of 88

DIGITAL POWER 3



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC DIGITAL POWER 3
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 28 of 88

SOC GROUND

U59Q

Ground/VSS1

A1	VSS	VSS	L19
A2	VSS	VSS	L21
A5	VSS	VSS	L23
A7	VSS	VSS	L31
A10	VSS	VSS	M2
A12	VSS	VSS	M5
A15	VSS	VSS	M8
A20	VSS	VSS	N17
A23	VSS	VSS	AJ16
A25	VSS	VSS	M16
A28	VSS	VSS	AL16
A34	VSS	VSS	M20
A37	VSS	VSS	M22
B6	VSS	VSS	M24
B9	VSS	VSS	M30
B11	VSS	VSS	M32
B13	VSS	VSS	N3
B16	VSS	VSS	N6
B19	VSS	VSS	N9
B22	VSS	VSS	N15
B24	VSS	VSS	N19
B26	VSS	VSS	N21
B29	VSS	VSS	N25
B31	VSS	VSS	N31
B38	VSS	VSS	N38
C2	VSS	VSS	P1
C4	VSS	VSS	P4
C8	VSS	VSS	P7
C14	VSS	VSS	P8
C17	VSS	VSS	P10
C18	VSS	VSS	P16
C21	VSS	VSS	P18
C27	VSS	VSS	P20
C30	VSS	VSS	P22
D3	VSS	VSS	P24
D6	VSS	VSS	P26
D7	VSS	VSS	P30
D10	VSS	VSS	P32
D15	VSS	VSS	P35
D20	VSS	VSS	P37
D23	VSS	VSS	R2
D28	VSS	VSS	R5
D35	VSS	VSS	R9
E2	VSS	VSS	R11
E5	VSS	VSS	R13
E9	VSS	VSS	R15
E12	VSS	VSS	R17
E13	VSS	VSS	R19
E16	VSS	VSS	R23
E19	VSS	VSS	R25
E22	VSS	VSS	R27
E25	VSS	VSS	R32
E26	VSS	VSS	R34
E29	VSS	VSS	R36
E31	VSS	VSS	R38
F1	VSS	VSS	T3
F4	VSS	VSS	T6
F7	VSS	VSS	T8
F8	VSS	VSS	AR28
F11	VSS	VSS	T12
F14	VSS	VSS	T14
F17	VSS	VSS	T16
F21	VSS	VSS	T18
F24	VSS	VSS	T20
F27	VSS	VSS	T22
F30	VSS	VSS	T24
G3	VSS	VSS	T26
G6	VSS	VSS	T28
G15	VSS	VSS	T31
G18	VSS	VSS	T33
G20	VSS	VSS	T35
G28	VSS	VSS	T37
H2	VSS	VSS	U3
H5	VSS	VSS	U6
H7	VSS	VSS	U9
H8	VSS	VSS	U13
H10	VSS	VSS	U19
H16	VSS	VSS	U21
H18	VSS	VSS	U23
H20	VSS	VSS	U25
H22	VSS	VSS	U27
H24	VSS	VSS	U30
H26	VSS	VSS	U32
H28	VSS	VSS	U34
H30	VSS	VSS	U36
H31	VSS	VSS	U38
J1	VSS	VSS	V2
J4	VSS	VSS	V5
J9	VSS	VSS	V8
J11	VSS	VSS	V10
J13	VSS	VSS	V12
J15	VSS	VSS	V20
J17	VSS	VSS	V22
J19	VSS	VSS	V24
J21	VSS	VSS	V26
J23	VSS	VSS	V28
J25	VSS	VSS	V31
J27	VSS	VSS	V33
J29	VSS	VSS	V35
J32	VSS	VSS	V37
K2	VSS	VSS	W1
K6	VSS	VSS	W4
K8	VSS	VSS	W7
K10	VSS	VSS	W9
K12	VSS	VSS	W11
K14	VSS	VSS	W13
K16	VSS	VSS	W19
K18	VSS	VSS	W25
K20	VSS	VSS	W27
K22	VSS	VSS	W29
K24	VSS	VSS	W34
K26	VSS	VSS	W36
L1	VSS	VSS	W38
L5	VSS	VSS	Y3
L9	VSS	VSS	Y6
L11	VSS		
L13	VSS		

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

XJ784S4GAALY

DGND DGND

U59R

Ground/VSS2

Y8	VSS	VSS	AH30
Y10	VSS	VSS	AH32
Y12	VSS	VSS	AH35
Y14	VSS	VSS	AJ3
Y20	VSS	VSS	AJ6
Y22	VSS	VSS	AJ9
Y24	VSS	VSS	AJ11
Y30	VSS	VSS	AL1
Y32	VSS	VSS	AK11
Y33	VSS	VSS	AK12
Y35	VSS	VSS	AL4
Y37	VSS	VSS	AJ27
AA2	VSS	VSS	AJ22
AA5	VSS	VSS	AJ31
AA9	VSS	VSS	AK15
AA11	VSS	VSS	AK10
AA13	VSS	VSS	AK17
AA19	VSS	VSS	AK16
AA21	VSS	VSS	AK18
AA25	VSS	VSS	AK19
AA29	VSS	VSS	AK22
AA34	VSS	VSS	AK24
AA36	VSS	VSS	AK23
AA38	VSS	VSS	AK28
AB1	VSS	VSS	AK30
AB5	VSS	VSS	AK32
AB8	VSS	VSS	AM3
AB10	VSS	VSS	AL12
AB12	VSS	VSS	AL13
AB14	VSS	VSS	AL15
AB20	VSS	VSS	AL17
AB22	VSS	VSS	AL19
AB24	VSS	VSS	AL21
AB28	VSS	VSS	AM32
AB30	VSS	VSS	AN31
AB32	VSS	VSS	AN34
AB35	VSS	VSS	AL29
AB37	VSS	VSS	AL31
AC2	VSS	VSS	AM6
AC6	VSS	VSS	AM11
AC9	VSS	VSS	AM13
AC11	VSS	VSS	AM15
AC13	VSS	VSS	AM18
AC15	VSS	VSS	AM20
AC17	VSS	VSS	AM23
AC19	VSS	VSS	AP33
AC21	VSS	VSS	AM38
AC23	VSS	VSS	AN1
AC25	VSS	VSS	AN4
AC27	VSS	VSS	AN7
AC29	VSS	VSS	AN10
AC31	VSS	VSS	AN12
AD1	VSS	VSS	AN14
AD4	VSS	VSS	AN16
AD8	VSS	VSS	AN19
AD10	VSS	VSS	AN22
AD12	VSS	VSS	AN25
AD14	VSS	VSS	AR31
AD16	VSS	VSS	AR34
AB33	VSS	VSS	AR37
AD20	VSS	VSS	AP3
AD22	VSS	VSS	AP6
AD24	VSS	VSS	AP9
AD26	VSS	VSS	AP12
AD28	VSS	VSS	AP15
AD30	VSS	VSS	AP18
AD32	VSS	VSS	AP21
AD35	VSS	VSS	AP24
AE2	VSS	VSS	AT27
AE5	VSS	VSS	AT30
AE11	VSS	VSS	AP36
AE15	VSS	VSS	AT33
AE17	VSS	VSS	AR1
AE19	VSS	VSS	AR4
AE21	VSS	VSS	AR7
AE23	VSS	VSS	AR10
AE25	VSS	VSS	AR13
AE27	VSS	VSS	AR16
AE29	VSS	VSS	AR19
AE31	VSS	VSS	AR22
AF3	VSS	VSS	AR25
AF6	VSS	VSS	AU28
AF8	VSS	VSS	AU31
AF10	VSS	VSS	AU34
AF12	VSS	VSS	AT3
AF14	VSS	VSS	AT6
AF16	VSS	VSS	AT9
M29	VSS	VSS	AT12
AF20	VSS	VSS	AT15
AF22	VSS	VSS	AT18
AF24	VSS	VSS	AT21
AF26	VSS	VSS	AT24
AF28	VSS	VSS	AU37
AF30	VSS	VSS	AT36
AF32	VSS	VSS	AU1
AG1	VSS	VSS	AU4
AG4	VSS	VSS	AU7
AG7	VSS	VSS	AU10
AG9	VSS	VSS	AU13
N32	VSS	VSS	AU16
AG15	VSS	VSS	AU19
AG19	VSS	VSS	AU22
AH19	VSS	VSS	AU25
AG25	VSS	VSS	AV29
AG27	VSS	VSS	AU38
AG29	VSS	VSS	AV1
AG31	VSS	VSS	AV2
AH2	VSS	VSS	AV5
AH5	VSS	VSS	AV8
AH8	VSS	VSS	AV11
AH10	VSS	VSS	AV14
AH14	VSS	VSS	AV17
AH22	VSS	VSS	AV20
AH23	VSS	VSS	AV23
AH26	VSS	VSS	AV26
AJ8	VSS	VSS	AV32
AP27	VSS	VSS	AV35
AP30	VSS	VSS	AK25
		VSS	AK27
		VSS	AM25
		VSS	AM27
		VSS	AL10
		VSS	AL14
		VSS	AL18
		VSS	AM30
		VSS	AN28
		VSS	AL26

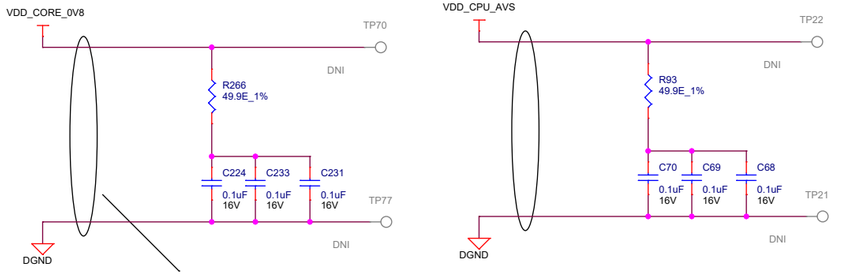
General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<tbd>

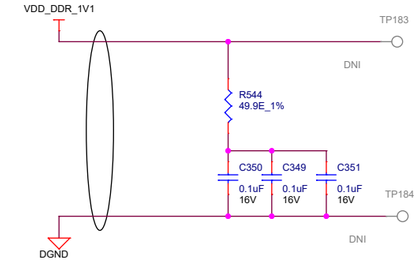
XJ784S4GAALY

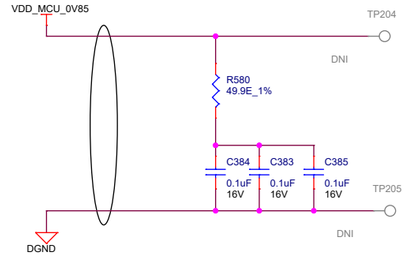
DGND DGND

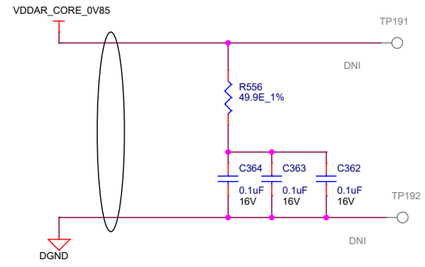
SoC Supply Noise Kelvin Sensing

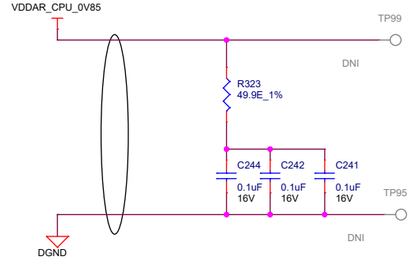


Route supply & Gnd connections from SoC PoL as a pseudo differential pair to TPs near R & C termination for easy access









Project : J7 EVM		Title: SOC GROUND
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 29 of 88

PMIC

"PCB Notes":
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:
1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.

Route as Pseudo diff pair traces
(See "PCB Notes")

U30 CSD16407Q5
VSYS_3V3
R80 240E
R78 240E
VCCA_3V3
TP30
FL41 1uF
FL40 1uF
C985 2.2uF 0603 6.3V
C963 0.1uF 16V 0402
VCCA_3V3_DDR
C1060 10uF 16V 0805
C1059 10uF 16V 0805
C293 10uF 16V 0805
C294 10uF 16V 0805
FL47 1uF
FL48 1uF
C973 2.2uF 0603 6.3V
C278 10uF 16V 0805
C261 10uF 16V 0805
C928 10uF 16V 0805
C260 10uF 16V 0805
C929 10uF 16V 0805
C1001 10uF 16V 0805
C1015 2.2uF 0603 6.3V
C1025 2.2uF 0603 6.3V
C1035 2.2uF 0603 6.3V
C1039 2.2uF 0603 6.3V
R154 0E
VSYS_SENSE
D30 SZMM3Z10VST1G
DGND

U68
4 VCCA
48 VIO_IN
26 PVIN_B1
17 PVIN_B2
45 PVIN_B3
54 PVIN_B4
35 PVIN_B5
8 PVIN_LDO4
10 PVIN_LDO3
12 PVIN_LDO12
52 OVPGDRV
51 VSYS_SENSE
36 VBACKUP
40 OSC32KCAP
38 OSC32KIN
39 OSC32KOUT
1 AMUXOUT
30 SDA_I2C1/SDI_SPI
31 SCL_I2C1/SCK_SPI
20 nPWRON/ENABLE
14 nINT
25 nRSTOUT
29 EN_DRV
32 GPIO1
33 GPIO2
46 GPIO3
47 GPIO4
23 GPIO5
24 GPIO6
18 GPIO7
41 GPIO8
19 GPIO9
42 GPIO10
53 GPIO11
57 GND
5 REFGND1
6 REFGND2
TPS6594133ARWERQ1

SW_B1A 27
SW_B1B 28
FB_B1 22
FB_Voltage at Load
VDD_PMIC_BUCK_SW1
L34 0.22uH TFM252012ALMAR22MTAA
VDD_DDR_1V1
C298 47uF 1210 6.3V
C1071 47uF 1210 6.3V

SW_B2A 15
SW_B2B 16
FB_B2 21
FB_Gnd/Ref at Load
VDD_PMIC_BUCK_SW2
L33 0.22uH TFM252012ALMAR22MTAA
C1072 47uF 1210 6.3V
C299 47uF 1210 6.3V

SW_B3A 43
SW_B3B 44
FB_B3 49
VDD_RAM_0V85
VDD_PMIC_BUCK_SW3
L31 0.22uH TFM252012ALMAR22MTAA
VDD_RAM_0V85_REG
C254 47uF 1210 6.3V
C891 47uF 1210 6.3V

SW_B4A 55
SW_B4B 56
FB_B4 50
VDD_IO_1V8
VDD_PMIC_BUCK_SW4
L30 0.22uH TFM252012ALMAR22MTAA
VDD_IO_1V8_REG
C253 47uF 1210 6.3V
C892 47uF 1210 6.3V

SW_B5A 34
FB_B5 37
VDD_MCU_0V85
VDD_PMIC_BUCK_SW5
L32 0.22uH TFM252012ALMAR22MTAA
VDD_MCU_0V85_REG
C273 47uF 1210 6.3V
C994 47uF 1210 6.3V

Note: Keepout needs to be provided for the VDD_DDR_1V1 and Gnd vias of feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD_DDR_1V1 and DGND feedback traces

VOUT_LDOVINT 2
VOUT_LDOVRTC 3
VOUT_LDO1 13
VOUT_LDO2 11
VOUT_LDO3 9
VOUT_LDO4 7
TP308 VINT_PMIC_1V8
TP310 VRTC_PMIC_1V8
VDD_MCUIO_1V8_REG
VDD_MCUIO_3V3_REG
VDA_DLL_0V8_REG
VDA_MCU_1V8_REG
C267 2.2uF 0603 6.3V
C271 2.2uF 0603 6.3V
C288 2.2uF 0603 6.3V
C286 2.2uF 0603 6.3V
C281 2.2uF 0603 6.3V
C277 2.2uF 0603 6.3V

VCCA_3V3
5988170107F
LD10
R433 220E 1%
TP150
VDA_MCU_1V8 R1033 10K_1% 0402
VDD_DDR_1V1 R557 10K_1% 0402
VCCA_3V3 R1063 DNI 0402
VDA_MCU_1V8 R1062 10K_1% 0402
VDD_MCUIO_1V8 R448 10K_1% 0402

C977 0.1uF 0402 16V
C941 9pF 0402 50V
C917 9pF 0402 50V
ECS-.327-9-34QCS-TR Y10 32.768KHz
LEOA_OSC32KCAP
LEOA_OSC32KIN
LEOA_OSC32KOUT
TP153 TP220 TP158 TP127

TP130 AMUXOUT_A
(31,32,34,79) H_WKUP_I2C0_SDA
(31,32,34,79) H_WKUP_I2C0_SCL
(79) PMIC_ENABLE
(18) H_MCU_INTn
(43) H_MCU_PORz
H_MCU_INTn
H_MCU_PORz
EN_DRV_OUT
(20,50) MCU_I2C0_SCL
(20,50) MCU_I2C0_SDA
(20) SOC_SAFETY_ERRZ
R1035 0E 0402 PMIC_GPIO3
SOC_PWR_WKn
R1026 0E 0402 PMIC_GPIO4
(33) EN_GPIO_RET_3V3
(14,33) EN_DDR_RET_1V1
(20) MCU_SAFETY_ERRZ
R1081 0E PMIC_GPIO7
R398 0E 0402 PMIC_GPIO8
(33,34) EN_3V3_VIO
(33,34) MCU_PWRGRP_IRQn
(43) H_SOC_PORz
(79) PMIC_WDOG_DISABLE
(20) PMIC_POWER_EN1
R1061 DNI 0402
TP123

C1050 0.1uF 0402 16V
R1061 to be mounted during emulator debug requiring SoC to enable PMIC power resource (i.e. VDD_CORE)

(31,32,33,34) MAIN_PWRGRP_IRQn
U234 SN74LVC1G126DBVR
MAIN_PWRGRP_IRQn_BUF
R1089 1K_1% 0402
R1079 10K_1% 0402
(20,44,62) MCU_PORZ_OUT
R1123 0E 0402
SOC_PORZ_OUT
R1111 DNI 0402
(20,36,39,44,50,59,63,70,71,72)
R1122 DNI 0402

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

SoC,Open-Drain, Active Low
VDD_GPIORET_IO_3V3
R647 10K_1% 0402
C427 0.1uF 0402 16V
(20) H_MCU_WK1n
(20) H_MAIN_WK0n
R646 0E 0402
R645 DNI 0402
MCU_WK1n
U134 SN74LVC1G07DRLRG4
VCCA_3V3
R627 10K_1% 0402
SOC_PWR_WKn
U137 BSS138LT1G
(57) CAN_WKUP
R658 0E 0402
R_CAN_WKUP
R659 DNI 0402

SN74LVC1G07 is used to isolate power from PMIC to SoC when SoC is powered off

Active High 1.8V logic

VSYS_3V3
R1301 10K_1% 0402
C1268 0.1uF 0402 16V
(42) PB_CAN_WAKEn
0E R1302
U278 SN74LVC1G07DRLRG4
SOC_PWR_WKn

Project : J7 EVM	TEXAS INSTRUMENTS	Title: PMIC A
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 30 of 88

VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_xxx_HCPS_VOSNS/_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

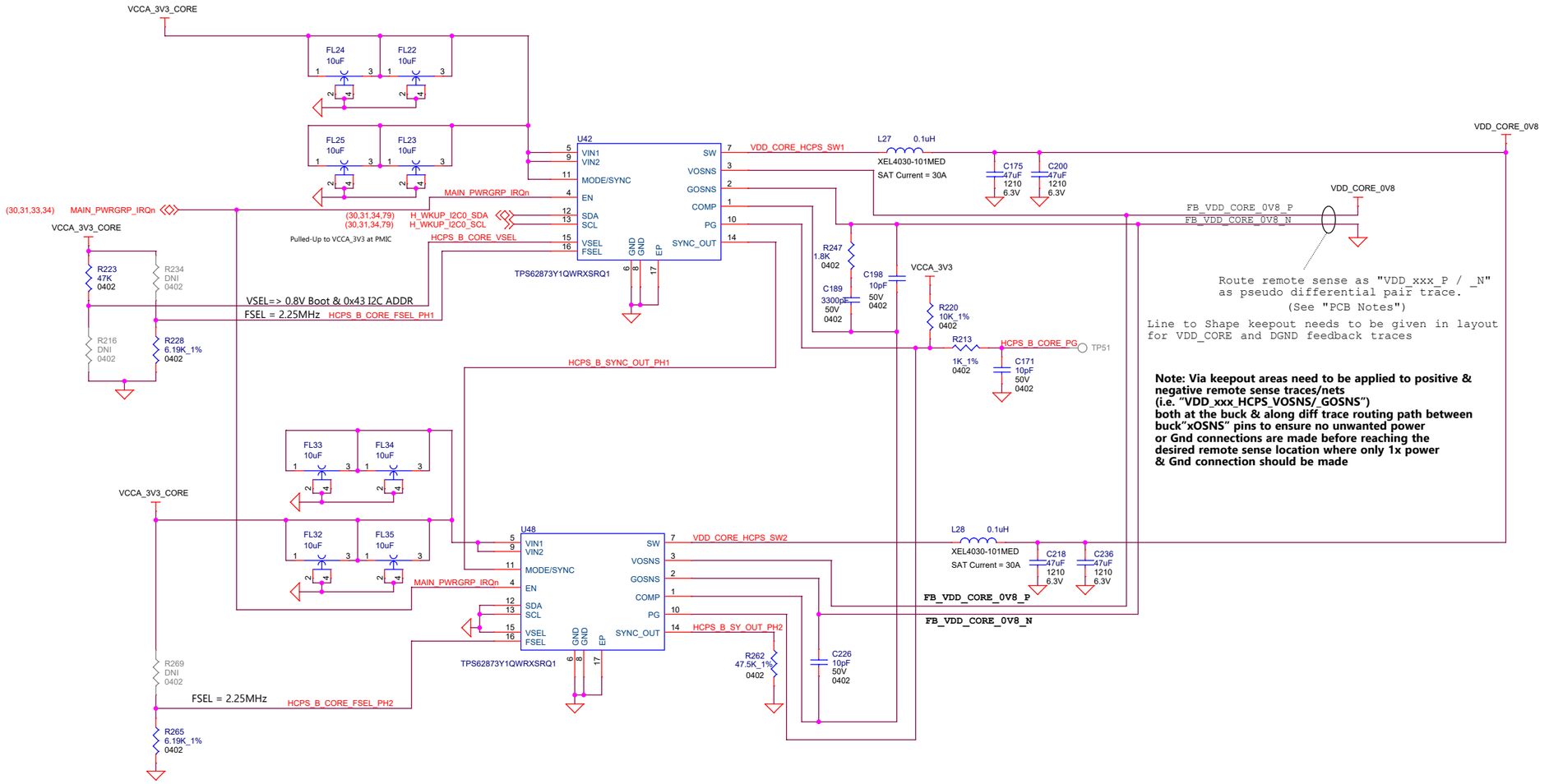
Route remote sense as "VDD_xxx_P / _N" as pseudo differential pair trace. (See "PCB Notes")

Note: A 2nd alternative remote sense location & diff trace pair have been shown to enable TI internal evaluation & testing only. End products should use remote sense attached under SoC in middle of BGA power ball field. Any improved performance due to 2nd remote sense location will be captured in future EVM SCH once test results are verified.

VCCA_3V3_CPU_AVS
FL11 10uF
FL12 10uF
FL10 10uF
FL13 10uF
(30,32,33,34) MAIN_PWRGRP_IRQn
U35
VIN1
VIN2
MODE/SYNC
EN
SDA
SCL
VSEL
FSEL
SW
VOSNS
GOSNS
COMP
PG
SYNC_OUT
GND
GND
EP
TPS62873Y1QWRXSRQ1
(30,32,34,79) H_WKUP_I2C0_SDA
(30,32,34,79) H_WKUP_I2C0_SCL
HCPS_A_CPU_VSEL
HCPS_A_CPU_FSEL_PH1
VDD_CPU_HCPS_SW1
L24 0.1uH
XEL4030-101MED
SAT Current = 30A
C178 47uF 1210 6.3V
C179 47uF 1210 6.3V
VDD_CPU_HCPS_VOSNS
VDD_CPU_HCPS_GOSNS
R186 1.8K 0402
C158 10pF 50V 0402
C155 3300pF 50V 0402
R908 10K_1% 0402
R907 1K_1% 0402
HCPS_A_CPU_PG
TP38
C705 10pF 50V 0402
VDD_CPU_AVS
R208 0E
R203 0E
FB1_VDD_CPU_AVS_P
FB1_VDD_CPU_AVS_N
R205 DNI
R201 DNI
FB2_VDD_CPU_AVS_P
FB2_VDD_CPU_AVS_N
R196 DNI 0402
R194 DNI 0402
R197 6.19K_1% 0402
R195 6.19K_1% 0402
VSEL=> 0.8V Boot & 0x40 I2C ADDR
FSEL = 2.25MHz
VCCA_3V3
R206 20K_1% 0402
R982 10K_1%
U216
U217
VDA_DLL_0V8
RE1J002YNTCL
DGND
HCPS_A_SYNC_OUT_PH1
FL16 10uF
FL17 10uF
FL15 10uF
FL14 10uF
U36
MAIN_PWRGRP_IRQn
FSEL = 2.25MHz
HCPS_A_CPU_FSEL_PH2
VDD_CPU_HCPS_SW2
L25 0.1uH
XEL4030-101MED
SAT Current = 30A
C180 47uF 1210 6.3V
C181 47uF 1210 6.3V
FB_VDD_CPU_AVS_P
FB_VDD_CPU_AVS_N
C154 10pF 50V 0402
R188 DNI 0402
R189 6.19K_1% 0402
HCPS_A_SYNC_OUT_PH2
R190 47.5K_1% 0402
FL18 10uF
FL19 10uF
FL20 10uF
FL21 10uF
U37
MAIN_PWRGRP_IRQn
FSEL = 2.25MHz
HCPS_A_CPU_FSEL_PH3
VDD_CPU_HCPS_SW3
L26 0.1uH
XEL4030-101MED
SAT Current = 30A
C182 47uF 1210 6.3V
C183 47uF 1210 6.3V
FB_VDD_CPU_AVS_P
FB_VDD_CPU_AVS_N
C156 10pF 50V 0402
R191 DNI 0402
R192 6.19K_1% 0402
HCPS_A_SYNC_OUT_PH3
R193 47.5K_1% 0402

Project : J7 EVM	TEXAS INSTRUMENTS	Title: HCPS A
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 31 of 88

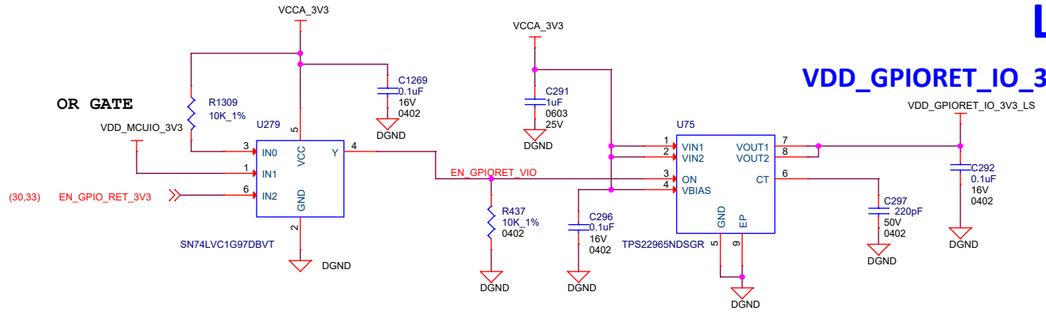
VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



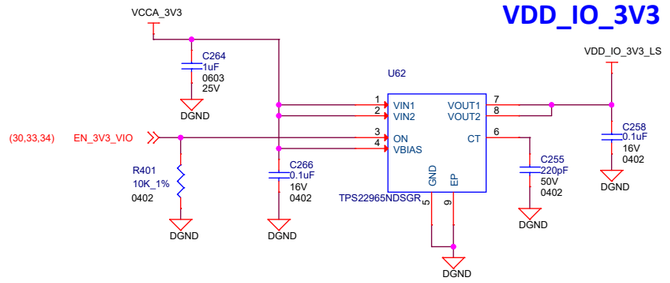
Project : J7 EVM	TEXAS INSTRUMENTS	Title: HCPS B
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 32 of 88

LOAD SWITCHES

VDD_GPIORET_IO_3V3

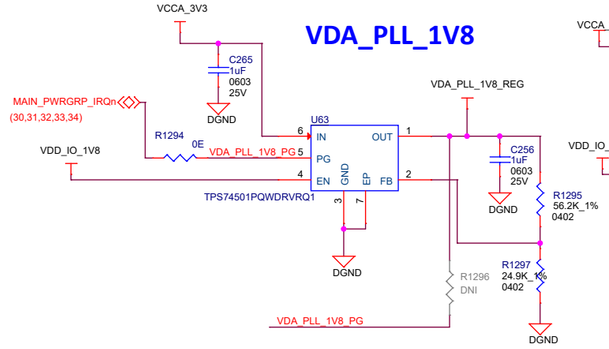


VDD_IO_3V3

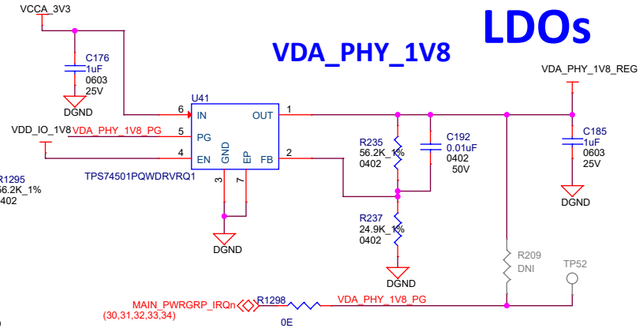


LDOs

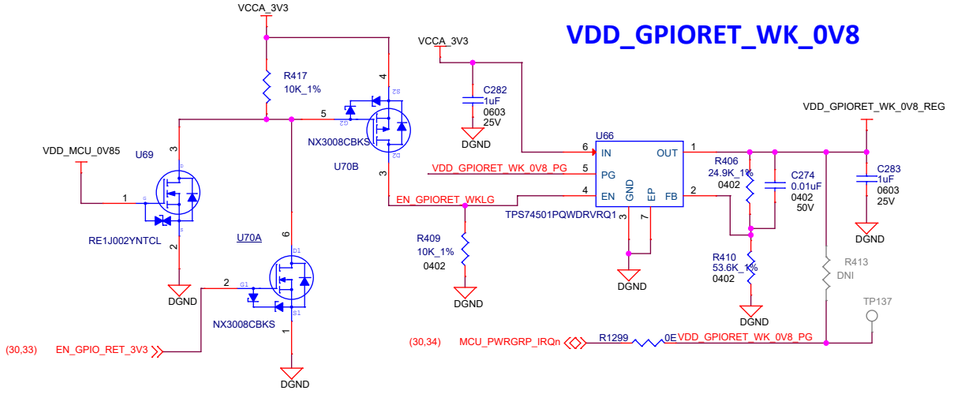
VDA_PLL_1V8



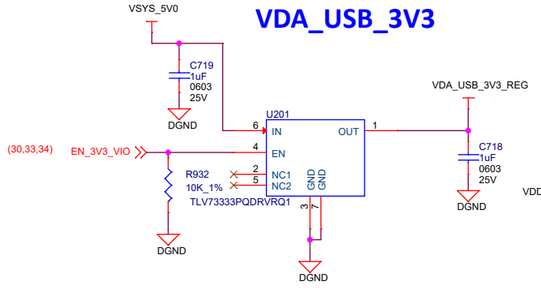
VDA_PHY_1V8



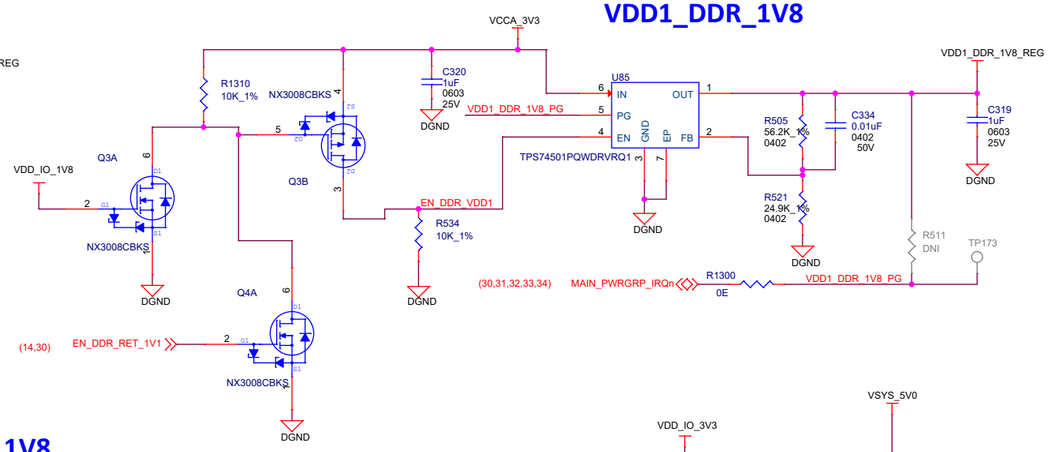
VDD_GPIORET_WK_0V8



VDA_USB_3V3



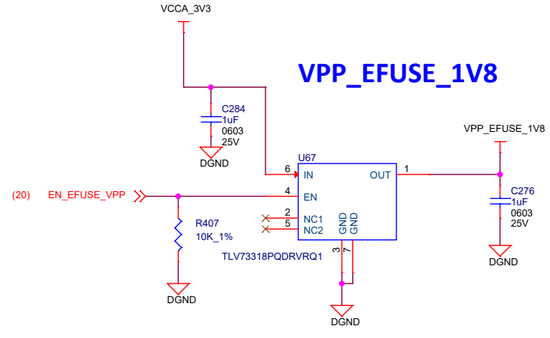
VDD1_DDR_1V8



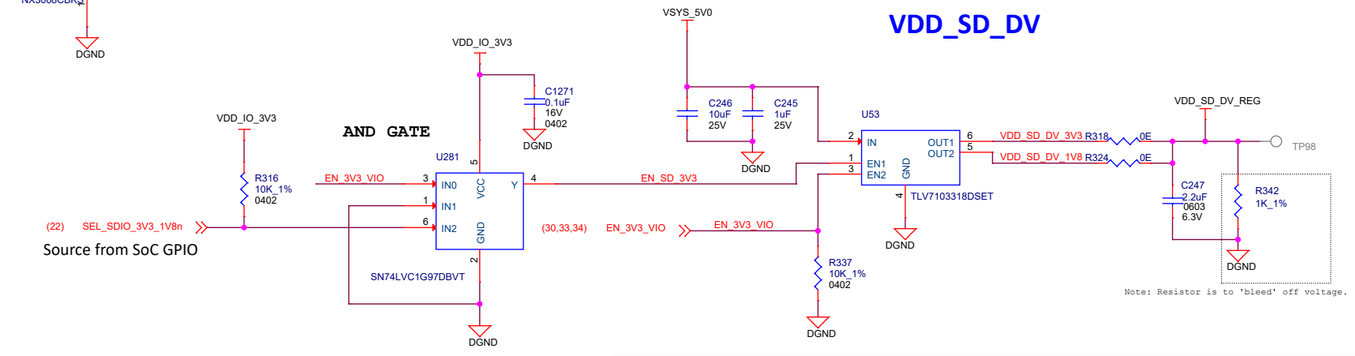
EN_GPIORET_VIO & EN_GPIORET_WKLG & EN_DDR_VDD1 Truth table

"OR" Gate Logic			States		
X	Y	OUTPUT	Input - X	Input - Y	Output
0	0	0	OFF	OFF	OFF
0	1	1	OFF	ON	ON
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON

VPP_EFUSE_1V8



VDD_SD_DV



Note: Resistor is to 'bleed' off voltage.

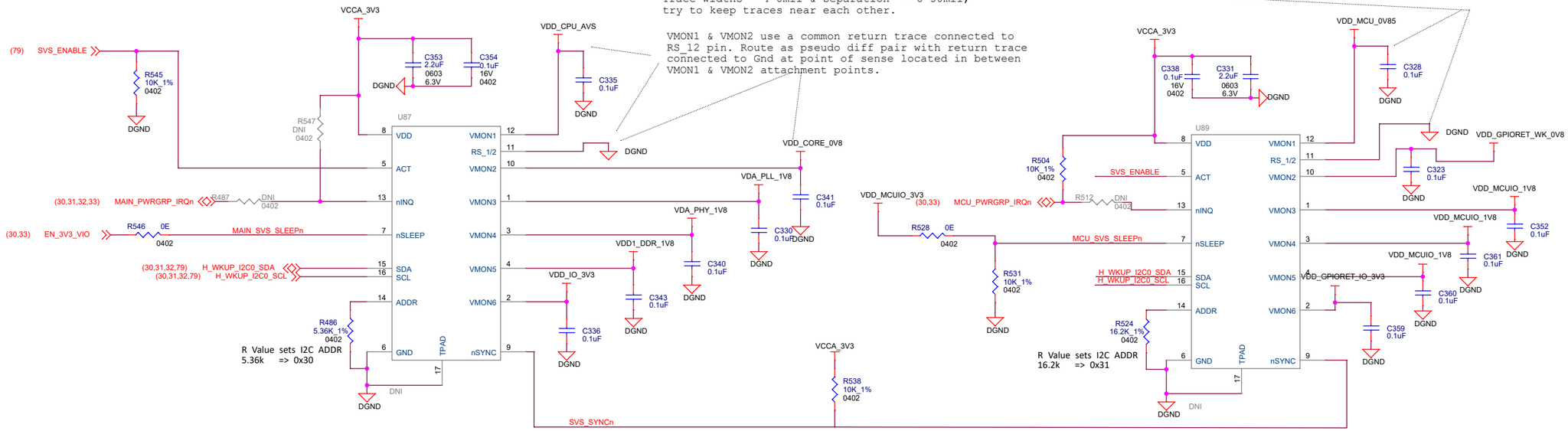
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC LDO's and LD_SWITCHES
	Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
	Date: Friday, May 05, 2023	Sheet 33 of 88

Safety Voltage Supervisors

Power rail voltage > 1.0V can
connect to VMON3-6 inputs
using single-ended traces.
Trace widths = 4-8mil, as short as possible
& try to avoid routing near HF signals.

Any power rail voltage < 1.0V should
connect to VMON1 & VMON2 inputs
using "Pseudo Diff Pair Trace" routes.
Trace widths = 4-8mil & Separation = 8-50mil,
try to keep traces near each other.

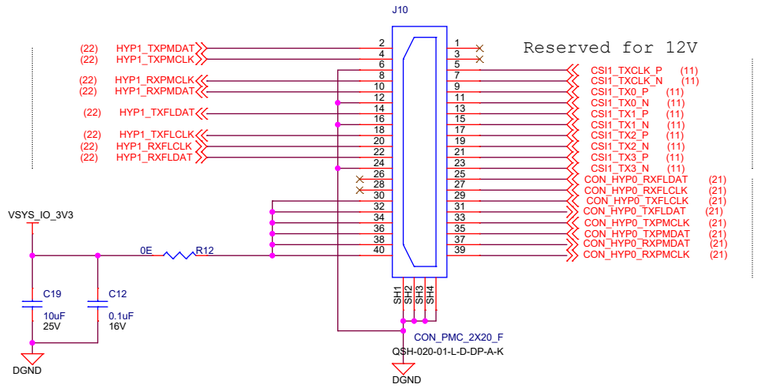
VMON1 & VMON2 use a common return trace connected to
RS_12 pin. Route as pseudo diff pair with return trace
connected to Gnd at point of sense located in between
VMON1 & VMON2 attachment points.



Project : J7 EVM	TEXAS INSTRUMENTS	Title: 2:1 MUX's
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 34 of 88

HYPERLINK SIDEBAND CONNECTOR

Hyperlink1
Sideband Interface

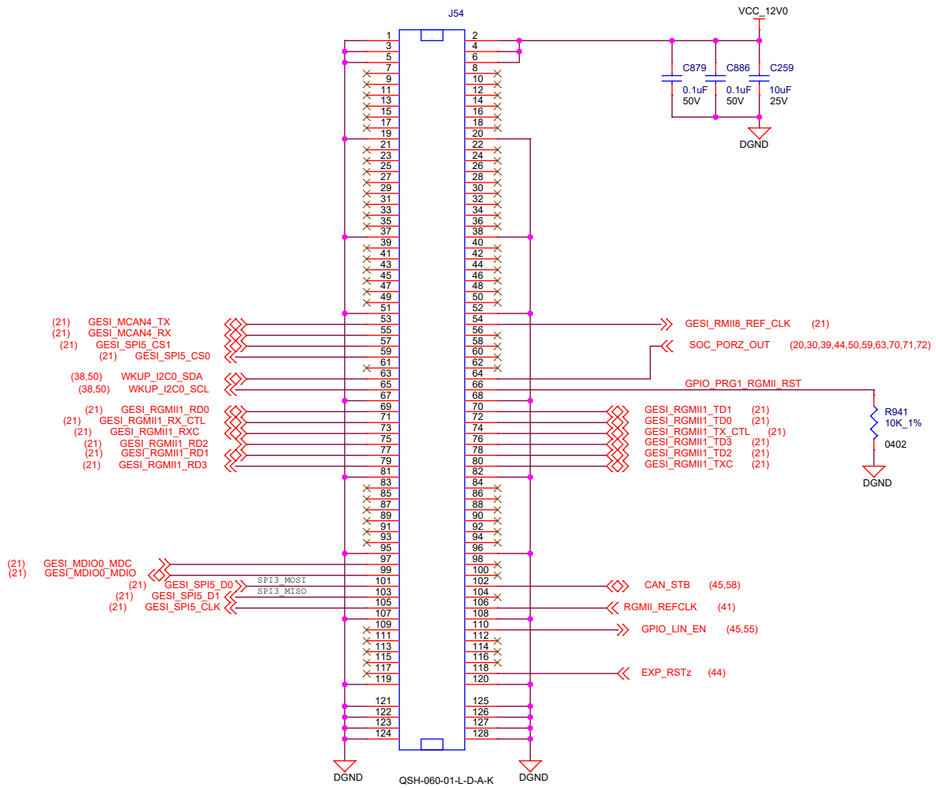


CSI-TX Interface

Hyperlink0
Sideband Interface

Project : J7 EVM	Texas Instruments	Title: HYPERLINK & CSI TX CONNECTOR	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 35 of 88

GESI_EXP_CONN

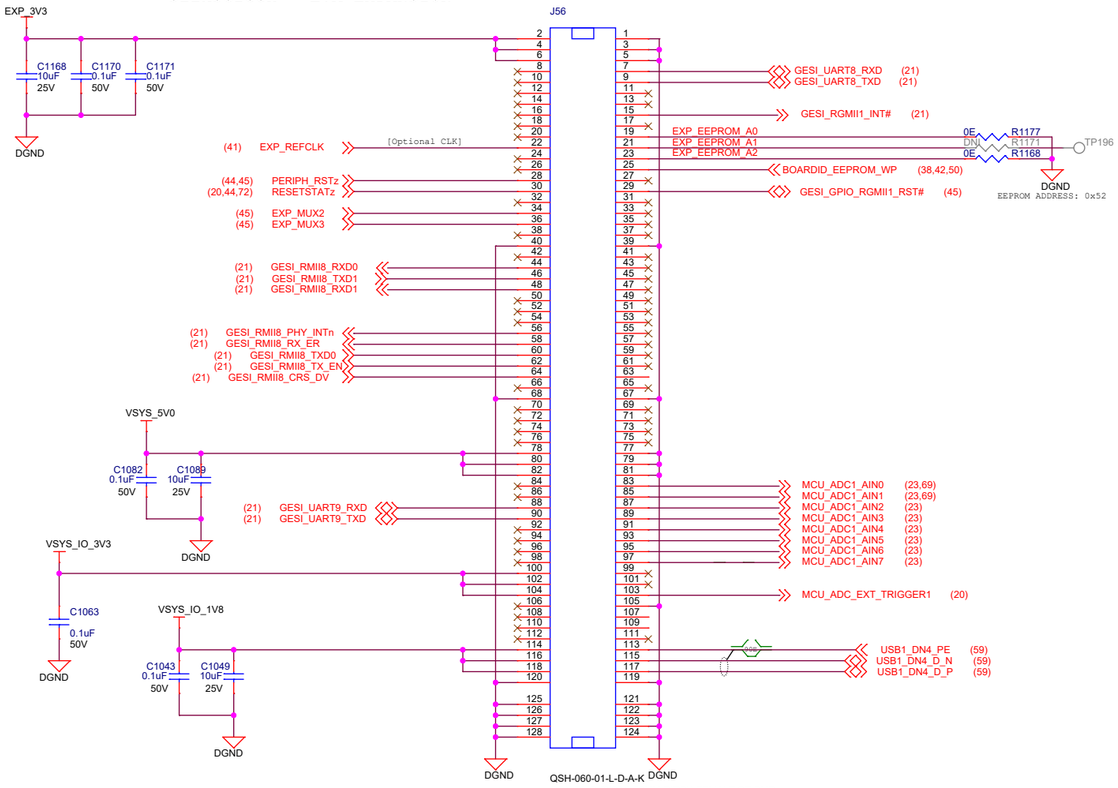


CON PMC 2X60 0.50MM PITCH FEMALE ST SMD

Place test point near Expansion connector

(21) GESI_RMII8_CLKOUT — TP117

Silkscreen "EVM EXPANSION"



CON PMC 2X60 0.50MM PITCH FEMALE ST SMD

Project : J7 EVM		Title: GESI_EXP_CONN
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 36 of 88

CSI2 EXPANSION CONNECTORS

Level Translation for LVCMOS

VSYS_IO_3V3 — R522 200K — VREF2_CSI — U88 PCA9306DCTR (VREF2, VREF1, EN, SCL2, SCL1, SDA2, SDA1, GND) — VCC_CSI_IO — R510 10K — R501 10K

(22,45) I2C5_SCL — CSI2_I2C_SCL_DV

(22,45) I2C5_SDA — CSI2_I2C_SDA_DV

C339 0.1uF 50V — DGND — C342 0.1uF 50V — DGND

VSYS_IO_3V3 — C317 0.1uF 50V — DGND — U80 SN74AVC4T245PW (VCCB, VCCA, 1B1, 1B2, 2B1, 2B2, 1A1, 1A2, 2A1, 2A2, 1DIR, 2DIR, 1OE, 2OE, GND2, GND1) — VCC_CSI_IO — C316 0.1uF 50V — DGND

(45) CSI2_EXP_A_GPIO0 — CSI2_A_GPIO0_DV

(41) CSI2_REFCLK — CSI2_A_REFCLK_DV

CSI2_B_REFCLK_DV

(45) CSI2_EXP_RSTz — R471 0E — CSI2_RSTz_DV

R469 10K — DGND

DIR LOW: 1B --> 1A
LOW: 2B --> 2A

VSYS_IO_3V3 — C1075 0.1uF 50V — DGND — TP225 — VCC_CSI_IO — C1105 0.1uF 50V — DGND — U242 (VCCB, VCCA, PAD, GND, OE)

(45) CSI2_EXP_A_GPIO1 — CSI2_A_GPIO1_DV

(22) CSI2_EXP_A_GPIO2 — CSI2_A_GPIO2_DV

(45) CSI2_EXP_A_GPIO3 — CSI2_A_GPIO3_DV

(22) CSI2_EXP_A_GPIO4 — CSI2_A_GPIO4_DV

(45) CSI2_EXP_B_GPIO1 — CSI2_B_GPIO1_DV

(45) CSI2_EXP_B_GPIO2 — CSI2_B_GPIO2_DV

(45) CSI2_EXP_B_GPIO3 — CSI2_B_GPIO3_DV

(45) CSI2_EXP_B_GPIO4 — CSI2_B_GPIO4_DV

10 TXS0108_OE R1134 10K VCC_CSI_IO

TXS0108ERGYR — DGND

CSI2_EXP_A_GPIO2, 4 are connected to SOC GPIO
and others are from IO expander

Auxiliary 12V Power Output for CSI2

VCC_12V0 — J47 — 1757242
CON TERMINAL BLOCKS 1X2 5.08MM PITCH MALE RT TH

DGND

Silkscreen "12V PWR OUT"

VCC_12V0 — C410 0.1uF 50V — C407 10uF 25V — DGND

J57

CSI2_I2C_SCL_DV [SCL] — CSI2_I2C_SDA_DV [SDA] — CSI2_A_GPIO0_DV [GPIO/PWM_A] — CSI2_A_GPIO1_DV [GPIO/PWM_B] — CSI2_A_REFCLK_DV [25M REFCLK] — CSI2_RSTz_DV [RESETz] — CSI2_A_GPIO2_DV [MOSI/GPIO] — CSI2_A_GPIO3_DV [SCLK/GPO] — CSI2_A_GPIO4_DV [CS/GPIO] — CSI1_RX3_P — CSI1_RX3_N — [3V3] — [VIO]

CSI0_RXCLK_P (11) — CSI0_RXCLK_N (11) — CSI0_RX0_P (11) — CSI0_RX0_N (11) — CSI0_RX1_P (11) — CSI0_RX1_N (11) — CSI0_RX2_P (11) — CSI0_RX2_N (11) — CSI0_RX3_P (11) — CSI0_RX3_N (11)

CSI2 Port 0

CSI1_RXCLK_P (11) — CSI1_RXCLK_N (11) — CSI1_RX0_P (11) — CSI1_RX0_N (11) — CSI1_RX1_P (11) — CSI1_RX1_N (11) — CSI1_RX2_P (11) — CSI1_RX2_N (11) — CSI1_RX3_P (11) — CSI1_RX3_N (11)

CSI2 Port 1

SH1 SH2 SH3 SH4

QSH-020-01-L-D-DP-A-K
CON PMC 2X20 0.50MM PITCH FEMALE ST SMD

Silkscreen "CSI2-EXP"

EXP_3V3 — C1164 0.1uF 50V — C1162 10uF 25V — VCC_CSI_IO — C1165 0.1uF 50V — C1163 10uF 25V — DGND

VCC_12V0 — C906 0.1uF 50V — C937 10uF 25V — DGND

J55

CSI2_I2C_SCL_DV [SCL] — CSI2_I2C_SDA_DV [SDA] — CSI2_B_GPIO1_DV [GPIO/PWM_B] — CSI2_B_REFCLK_DV [25M REFCLK] — CSI2_RSTz_DV [RESETz] — CSI2_B_GPIO2_DV [MOSI/GPIO] — CSI2_B_GPIO3_DV [SCLK/GPO] — CSI2_B_GPIO4_DV [CS/GPIO] — [3V3] — [VIO]

CSI2_RXCLK_P (11) — CSI2_RXCLK_N (11) — CSI2_RX0_P (11) — CSI2_RX0_N (11) — CSI2_RX1_P (11) — CSI2_RX1_N (11) — CSI2_RX2_P (11) — CSI2_RX2_N (11) — CSI2_RX3_P (11) — CSI2_RX3_N (11)

CSI2 Port 2

SH1 SH2 SH3 SH4

QSH-020-01-L-D-DP-A-K
CON PMC 2X20 0.50MM PITCH FEMALE ST SMD

Silkscreen "CSI2-EXP-AUX"

EXP_3V3 — C815 0.1uF 50V — C809 10uF 25V — VCC_CSI_IO — C816 0.1uF 50V — C810 10uF 25V — DGND

LVCMOS IO Voltage Selection

VSYS_5V0 — C1212 10uF 25V — C1213 1uF 10V — DGND

U265 TLV7103318DSET (IN, EN1, EN2, GND, OUT1, OUT2)

VLDO_CSI_3V3 — R1240 0E — VCC_CSI_IO

VLDO_CSI_1V8 — R1241 0E — C1192 2.2uF 10V — R1233 1K_1% — DGND

(42) CSI_VIO_SEL

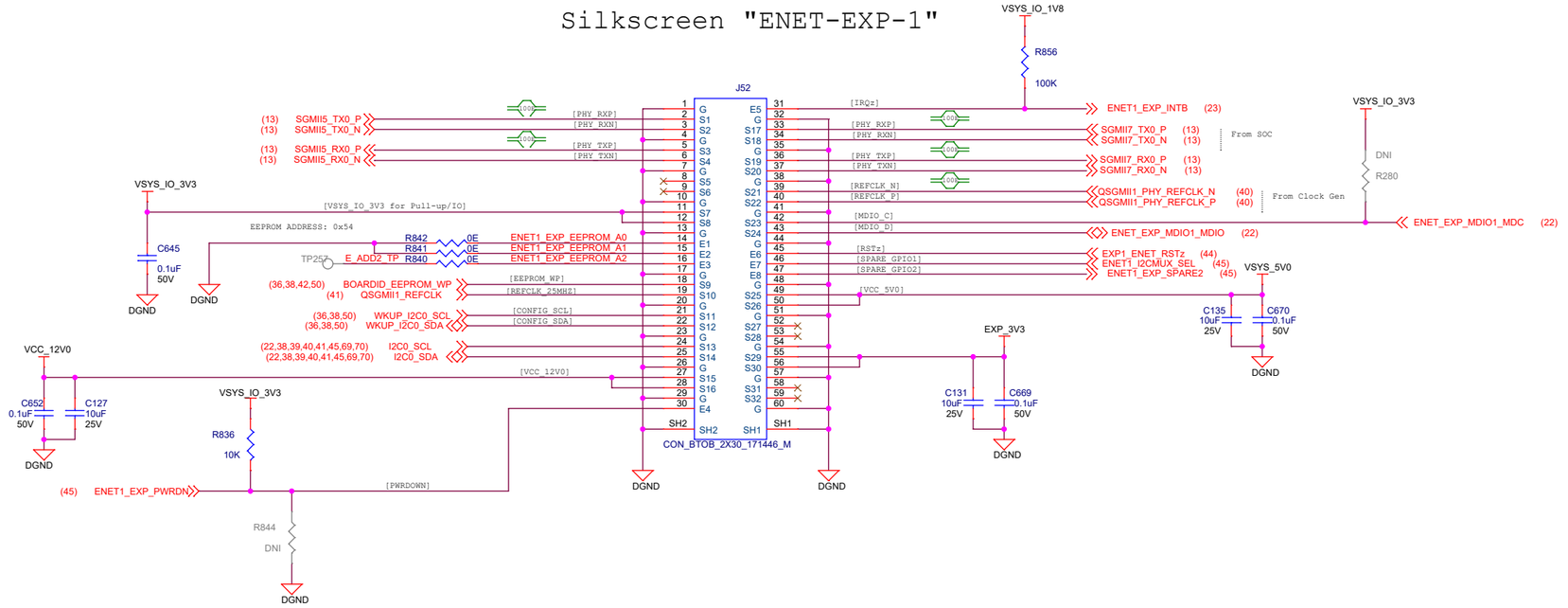
See DIP Switch for Selection Control

Note: Resistor is to 'bleed' off voltage.

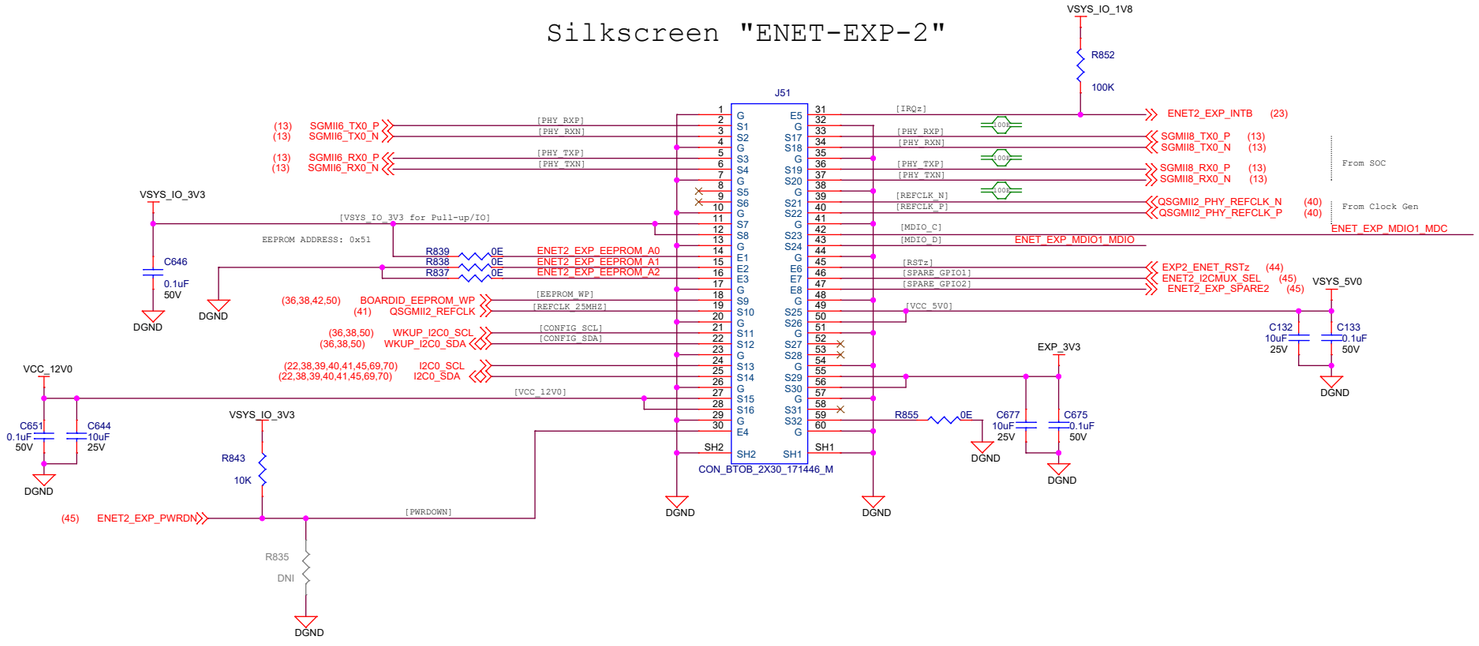
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CSI2 EXPANSION CONNECTORS	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 37 of 88

ENET EXPANSION CONNECTOR

Silkscreen "ENET-EXP-1"

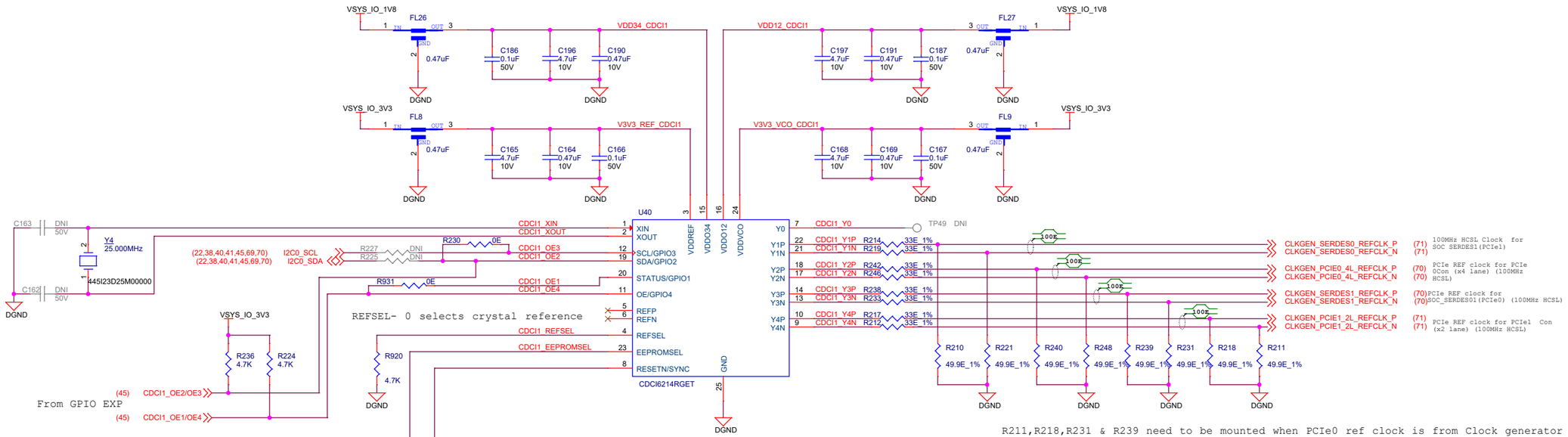


Silkscreen "ENET-EXP-2"



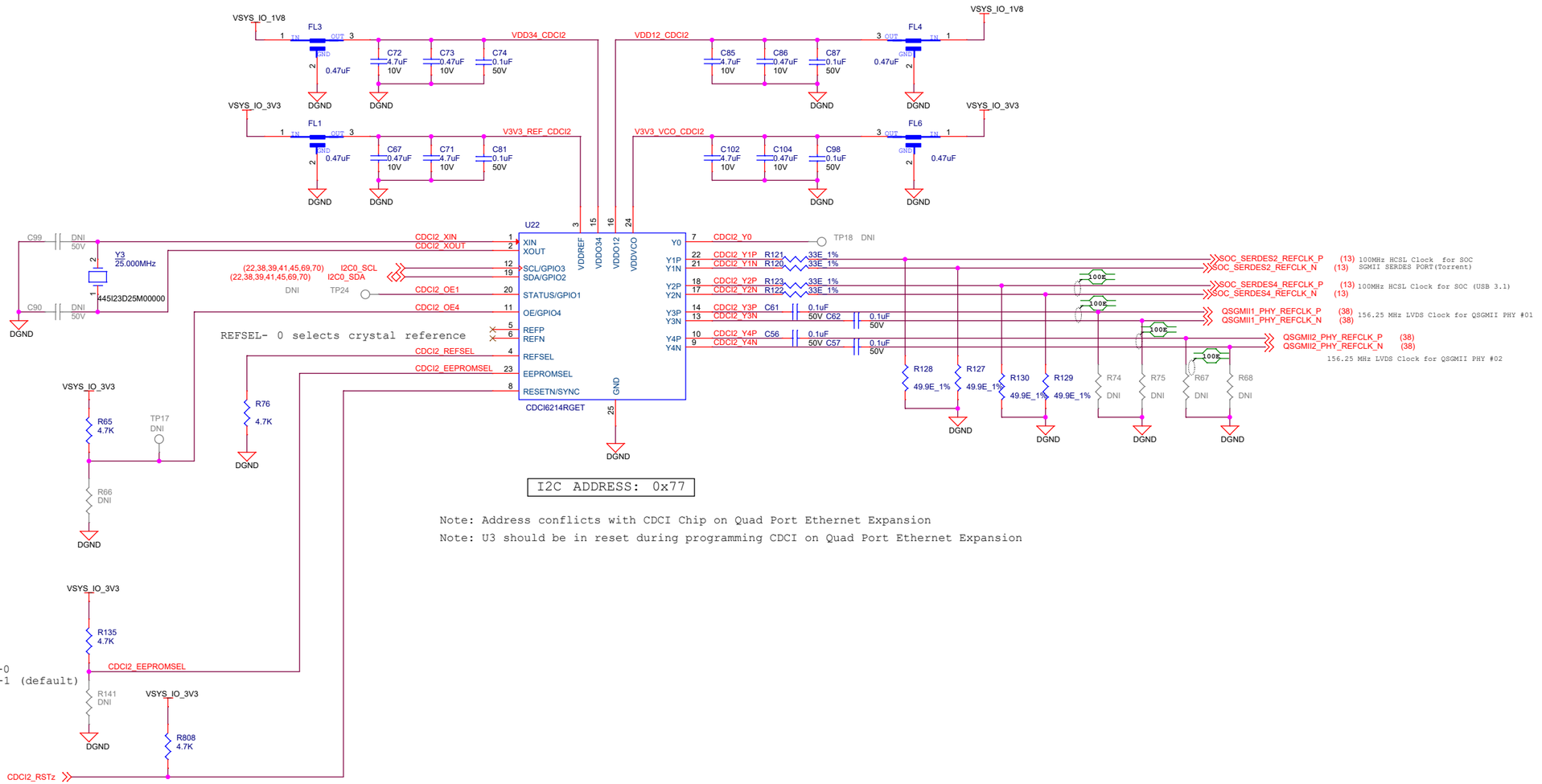
Project : J7 EVM	TEXAS INSTRUMENTS	Title: ENET EXPANSION CONNECTOR
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 38 of 88

SERDES CLOCK GENERATOR #1



Project : J7 EVM	Texas Instruments	Title: SERDES CLOCK GENERATOR #1
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 39 of 88

SERDES CLOCK GENERATOR #2



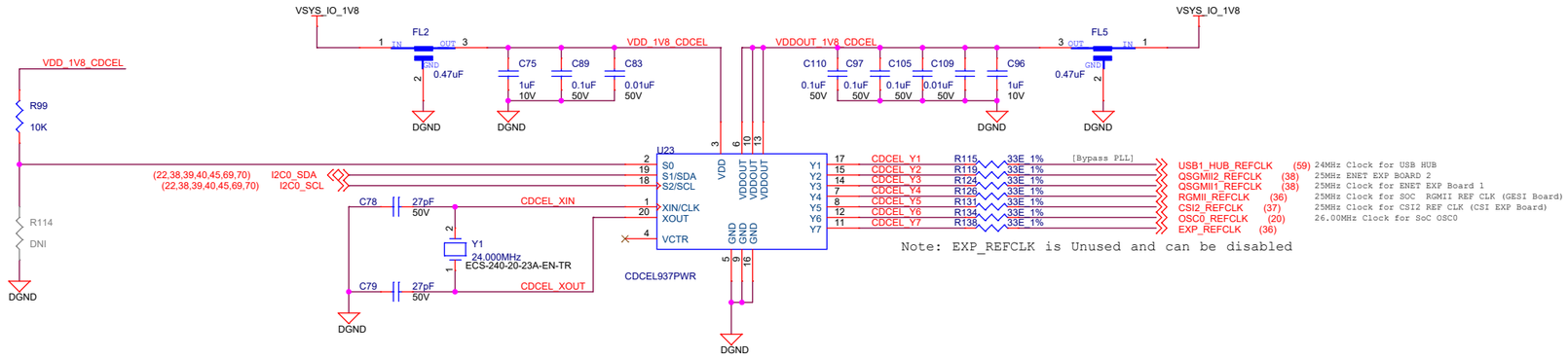
I2C ADDRESS: 0x77

Note: Address conflicts with CDCI Chip on Quad Port Ethernet Expansion

Note: U3 should be in reset during programming CDCI on Quad Port Ethernet Expansion

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES CLOCK GENERATOR #2
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 40 of 88

PERIPHERAL CLOCK GENERATOR



I2C ADDRESS: 0x6D

Project : J7 EVM	TEXAS INSTRUMENTS	Title: PERIPHERAL CLOCK GENERATOR
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 41 of 88

RESET BUTTONs

SILK: "MCU PORZ"

SW14 — 7914G-1-000E — SW_PB_MCU_PORz — DGND

SILK: "MCU WARM RESET"

SW12 — 7914G-1-000E — SW_PB_MCU_RESETz — DGND

SILK: "MAIN PORZ"

SW10 — 7914G-1-000E — SW_PB_PORz — DGND

SILK: "MAIN WARM RESET"

SW9 — 7914G-1-000E — SW_PB_RESETz — DGND

SILK: "SOC INT1"

SW6 — 7914G-1-000E — SW_PB_EXTINTn — DGND

SILK: "SOC INT2"

SW5 — 7914G-1-000E — SW_PB_SYS_IRQz — DGND

SILK: "CAN_WAKE"

SW15 — 7914G-1-000E — PB_CAN_WAKEn (57) — DGND

U98 MAX6818EAP+T

VSYS_3V3, 0.1uF 50V C372, DGND

IN1 PB_MCU_PORz (43)
IN2 PB_MCU_RESETz (43)
IN3 PB_PORz (43)
IN4 PB_RESETz (43)
IN5 PB_EXTINTn
IN6 PB_SYS_IRQz
IN7, IN8 NC

MAX6818_CH# → CH
MAX6818_EN# → EN

R539 DNI — DGND
R568 0E — DGND

U92 SN74LVC1G08DBVRE4

VSYS_IO_3V3, C355 0.1uF 50V, DGND

(53,73) TA_SOC_INT1z — From Test Automation header

To EXT_INTn pin on SoC
SOC_EXTINTn (22)
(SOC_IRQ1#)

U102 SN74LVC1G08DBVRE4

VSYS_MCUIO_3V3, C365 0.1uF 50V, DGND

(53,73) TA_SOC_INT2z — From Test Automation header

SYS_IRQz (20)
(SOC_IRQ2#)

U123 TPS3808G33DBVR

VSYS_3V3, 0.1uF 50V C420, DGND

R585 1K_1%

SENSE, VDD, RESET → VSYSMON_RESET#, MR ← PB_SYS_IRQz, CT, GND

U113 SN74LVC2G74

R589 10K

(20) SYS_MCU_PWRDN

R578 1K_1%

C404 0.1uF 50V

R606 0E

(53,73) TA_POWERDOWNz — From Test automation header

(43,80) SYS_PWR_PG

R623 10K, R612 10K

U130 SN74LVC1G11DCKR

C421 0.1uF 50V

TP226

SYS_MCU_EN (79)

VSYS_MCUIO_3V3, VSYS_IO_3V3, VSYS_3V3

R40–R47 1K_1%

SW2 218-10LPST

OSPI/ONAND_MUX_SEL (18,20)
CANUART_MUX_SEL0 (22,45)
USBC_MODE_SEL1 (45,61)
USBC_MODE_SEL0 (45,61)
PCIe0_4L_MODE_SEL (45,70)
PCIe1_2L_MODE_SEL (45,71)
CSI_VIO_SEL (37)
XDS110_BUF_SELn (53)
BOARDID_EEPROM_WP (36,38,50)
USER_INPUT1 (45)

R32–R41 10K

CONFIG DIP SWITCH

R2 330E, R1 330E

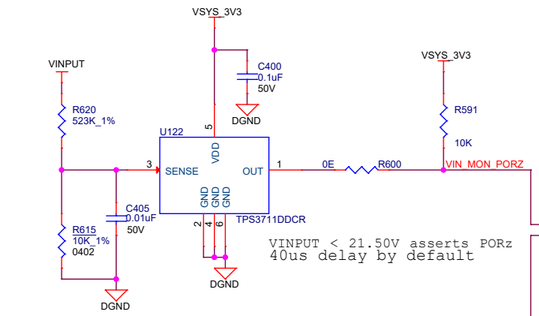
LD3 5988170107F GREEN
LD2 5988170107F GREEN

USER_LED1 (45)
USER_LED2 (45)

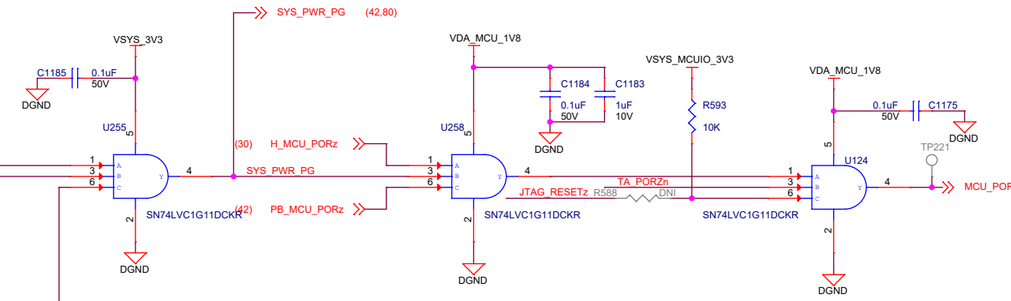
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET BUTTONs	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 42 of 88

RESET INPUTS

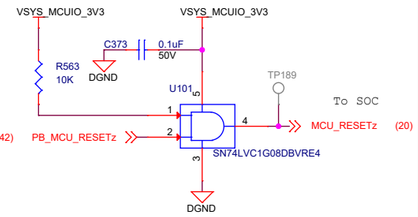
Under Voltage Monitor (VINPUT)

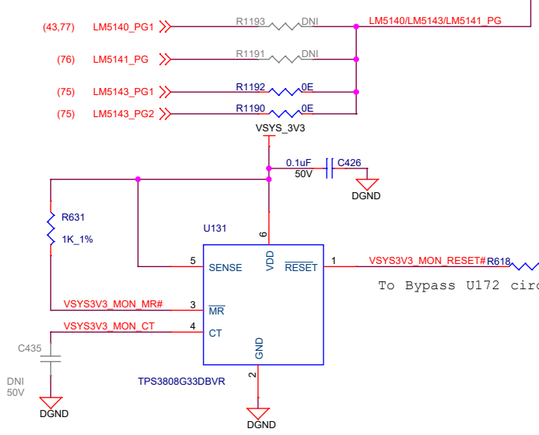


MCU PORZ

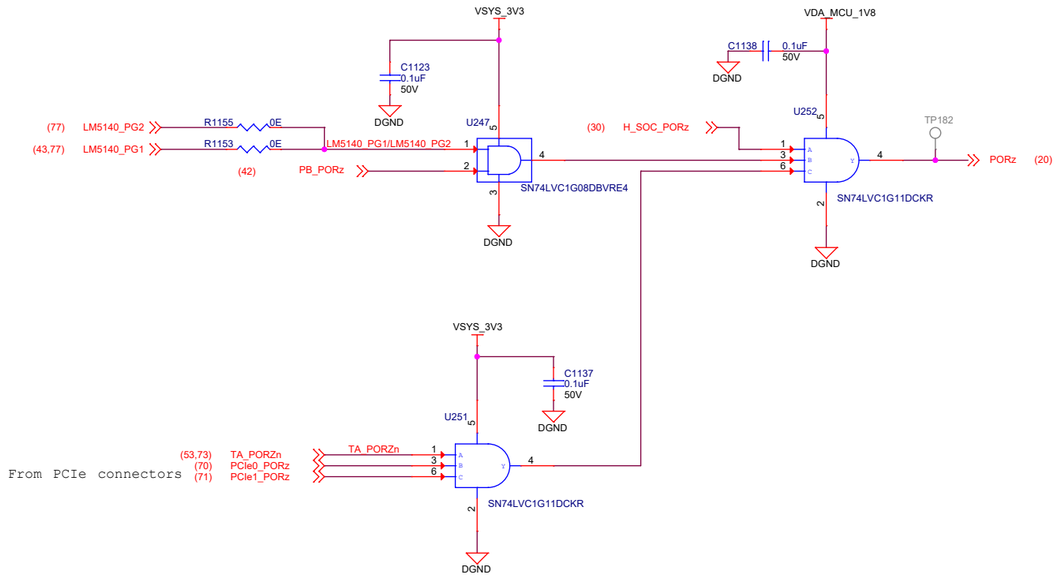


MCU_RESET

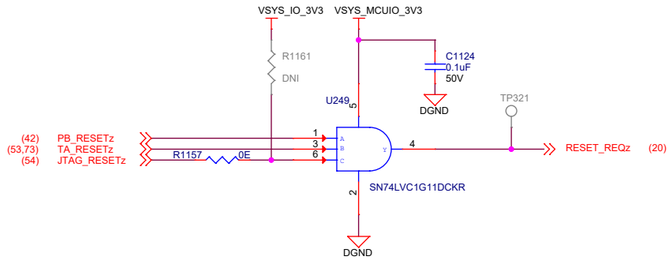




SOC PORZ

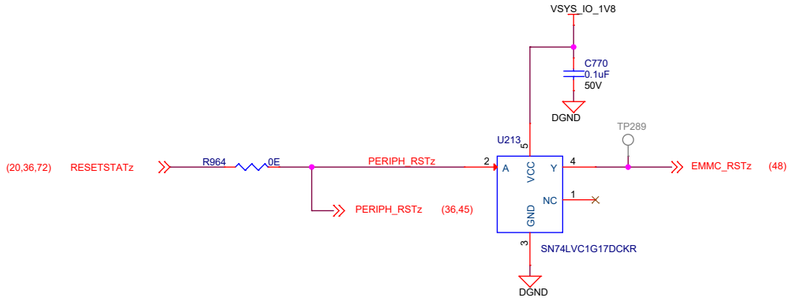


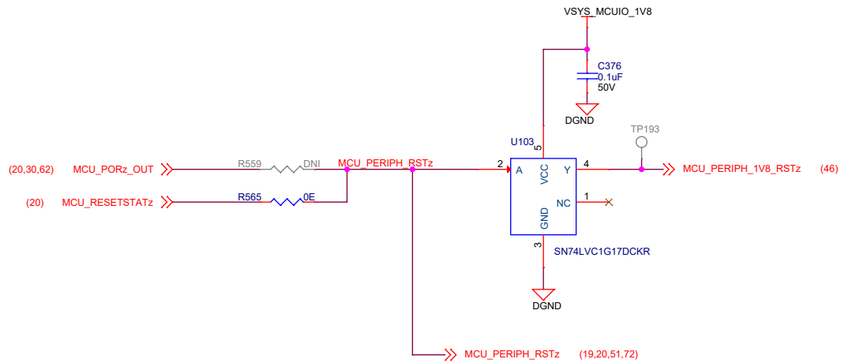
SOC RESET

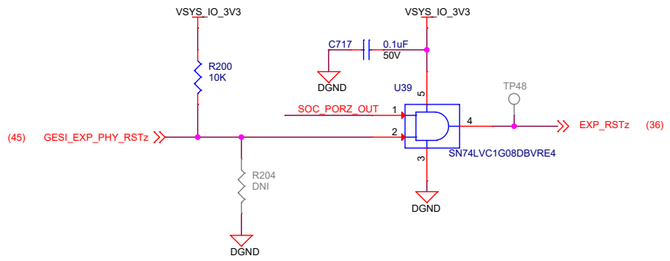


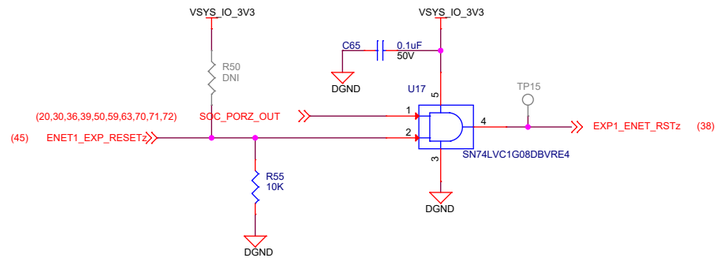
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET INPUTS
	Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
	Date: Friday, May 05, 2023	Sheet 43 of 88

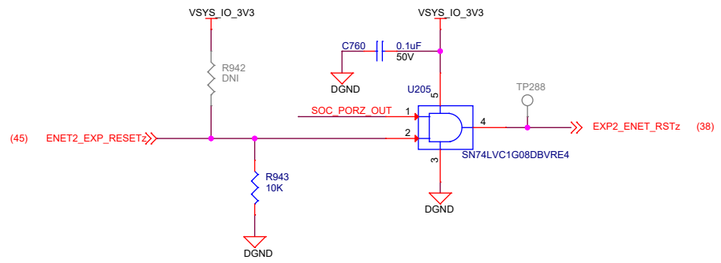
RESET OUTPUTS







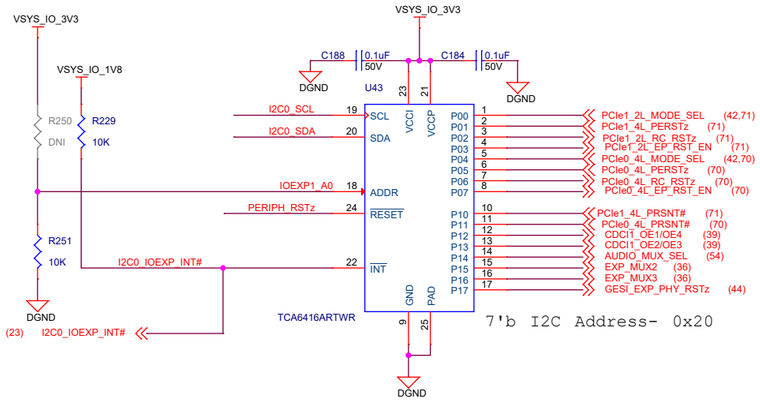




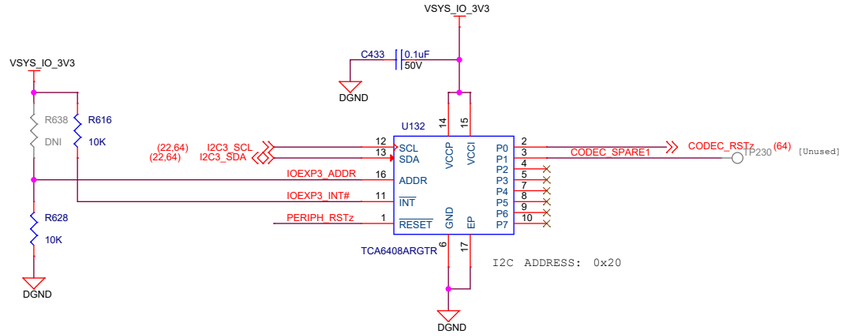
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET OUTPUTS
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 44 of 88

GPIO EXPANDERS

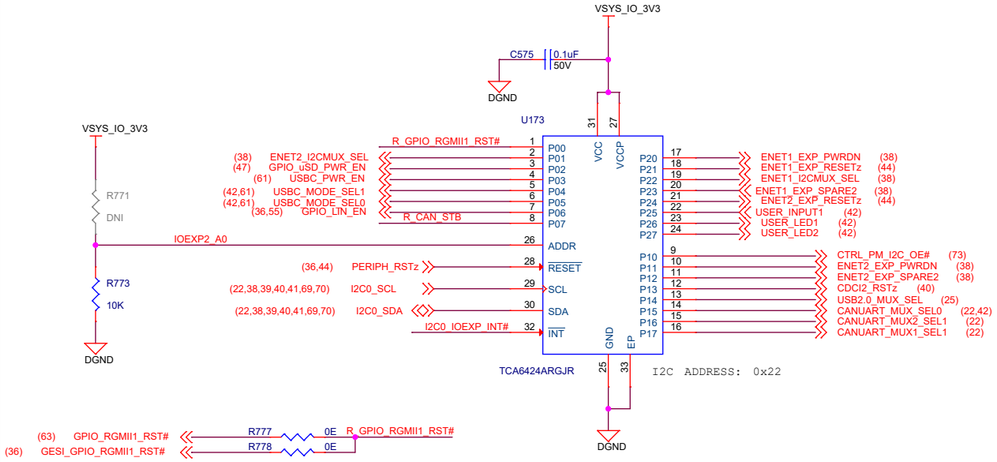
I2C GPIO EXPANDER1



I2C GPIO EXPANDER3

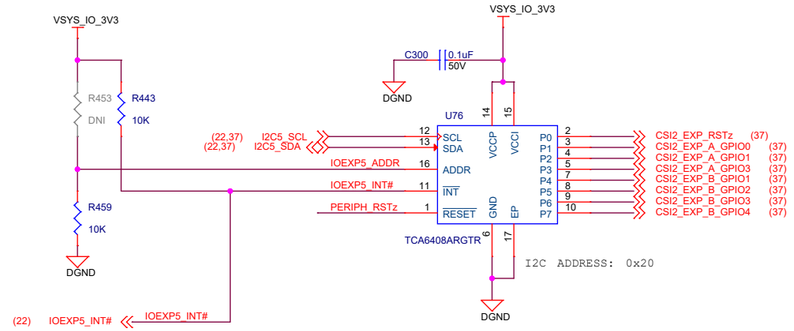


I2C GPIO EXPANDER2



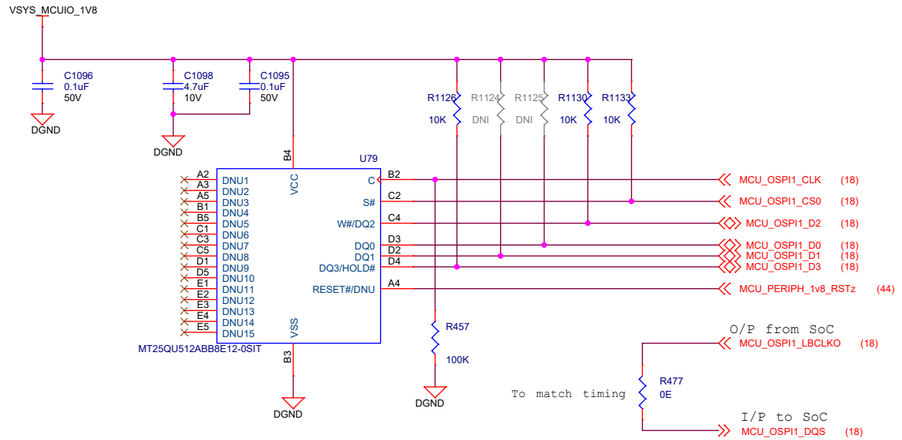
I2C GPIO EXPANDER4

I2C GPIO EXPANDER5



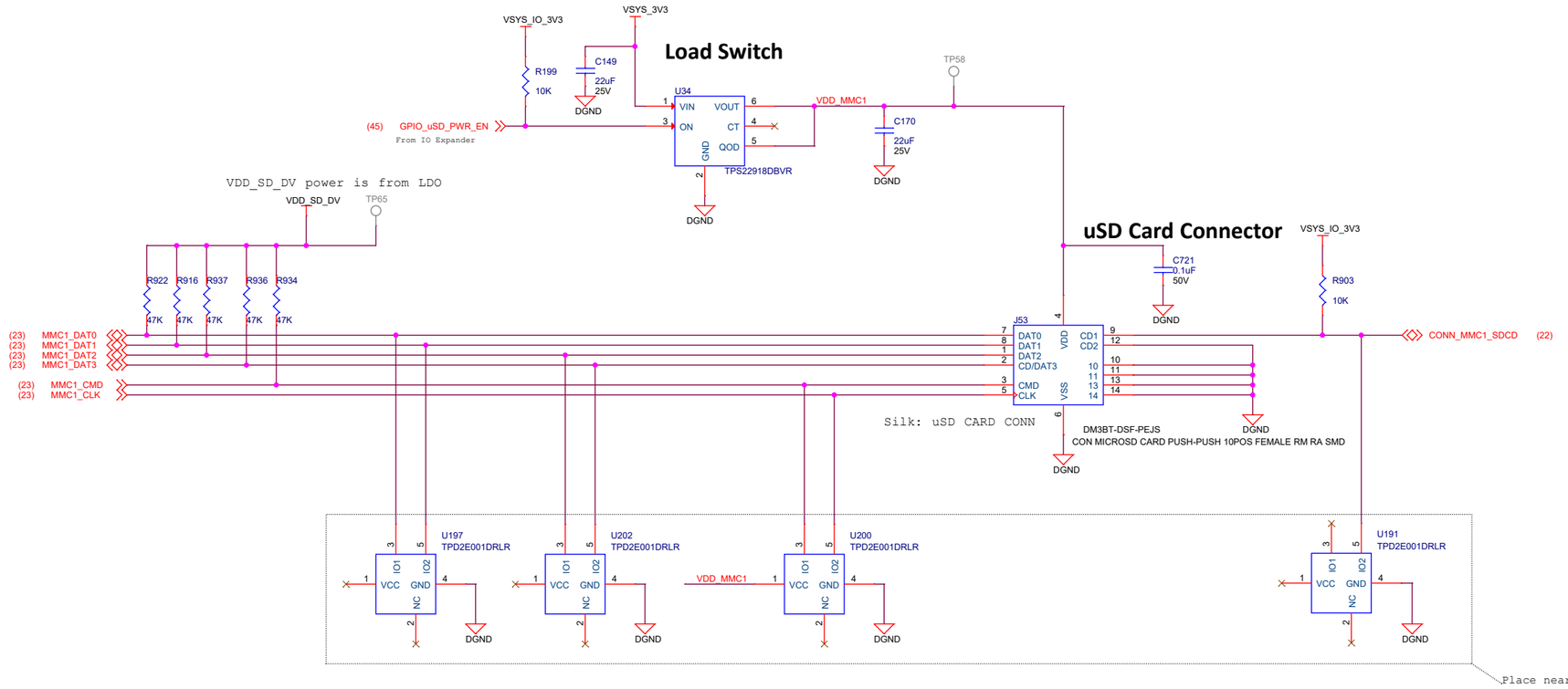
Project : J7 EVM	TEXAS INSTRUMENTS	Title: GPIO EXPANDERS	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 45 of 88

SPI NOR Flash



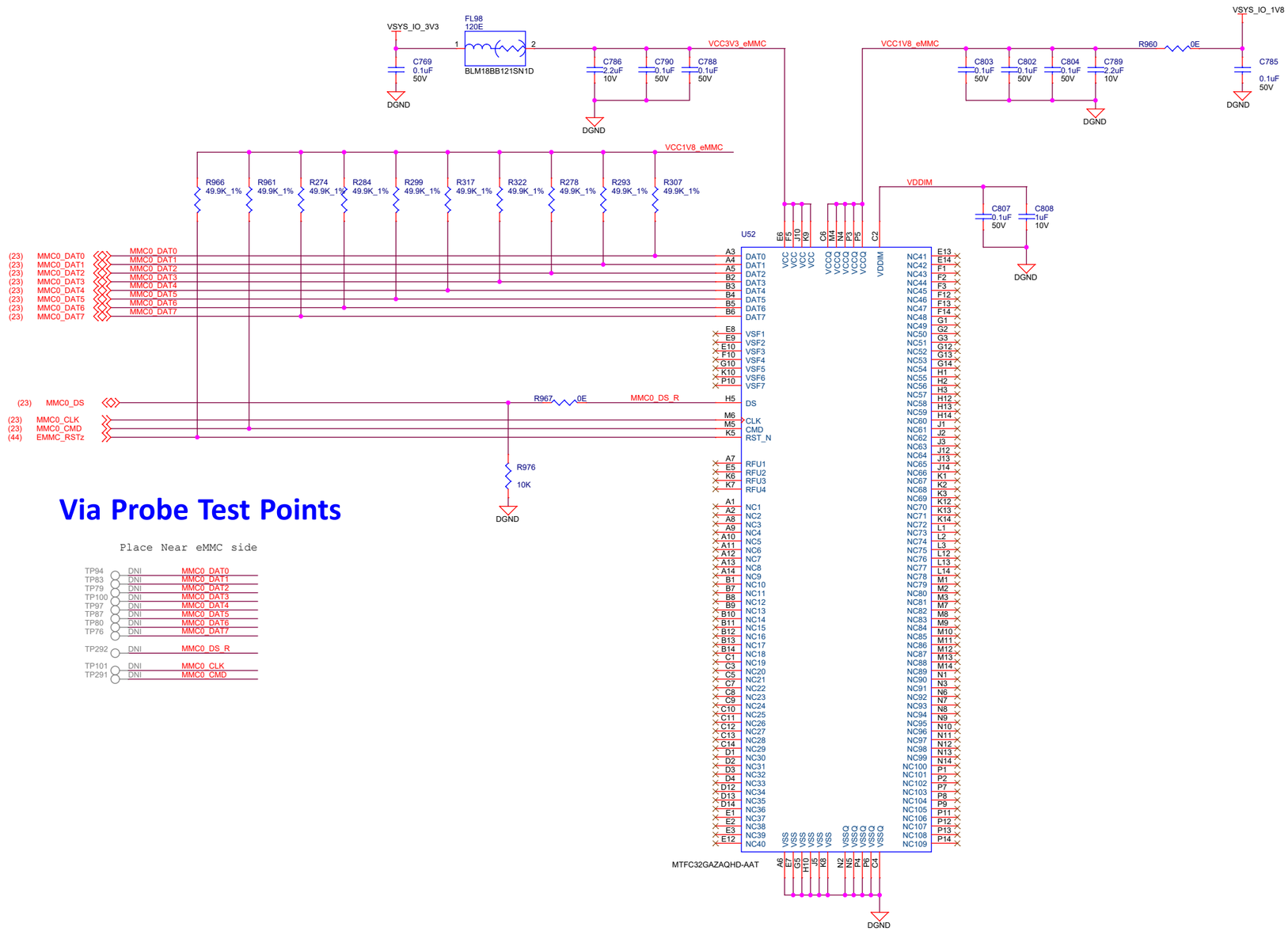
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SPI NOR FLASH
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 46 of 88

Micro SD CARD INTERFACE



Project : J7 EVM	TEXAS INSTRUMENTS	Title: Micro SD CARD INTERFACE
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 47 of 88

eMMC FLASH

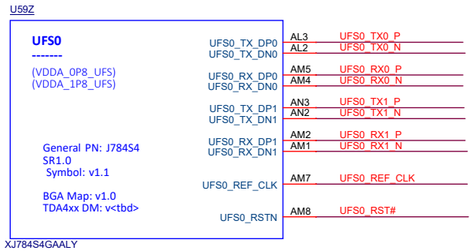


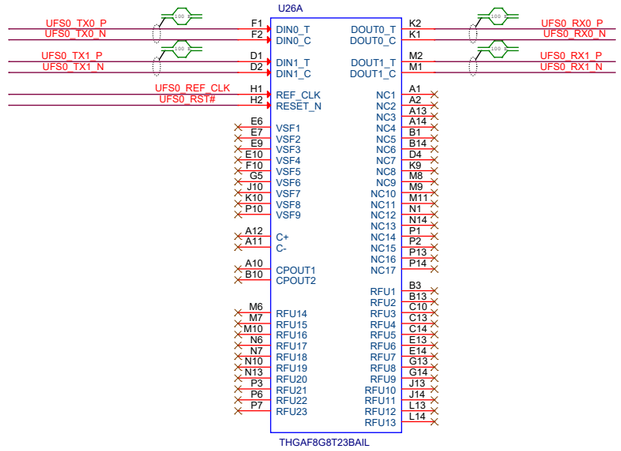
Via Probe Test Points

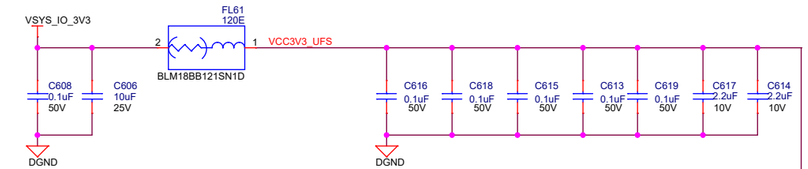
Place Near eMMC side

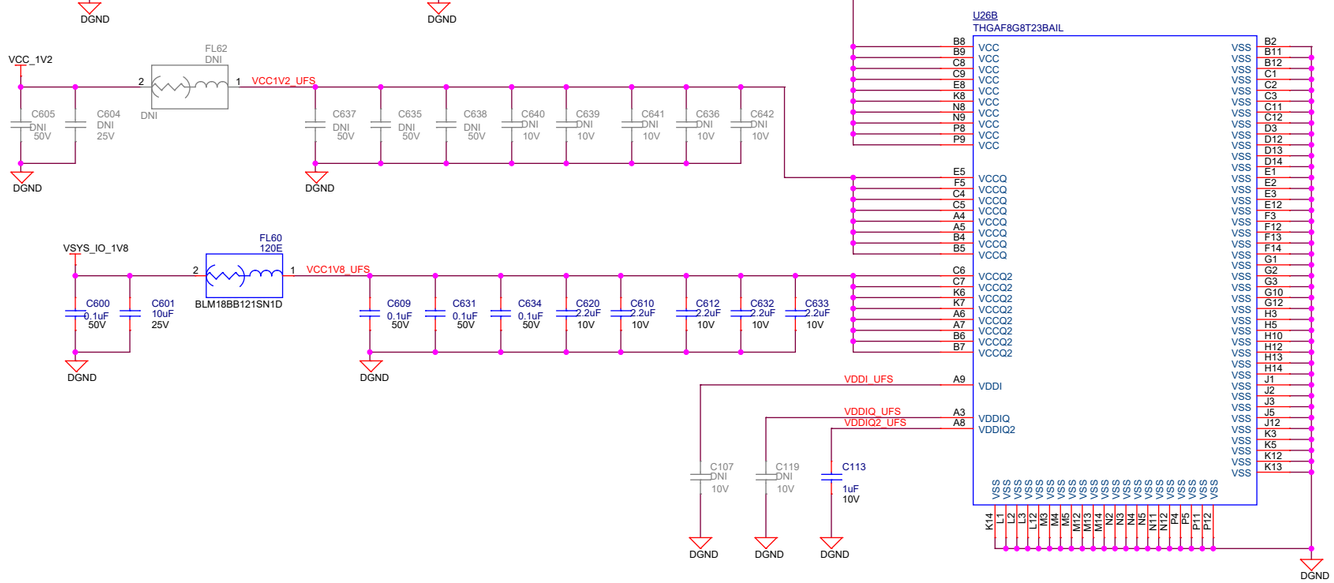
Project : J7 EVM	TEXAS INSTRUMENTS	Title: eMMC FLASH
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 48 of 88

UFS FLASH



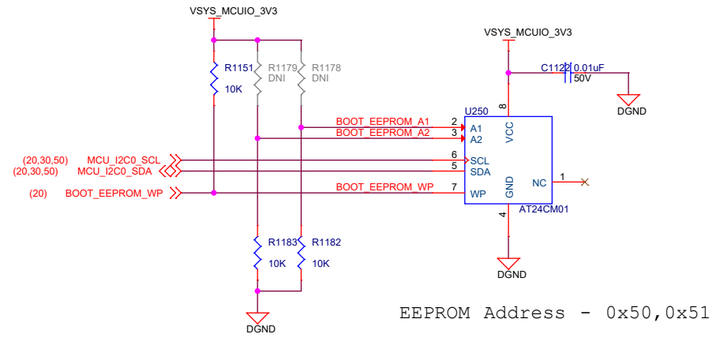






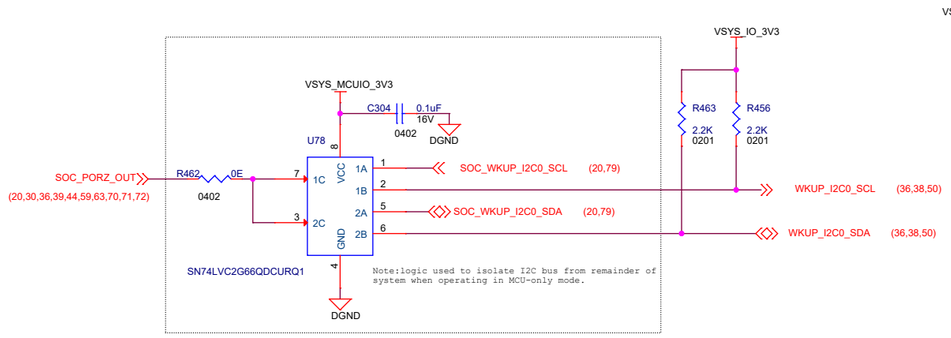
Project : J7 EVM	TEXAS INSTRUMENTS	Title: UFS FLASH
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 49 of 88

BOOT EEPROM

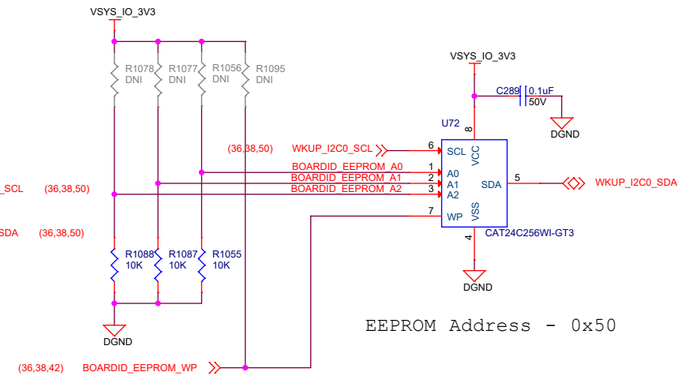


EEPROM Address - 0x50,0x51

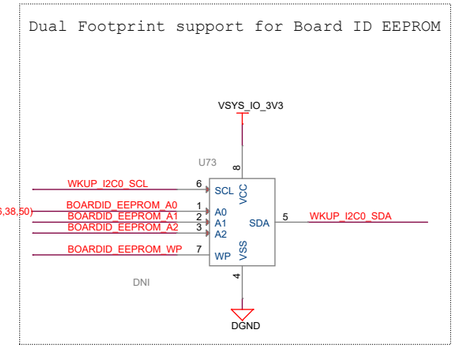
I2C for BOARD ID EEPROMs



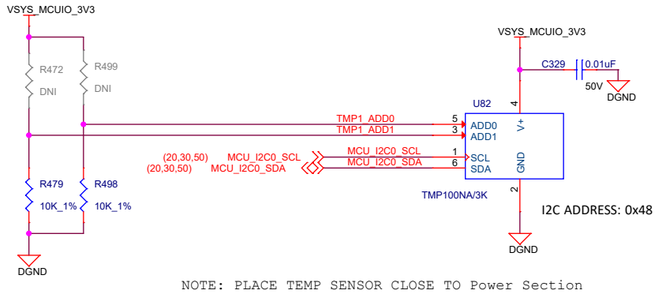
BOARD ID EEPROM



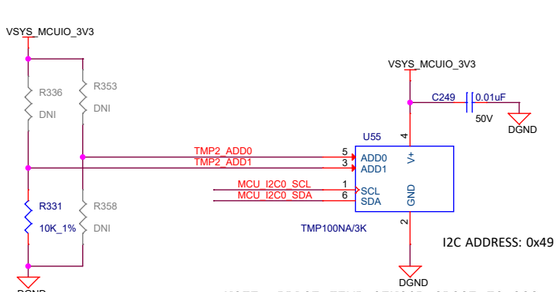
EEPROM Address - 0x50



TEMPERATURE SENSORS (TI EVM Only)



NOTE: PLACE TEMP SENSOR CLOSE TO Power Section

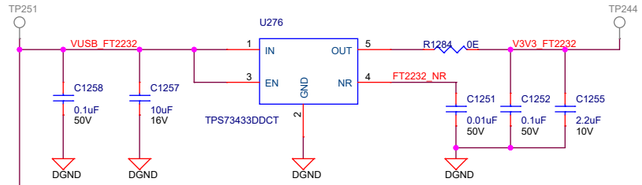


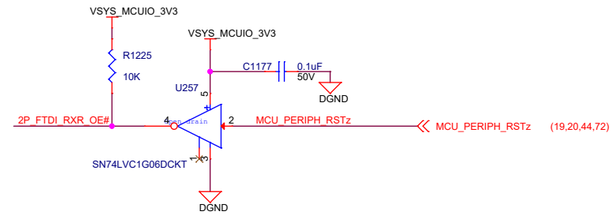
NOTE: PLACE TEMP SENSOR CLOSE TO SOC

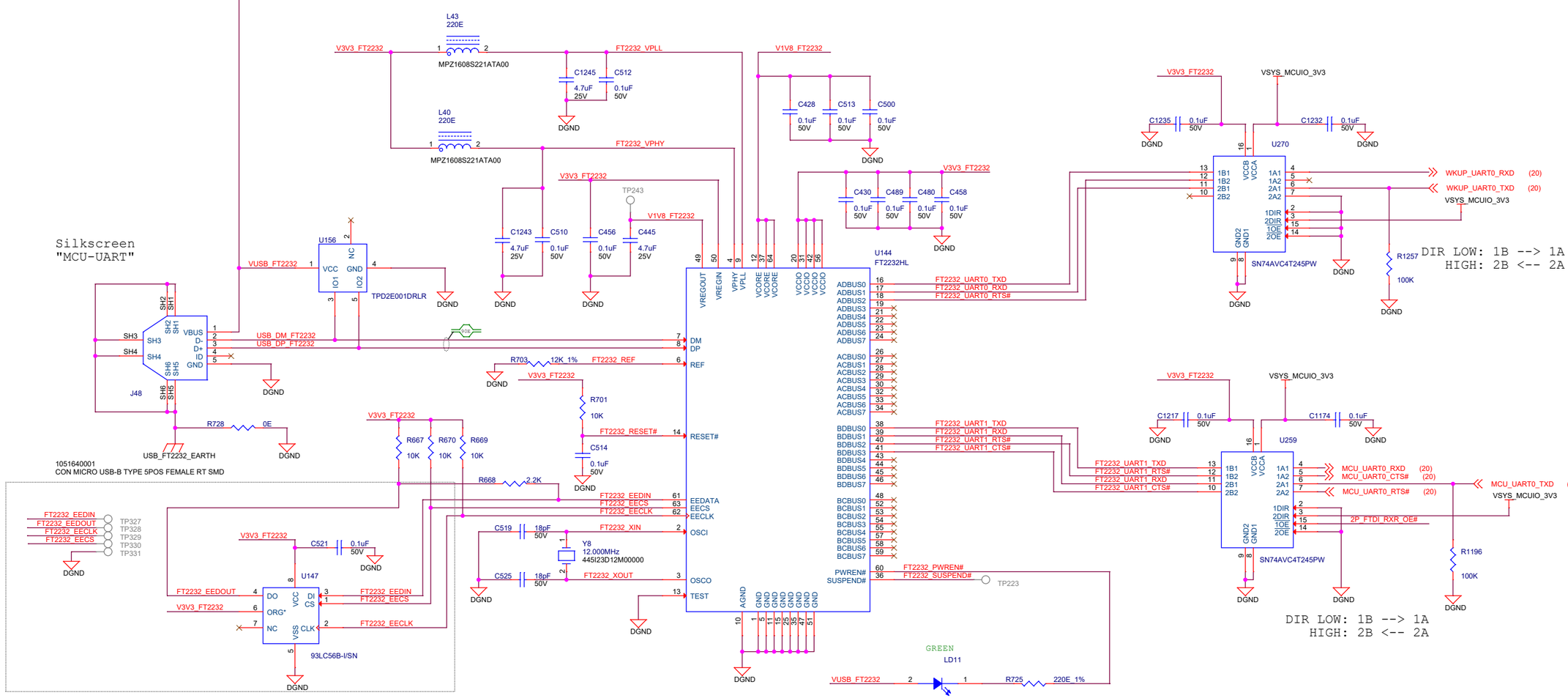
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EEPROM	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 50 of 88

DUAL PORT FTDI

Note: FTDI Power sourced from USB.







Note: FTDI EEPROM for storing manufacturing/configuration information.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DUAL PORT FTDI	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 51 of 88

QUAD PORT FTDI

Note: FTDI Power sourced from USB.

TP248 TP246

U277 TPS73433DDCT

VUSB_FT4232 → IN; OUT → V3V3_FT4232

R1285 0E

FT4232_NR

C1261 0.1uF 50V

C1260 10uF 16V

C1253 0.01uF 50V

C1254 0.1uF 50V

C1256 2.2uF 10V

DGND

L42 220E — MPZ1608S221ATA00 — V3V3_FT4232 → FT4232_VPLL

L41 220E — MPZ1608S221ATA00 — FT4232_VPHY

C1246 4.7uF 25V

C515 0.1uF 50V

C1244 4.7uF 25V

C511 0.1uF 50V

V1V8_FT4232

C516 0.1uF 50V

C502 0.1uF 50V

C429 0.1uF 50V

C431 0.1uF 50V

C1239 0.1uF 50V

C481 0.1uF 50V

C460 0.1uF 50V

Silkscreen "MAIN-UART"

U157 TPD2E001DRLR

VUSB_FT4232

C457 0.1uF 50V

TP322

V1V8_FT4232

C449 4.7uF 25V

J49

VBUS D+ D- ID GND

USB_DM_FT4232

USB_DP_FT4232

R729 0E → USB_FT4232_EARTH

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD

U145 FT4232HL

VREGOUT VREGIN VPHY VPLL VCORE VCORE VCORE VCCIO VCCIO VCCIO VCCIO

DM DP REF RESET EEDATA EECS EECLK OSCI OSCO TEST

R704 12K_1% FT4232_REF

R702 10K

C517 0.1uF 50V

FT4232_RESET#

R1266 10K R1270 10K R1269 10K

R1268 2.2K

FT4232_EEDIN FT4232_EECS FT4232_EECLK

C509 18pF 50V

C523 18pF 50V

Y7 12.000MHz 445I23D12M00000

FT4232_XIN FT4232_XOUT

ADBUS0 FT4232_UART0_TXD
ADBUS1 FT4232_UART0_RXD
ADBUS2 FT4232_UART0_RTS#
ADBUS3 FT4232_UART0_CTS#
ADBUS4 ADBUS5 ADBUS6 ADBUS7

BDBUS0 FT4232_UART1_TXD
BDBUS1 FT4232_UART1_RXD
BDBUS2 BDBUS3 BDBUS4 BDBUS5 BDBUS6 BDBUS7

CDBUS0 FT4232_UART2_TXD
CDBUS1 FT4232_UART2_RXD
CDBUS2 CDBUS3 CDBUS4 CDBUS5 CDBUS6 CDBUS7

DDBUS0 FT4232_UART3_TXD
DDBUS1 FT4232_UART3_RXD
DDBUS2 FT4232_UART3_RTS#
DDBUS3 DDBUS4 DDBUS5 DDBUS6 DDBUS7

PWREN FT4232_PWREN#
SUSPEND FT4232_SUSPEND#

TP224

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 AGND

U275 93LC56B-I/SN

FT4232_EEDOUT V3V3_FT4232 C1264 0.1uF 50V

GREEN LD12 — VUSB_FT4232 → R727 220E_1% — 5988170107F

Note: FTDI EEPROM for storing manufacturing/configuration information.

U273 SN74AVC4T245PW

V3V3_FT4232 C490 0.1uF 50V

VSYS_IO_3V3 C1216 0.1uF 50V

FT4232_UART0_TXD FT4232_UART0_RTS# FT4232_UART0_RXD FT4232_UART0_CTS#

UART8_RXD (22) UART8_CTSn (22) UART8_RTSn (22) UART8_TXD (22)

1DIR 2DIR 1OE 2OE

R1262 100K

DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

U264 SN74AVC4T245PW

C1214 0.1uF 50V

C1236 0.1uF 50V

FT4232_UART1_TXD FT4232_UART2_TXD FT4232_UART1_RXD FT4232_UART2_RXD

UART5_RXD (22) UART2_RXD (22) UART5_TXD (22) UART2_TXD (22)

R1227 100K

R1228 100K

DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

U143 SN74AVC4T245PW

C501 0.1uF 50V

C441 0.1uF 50V

FT4232_UART3_TXD FT4232_UART3_RXD

UART3_RXD (22) UART3_TXD (54)

R635 100K

DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

Project : J7 EVM	TEXAS INSTRUMENTS	Title: QUAD PORT FTDI
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 52 of 88

XDS110 DEBUGGER

Silkscreen "XDS110"

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD

U6 TPS79601DRBR

U2 TPD4E004DRYR

U10 SN74AVC8T245PWR

SN74AVC8T245PWR buffer is used to isolate test automation from xds110

U170B TM4C1294NCPDTT3R

U170A TM4C1294NCPDTT3R

U170C TM4C1294NCPDTT3R

U29 SN74CB3Q3125PWR

U13 LM4040B25IDCKR

LD6 LP L296-J2L2-25 GREEN

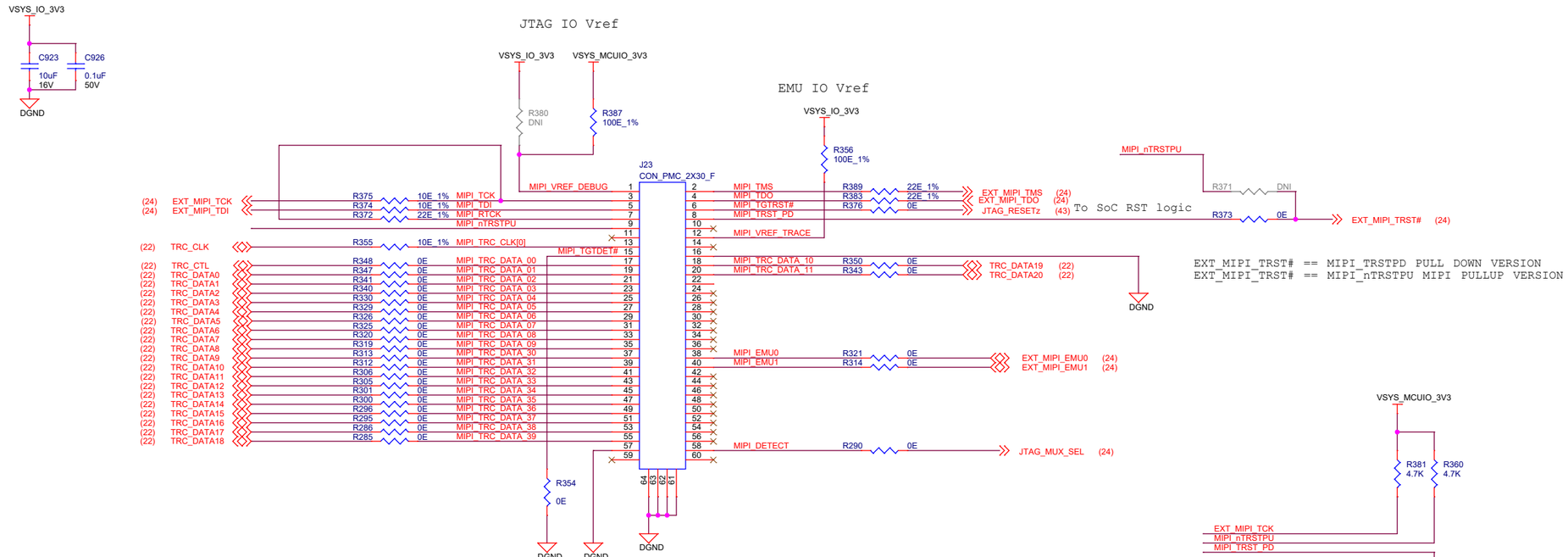
LD1 LS Q976-NR-1 RED

Y9 16.000MHZ NX3225GA-16.000M-STD-CRG-1

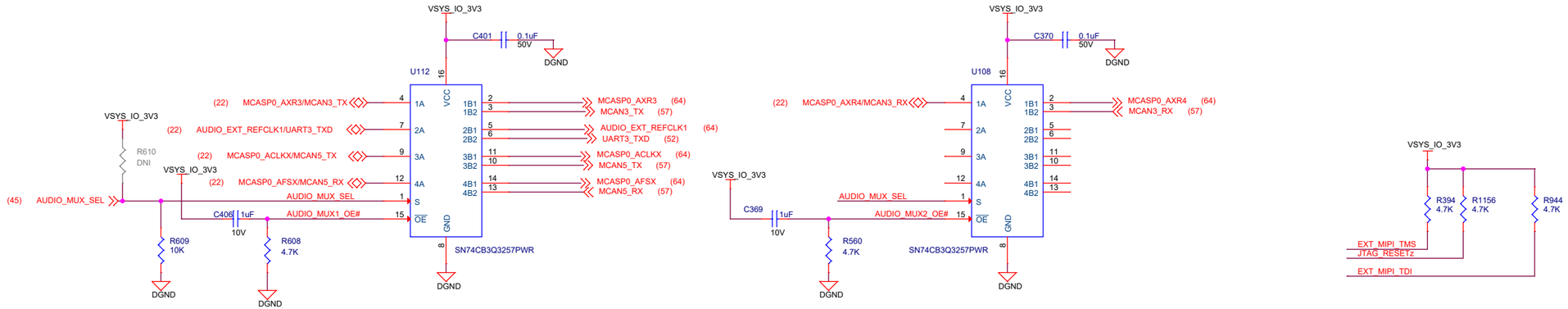
Set the unique ID of the debugger

Project : J7 EVM	Title: XDS110 DEBUGGER		
	Size: C	PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 53 of 88	

JTAG MIPI60 CONNECTOR



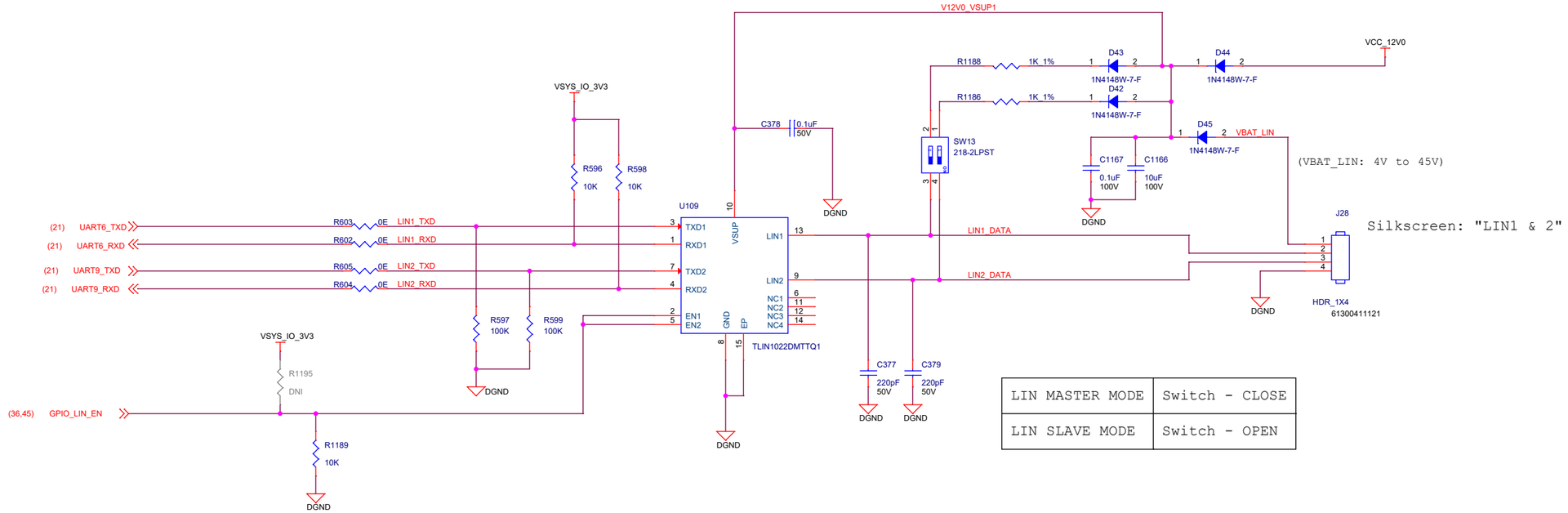
Silkscreen: "MIPI-60"



JTAG - 1:2 MUX : Truth Table

Project : J7 EVM	TEXAS INSTRUMENTS	Title: JTAG MIPI60 CONNECTOR	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 54 of 88

LIN INTERFACE

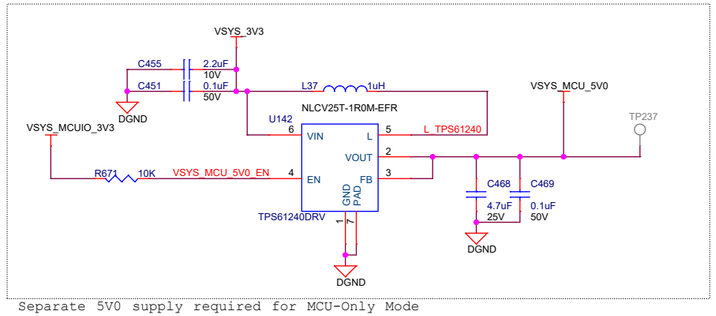


LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

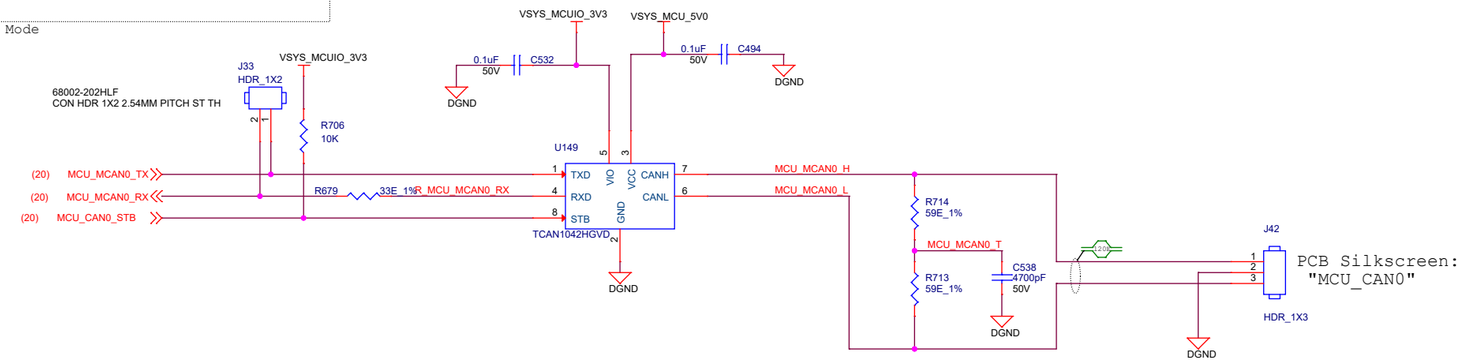
Project : J7 EVM	TEXAS INSTRUMENTS	Title: LIN INTERFACE	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 55 of 88

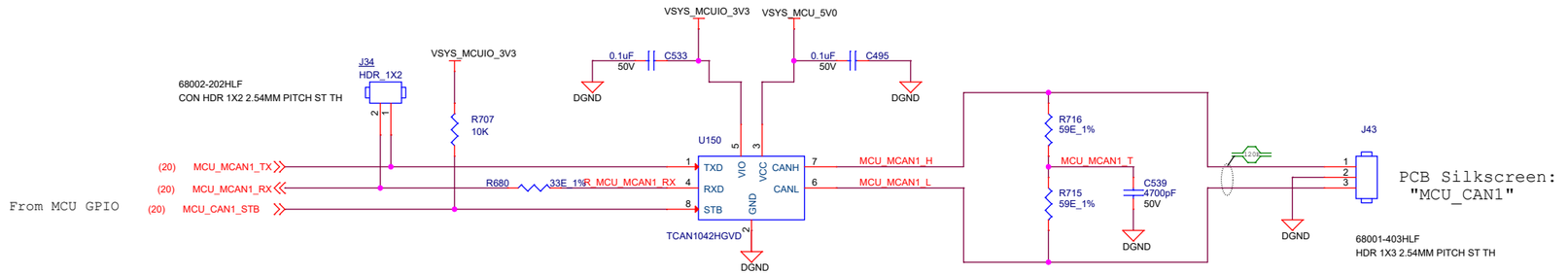
CAN TRANSCEIVERS #1-MCU DOMAIN

VSYS_MCU_5V0 GENERATION



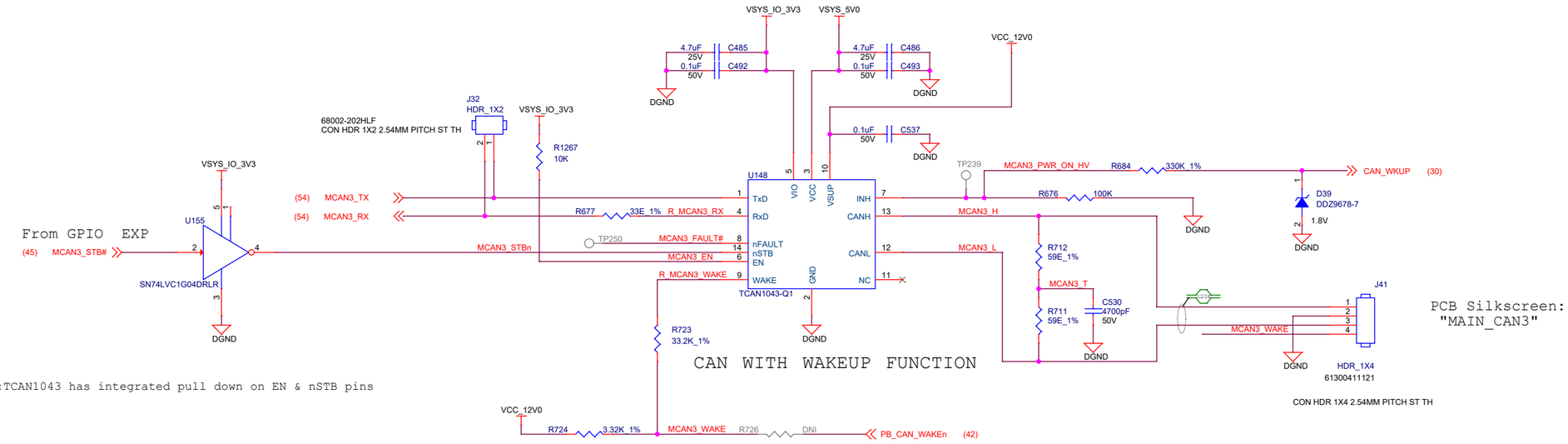
Separate 5V0 supply required for MCU-Only Mode

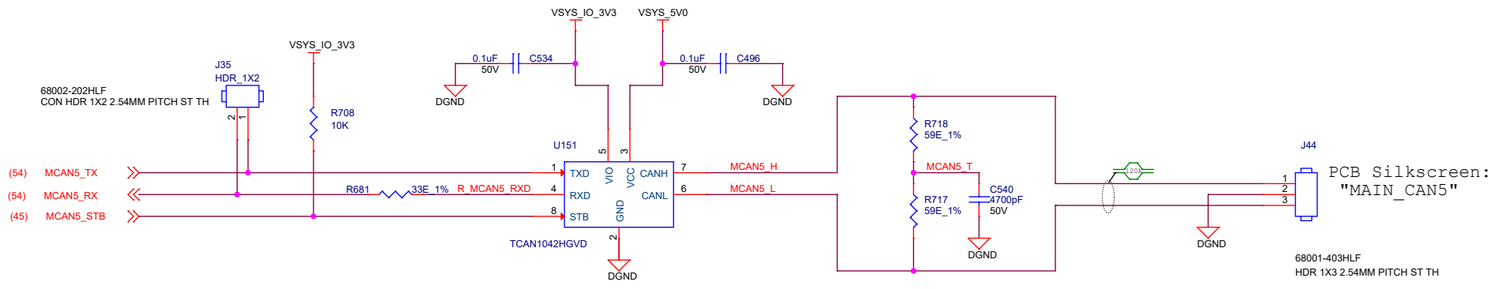




Project : J7 EVM	Texas Instruments	Title: CAN TRANSCEIVERS #1	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 56 of 88

CAN TRANSCEIVERS #2-MAIN DOMAIN



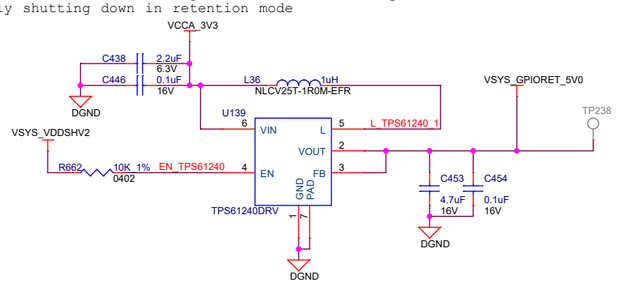


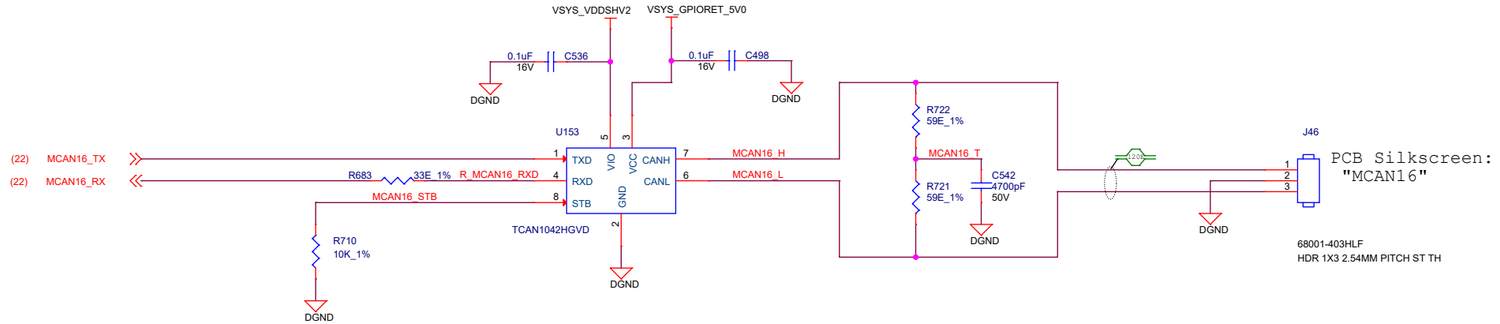
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CAN TRANSCEIVER #2
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 57 of 88

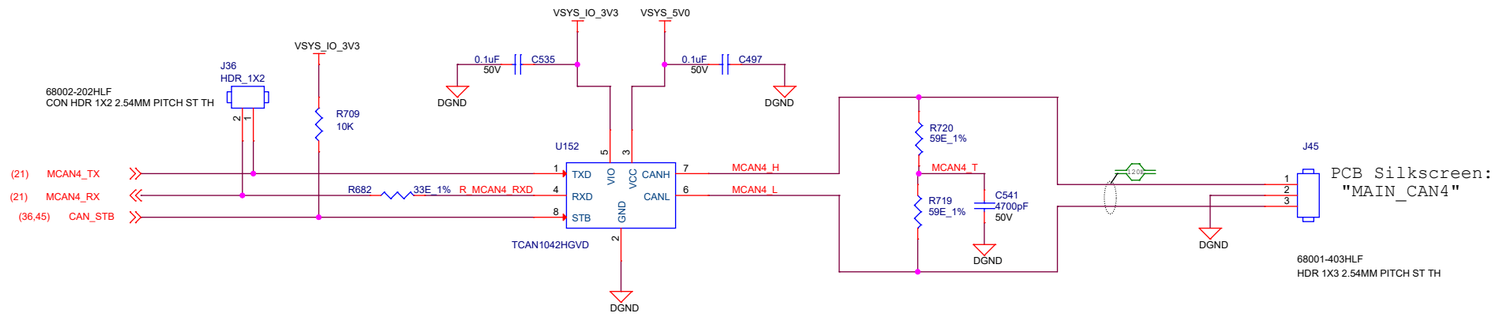
CAN TRANSCEIVER

VSYS_GPIORET_5V0 GENERATION

Note: Booster convertor required for EVM due to system 5V supply shutting down in retention mode

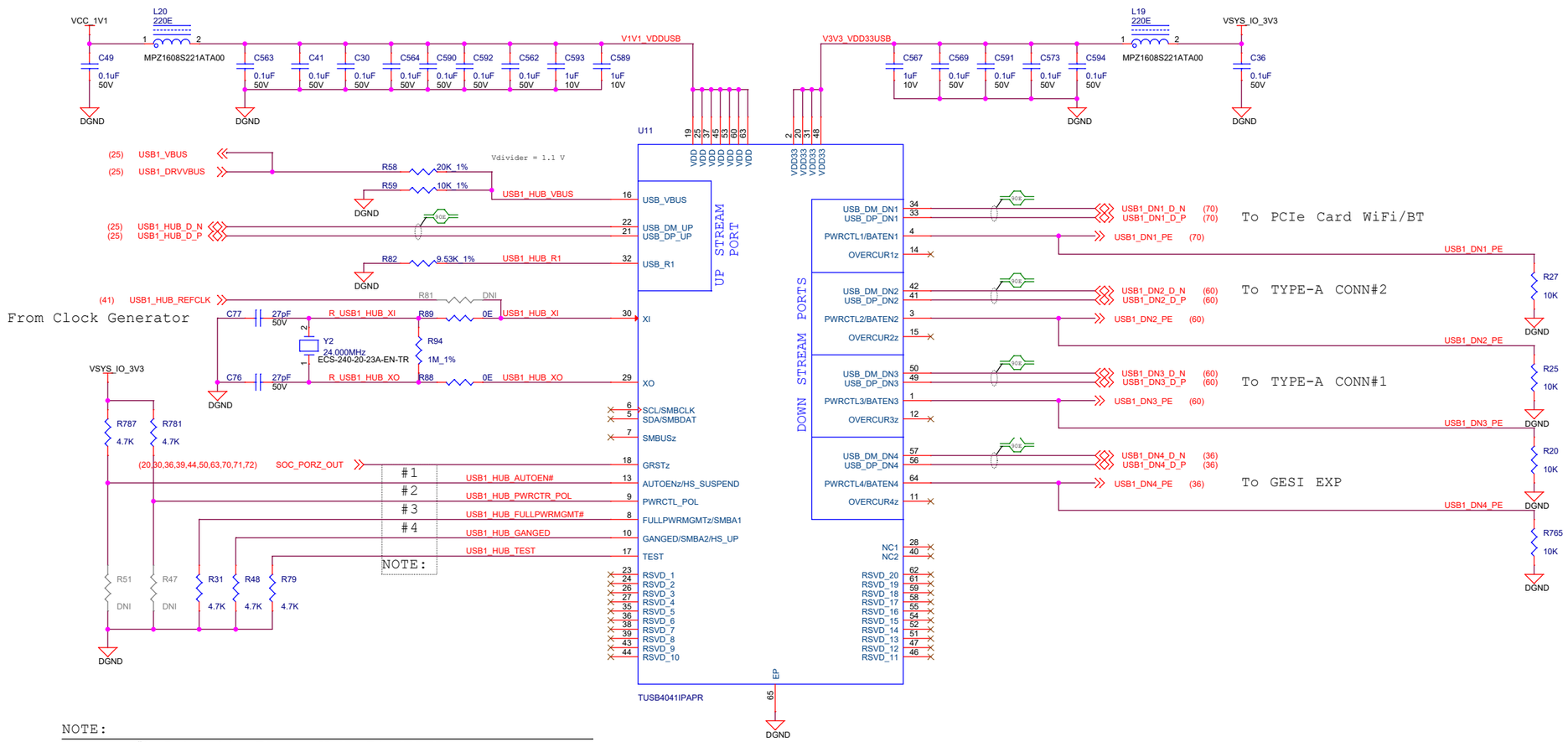






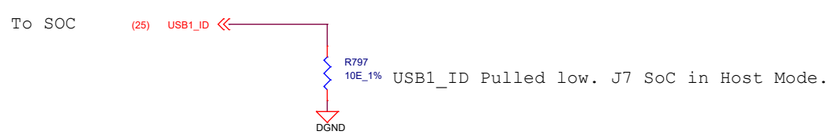
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CAN TRANSCEIVER #3
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 58 of 88

USB HUB



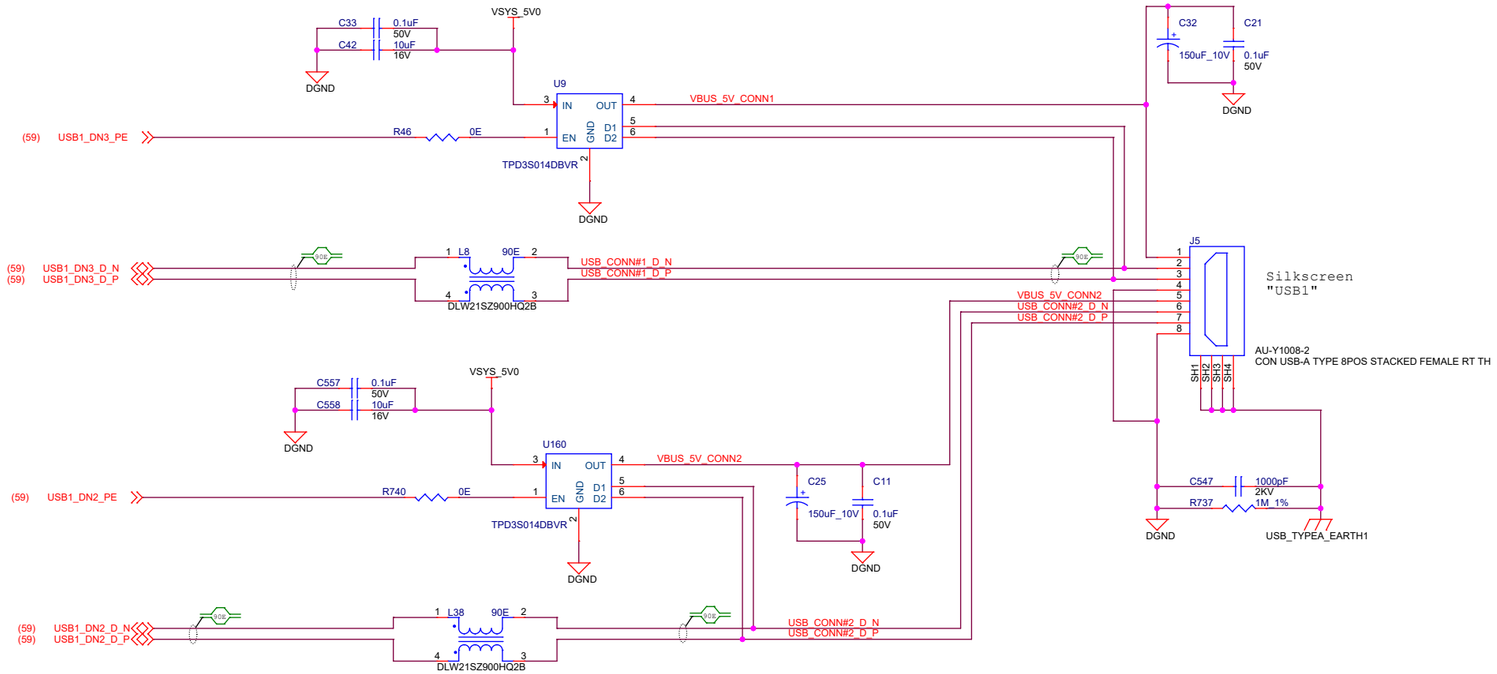
NOTE:

#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Individual Power Control Enabled



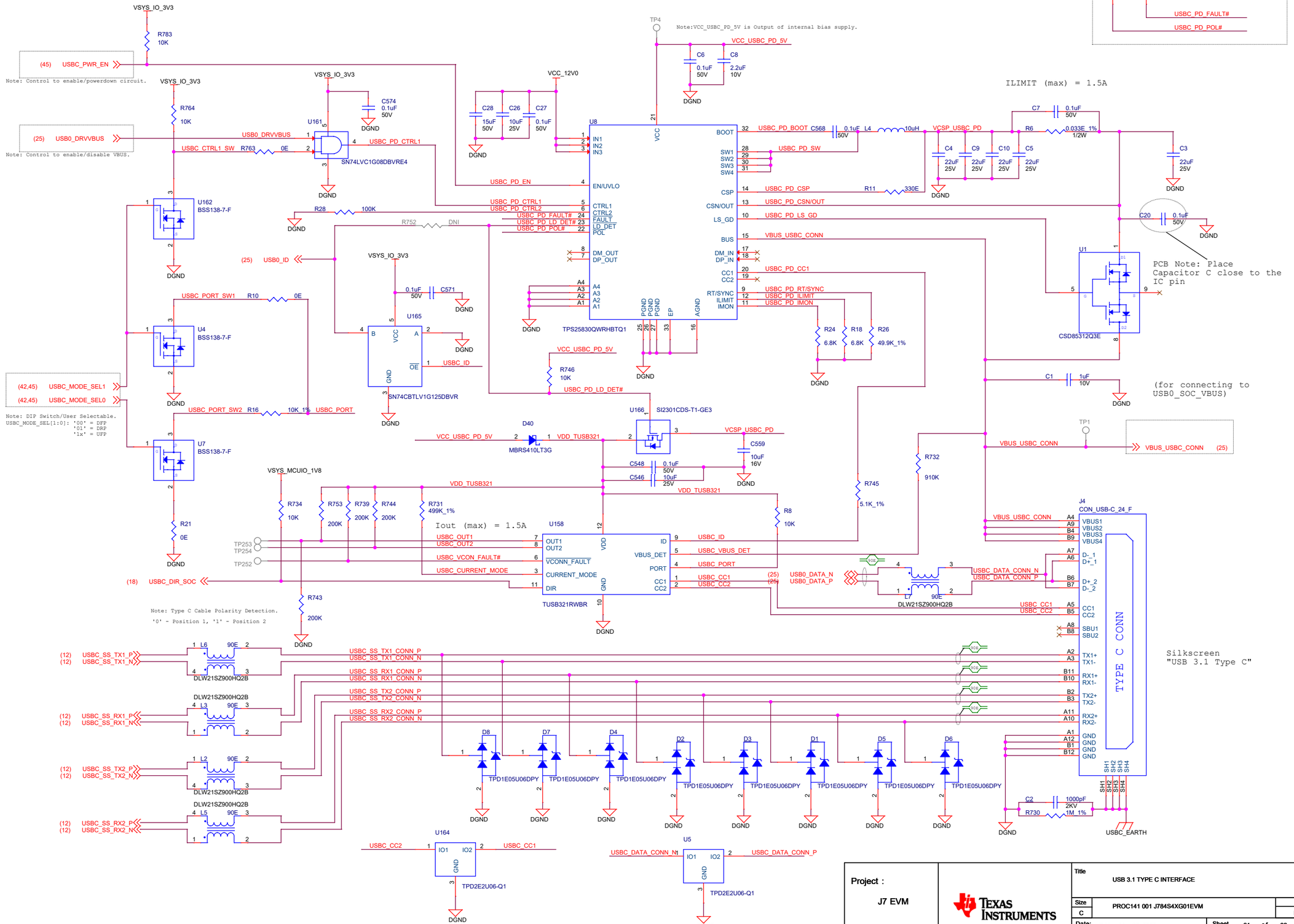
Project : J7 EVM		Title: USB HUB	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 59 of 88

USB 2.0 TYPE-A CONNECTORS



Project : J7 EVM	TEXAS INSTRUMENTS	Title: USB 2.0 TYPE-A CONNECTORS
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 60 of 88

USB 3.1 TYPE C INTERFACE



Project : J7 EVM	Title: USB 3.1 TYPE C INTERFACE	
	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 61 of 88

TEXAS INSTRUMENTS

MCU GB ETHERNET

VDD1P0 supply voltage is connected to VCC_1V1.
VDD1P0 supply range is 0.95V to 1.155V

RESET LOGIC

From GPIO (default Pull-up pin) of MCU domain

To GPIO of MCU domain

RJ45

RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS

Set Mode 3 [Autoneg Disable - 0]

PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0nS
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2nS

Silk Screen "MCU_RGMII1"

Project :	J7 EVM
Title	MCU GB ETHERNET
Size	C
	PROC141 001 J784S4XG01EVM
Rev	E4
Date:	Friday, May 05, 2023
Sheet	62 of 88

RGMII1

VDD1P0 supply voltage is connected to VCC_1V1.
VDD1P0 supply range is 0.95V to 1.155V

VSYS_IO_3V3: C436 0.1uF 50V, C422 0.1uF 50V, C1198 0.1uF 50V, C1189 1uF 10V, C1187 10uF 16V → DGND

VCC_1V1: C1181 10uF 16V, C477 1uF 10V, C1180 1uF 10V, C1191 0.1uF 50V, C423 0.1uF 50V, C1225 0.1uF 50V, C442 0.1uF 50V → DGND

VDD_2V5: C476 1uF 10V, C478 1uF 10V, C1224 0.1uF 50V, C1226 0.1uF 50V → DGND

TP235 DNI

U262 DP83867ERGZT

(21) RGMII1_TD0	28	TX_D0/SGMII_SIN	
(21) RGMII1_TD1	27	TX_D1/SGMII_SIP	
(21) RGMII1_TD2	26	TX_D2	
(21) RGMII1_TD3	25	TX_D3	
(21) RGMII1_TX_CTL	37	TX_CTRL	
(21) RGMII1_TXC	29	GTX_CLK	
R1202 0E RGMII1_RD0_R	33	RX_D0/SGMII_COP	
R1213 0E RGMII1_RD1_R	34	RX_D1/SGMII_CON	
R1201 0E RGMII1_RD2_R	35	RX_D2/SGMII_SOP	
R1212 0E RGMII1_RD3_R	36	RX_D3/SGMII_SON	
R1205 0E RGMII1_RX_CTL_R	38	RX_CTRL	
R1214 0E RGMII1_RXC_R	32	RX_CLK	
TP229 RGMII1_CLK_OUT	18	CLK_OUT	
C1208 27pF / Y13 25.000MHz 445I23D25M00000 / C1219 27pF	15	X_I	
RGMII1_XOUT	14	X_O	
	16	MDC	
(21) RGMII1_MDIO0_MDC	17	MDIO	
(21) RGMII1_MDIO0_MDIO			
RGMII1_RESET_N	43	RESET_N	
	44	INT/PWDN	
	20	JTAG_CLK	
	23	JTAG_TDI	
	21	JTAG_TDO	
	22	JTAG_TMS	
	49	EP	
RGMII1_RBIAS 11K_1% R1259 DGND	12	RBIAS	
RGMII1_GPIO0_100	39	GPIO_0	
RGMII1_GPIO1	40	GPIO_1	
RGMII1_D0_P	1	TD_P_A	
RGMII1_D0_N	2	TD_M_A	
RGMII1_D1_P	4	TD_P_B	
RGMII1_D1_N	5	TD_M_B	
RGMII1_D2_P	7	TD_P_C	
RGMII1_D2_N	8	TD_M_C	
RGMII1_D3_P	10	TD_P_D	
RGMII1_D3_N	11	TD_M_D	
RGMII1_LED0	47	LED0	
RGMII1_LED1_1000	46	LED1	
RGMII1_LED2_ACT	45	LED2	

RESET LOGIC

VSYS_IO_3V3: R561 10K; U107 SN74LVC1G08DBVRE4; C397 0.1uF 50V → DGND

(20,30,36,39,44,50,59,70,71,72) SOC_PORZ_OUT

(45) GPIO_RGMII1_RST# → R567 DNI → DGND

VSYS_IO_3V3: R1245 2.2K → (21) RGMII1_INT#

RJ45

J39

RGMII1_D0_N	10	J2
RGMII1_D1_P	7	J3
RGMII1_D1_N	8	J6
RGMII1_D2_P	5	J4
RGMII1_D2_N	6	J5
RGMII1_D3_P	3	J7
RGMII1_D3_N	4	J8
	1	
	2	J1
	9	
	SH1	15
	SH2	16

VSYS_IO_3V3: R1288 220E_1%

RGMII1_LED2_ANODE → 11 YELLOW GREEN RIGHT LED

RGMII1_ACT_LED → 12 YELLOW GREEN LEFT LED

RGMII1_1000Mbps → 13

RGMII1_100Mbps → 14

LPJG16314A4NL
CON RJ-45 FEMALE 14POS RT TH

C1248 1000pF 2KV, R697 1M_1% → DGND, MCU_ETH_EARTH

VSYS_IO_3V3: R1291 220E_1%, R1289 220E_1% → DGND

Silk Screen : "RGMII1"

VSYS_IO_3V3: R1218 DNI, R1217 DNI, R1221 5.76K_1%, R1261 10K_1%, R1249 DNI, R629 DNI, R1235 DNI, R649 DNI

RGMII1_RD0_R
RGMII1_RD2_R
RGMII1_RX_CTL_R
RGMII1_LED1_1000
RGMII1_LED2_ACT
RGMII1_GPIO0_100
RGMII1_GPIO1
RGMII1_LED0

R1200 DNI, R1199 DNI, R1224 2.49K_1%, R1256 2.49K_1%, R1254 DNI, R621 DNI, R1232 DNI, R654 DNI → DGND

Set Mode 3 [Autoneg Disable - 0]

PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS

RGMII1_100Mbps → U126 BSS138-7-F, gate RGMII1_GPIO0_100 → DGND

RGMII1_1000Mbps → U272 BSS138-7-F, gate RGMII1_LED1_1000 → DGND

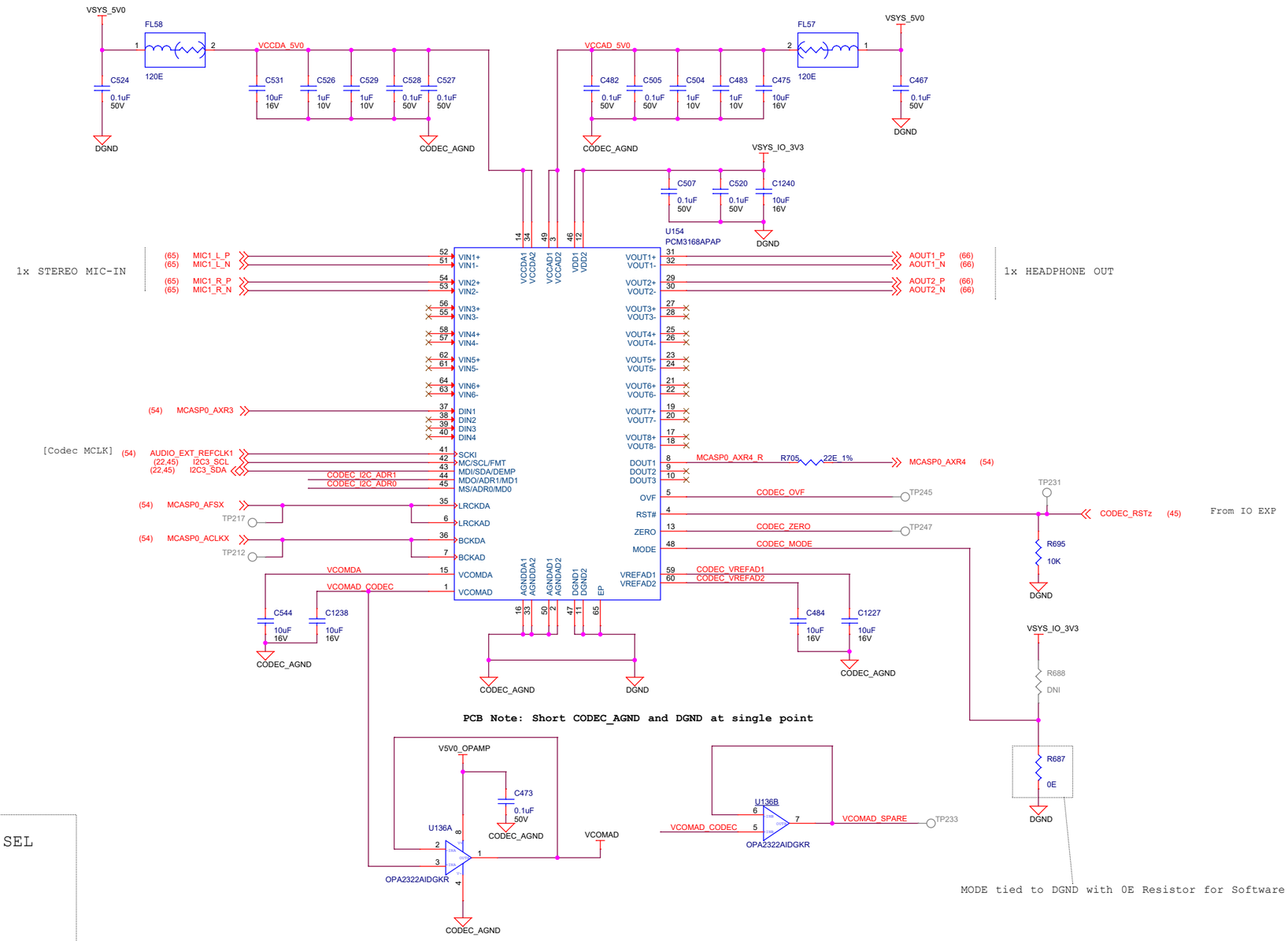
RGMII1_ACT_LED → U140 BSS138-7-F, gate RGMII1_LED2_ACT → DGND

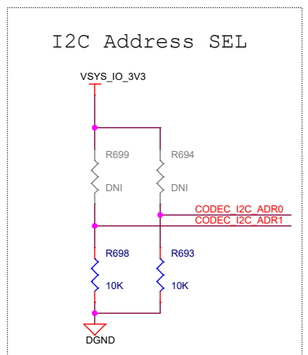
LED_2-MODE1 & LED_1-MODE2-TX SKEW=0nS
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2nS

Project : J7 EVM		Title	RGMII1
		Size C	PROC141 001 J784S4XG01EVM — Rev E4
		Date: Friday, May 05, 2023	Sheet 63 of 88

TEXAS INSTRUMENTS

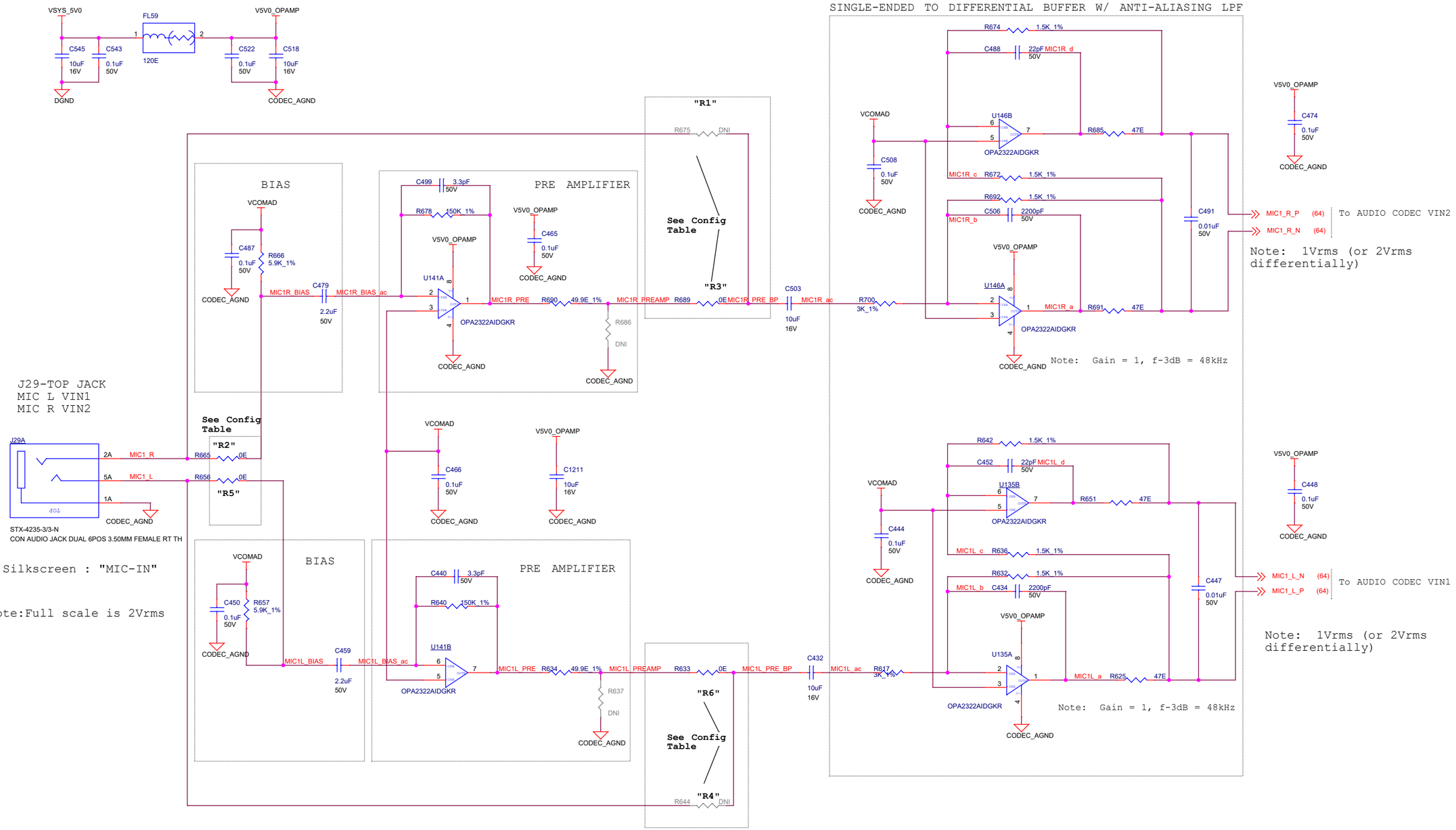
AUDIO I/F CODEC





Project : J7 EVM		Title: AUDIO I/F CODEC	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 64 of 88

AUDIO I/F - STEREO MIC #1



Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

Project : J7 EVM

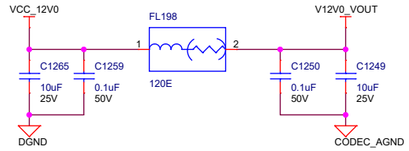
TEXAS INSTRUMENTS

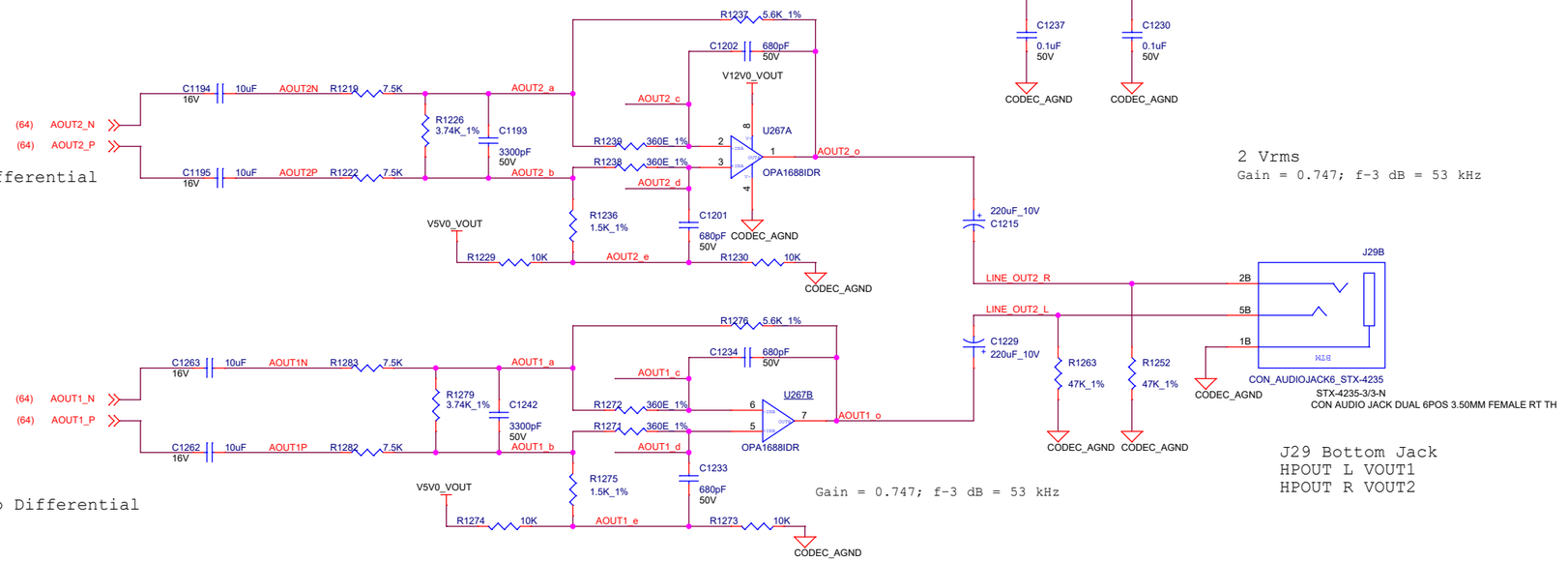
Title: AUDIO I/F - STEREO MIC #1

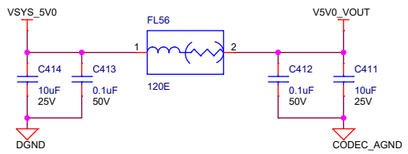
Size: C | PROC141 001 J784S4XG01EVM | Rev: E4

Date: Friday, May 05, 2023 | Sheet 65 of 88

AUDIO I/F - STEREO HEADPHONE OUT # 1

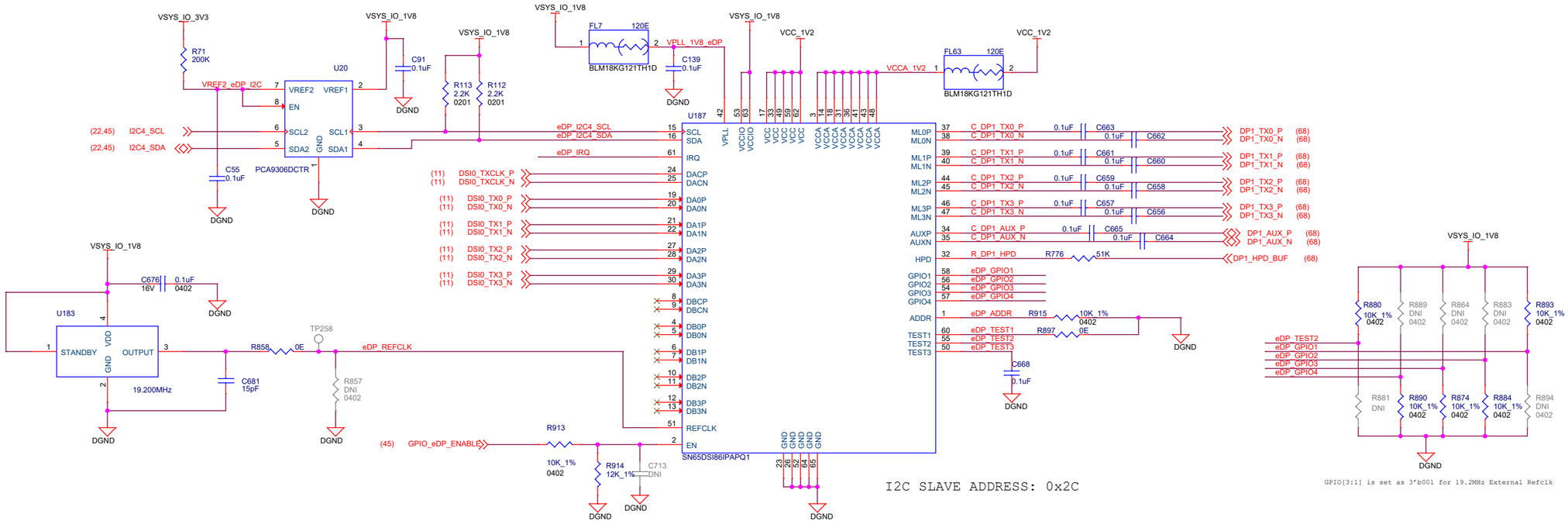


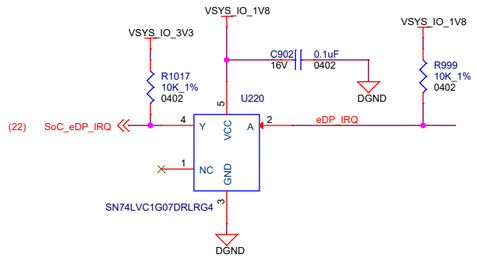


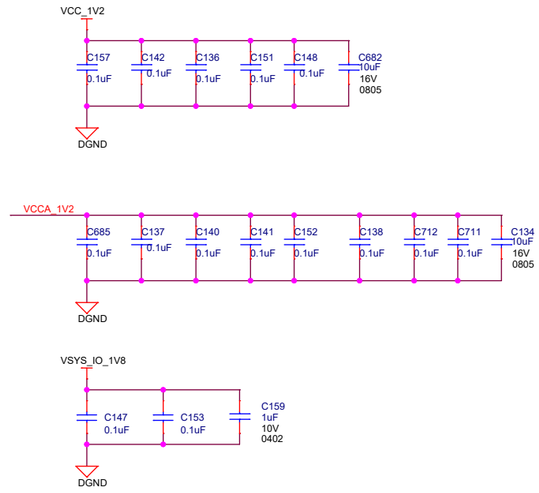


Project : J7 EVM		Title: AUDIO I/F - STEREO LINE OUT & HP OUT# 1	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 66 of 88

DSI to eDP Bridge







Project : J7 EVM	TEXAS INSTRUMENTS	Title: DSI TO EDP BRIDGE	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 67 of 88

DISPLAY PORT INTERFACE

Display Port Connector1

(13) DP0_TX0_P
(13) DP0_TX0_N
(13) DP0_TX1_P
(13) DP0_TX1_N
(13) DP0_TX2_P
(13) DP0_TX2_N
(13) DP0_TX3_P
(13) DP0_TX3_N
(12) DP0_AUX_P
(12) DP0_AUX_N

DLW21SZ900HQ2B
L14 90E
L11 90E
L16 90E
L12 90E
L18 90E

CON_DP0_TX0_P
CON_DP0_TX0_N
CON_DP0_TX1_P
CON_DP0_TX1_N
CON_DP0_TX2_P
CON_DP0_TX2_N
CON_DP0_TX3_P
CON_DP0_TX3_N
CON_DP0_AUX_P
CON_DP0_AUX_N

D14 D13 D20 D19
D16 D15 D26 D25
D28 D27
TPD1E05U06DPY

VSYS_IO_3V3
R45 100K
R44 100K
DGND

J9
ML_L0_P ML_L0_N
ML_L1_P ML_L1_N
ML_L2_P ML_L2_N
ML_L3_P ML_L3_N
AUX_CH_P AUX_CH_N
HPD
CONFIG1 CONFIG2
PWR RETURN
GND SH1 SH2 SH3 SH4

R757 0E DP0_CONFIG1
R754 0E DP0_CONFIG2

V3V3_DP0
C23 0.1uF 50V
C560 10uF 16V

Silkscreen: "DISPLAY PORT CONN0"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1

Display Port Connector2

(67) DP1_TX0_P
(67) DP1_TX0_N
(67) DP1_TX1_P
(67) DP1_TX1_N
(67) DP1_TX2_P
(67) DP1_TX2_N
(67) DP1_TX3_P
(67) DP1_TX3_N
(67) DP1_AUX_P
(67) DP1_AUX_N

DLW21SZ900HQ2B
L13 90E
L9 90E
L15 90E
L10 90E
L17 90E

CON_DP1_TX0_P
CON_DP1_TX0_N
CON_DP1_TX1_P
CON_DP1_TX1_N
CON_DP1_TX2_P
CON_DP1_TX2_N
CON_DP1_TX3_P
CON_DP1_TX3_N
CON_DP1_AUX_P
CON_DP1_AUX_N

D10 D9 D18 D17
D12 D11 D22 D21
D24 D23
TPD1E05U06DPY

VSYS_IO_3V3
R43 100K
R42 100K
DGND

J8
ML_L0_P ML_L0_N
ML_L1_P ML_L1_N
ML_L2_P ML_L2_N
ML_L3_P ML_L3_N
AUX_CH_P AUX_CH_N
HPD
CONFIG1 CONFIG2
PWR RETURN
GND SH1 SH2 SH3 SH4
CON_MUSB_20_F

R758 0E DP1_CONFIG1
R755 0E DP1_CONFIG2

V3V3_DP1
C566 10uF 16V
C22 0.1uF 50V

Silkscreen: "DISPLAY PORT CONN1"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN2

HPD buffer

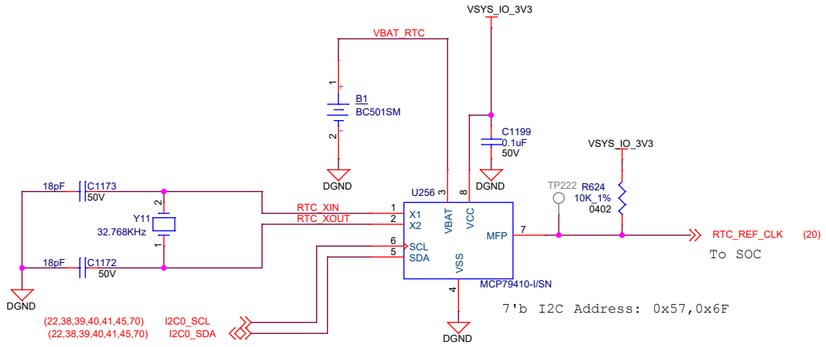
VSYS_IO_3V3
C1266 0.1uF 50V
U167
DP0_HPD
R759 100K
DP0_HPD_BUF (22)
NC
SN74LVC1G17DCKR

VSYS_IO_3V3
C1267 0.1uF 50V
U168
DP1_HPD
R760 100K
DP1_HPD_BUF (67)
NC
SN74LVC1G17DCKR

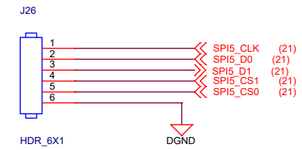
DGND

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DISPLAY PORT INTERFACE	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 68 of 88

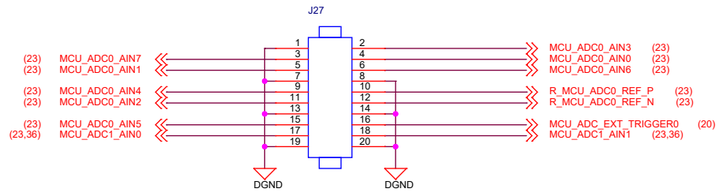
RTC



SPI Header



ADC INTERFACE



ADC Connector

I3C Header

Silk Screen MCU-I3C

Project : J7 EVM	TEXAS INSTRUMENTS	Title: ADC,RTC,I3C,APPLE AUTH_INTERFACE
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 69 of 88

x4LANE PCIe0 Interface

x4 Lane PCIe Connector

MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L (default)
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L
EP	R3,R2,R5, R6,R4	R1	Set for 2L

EXP_3V3 C630 0.1uF 50V C597 10uF 25V DGND
VCC_12V0 C118 10uF 25V C611 0.1uF 50V DGND
VSYS_IO_3V3 R87 10K R86 10K R85 10K R84 10K DGND
R815 10K "R1" "R3" R814 DNI R813 DNI "R4"
R823 10K R825 0E R824 10K R812 0E "R5" "R2" R811 0E "R6" R818 0E

J14

A1	PRSNT1#	+12V	B1		
A2	+12V	+12V	B2		
A3	+12V	+12V	B3		
A4	GND	GND	B4		
A5	JTAG2	SMCLK	B5	PCIe0_4L_SCL	
A6	JTAG3	SMDAT	B6	PCIe0_4L_SDA	
A7	JTAG4	GND	B7		
A8	JTAG5	+3.3V	B8		
A9	+3.3V	JTAG1	B9	PCIe0_TRST#	
A10	+3.3V	3.3VAUX	B10	V3V3_VAUX_PCIe0	
A11	PERST#	WAKE#	B11	PCIe0_INT#	
A12	GND	RSVD4	B12	PCIe0_CLKREQ#	
A13	REFCLK+	GND	B13		
A14	REFCLK-	PETP0	B14	PCIE0_TX0_P (13)	
A15	GND	PETN0	B15	PCIE0_TX0_N (13)	
A16	PERP0	GND	B16		
A17	PERN0	PRSNT2#_1	B17	PCIe0_PRSNT2#_1	
A18	GND	GND	B18		
A19	RSVD1	PETP1	B19	PCIE0_TX1_P (13)	
A20	GND	PETN1	B20	PCIE0_TX1_N (13)	
A21	PERP1	GND	B21		
A22	PERN1	GND	B22		
A23	GND	PETP2	B23	PCIE0_TX2_P (13)	
A24	GND	PETN2	B24	PCIE0_TX2_N (13)	
A25	PERP2	GND	B25		
A26	PERN2	GND	B26		
A27	GND	PETP3	B27	PCIE0_TX3_P (13)	
A28	GND	PETN3	B28	PCIE0_TX3_N (13)	
A29	PERP3	GND	B29		
A30	PERN3	RSVD3	B30		
A31	GND	PRSNT2#_2	B31	PCIe0_PRSNT2#_2	
A32	RSVD2	GND	B32		

PCIe0_PRSNT1# PCIe0_TCK PCIe0_TDI PCIe0_TDO PCIe0_TMS PCIe0_4L_PERSTz
CON_PCIE0_4L_REFCLK_P CON_PCIE0_4L_REFCLK_N
(13) PCIE0_RX0_P (13) PCIE0_RX0_N
(13) PCIE0_RX1_P (13) PCIE0_RX1_N
(13) PCIE0_RX2_P (13) PCIE0_RX2_N
(13) PCIE0_RX3_P (13) PCIE0_RX3_N (45) PCIe0_4L_PERSTz [To IO EXP]

VSYS_IO_3V3 R779 DNI DNI (45) PCIe0_4L_RC_RSTz [O/P of IO EXP] R782 10K DGND
C595 0.1uF 50V U175 SN74LVC1G08DBVRE4 PCIe0_AND_OUT
C34 0.1uF 50V U15 SN74CBTLV1G125DBVR PCIe0_4L_PERSTz
(20,30,36,39,44,50,59,63,70,71,72) SOC_PORZ_OUT
VSYS_IO_3V3 R54 DNI DNI C48 0.1uF 50V U14 SN74LVC1G00DCKRG4
From DIP SW (42,45) PCIe0_4L_MODE_SEL (45) PCIe0_4L_EP_RST_EN From IO EXP
PCIe0_NAND_OUT R73 10K DGND

C596 0.1uF 50V R802 10K TP16 U176 SN74CBTLV1G125DBVR PCIe0_PORz (43) To 3-in AND Gate

USB FOR WIFI/BT

C549 150uF_10V C561 0.1uF 50V VSYS_5V0 C556 0.1uF 50V C555 10uF 16V
J2 VBUS_5V_WIFI/BT U163 TPD3S014DBVR 0E R772 USB1_DN1_PE (59)
L39 90E DLW21SZ900HQ2B USB1_DN1_D_N (59) USB1_DN1_D_P (59)

I2C MUX

VSYS_IO_3V3 R820 DNI R821 DNI R157 10K R819 10K R822 10K
U181 TCA9543APWR
TCA9543_A0 TCA9543_A1 TCA9543_INT# (22,38,39,40,41,45,69) I2C0_SCL (22,38,39,40,41,45,69) I2C0_SDA
(20,30,36,39,44,50,59,63,70,71,72) SOC_PORZ_OUT
C655 0.1uF 50V R146 4.7K R147 4.7K R145 10K R159 4.7K R158 4.7K R160 10K
PCIe0_4L_SDA PCIe0_4L_SCL PCIe0_INT#
PCIe1_2L_SDA (71) PCIe1_2L_SCL (71) PCIe1_INT# (71)

I2C ADDRESS: 0X70

CLOCK ROOT SELECTION

	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

Place R1,R2 close to SOC
"R1" R176 0E "R2" R166 0E CLKGEN_SERDES1_REFCLK_P (39) CLKGEN_SERDES1_REFCLK_N (39)
"R5" R77 0E "R6" R92 0E CLKGEN_PCIE0_4L_REFCLK_P (39) CLKGEN_PCIE0_4L_REFCLK_N (39)
Place R5,R6 close to PCIe connector
"R3" R177 DNI R_SERDES1_REFCLK_P "C1" C63 DNI 50V
"R4" R167 DNI R_SERDES1_REFCLK_N "C2" C66 DNI 50V
to SOC (13) SOC_SERDES1_REFCLK_P (13) SOC_SERDES1_REFCLK_N
"Added to avoid stub" Place R3,R4 close to SOC
Place C1, C2 close to PCIe connector
R83 DNI to PCIe Con (x4 Lane) CON_PCIE0_4L_REFCLK_P CON_PCIE0_4L_REFCLK_N

Project : J7 EVM
TEXAS INSTRUMENTS
Title: x1LANE PCIe INTERFACE
Size: C | PROC141 001 J784S4XG01EVM | Rev: E4
Date: Friday, May 05, 2023 | Sheet 70 of 88

x2LANE PCIe1 Interface(J17)

x4 Lane PCIe Connector

MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L (default)
EP	R3,R2,R5, R6,R4	R1	Set for 2L

EXP_3V3 C691 0.1uF 50V C654 10uF 25V DGND

VCC_12V0 C693 10uF 25V C692 0.1uF 50V DGND

VSYS_IO_3V3 R164 10K R163 10K R162 10K

VSYS_IO_3V3 "R1" R854 10K "R3" R853 DNI PCIe1_PRSNT1# DGND

R848 DNI

R161 10K DGND

J17

A1	PRSNT1#		B1		
A2	+12V		B2	+12V	
A3	+12V		B3	+12V	
A4	GND		B4	GND	
A5	JTAG2	PCIe1_TCK	B5	SMCLK	PCIe1_2L_SCL (70)
A6	JTAG3	PCIe1_TDI	B6	SMDAT	PCIe1_2L_SDA (70)
A7	JTAG4	PCIe1_TDO	B7	GND	
A8	JTAG5	PCIe1_TMS	B8	+3.3V	
A9	+3.3V		B9	JTAG1	PCIe1_TRST#
A10	+3.3V		B10	3.3VAUX	V3V3_VAUX_PCIe1
A11	PERST#	PCIe1_4L_PERSTz	B11	WAKE#	PCIe1_INT# (70)
A12	GND		B12	RSVD4	PCIe1_CLKREQ#
A13	REFCLK+	CON_PCIE1_2L_REFCLK_P	B13	GND	
A14	REFCLK-	CON_PCIE1_2L_REFCLK_N	B14	PETP0	PCIE1/HYP0_TX0_P (12)
A15	GND		B15	PETN0	PCIE1/HYP0_TX0_N (12)
A16	PERP0	(12) PCIE1/HYP0_RX0_P	B16	GND	
A17	PERN0	(12) PCIE1/HYP0_RX0_N	B17	PRSNT2#_1	PCIe1_PRSNT2_1#
A18	GND		B18	GND	
A19	RSVD1		B19	PETP1	PCIE1/HYP0_TX1_P (12)
A20	GND		B20	PETN1	PCIE1/HYP0_TX1_N (12)
A21	PERP1	(12) PCIE1/HYP0_RX1_P	B21	GND	
A22	PERN1	(12) PCIE1/HYP0_RX1_N	B22	GND	
A23	GND		B23	PETP2	PCIE1/HYP0_TX2_P (12)
A24	GND		B24	PETN2	PCIE1/HYP0_TX2_N (12)
A25	PERP2	(12) PCIE1/HYP0_RX2_P	B25	GND	
A26	PERN2	(12) PCIE1/HYP0_RX2_N	B26	GND	
A27	GND		B27	PETP3	PCIE1/HYP0_TX3_P (12)
A28	GND		B28	PETN3	PCIE1/HYP0_TX3_N (12)
A29	PERP3	(12) PCIE1/HYP0_RX3_P	B29	GND	
A30	PERN3	(12) PCIE1/HYP0_RX3_N	B30	RSVD3	
A31	GND		B31	PRSNT2#_2	PCIe1_PRSNT2_2#
A32	RSVD2		B32	GND	

85E

VCC_12V0 EXP_3V3 DGND

VSYS_IO_3V3 R871 DNI EXP_3V3 R872 0E

R882 "R2" 0E

R879 0E

R878 0E PCIe1_4L_PRSNT# (45) To IO EXP

R873 10K DGND

VSYS_IO_3V3 R902 DNI DNI C708 0.1uF 50V U190

(45) PCIe1_2L_RC_RSTz [O/P of IO EXP] R901 10K DGND

SN74LVC1G08DBVRE4

PCIe1_AND_OUT

VSYS_IO_3V3 C177 0.1uF 50V U38

SN74CBTLV1G125DBVR

PCIe1_4L_PERSTz PCIe1_4L_PERSTz (45) [To IO EXP]

(20,30,36,39,44,50,59,63,70,72) SOC_PORZ_OUT

VSYS_IO_3V3 R182 DNI DNI C161 0.1uF 50V U33

From DIP SW

(42,45) PCIe1_2L_MODE_SEL

(45) PCIe1_2L_EP_RST_EN From IO EXP

R183 10K DGND

SN74LVC1G00DCKRG4

PCIe1_NAND_OUT

VSYS_IO_3V3 C715 0.1uF 50V R912 10K U196 TP40

PCIe1_PORz (43) To 3-in AND Gate

SN74CBTLV1G125DBVR

CLOCK ROOT SELECTION

	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

Place R1,R2 close to SOC

"R1" R171 DNI "R2" R170 DNI CLKGEN_SERDES0_REFCLK_P (39) CLKGEN_SERDES0_REFCLK_N (39)

"R5" R155 DNI "R6" R152 DNI CLKGEN_PCIE1_2L_REFCLK_P (39) CLKGEN_PCIE1_2L_REFCLK_N (39)

Place R5,R6 close to PCIe connector

to SOC (12) SOC_SERDES0_REFCLK_P (12) SOC_SERDES0_REFCLK_N

"R3" R169 0E R_SERDES0_REFCLK_P C129 0E "C1"

"R4" R168 0E R_SERDES0_REFCLK_N C125 0E "C2"

"Added to avoid stub" Place R3,R4 close to SOC

R153 DNI

to PCIe Con (x2 Lane) CON_PCIE1_2L_REFCLK_P CON_PCIE1_2L_REFCLK_N

Project : J7 EVM

Texas Instruments

Title: x2LANE PCIe Interface

Size: C | PROC141 001 J784S4XG01EVM | Rev: E4

Date: Friday, May 05, 2023 | Sheet 71 of 88

BOOT MODE BUFFER & SWITCHES

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

I2C ADDRESS: 0x22

BOOTMODE Control Buffers

Place TP1 and TP2 with 100mils spacing to insert external jumper

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

DIR = H: A -> B

DIR = H: A -> B

TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

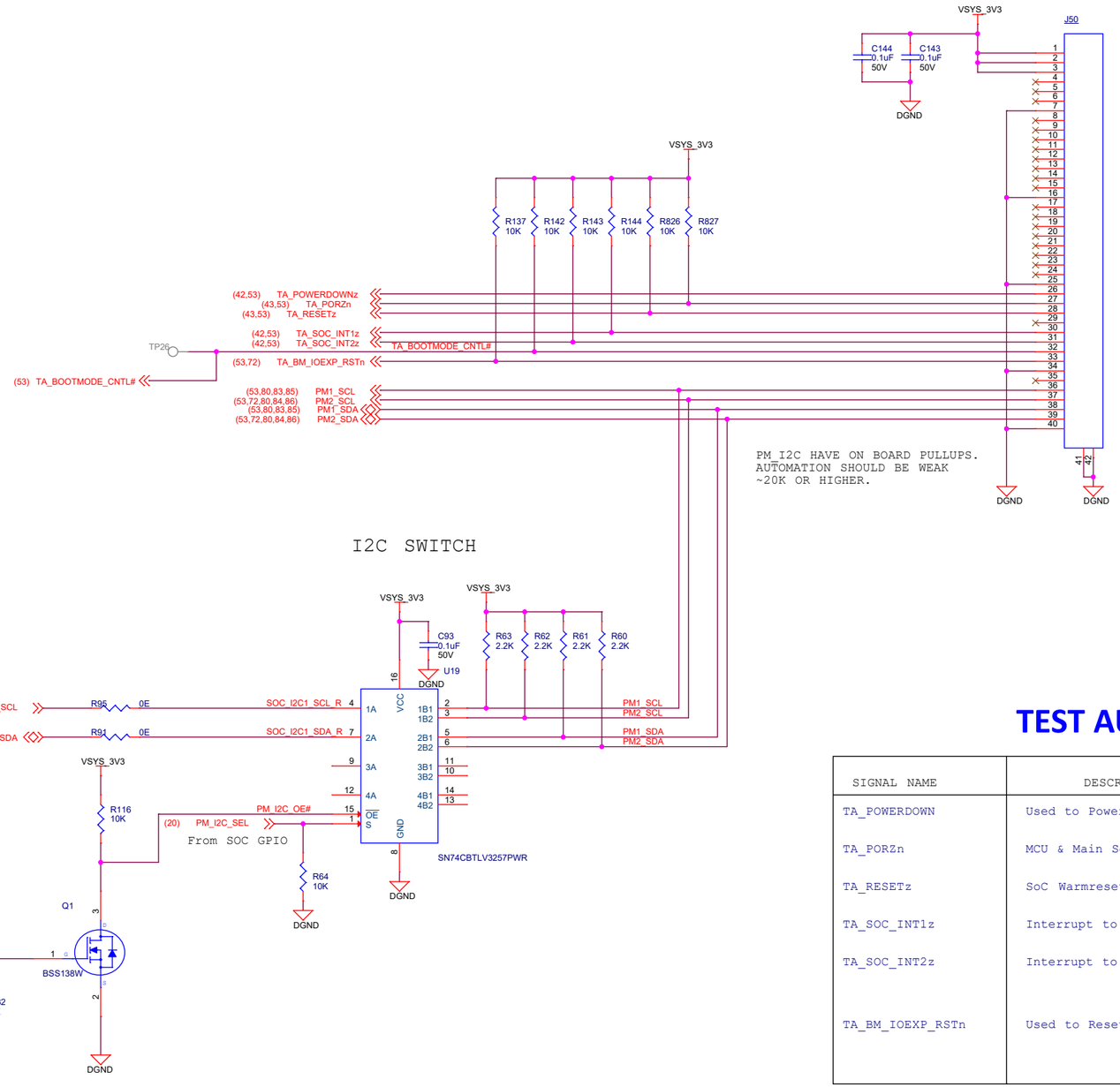
Project : J7 EVM

TEXAS INSTRUMENTS

Title: BOOT MODE BUFFER & SWITCHES

Size		Rev
C	PROC141 001 J784S4XG01EVM	E4
Date: Friday, May 05, 2023	Sheet 72 of 88	

TEST AUTOMATION HEADER

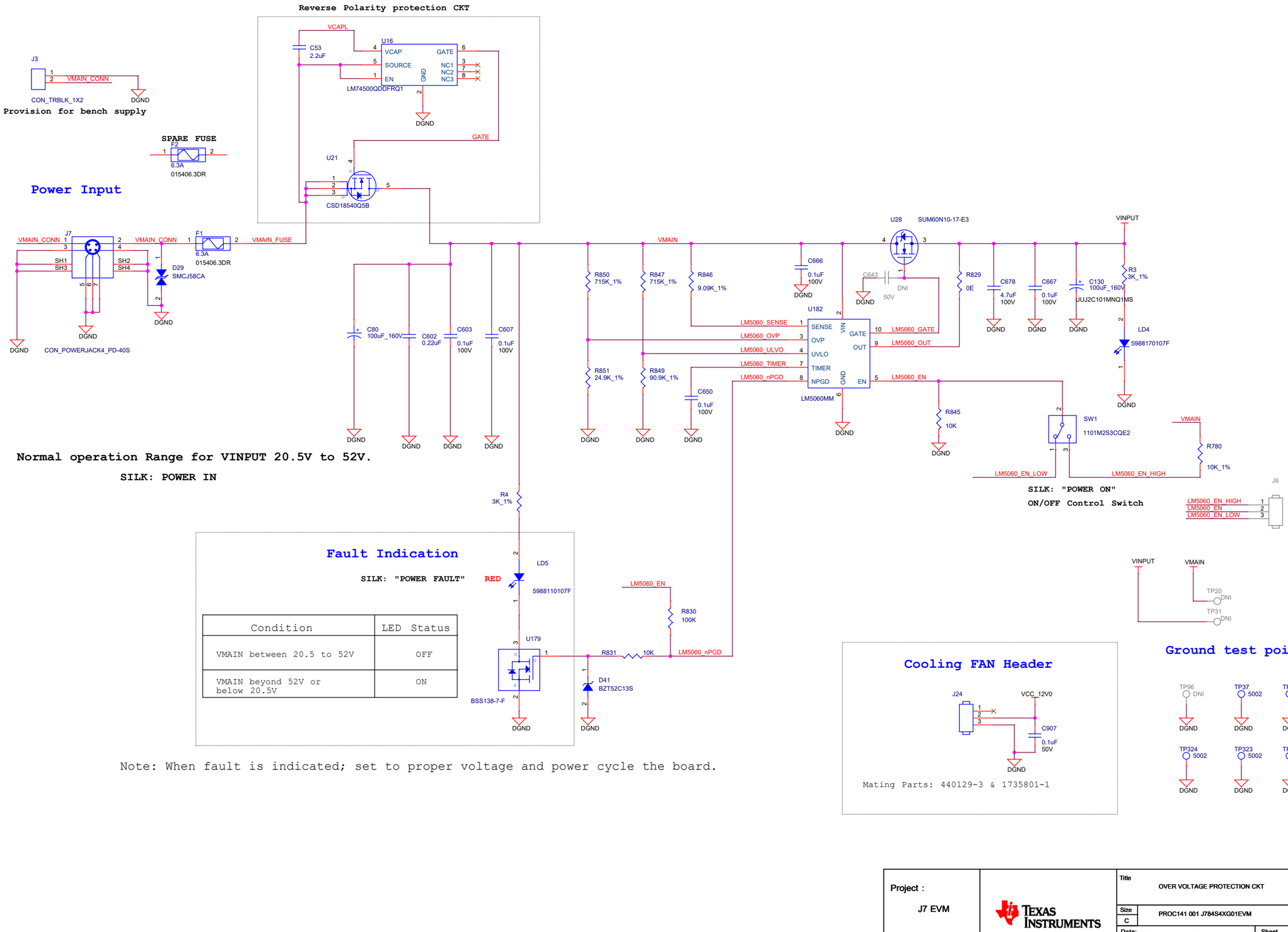


TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Project : J7 EVM	TEXAS INSTRUMENTS	Title: TEST AUTOMATION HEADER Size: C — PROC141 001 J784S4XG01EVM — Rev: E4 Date: Friday, May 05, 2023 — Sheet 73 of 88

OVER VOLTAGE PROTECTION CIRCUIT



Condition	LED Status
VMAIN between 20.5 to 52V	OFF
VMAIN beyond 52V or below 20.5V	ON

Normal operation Range for VINPUT 20.5V to 52V.

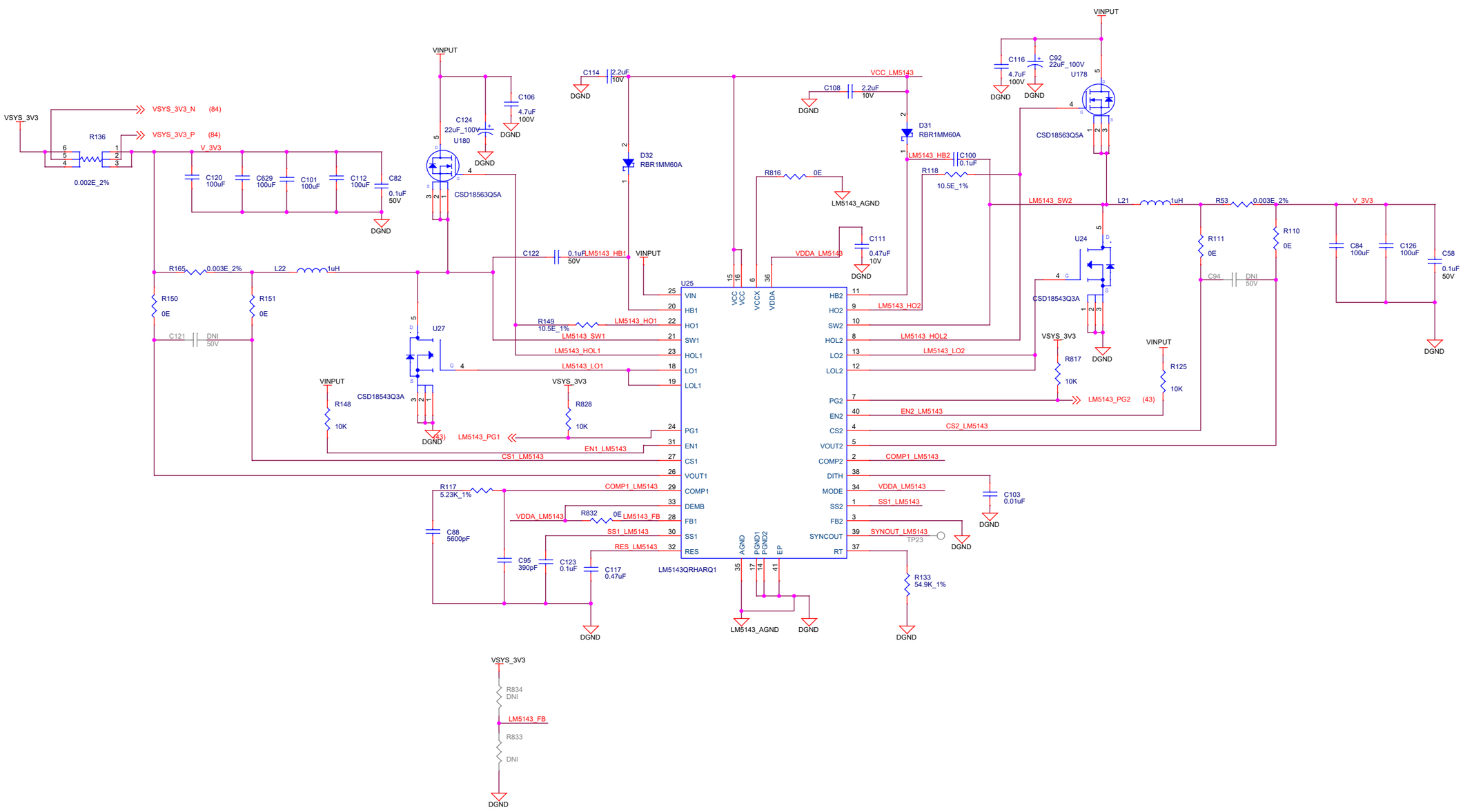
SILK: POWER IN

Note: When fault is indicated; set to proper voltage and power cycle the board.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: OVER VOLTAGE PROTECTION CKT	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 74 of 88

TI WEBENCH Simulation Inputs:
Vin (min) = 24V Vin (max) = 48V
Vout = 3.3V@30A
Ta = 25 deg

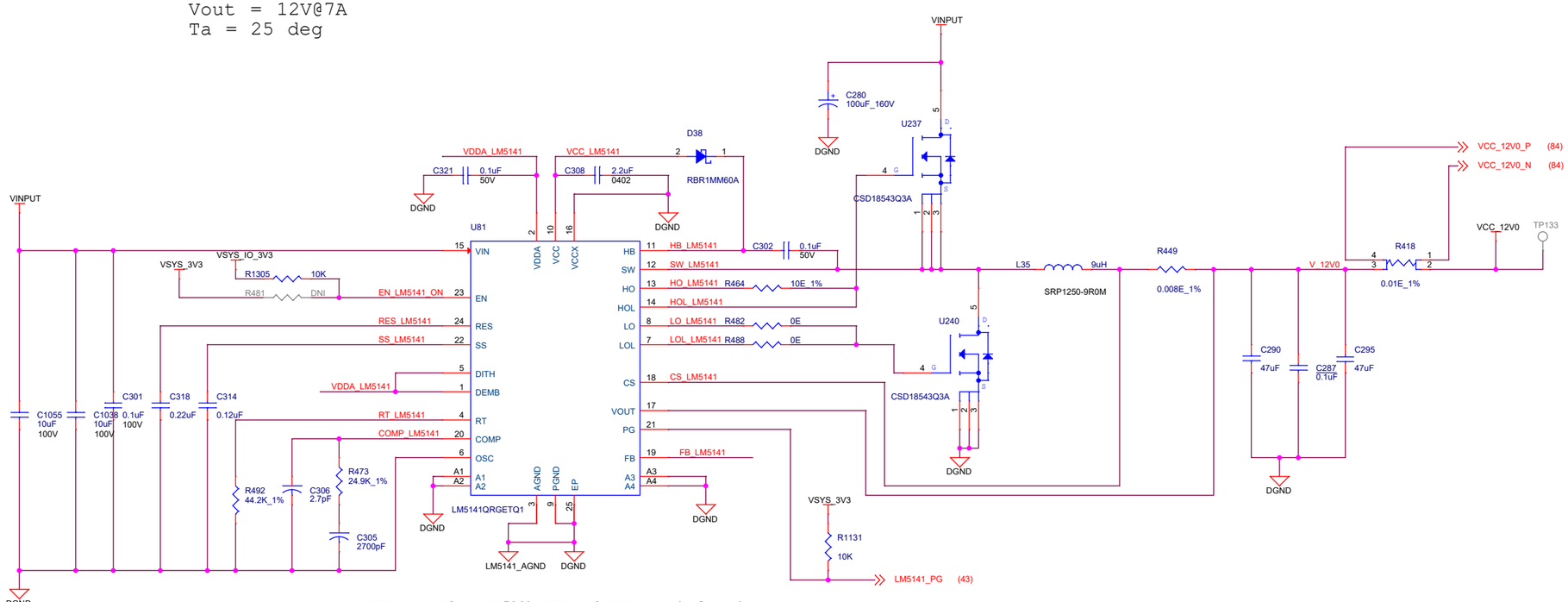
POWER SUPPLY #1



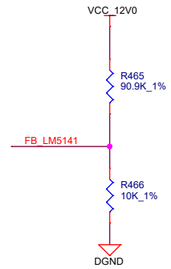
Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY #3	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 75 of 88

POWER SUPPLY #2

TI WEBENCH Simulation Inputs:
Vin (min) = 24V Vin (max) = 48V
Vout = 12V@7A
Ta = 25 deg



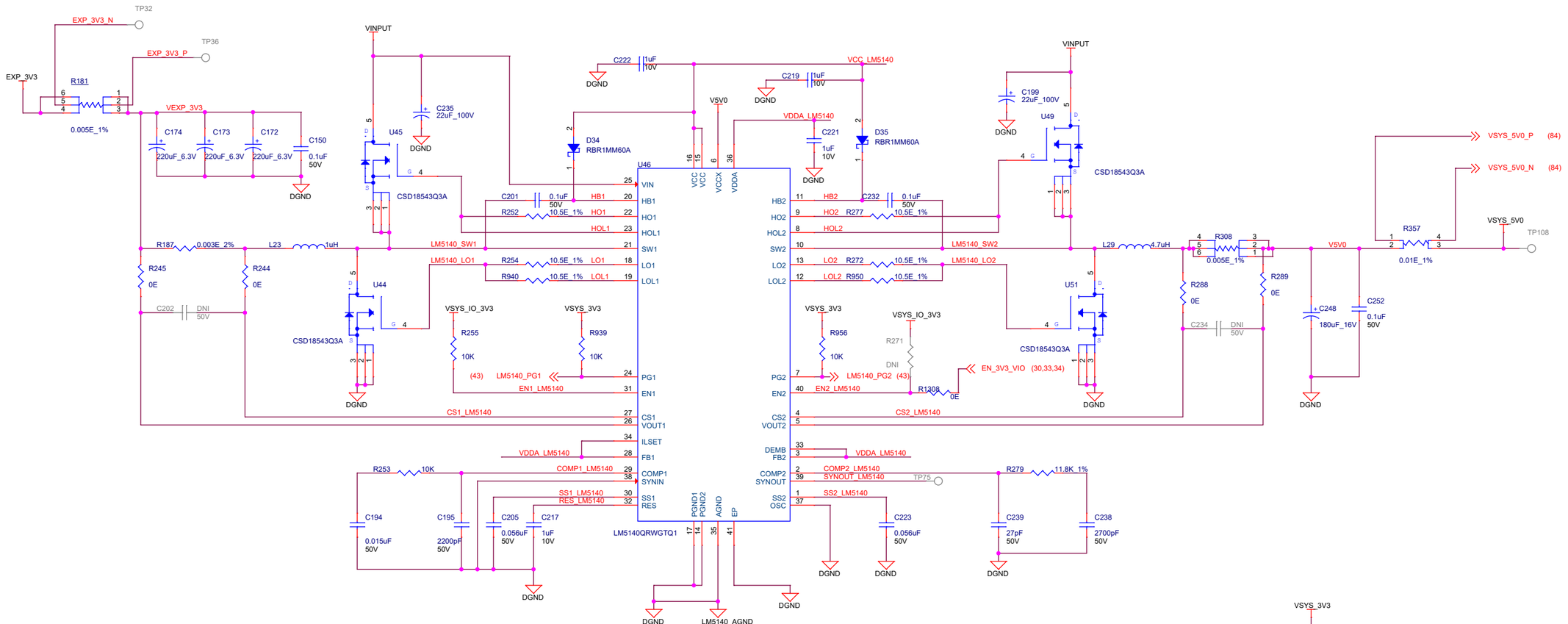
PCB Note: Short LM5141_AGND and DGND at single point



Project : J7 EVM	Texas Instruments	Title: POWER SUPPLY #2	
		Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
		Date: Friday, May 05, 2023	Sheet 76 of 88

POWER SUPPLY #3
3.3V AND 5V GENERATION

TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout1 = 3.3V@10A; Vout2 = 5V@7A
Ta = 25 deg



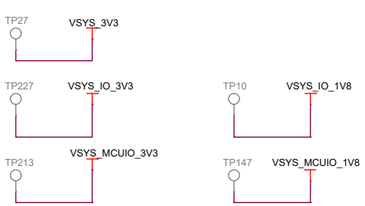
PCB Note: Short LM5140_AGND and DGND at single point

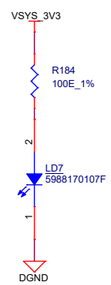
FB1 connected to VDDA to set VOUT1=3.3V
FB2 connected to VDDA to set VOUT2=5V

OSC pin to VCC sets fs=2.2MHz
OSC pin to GND sets fs=440kHz

DEMB-VDDA- FPWM mode operation
DEMB-GND- enables diode emulation

ILSET pin to VDDA sets current limit
threshold to 73 mV
ILSET pin to GND sets current limit
threshold to 48 mV





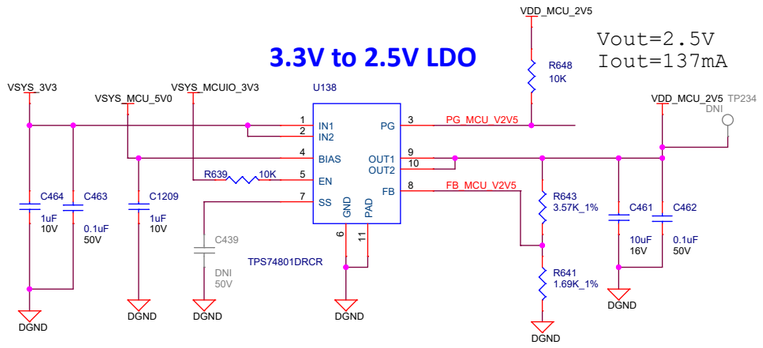
Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY #1
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 77 of 88

POWER SUPPLY #4

ETHERNET POWER- MCU RGMII

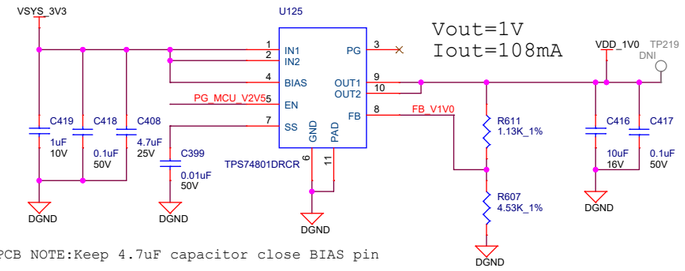
3.3V to 2.5V LDO

Vout=2.5V
Iout=137mA



3.3V to 1.0V LDO

Vout=1V
Iout=108mA

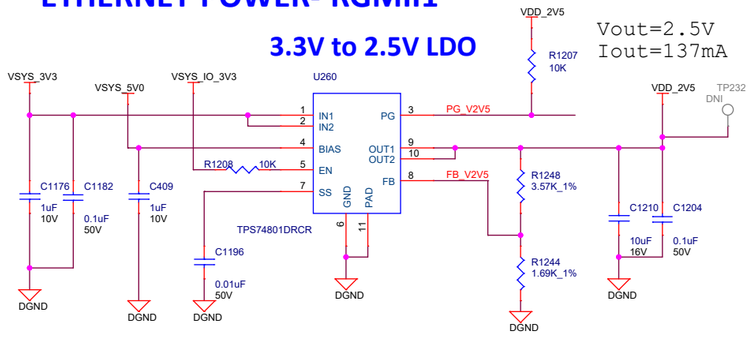


PCB NOTE:Keep 4.7uF capacitor close BIAS pin

ETHERNET POWER- RGMII1

3.3V to 2.5V LDO

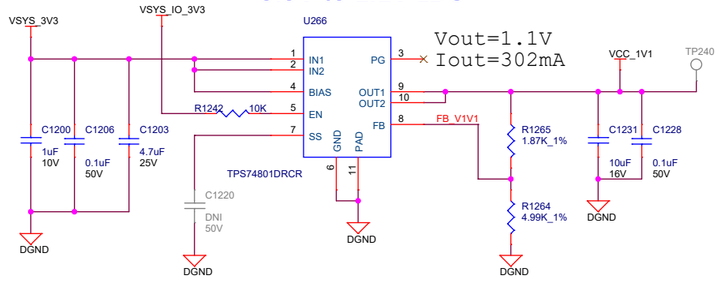
Vout=2.5V
Iout=137mA



USB HUB POWER & ETHERNET POWER - RGMII1

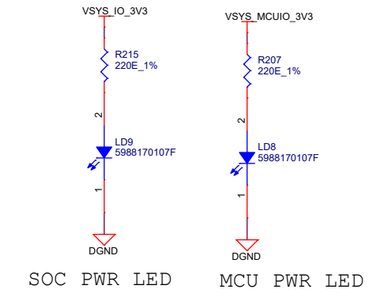
3.3V to 1.1V LDO

Vout=1.1V
Iout=302mA



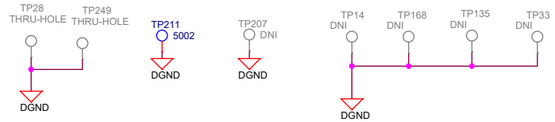
PCB NOTE:Keep 4.7uF capacitor close BIAS pin

POWER INDICATION LED's



SOC PWR LED MCU PWR LED

GROUND TEST POINTS

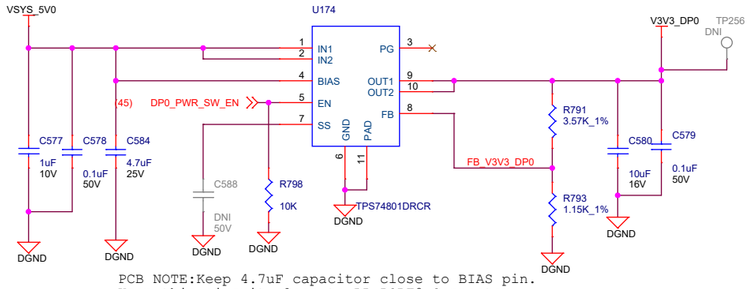


PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

Display Port0

5V to 3.3V LDO

Vout=3.3V
Iout=500mA

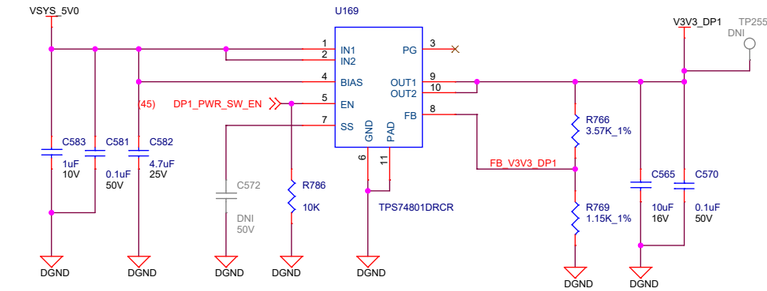


PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT0 Connector

Display Port1

5V to 3.3V LDO

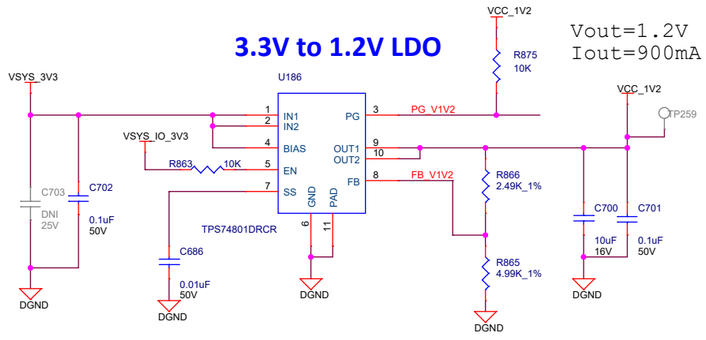
Vout=3.3V
Iout=500mA



PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT1 Connector.

3.3V to 1.2V LDO

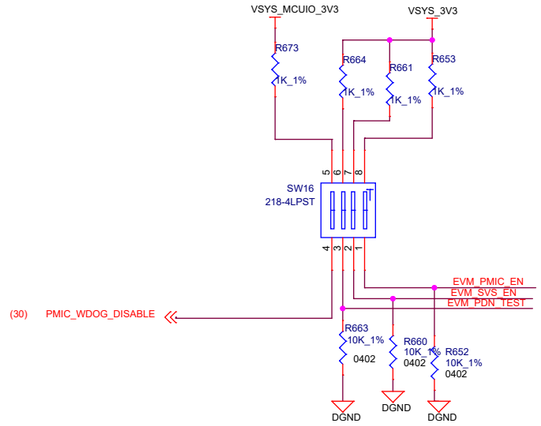
Vout=1.2V
Iout=900mA

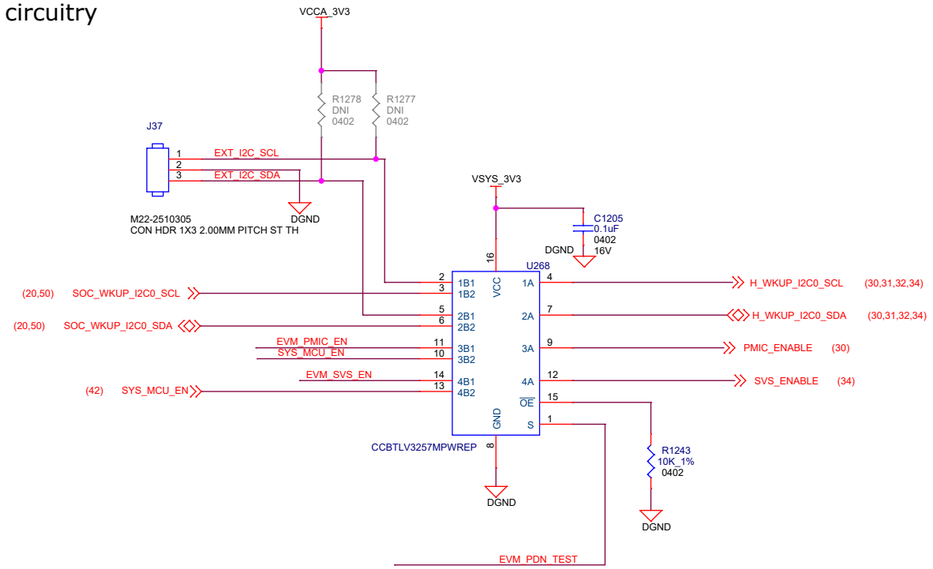


Project : J7 EVM	Title: POWER SUPPLY #4	
	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 78 of 88

EVM PMIC Support Circuitry

EVM development & evaluation Test circuitry
(TI EVM Only)





(EVM Bd Setting & Leo NVM Default):

SW16	Function
-1 = Closed (High) **= Open (Low)**	Enable the PMIC by overriding SYS_MCU_ENABLE **Enble the PMIC from SYS_MCU_EN**
-2 = Closed (High) **= Open (Low)**	ENABLE SVS EN from SW16.2 **ENABLE SVS EN FROM SYS_MCU_EN**
-3 = Closed (High) = Open (Low)	**1. PMIC EN from SYS_MCU_EN** **2. On Board WKUP I2C0 is selected** **3. SVS_EN is controlled from SYS_MCU_EN** 1. PMIC_EN is controlled from SW16.1 2. EXT_I2C is selected 3. SVS_EN is controlled from SW16.2
-4 = Closed (High) = Open (Low)	**Disable WDOG Timer** Enable WDOG Timer

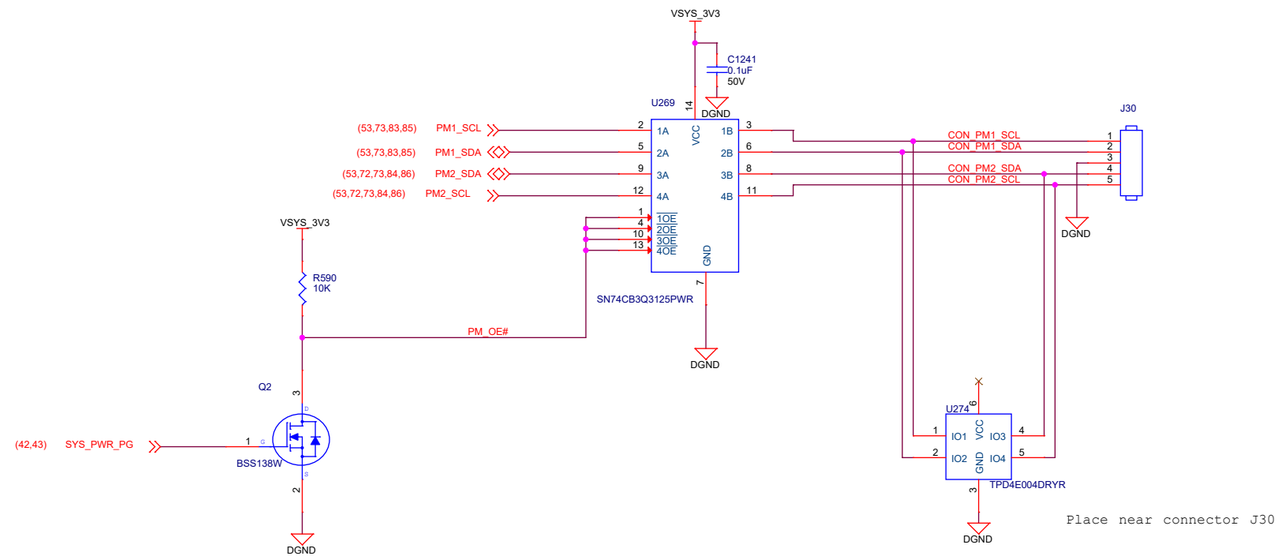
OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open

Project : J7 EVM	TEXAS INSTRUMENTS	Title: PMIC SUPPORT CIRCUITRY	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 79 of 88

EVM POWER MEASUREMENT I2C BUS ISOLATION

EVM development & evaluation Test circuitry

(TI EVM Only)

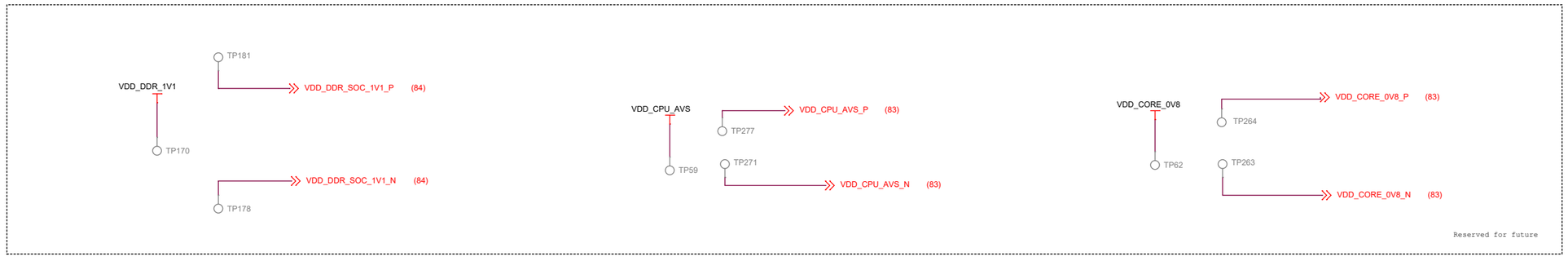


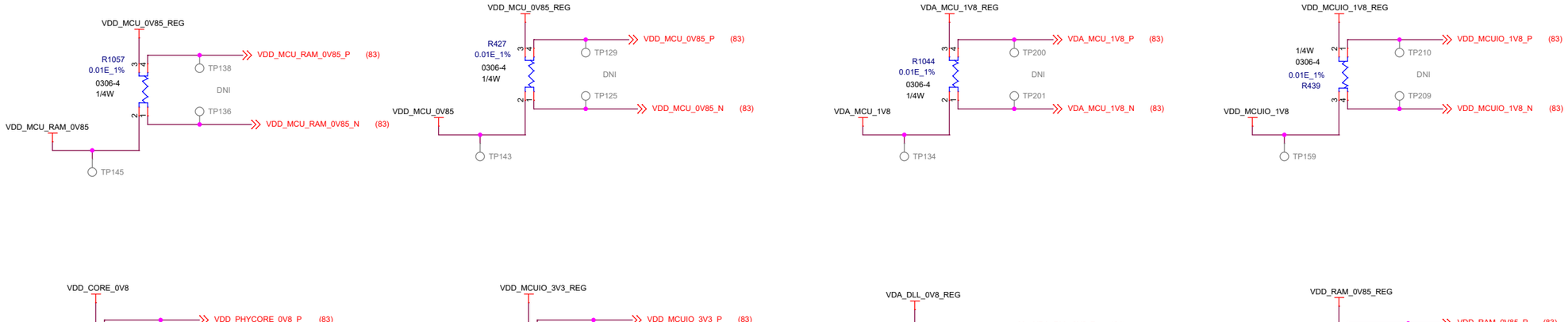
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EXTERNAL POWER MEASUREMENT WITH ISOLATION
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 80 of 88

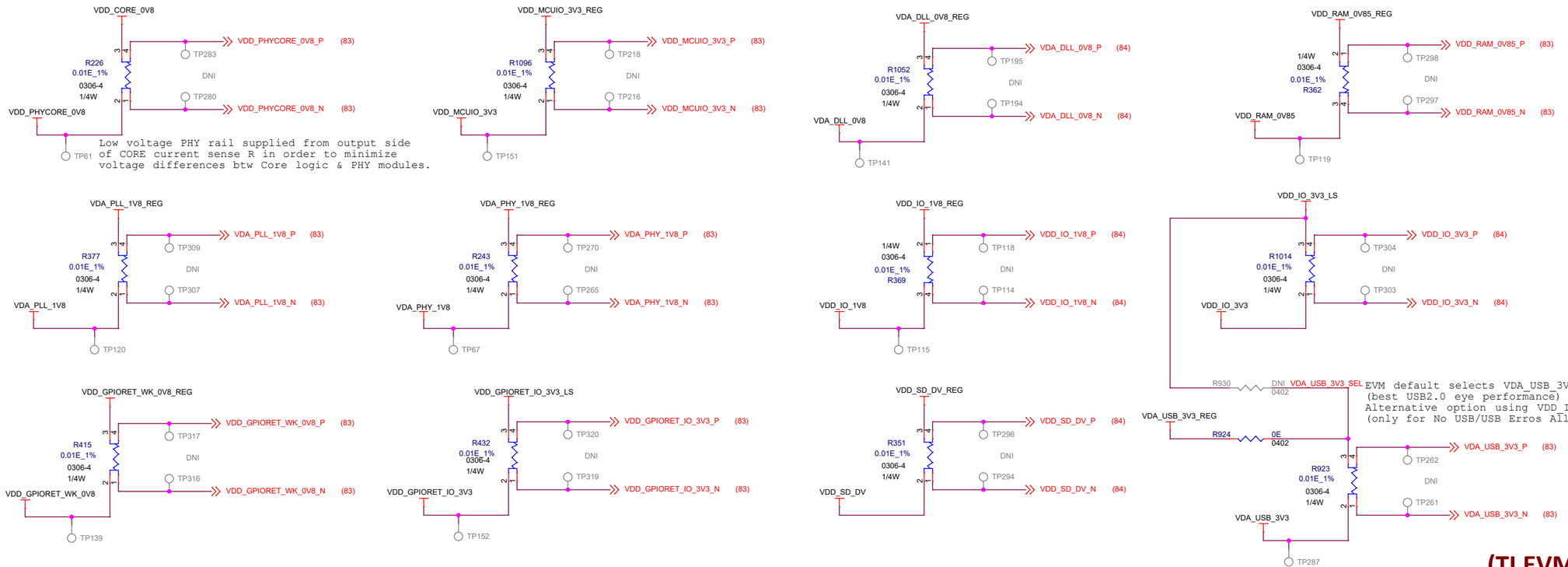
(TI EVM Only)

SOC Current Sense Resistors

(TI EVM Only)





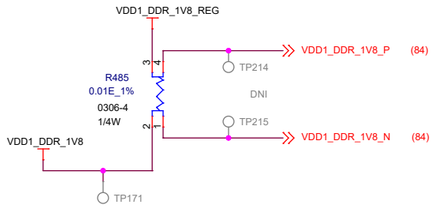


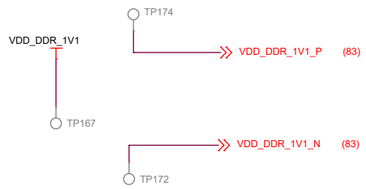
(TI EVM Only)

(TI EVM Only)

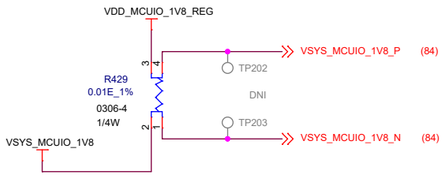
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC Current Sense Resistors
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 81 of 88

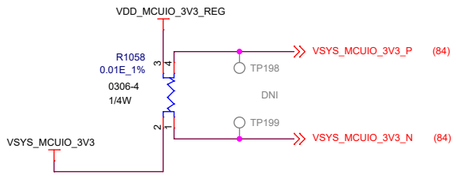
LPDDR4 SDRAM Current Sense Resistors

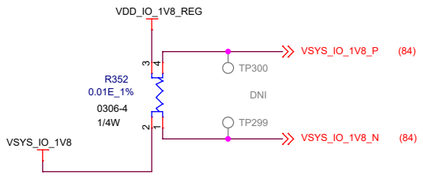


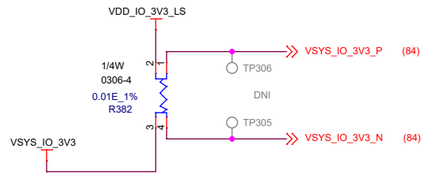


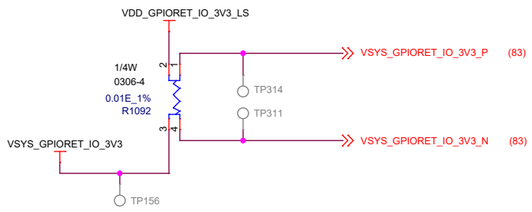
Peripheral Current Sense Resistors



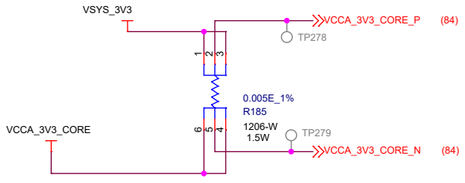


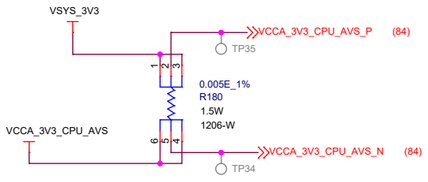


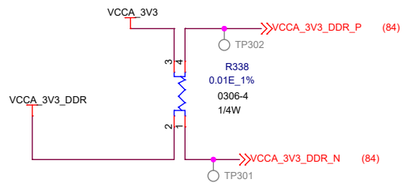




CORE, AVS and DDR input supply sense resistors



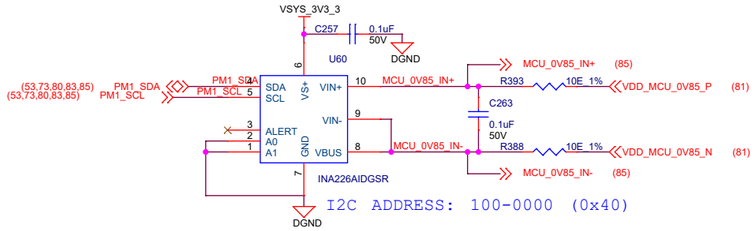


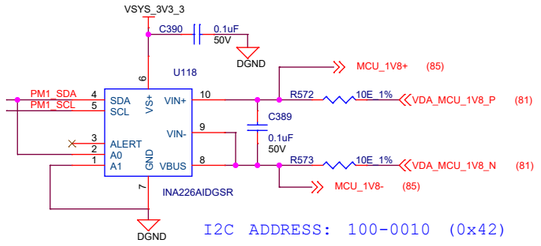


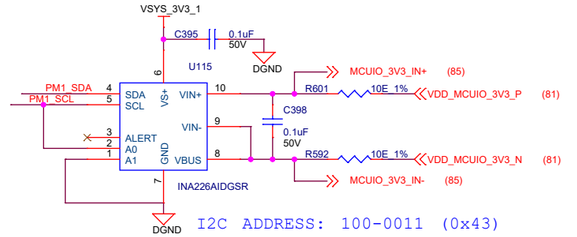
Project : J7 EVM	TEXAS INSTRUMENTS	Title: Peripheral Current Sense Resistors
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 82 of 88

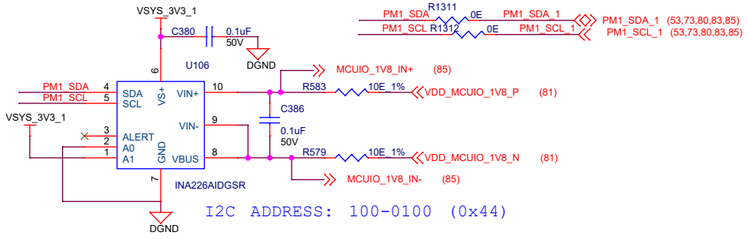
CURRENT MONITORS #1

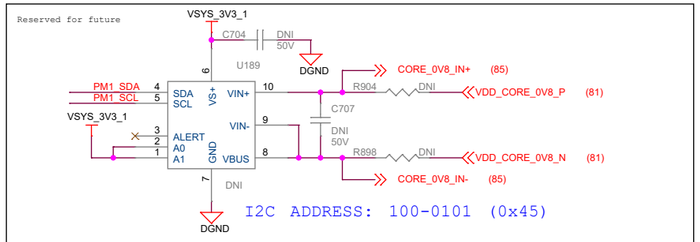
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA

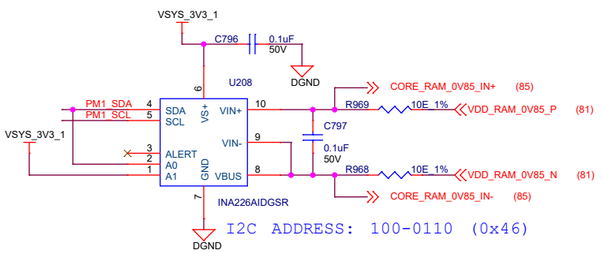


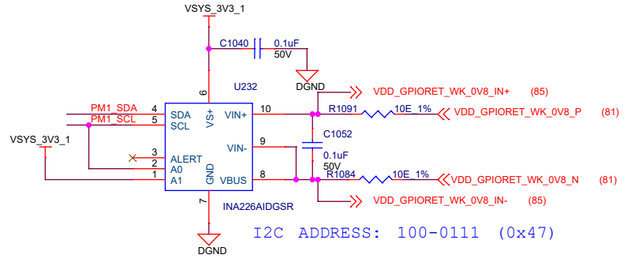


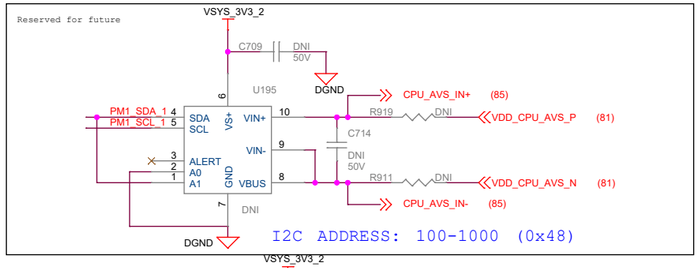


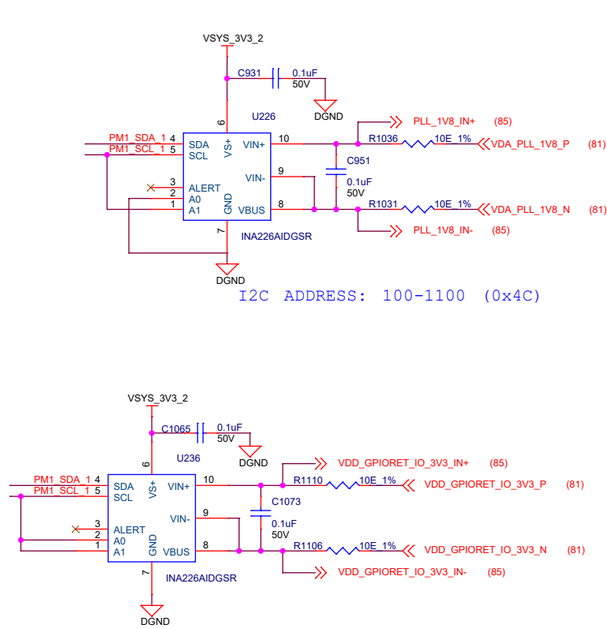


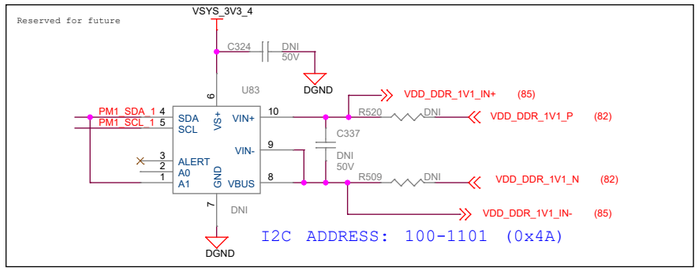


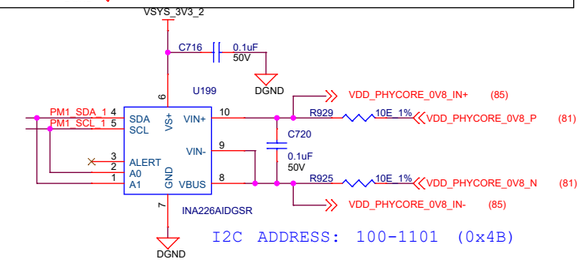


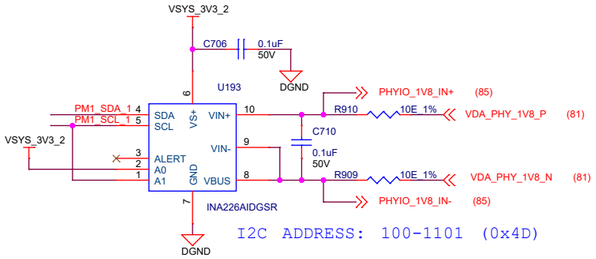


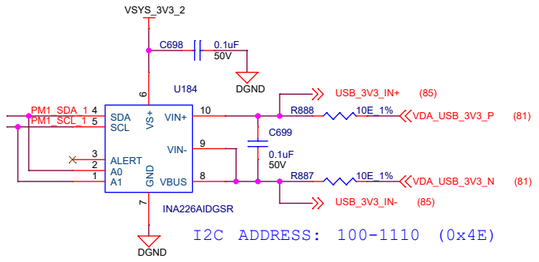


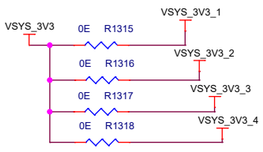


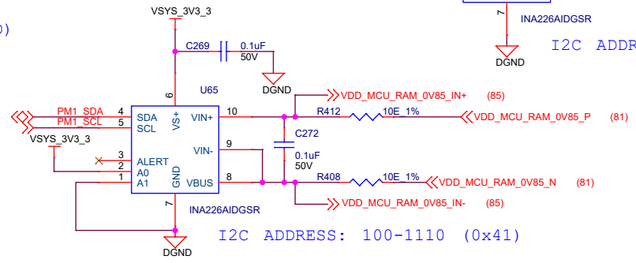








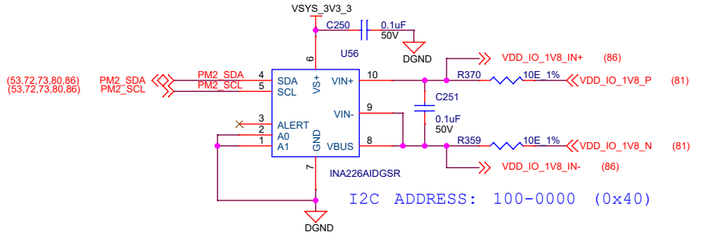


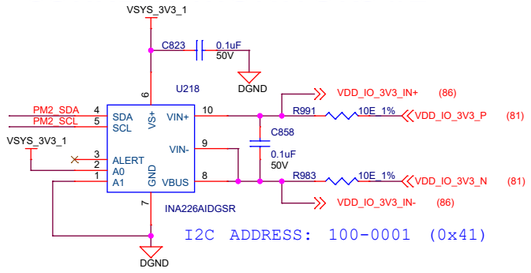


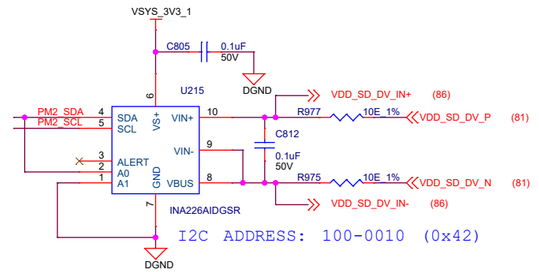
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CURRENT MONITORS #1	
		Size: C	PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023	Sheet 83 of 88

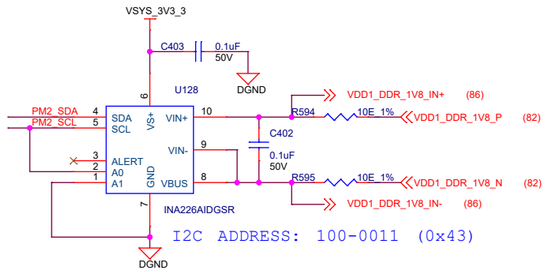
CURRENT MONITORS #2

Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

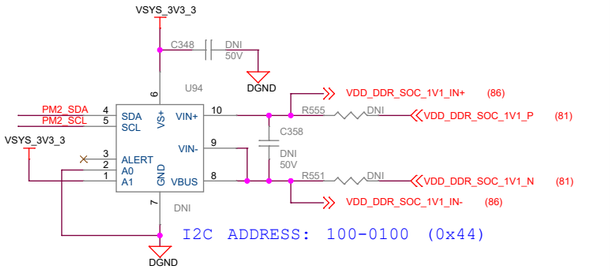


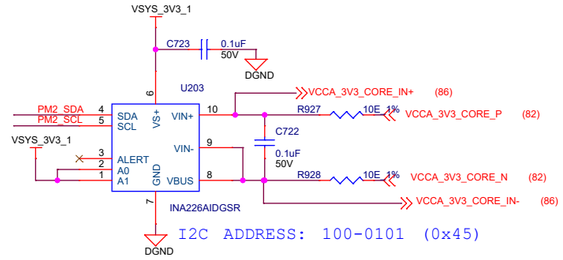


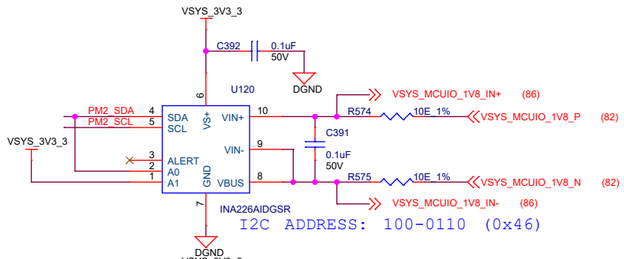


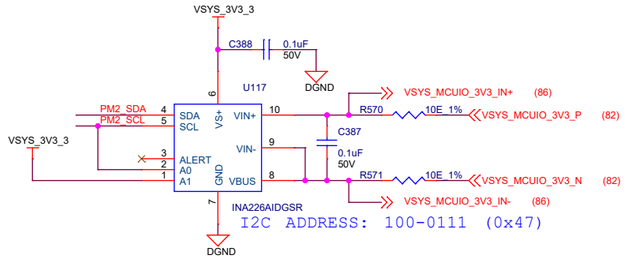


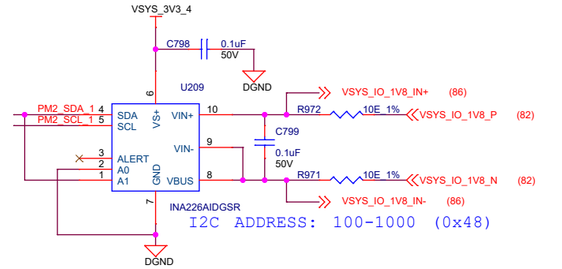
Reserved for future

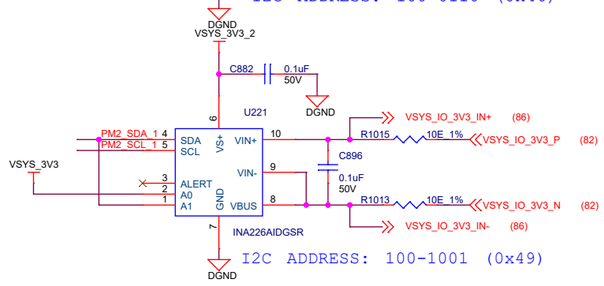


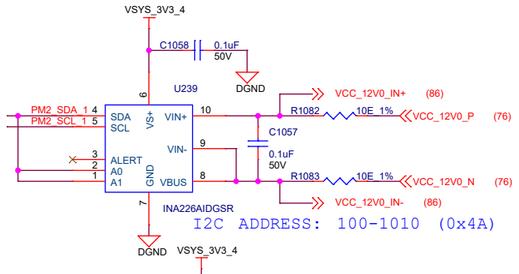


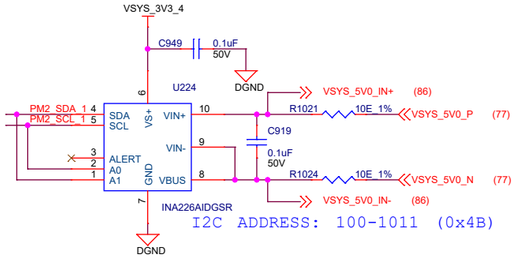


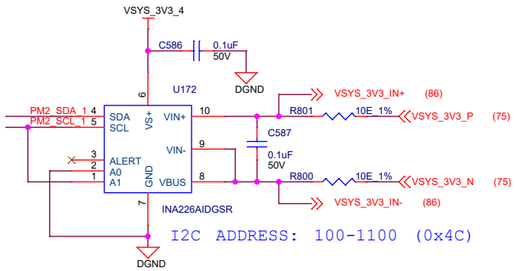


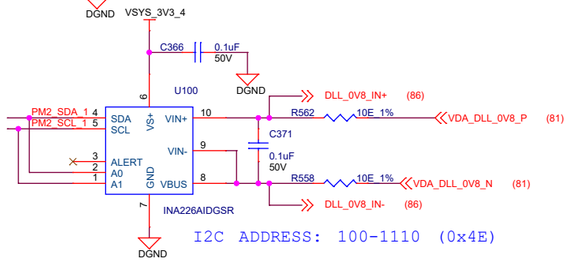


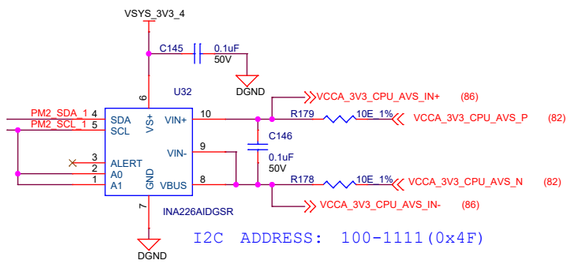


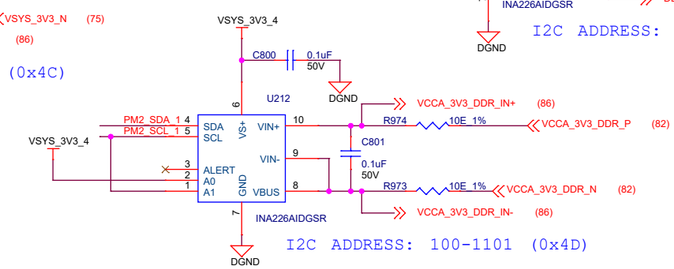


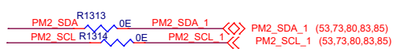










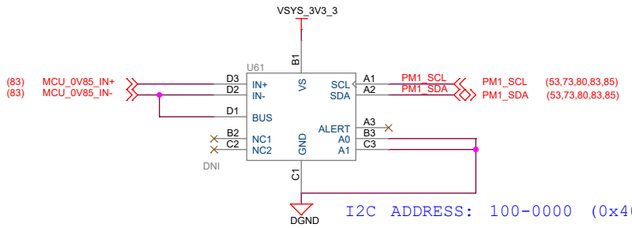


Project : J7 EVM	Title: CURRENT MONITORS #2	
	Size: C — PROC141 001 J784S4XG01EVM	Rev: E4
	Date: Friday, May 05, 2023	Sheet 84 of 88

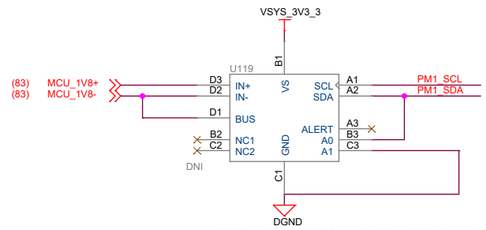
TEXAS INSTRUMENTS

CURRENT MONITORS - INA231

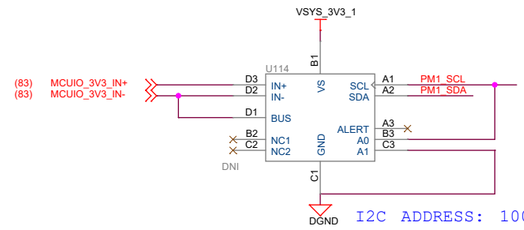
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA



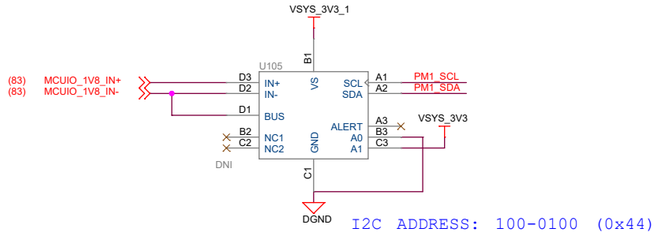
I2C ADDRESS: 100-0000 (0x40)



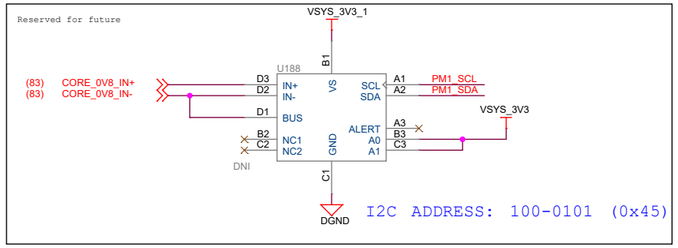
I2C ADDRESS: 100-0010 (0x42)



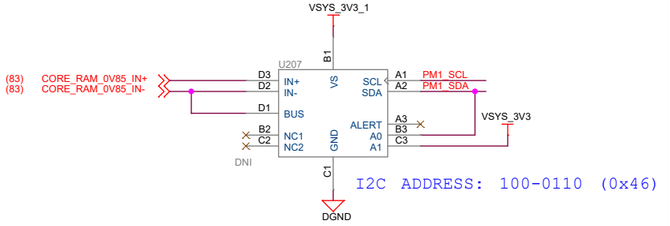
I2C ADDRESS: 100-0011 (0x43)



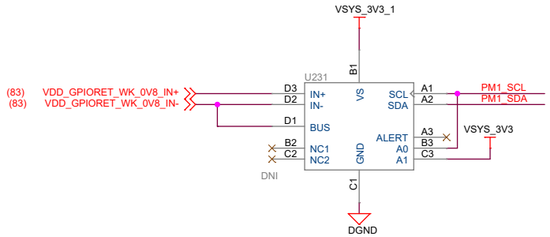
I2C ADDRESS: 100-0100 (0x44)



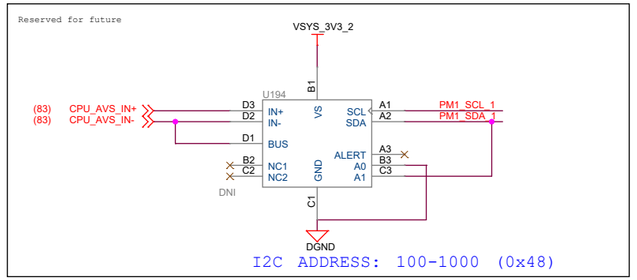
I2C ADDRESS: 100-0101 (0x45)



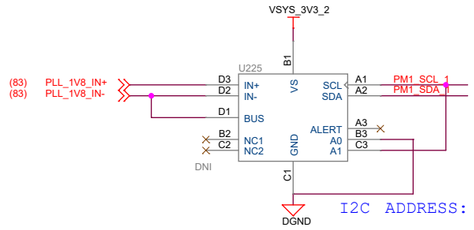
I2C ADDRESS: 100-0110 (0x46)



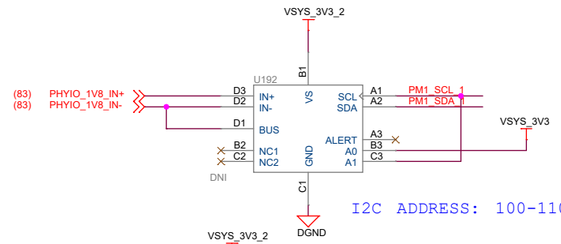
I2C ADDRESS: 100-0111 (0x47)



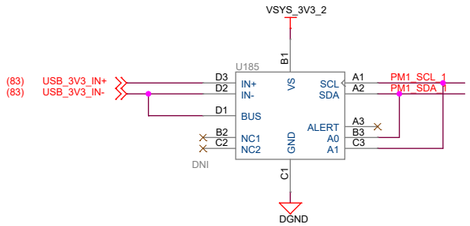
I2C ADDRESS: 100-1000 (0x48)



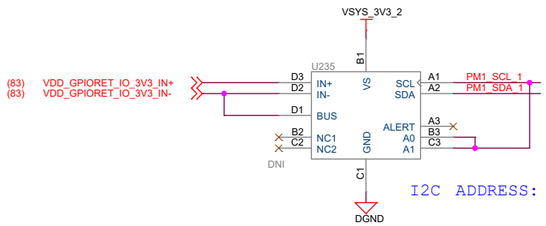
I2C ADDRESS: 100-1100 (0x4C)



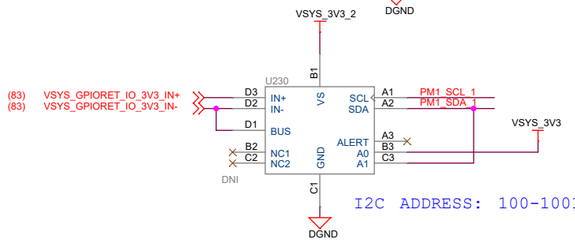
I2C ADDRESS: 100-1101 (0x4D)



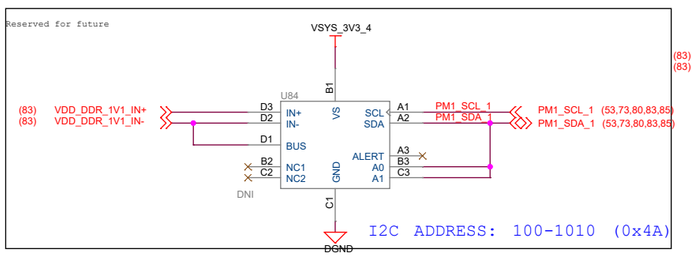
I2C ADDRESS: 100-1110 (0x4E)



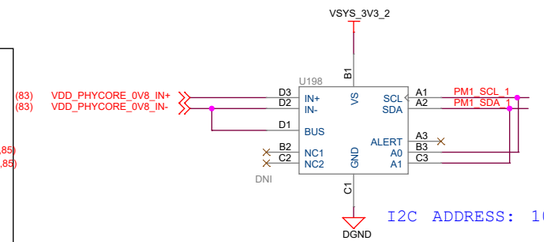
I2C ADDRESS: 100-1111 (0x4F)



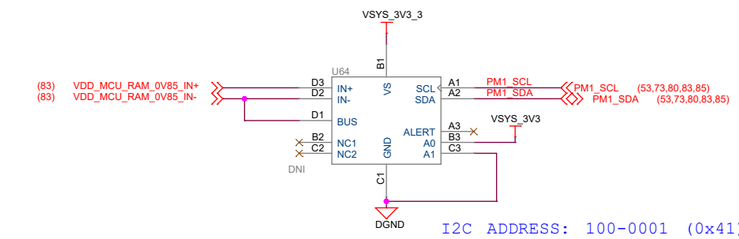
I2C ADDRESS: 100-1001 (0x49)



I2C ADDRESS: 100-1010 (0x4A)



I2C ADDRESS: 100-1011 (0x4B)

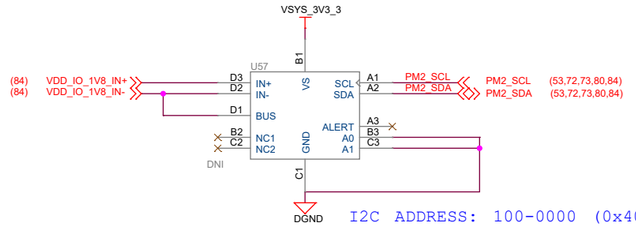


I2C ADDRESS: 100-0001 (0x41)

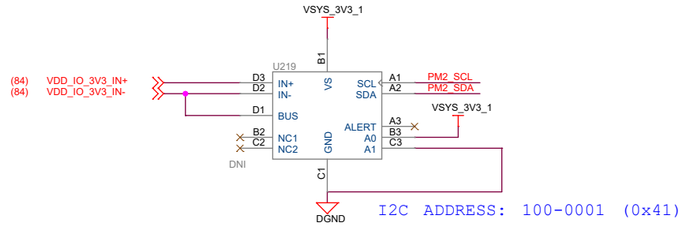
Project : J7 EVM	Title: CURRENT MONITORS#1- INA231
TEXAS INSTRUMENTS	Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
	Date: Friday, May 05, 2023 — Sheet 85 of 88

Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

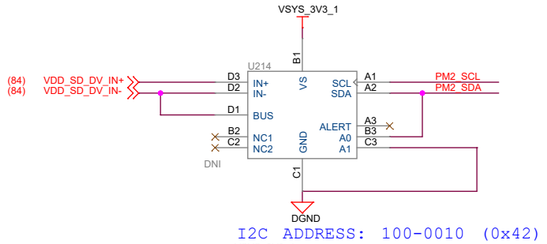
CURRENT MONITORS - INA231



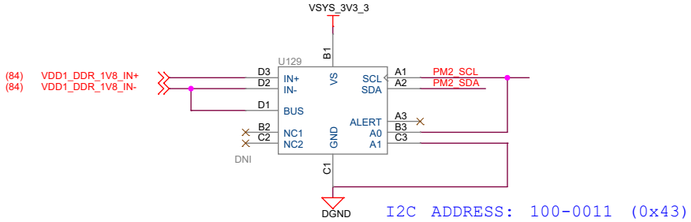
I2C ADDRESS: 100-0000 (0x40)



I2C ADDRESS: 100-0001 (0x41)

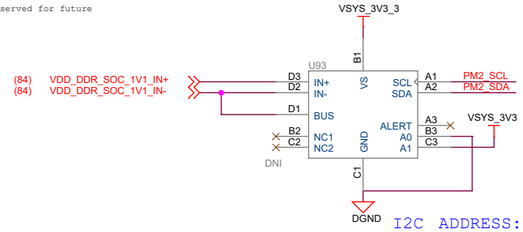


I2C ADDRESS: 100-0010 (0x42)

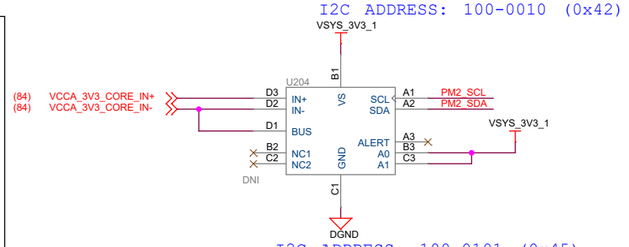


I2C ADDRESS: 100-0011 (0x43)

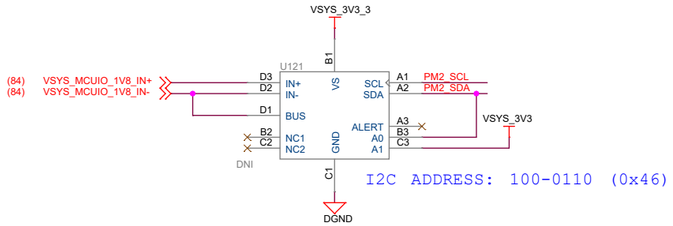
Reserved for future



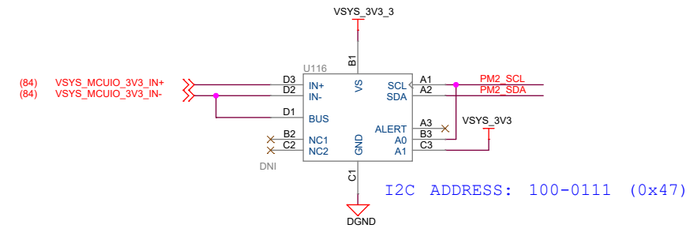
I2C ADDRESS: 100-0100 (0x44)



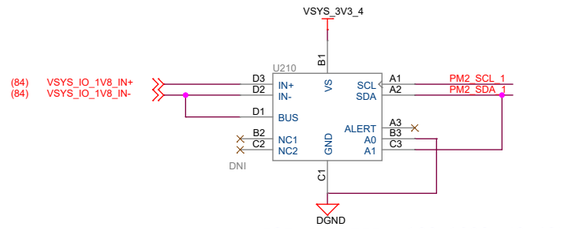
I2C ADDRESS: 100-0101 (0x45)



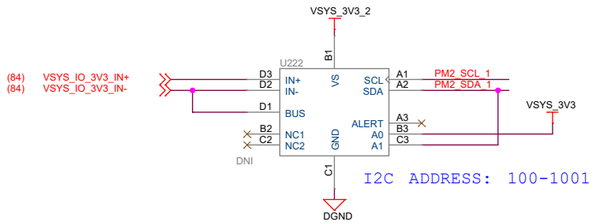
I2C ADDRESS: 100-0110 (0x46)



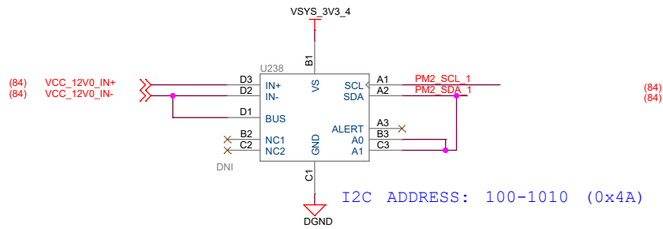
I2C ADDRESS: 100-0111 (0x47)



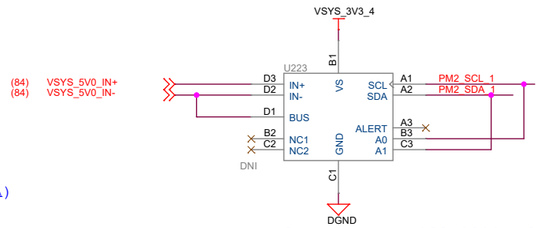
I2C ADDRESS: 100-1000 (0x48)



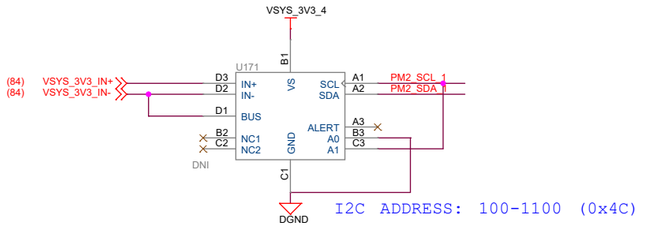
I2C ADDRESS: 100-1001 (0x49)



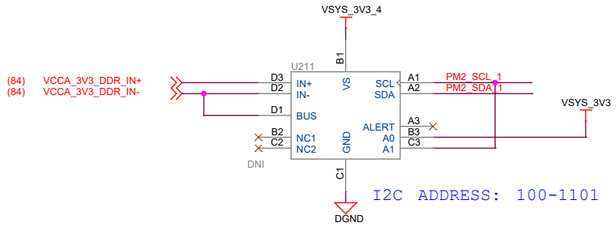
I2C ADDRESS: 100-1010 (0x4A)



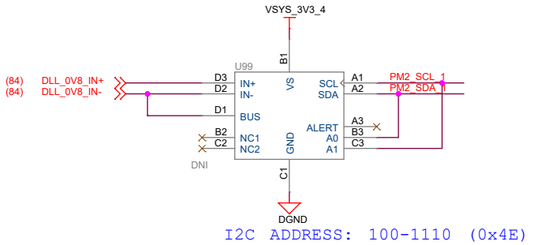
I2C ADDRESS: 100-1011 (0x4B)



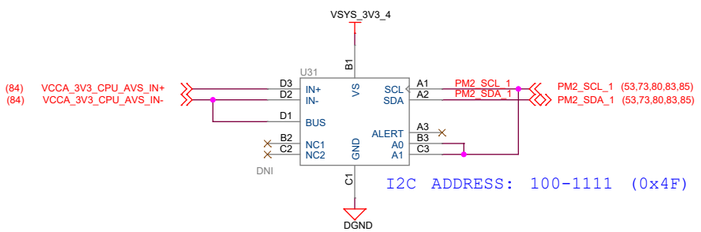
I2C ADDRESS: 100-1100 (0x4C)



I2C ADDRESS: 100-1101 (0x4D)



I2C ADDRESS: 100-1110 (0x4E)

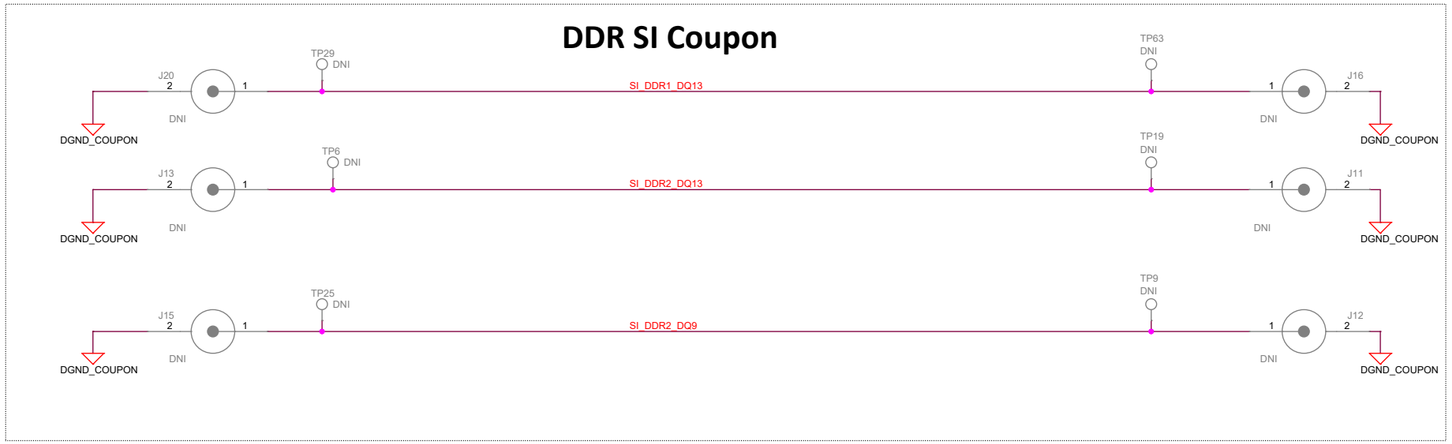


I2C ADDRESS: 100-1111 (0x4F)

Project : J7 EVM	TEXAS INSTRUMENTS	Title: CURRENT MONITORS#2- INA231
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 86 of 88

SI_SIMULATION_COUPON_BD

Test coupon not part of EVM design, to be used for TI test only



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SI_SIMULATION_ COUPON_BD
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 87 of 88

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

STANDOFFs

MH2	MH3	MH4	MH5	MH6	MH7	MH8	MH9
970300321	970300321	970300321	970300321	970300321	970300321	970300321	970300321

MH18	MH19	MH20	MH21	MH22	MH23	MH24	MH33
R30-4000502	R30-4000502	R30-4000502	R30-4000502	R30-4000502	R30-4000502	R30-4000502	R30-4000502

MH25	MH26	MH27	MH28	MH29	MH30	MH31	MH32
971150321	971150321	971150321	971150321	971150321	971150321	971150321	971150321

SCREWS

MH10	MH11	MH12	MH13
RM3X8MM 2701	RM3X8MM 2701	RM3X8MM 2701	RM3X8MM 2701

MH14	MH15	MH16	MH17
RM3X8MM 2701	RM3X8MM 2701	RM3X8MM 2701	RM3X8MM 2701

RUBBER FEET

M1	M2	M3	M4
728	728	728	728

M5	M6	M7	M8
728	728	728	728

SCREW FOR FAN ASSEMBLY

MH34	MH35	MH36	MH37
90116A165	90116A165	90116A165	90116A165

FIDUCIALS

FID1	FID2	FID3
FID_40X80	FID_40X80	FID_40X80

FID4	FID5	FID6
FID_40X80	FID_40X80	FID_40X80

BARE PCB

PCB1

PROC141E4

LOGOs

PCB LOGO	PCB LOGO	PCB LOGO	PCB LOGO
Texas Intruments	For Evaluation only; not FCC approved for resale	WEEE Mark	CE Mark
Texas Intruments	**For Evaluation only; not FCC approved for resale**	**WEEE Mark**	**CE Mark**

LABELS

Board Serial No.

LBL1 — PCB LABEL

AM6-COMPROCEVM

Assembly Revision.

LBL3 — PCB LABEL

AM6-COMPROCEVM

EVM Orderable No.

LBL2 — PCB LABEL

AM6-COMPROCEVM

Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J784S4XG01EVM
002:Soldered HS SoC	J784S4XH01EVM
003:Socketed SoC	J784S4XS01EVM

SOCKET

ACC1

DNI

HEAT SINK

ACC2

374724B00035G

PROCESSOR

ACC3

DNI

FAN

ACC4

CFM-4010V-185-314

CRIMP PIN

ACC5	ACC6
1735801-1	1735801-1

CONN HOUSING

ACC7

440129-3

Project : J7 EVM	TEXAS INSTRUMENTS	Title: HARDWARE SCHEMATICS
		Size: C — PROC141 001 J784S4XG01EVM — Rev: E4
		Date: Friday, May 05, 2023 — Sheet 88 of 88