

Convergence with PSpice® for TI

11/29/2021

Advanced Topic – Convergence Failures

Common Causes of Convergence Failures with PSpice for TI:

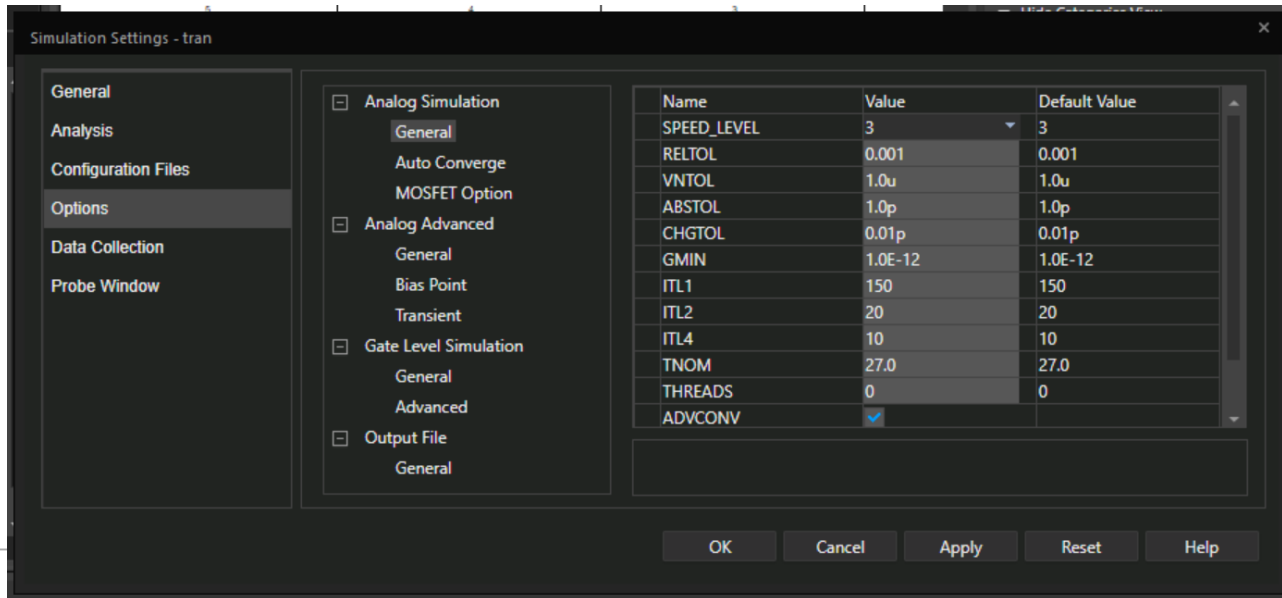
1. Lack of limitations
2. Rapid voltage transitions
3. Model discontinuities
4. ABM expression singularities
5. Large floating capacitors or small resistors

View the following slides for potential solutions. No solution is guaranteed to fix a convergence failure.

Advanced Topic – Convergence Settings

Some settings can be changed to aid the simulator with convergence

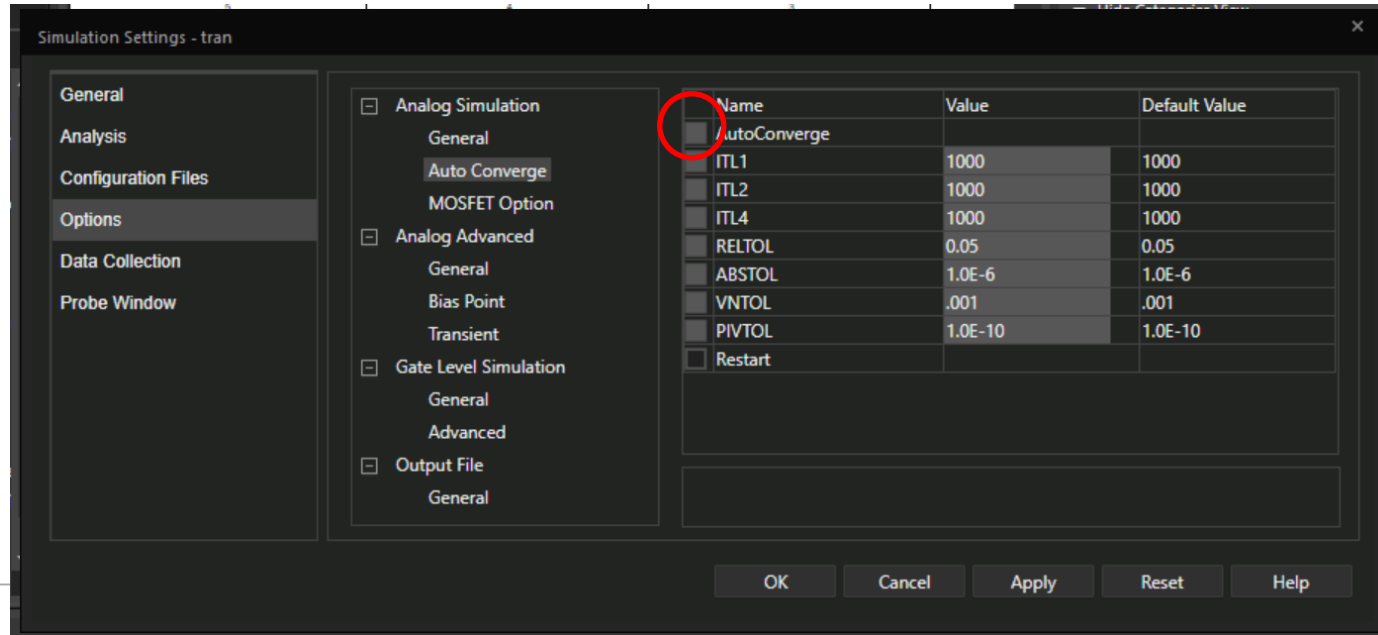
- Reducing GMIN (to 1.0E-14 for example)
- Increasing ITL4 (to 40 for example)
- Increasing VNTOL or ABSTOL by one or two orders of magnitude



*Please note that this could result in a reduction of accuracy. Proceed with caution.

Advanced Topic – Autoconvergence

- You can enable autoconvergence in the simulation profile. It is disabled by default.
- This will automatically relax tolerances to help find a solution.
- This could result in a reduction of accuracy. Proceed with caution.



Advanced Topic – Autoconvergence (continued)

- When enabled, autoconvergence will only be used when the simulator encounters a convergence failure and cannot recover. Otherwise the simulator will run as normal.
- If needed, autoconvergence will gradually loosen the tolerances until convergence can be achieved.
- If the tolerances are loosened to the Autoconvergence settings and convergence still is not achieved, then the simulator will stop and report the failure.
- See comparison of regular settings and autoconvergence settings below.

<input type="checkbox"/> Analog Simulation	
<input type="checkbox"/> General	
Auto Converge	
MOSFET Option	
<input type="checkbox"/> Analog Advanced	
<input type="checkbox"/> General	
Bias Point	
Transient	
<input type="checkbox"/> Gate Level Simulation	
<input type="checkbox"/> General	
Advanced	
<input type="checkbox"/> Output File	
<input type="checkbox"/> General	

Name	Value	Default Value
SPEED_LEVEL	3	3
RELTOL	0.001	0.001
VNTOL	1.0u	1.0u
ABSTOL	1.0p	1.0p
CHGTOL	0.01p	0.01p
GMIN	1.0E-12	1.0E-12
ITL1	150	150
ITL2	20	20
ITL4	10	10
TNOM	27.0	27.0
THREADS	0	0
ADVCONV	<input checked="" type="checkbox"/>	

<input type="checkbox"/> Analog Simulation	
<input type="checkbox"/> General	
Auto Converge	
MOSFET Option	
<input type="checkbox"/> Analog Advanced	
<input type="checkbox"/> General	
Bias Point	
Transient	
<input type="checkbox"/> Gate Level Simulation	
<input type="checkbox"/> General	
Advanced	
<input type="checkbox"/> Output File	
<input type="checkbox"/> General	

Name	Value	Default Value
AutoConverge		
ITL1	1000	1000
ITL2	1000	1000
ITL4	1000	1000
RELTOL	0.05	0.05
ABSTOL	1.0E-6	1.0E-6
VNTOL	.001	.001
PIVTOL	1.0E-10	1.0E-10
Restart		

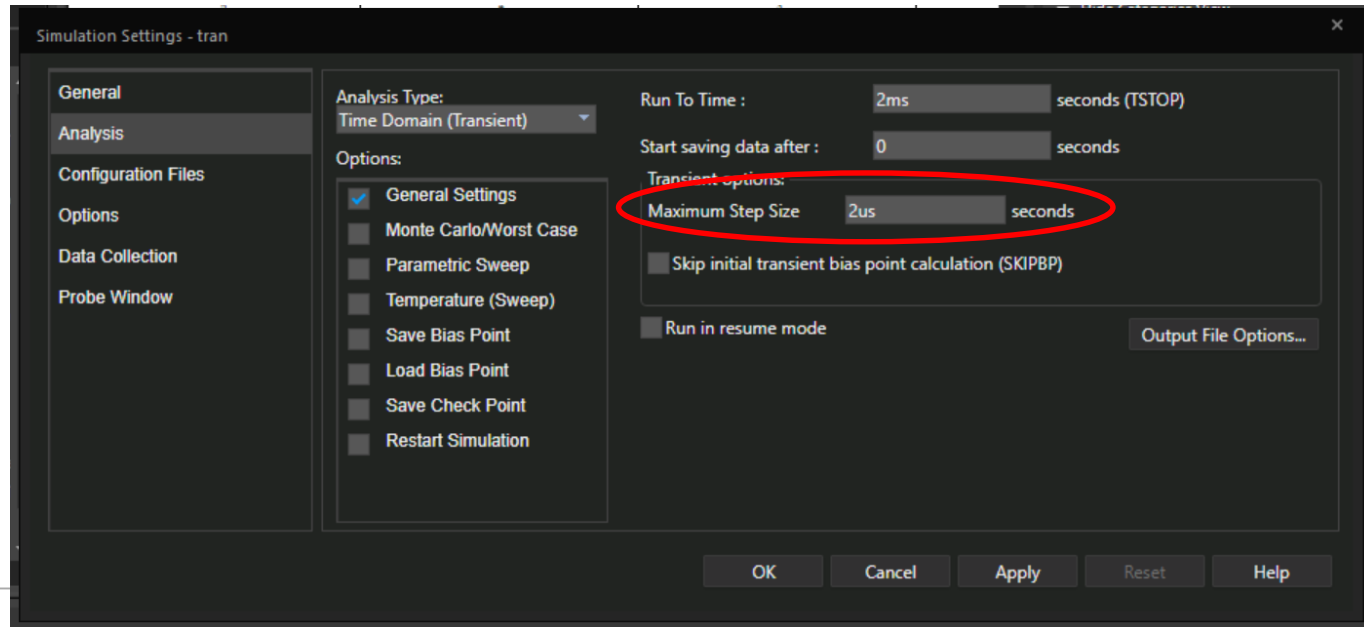
Advanced Topic – Discontinuities in Design

- It is possible that discontinuities or rapid changes are in the model itself. No amount of tweaks to the simulator can fix this. Please confirm that your model does not have significant discontinuities.
- One common cause of this problem are ideal voltage or current sources (or other ideal components). Increasing the rise and fall times of the sources will aid the simulator.

Reference	
Source Library	C:\CADENCE\PSPICETI
Source Package	VPULSE
Source Part	VPULSE.Normal
TD	
TF	
TR	
V1	
V2	
Value	VPULSE

Advanced Topic – Step Size

- For long simulations, convergence failures could be caused by large step sizes.
- You can limit the step size in the simulation profile. This will aid the simulator.
- Please note this may cause the simulation to run slower unnecessarily.



Advanced Topic – Pseudotransient Convergence Failure

- Full error: INFO(ORPSIM-16594): To improve Pseudotransient Convergence and Performance set following options to relax stabilization criteria for capacitor currents and inductor voltages: PTRANABSTOL=1e-5, PTRANVNTOL=1e-4
- Add the following text to the canvas:

@PSpice: .options PTRANABSTOL=1e-5 PTRANVNTOL=1e-4

- This could result in a reduction of accuracy. Proceed with caution.
- See further information in [the FAQ here](#)