TONSEL:On-time adjustment pin.
365 kHz/460 kHz setting: connect to VREG5
300 kHz/375 kHz setting: connect to VREG3

VREG5 R523 0/4 W10_TONSEL

SKIPSEL
OOA auto skip : Connect to VREG3
PWM only: Connect to VREF
Auto skip: Connect to GND

VREG3 R524 0/4 W10_SKIPSEL

ENC
VREG3 : Enable Channel 1 and Channel 2.
GND : Disable all circuit

VREG3 R533 4.7K/4 W10_ENC
C451 0.1U/25V/X5R/4

EN0
Open : LDOs on.
GND : Disable all circuit.

R542 0/4/X 3V5VEN0

TPS51123A_AGND TPS51123A_AGND W10_TONSEL
R525 20K/4/1 R526 20K/4/1
VREF_TPS51123A
W10_TPS51123A_VFB2 R528 13K/4/1 W10_FBVI2
C447 1U/25V/X5R/4
W10_FBVI1 R529 30.9K/4/1 W10_TPS51123A_VFB1
3VSB_OCP=12.2A
R531 68K/4/1 3V5VTRP2
5VSB_OCP=20.4A
R532 63.4K/4/1 5V5VTRP1

U40 TPS51123A
Internal soft start 1.6ms

V3P3A_OCP	7	VO2	TRIP2	VFB2	TONSEL	VREF	VFB1	TRIP1	TH-Pad	25	VO1	24	V5A_OCP
<175mA													R534 100K/4 V3P3A
VREG3	8	VREG3									PGOOD	23	W10_3VSB & 5VSB_PGOOD
C453 10U/25V/X5R/8													Power Good delay +/-5% 510us
W30_V3P3A_BOOT	9	VBST2									VBST1	22	W30_V5A_BOOT
W30_V3P3A_UGATE	10	DRVH2									DRVH1	21	W30_V5A_UGATE
W30_V3P3A_SW	11	LL2									LL1	20	W30_V5A_SW
W30_V3P3A_LGATE	12	DRVL2	EN0	SKIPSEL	GND	VIN	VREG5	ENC			DRVL1	19	W30_V5A_LGATE
			13	14	15	16	17	18					

TPS51123A/PQFN-24

W10_ENC
W10_SKIPSEL
TPS51123A_Vin C462 10U/25V/X5R/8
VREG5 C463 10U/25V/X5R/8
<175mA
R544 0/6 TPS51123A_AGND

V12A L18 0.47uH/17.5A TPS51123A_Vin

TPS51123A_Vin Q55
R614 2.2/6 C530 0.22u/16V/X5R/4 CSD87352Q5D/SON-8
W30_V3P3A_BOOT W30_V3P3A_BOOTR R616 10K/4
W30_V3P3A_UGATE R615 0/6
W30_V3P3A_SW W30_V3P3A_UGATER
W30_V3P3A_LGATE
C525 C526 C522 C523 C524 0.1U/25V/X5R/4 10U/25V/X5R/8
GND
DCR=4mR
Idc=17.5A
Isat=26A
Overlay
L26 0.47uH/17.5A
L3 0.47uH/4.5A
V3P3A_SWL
V3P3A_OCP V3P3A
R889 0/1206
SP1 Short/X
W10_TPS51123A_VFB2
R617 2.2/6
W30_V3P3A_SNUBBER
C529 4700P/50V/X7R/4
C528 10U/6.3V/X5R/6
EC22
as small as possible

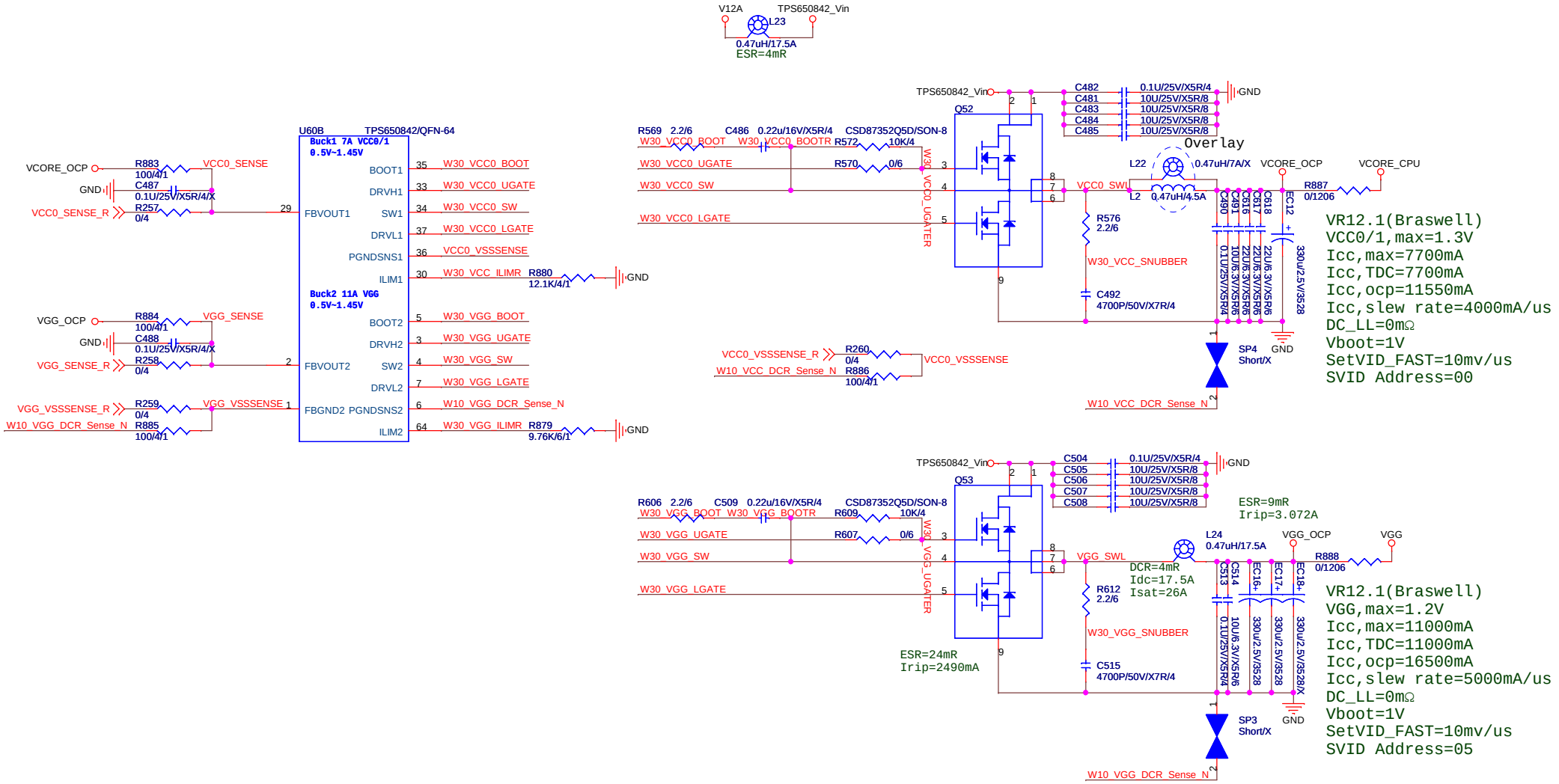
TPS51123A_Vin Q54
R608 2.2/6 C521 0.22u/16V/X5R/4 CSD87352Q5D/SON-8
W30_V5A_BOOT W30_V5A_BOOTR R611 10K/4
W30_V5A_UGATE R610 0/6
W30_V5A_SW W30_V5A_UGATER
W30_V5A_LGATE
C516 C517 C510 C511 C512 0.1U/25V/X5R/4 10U/25V/X5R/8
GND
as small as possible
L25 0.47uH/17.5A
V5A_SWL
V5A_OCP V5A
R890 0/1206
SP2 Short/X
W10_TPS51123A_VFB1
R613 2.2/6
W30_V5A_SNUBBER
C520 4700P/50V/X7R/4
C518 10U/6.3V/X5R/6
EC19
ESR=14mR
Irip=4950mA

D32 BAV99/SOT-23
TPS51123A_Vin V24A C464 0.1U/25V/X5R/4 W30_V5A_SW
C465 10U/25V/X5R/8 C466 4.7u/50V/X5R/8
V24A R547 2K/4 V18A
R548 10K/4 C467 0.1U/25V/X5R/4

J8 DC JACK D19
12V_JD FS2 PS3A/15V/SMD
V12A C282 0.1U/25V/X5R/4 P6SMBJ12CA/SMB
C283 22U/16V/X5R/1206 C284 22U/16V/X5R/1206 C285 22U/16V/X5R/1206

V5A R557 10K/4 PS_ON
Q73A Q73B
PS_ON# UM6K1N/SOT363-6
V18A R553 10K/4 C473 0.1U/25V/X5R/4
V12A Q45 AP2306AGN/SOT23-3 EN_V12S
V12S R551 10K/4 VSENABLE
C471 10U/25V/X5R/8 C469 0.1U/25V/X5R/4
V5A Q43 FDMS7694/MSL1-8
V5S C468 22U/6.3V/X5R/6
R558 0/4 VSS_PWRGD
R560 10K/4 C475 1000P/50V/X7R/4
V5A R555 10K/4 V5SEN#
V12S R556 10K/4 V3SENABLE
Q74A Q74B UM6K1N/SOT363-6
C474 0.1U/25V/X5R/4
V3P3A Q47 FDMS7694/MSL1-8
V3P3S C472 22U/6.3V/X5R/6
R550 100/4/1 V3SPWR
C470 1000P/50V/X7R/4
U49 FP6809/SOT23-3 RESET# VCC GND
R545 2.2K/4
R351 0/4 ATX_PWROK
V3SPWRGD

+V3P3S PWRGD



Ganlot Inc.		
Page	PMIC VCC/VGG	
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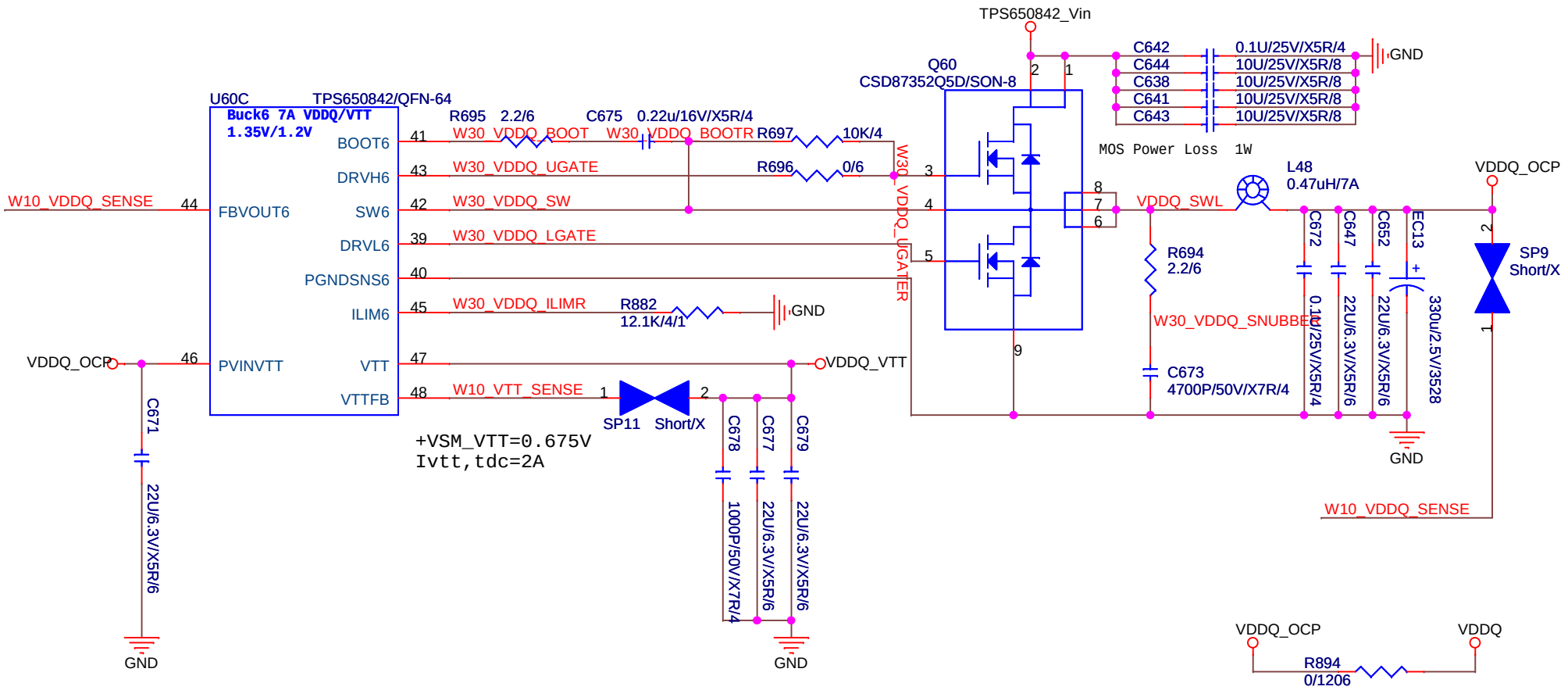

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Page: PMIC VDDQ & VDDQ_VTT		
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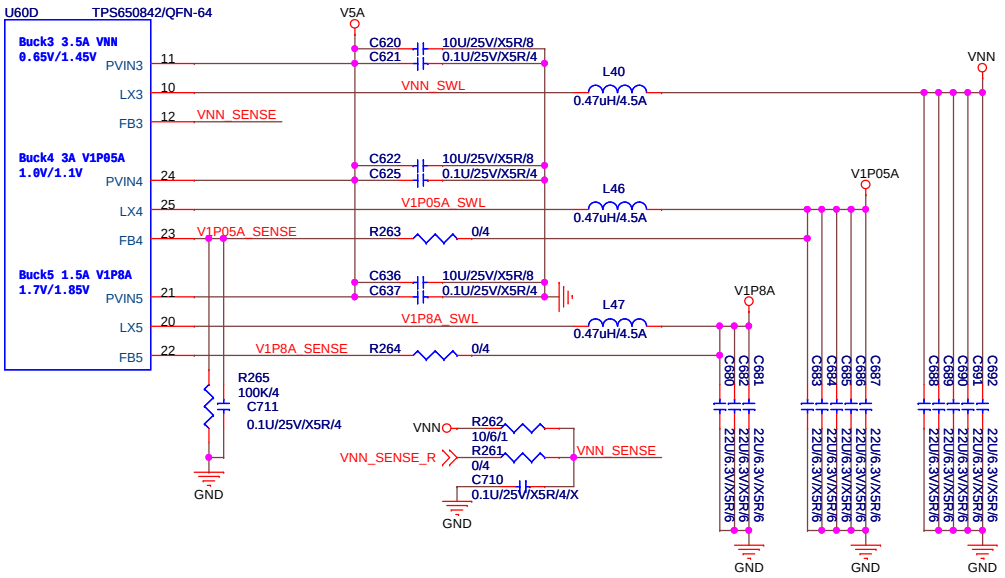

Power Rail (SoC)	N3000 (TDP-4W) (SDP-3W) (DC) (S0-Imax) (mA)	N3050 (TDP-6W) (SDP-4W) (DC) (S0 Imax) (mA)	N3700 (TDP-6W)(SDP-4W) (QC) (S0 Imax), (mA)	N3150 (TDP-6W) (SDP-4W) (QC) (Imax, mA)	S3 Imax (mA)	S4 Imax (mA)	S5 Imax (mA)
VCC0+VCC1 (merged)	3600	3600	7700	7700	0	0	0
VGG	11000	11000	11000	11000	0	0	0
VNN	3500	3500	3500	3500	175	175	175
V1P05A	1900	2000	2000	2000	15	15	15
V1P15S	500	500	500	500	0	0	0
V1P24A	500	500	500	500	5	5	5
V1P5S or V1P8S	20	20	20	20	1	0	0
V1P8A	550	550	550	550	5	5	5
V3P3A_PRIME	200	200	200	200	1	1	1
LPC IO (3.3V)	148	148	148	148	1	1	1
VSDIO (3.3V)	141	141	141	141	1	0	0
VSDIO (1.8V)	93	93	93	93	1	0	0
VDDQ (1.35V)	2400	2400	2400	2400	15	0	0
VCC_RTC	1	1	1	1	1	1	1

Notes:

1. VCC_RTC Iccmax in G3 state is 6uA. This current specification is valid at an ambient temperature of 25°C with 3V coin cell battery
2. The data in this table only represent peak or worst case conditions and does NOT represent sustained or average current requirements.
3. The data in this table should ONLY be used for power delivery or voltage regulator (VR) design. These numbers should only be used as guidance to enable appropriate power delivery or voltage regulator part selection and should not be used for Battery Life analysis

VNN,max=1.3V
Icc,max=3500mA
Icc,TDC=3500mA
Icc,ocp=5250mA
Icc,slew rate=500mA/us
DC_LL=0mΩ
Vboot=1V
SetVID_FAST=10mv/us
SVID Address=01

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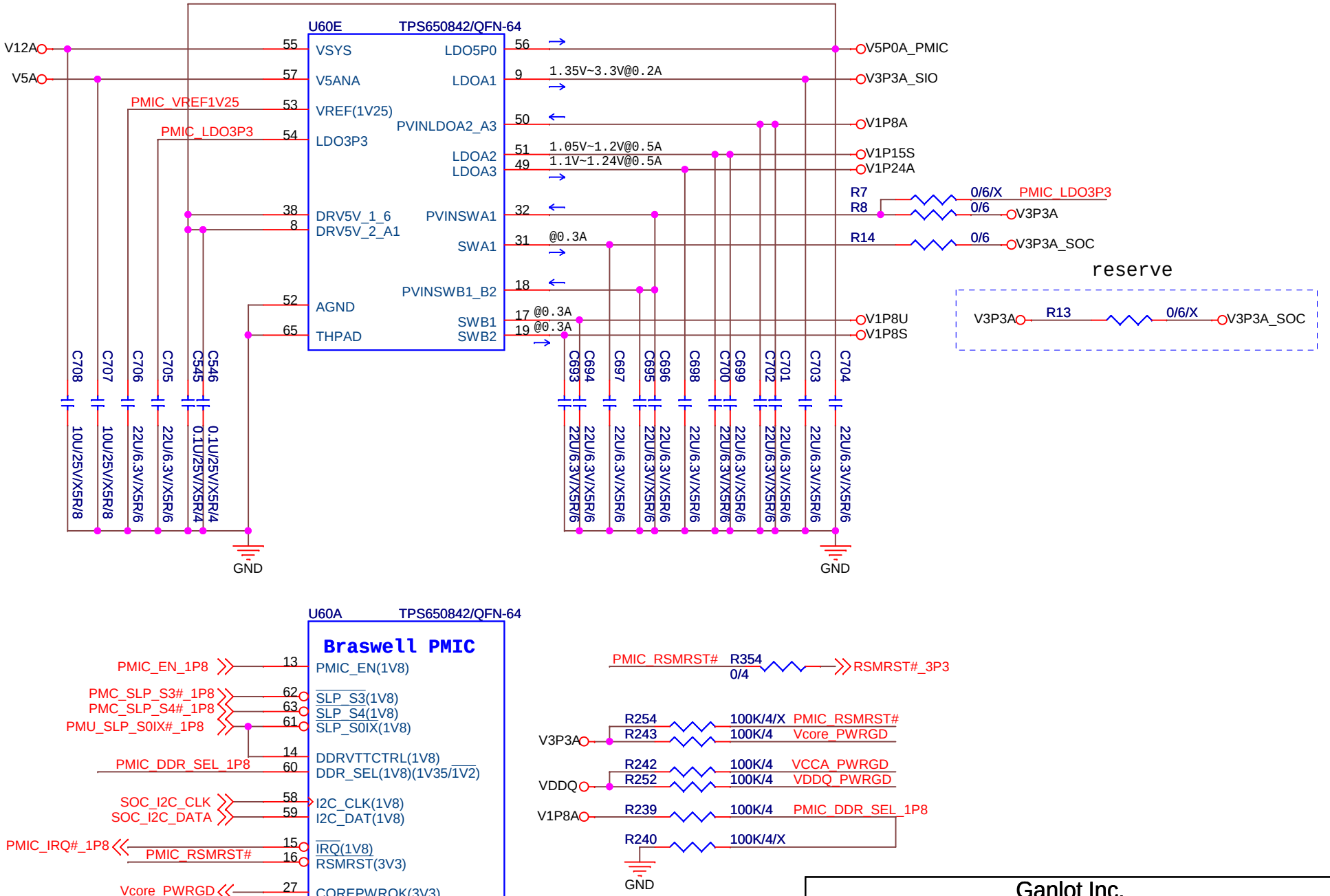

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