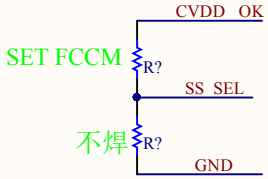
新选器件

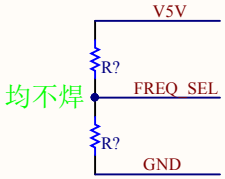
In Auto-skip Eco-mode, the LMZ31520 automatically reduces the switching frequency at light load conditions to maintain high efficiency. In FCCM, the controller keeps continuous conduction mode in light load condition and the switching frequency is kept almost constant over the entire load range. Transient performance is best in FCCM.

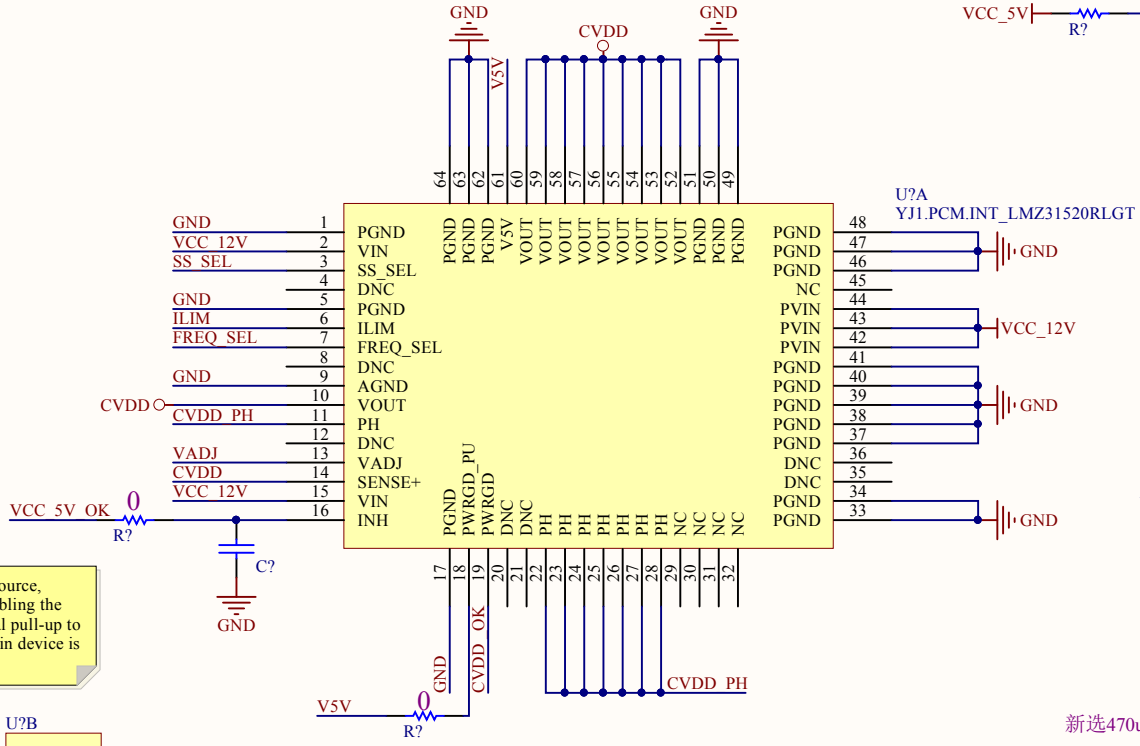
Table 3. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM32ER61E226K	25	22	2
TDK	X5R	C3216X5R1E476M	25	47	2
TDK	X5R	C3216X5R1C476M	16	47	2
Murata	X5R	GRM32ER61C476M	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Panasonic	EEH-ZA	EEH-ZA1E101XP	25	100	30
Kemet	T520	T520V107M010ASE025	10	100	25
Panasonic	POSCAP	6TPE100MI	6.3	100	25
Panasonic	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Panasonic	POSCAP	2TPF330M6	2.0	330	6
Panasonic	POSCAP	6TPE330MFL	6.3	330	15

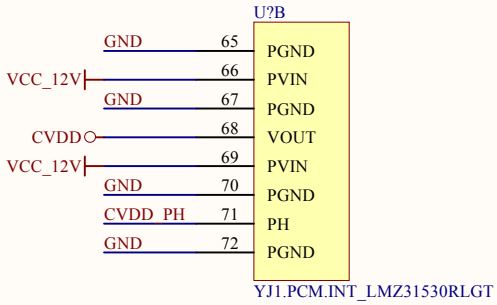
(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100kHz. 25°C.

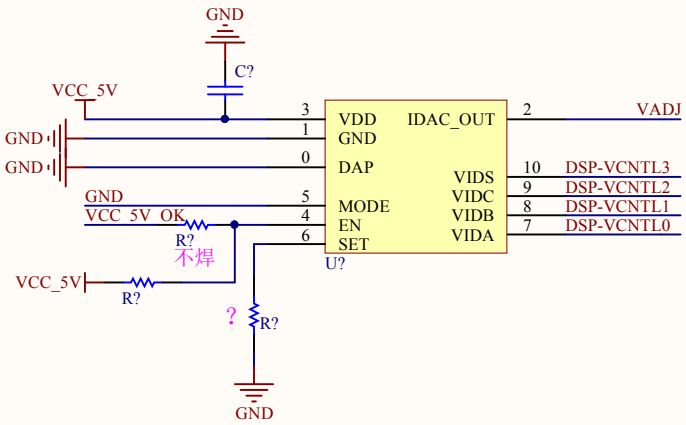


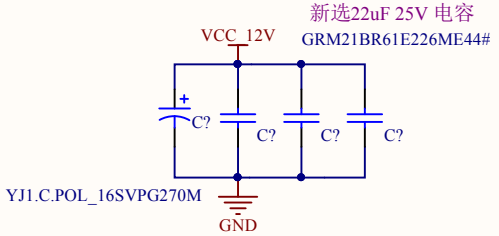


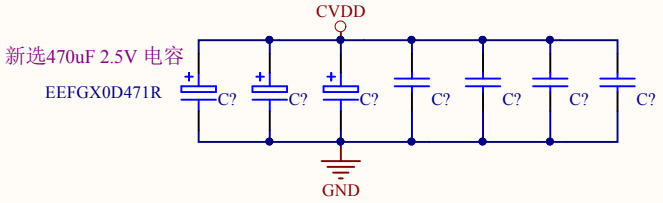


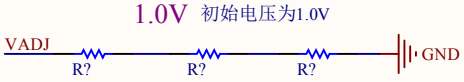
The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input











VOUT=1.0V RSET=2195欧

PWRGD_PU:Power Good pull-up pin. This pin is connected to a 100kΩ resistor which is tied to the PWRGD pin internally.Connect this pin to V5V or to any voltage between 1.3V and 6.5V

Title	UAPC3.0		
Design	陈龙3	Check 李 响	Approve 刘国伟
Size: A4		Number:	Revision:R1.0
Date: 2018/7/4		Time: 19:46:40	Sheet1 of N
File: E:\资料备份\项目资料\电力电子组工作\UAPC3.0硬件平台设计\UAPC3.0电路设计\电路设计-陈龙\PWRA_CVDD			

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