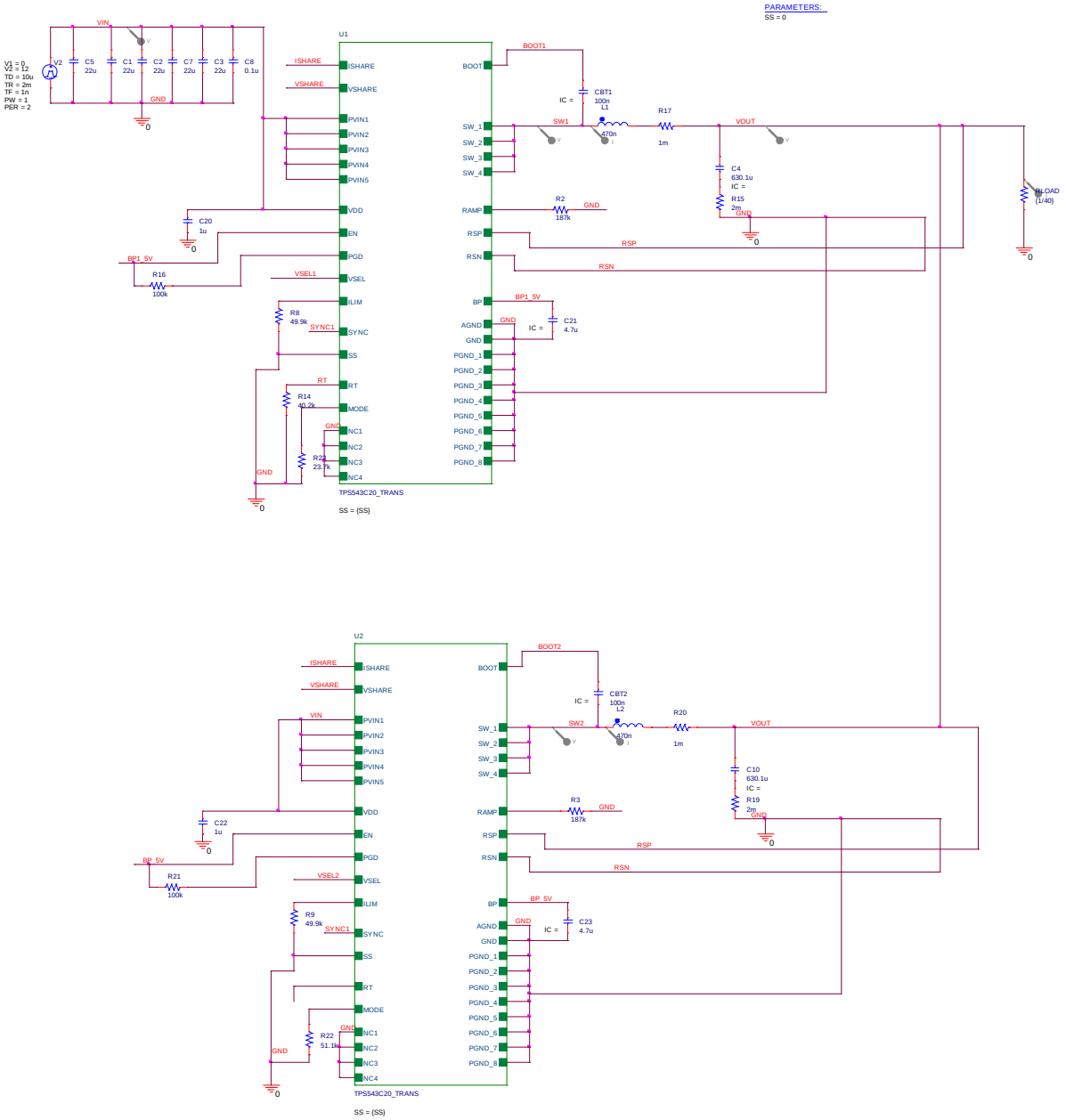
7. Validation of 2-ph operation

7.1 Start-up (VIN=12V VOUT=1V & ILOAD=40A)

PSPICE Schematic:



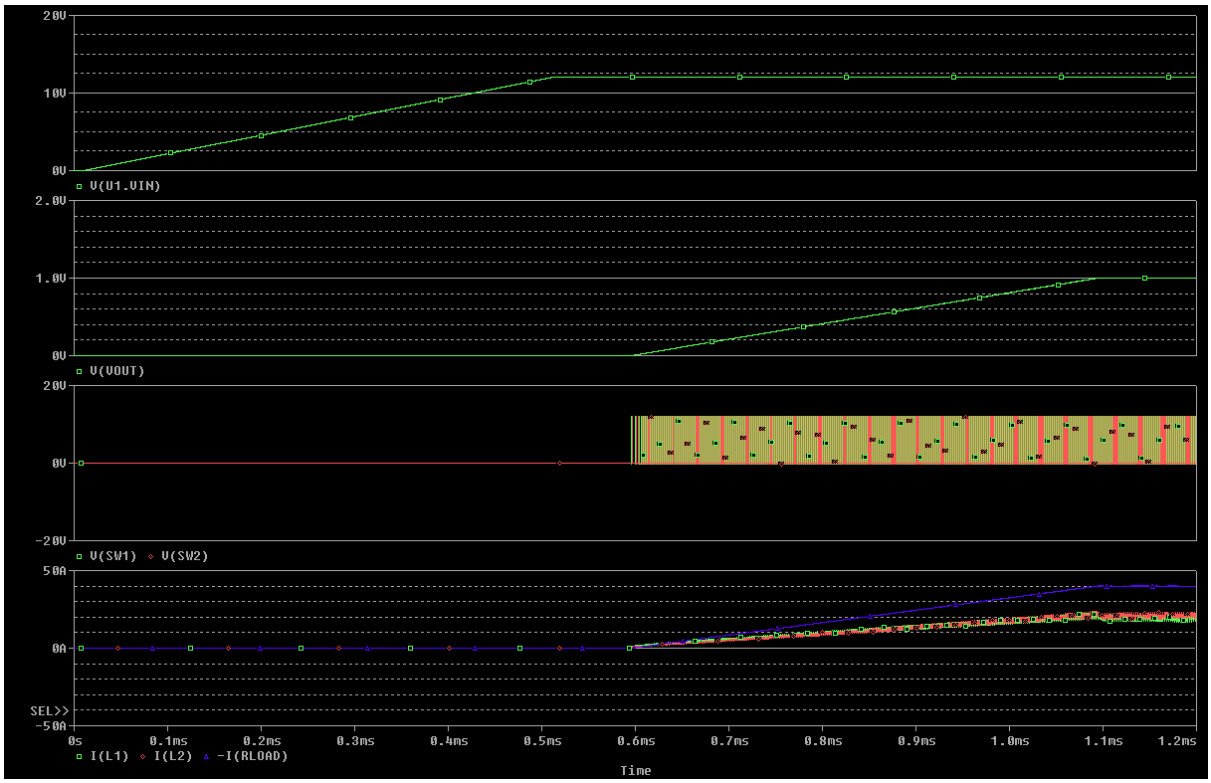
Description:

1. This test bench is configured to test 2 phase operation.
2. The slave operates at same frequency set by Master and RT of slave sets SYNC POINT.
3. For this test bench Master and slave operates at 500KHz and syncs at mid point.

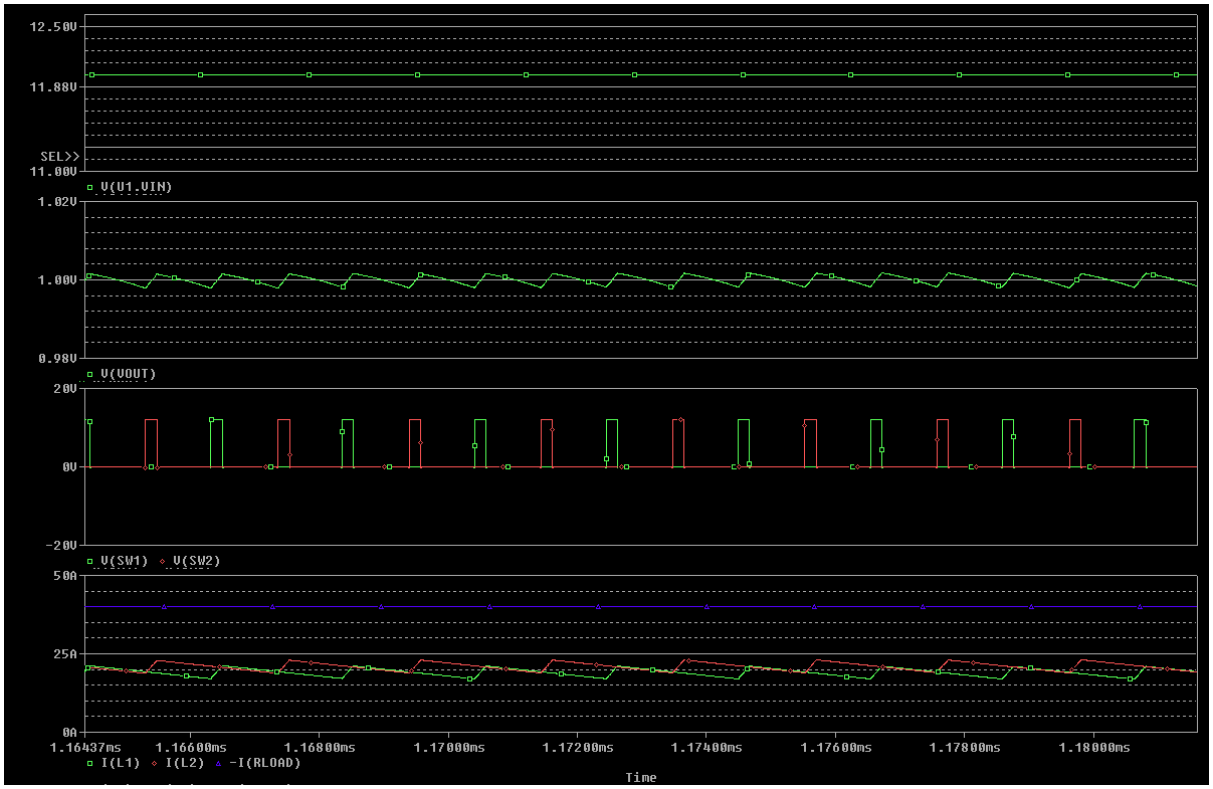
Test Conditions and Additional Analysis Options (if any):

4. ILOAD=40A
5. MODE=23.7K for master and 51.1k for Slave.
6. SS=GND (Soft start time of 0.5ms)
7. RAMP=187k for both Master and Slave device.
8. VSEL=Open Circuit
9. RT=40.2k and RT2=open for slave(SYNC at mid point)
10. L=470nH
11. Cout=630.1uF with ESR=2m

Simulation Results:



Zoomed Results:



Bench Results:

Tabulation of Results

PARAMETER	DATASHEET	Bench Data	PSPICE	UNIT
IL1(Inductor current in master)	-	20	19.13	A
IL1(Inductor current in Slave)	-	20	20.94	A
CURRENT SHARE ACCURACY ISHARE (acc) Output current sharing accuracy among stackable devices, defined as the ratio of the current difference between devices to total current.	+-15	~1	4.525	%

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