Power Tips #98: Designing a DCM flyback converter
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Many low-power and low-current applications use a discontinuous-conduction-mode (DCM) flyback converter. DCM operation is characterized by the rectifier current decreasing to zero before the start of the next switching cycle. This benefits the field-effect transistor (FET) and rectifier losses, and often reduces the transformer size.

By comparison, continuous-conduction-mode (CCM) operation maintains rectifier current conduction through the end of the switching period. CCM operation is best suited for medium- to high-power applications. For flyback design trade-offs and power-stage equations for a CCM flyback, see "Power Tips #76: Flyback converter design considerations" and "Power Tips #77: Designing a CCM flyback converter." But if you have a low-power application for a DCM flyback, read on. This article provides equations and a step-by-step methodology to guide you through the design process.

Figure 1 shows a simplified flyback schematic, while Figure 2 details the key component switching waveforms of DCM operation. Operation starts when FET Q1 turns on for duty cycle D. The current in the primary winding of T1, which always starts at zero, reaches a peak set by the primary winding inductance, input voltage and on-time t1. During this FET on-time, diode D1 is reverse-biased because of T1's secondary winding polarity, forcing all output current to be supplied by output capacitor COUT during times t1 and t3.

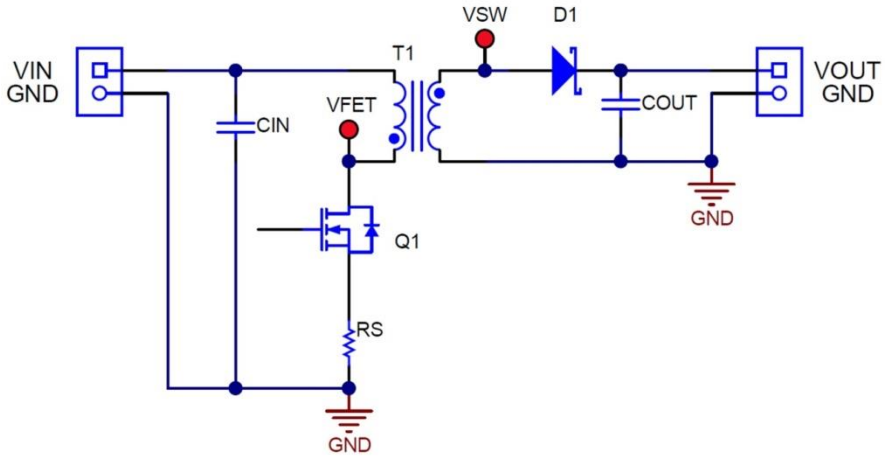

Figure 1: This simplified flyback converter can operate in either DCM or CCM.

When Q1 turns off during period 1-D, T1's secondary voltage polarity reverses, which allows D1 to conduct current to the load and recharge COUT. Current in D1 decreases linearly from its peak to zero during time t2. Once T1's stored energy is depleted, only residual ringing occurs during the remainder of period t3. This ringing is primarily due to T1 magnetizing inductance and Q1, D1 and T1 parasitic capacitances. This is easily seen in Q1's drain voltage during t3, which drops from VIN plus the reflected output voltage back to VIN, since T1 cannot support a voltage once current flow stops. Currents in CIN and COUT are identical to Q1 and D1, but without a DC offset.

Shaded areas A and B highlight the volt-microsecond products of the transformer during t1 and t2 that must be in balance to prevent saturation. Referenced to the secondary side, "A" represents (Vin/Nps) × t1. "B" represents (Vout + Vd) × t2, where Np/Ns is the transformer primary-to-secondary turns ratio.

Without an adequate dead time for t3, CCM operation may occur. While transitioning between DCM and CCM is acceptable, this article evaluates only DCM operation.

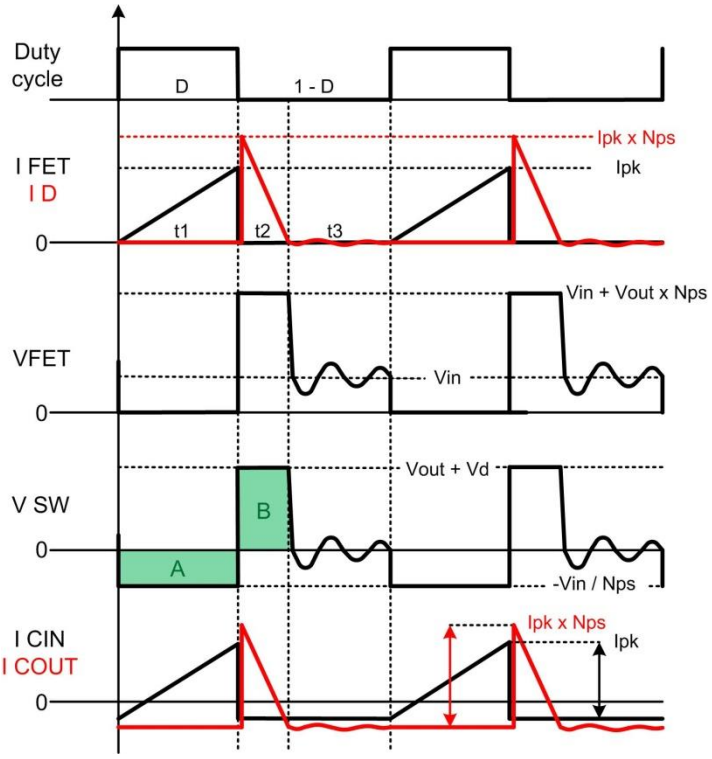

Figure 2: The key voltage and current switching waveforms for a DCM flyback.

Table 1 details characteristics of DCM operation relative to CCM. One key DCM attribute is that a lower primary inductance decreases the duty cycle regardless of the transformer's turns ratio. This attribute lets you set a particular maximum duty cycle, which may enable controller choices. This can be important if you are trying to use a specific controller or stay within certain on or off time limits. A lower inductance, which requires a lower average energy storage (albeit with a higher peak FET current) often results in a smaller transformer than CCM. Another DCM advantage is that it eliminates D1 reverse-recovery losses in standard rectifiers, since the current is zero at the end of t2. Reverse-recovery losses often appear as increased dissipation in Q1. The benefit of this becomes increasingly important at higher output voltages, where the reverse-recovery times of rectifiers increase with higher-voltage-rated diodes.

DCM advantages	**DCM disadvantages**
Lower primary inductance than CCM	Higher peak primary current
Inductance sets the maximum duty cycle	Higher peak rectifier current
Smaller transformer possible	Increased input capacitance
No rectifier reverse-recovery losses	Increased output capacitance
No (or minimal) FET turn-on losses	Potentially increased electromagnetic interference
No right half-plane zero in the control loop	Wider duty-cycle operation than CCM
Optimal for low output power	Increased bandwidth variation

Table 1: The smaller inductance of a low-power DCM flyback can allow a smaller transformer.

Several parameters are required when starting a design, along with the basic electrical specification. Start by selecting a switching frequency, a maximum operating duty cycle and an estimated efficiency. Equation 1 calculates time t1:

$$t1 = \frac{Dmax}{fsw} \qquad (1)$$

where Dmax is the desired maximum duty cycle.

Estimate the transformer's peak primary current, Ipk. For the FET's on voltage, Vds_on, and the current-sense resistor voltage, VRS, in Equation 2, assume small voltage drops that are appropriate for your design, like 0.5 V. You can update these voltage drops later.

$$Ipk = \frac{Pout_{max} \times (\frac{2}{Dmax})}{(Vin_{min} - Vds\_on - VRS) \times \eta} \qquad (2)$$

Equation 3 calculates the required transformer turns ratio, Np/Ns, based on equating areas A and B in Figure 2:

$$\frac{Np}{Ns} = \frac{(Vin_{min} - Vds\_on - VRS) \times t1}{\left(\frac{1}{fsw} \times (1-x) - t1\right) \times (Vout + Vd)} \qquad (3)$$

where x is a desired minimum idle time f or t3 (starting with x = 0.2).

If you would like to change Np/Ns, adjust Dmax and iterate again. Calculate the maximum "flat-top" voltages for Q1 (Vds_max) and D1 (VPIV_max) using Equations 4 and 5:

$$Vds_{max} = Vin_{max} + (Vout + Vd) \times \frac{Np}{Ns} \qquad (4)$$

$$VPIV\_max = Vout + \frac{Vin\_max}{\frac{Np}{Ns}} \qquad (5)$$

Since these components generally have ringing due to transformer leakage inductance, a rule of thumb is to expect the values from Equations 4 and 5 to be 10%-30% higher. If Vds_max is higher than anticipated, reducing Dmax will lower it, but VPIV_max will increase. Determine which component voltage is more critical and iterate again if necessary.

Calculate t1_max using Equation 6, which should be close to that in Equation 1:

$$t1\_max = \frac{(Vout + Vd) \times \frac{Np}{Ns} \times \left(\frac{1}{fsw} \times (1-x)\right)}{Vin_{min} + (Vout + Vd) \times \frac{Np}{Ns}} \qquad (6)$$

Calculate the maximum required primary inductance with Equation 7:

$$Lpri\_max = \frac{Vin\_min^2 \times t1\_max^2 \times \eta \times fsw}{2 \times Vout \times Iout\_max} \qquad (7)$$

If you select a lower inductance than Equation 7, increase x and decrease Dmax until Np/Ns and Lpri_max are equal to your desired values by iterating as necessary.

You can now calculate Dmax in Equation 8:

$$\mathrm{Dmax} = \sqrt{\frac{2 \times \mathrm{fsw} \times \mathrm{Vout} \times \mathrm{Iout\_max} \times \mathrm{Lpri}}{\mathrm{Vin\_min}^2 \times \eta}} \qquad (8)$$

And calculate the maximum Ipk and its maximum root-mean-square (RMS) value using Equations 9 and 10, respectively:

$$\mathrm{Ipkmax} = \sqrt{\frac{2 \times \mathrm{Vout} \times \mathrm{Iout\_max}}{\mathrm{Lpri} \times \mathrm{fsw} \times \eta}} \qquad (9)$$

$$\mathrm{Ipkrms} = \mathrm{Ipkmax}\sqrt{\frac{\mathrm{Dmax}}{3}} \qquad (10)$$

Calculate the maximum current-sense resistor value allowed, based on the selected controller's current-sense input minimum current limit threshold, Vcs (Equation 11):

$$\mathrm{RSmax} = \frac{\mathrm{Vcs}}{\mathrm{Ipkmax}} \qquad (11)$$

Use the values calculated for Ipkmax in Equation 9 and RS to verify that the assumed voltage drops for the FET Vds and sense resistor VRS in Equation 2 are close; iterate again if significantly different.

Use Equations 12 and 13 to calculate the maximum power dissipated in RS and conduction losses in Q1 from Equation 10:

$$\mathrm{P\ Rsns} = \mathrm{Ipkrms}^2 \times \mathrm{RS} \qquad \text{(actual)} \qquad (12)$$

$$\mathrm{P\ FETcond} = \mathrm{Ipkrms}^2 \times \mathrm{Rdson} \qquad (13)$$

FET switching losses are generally highest at Vinmax, so it's best to calculate Q1 switching losses over the full range of Vin (Equation 14):

$$\mathrm{P\ FETsw} = 0.25 \times \left(\frac{\mathrm{Qdrv}}{\mathrm{Idrv}}\right) \times \mathrm{fsw} \times \mathrm{Ipk} \times \mathrm{Vds} \qquad (14)$$

where Qdrv is the FET total gate charge and Idrv is the expected peak gate-drive current.

Equations 15 and 16 calculate the total power loss from charging and discharging the FET's nonlinear Coss capacitance. The integrand in Equation 15 should closely match the actual FET's Coss data-sheet curve between 0 V and its actual operating Vds. Coss losses are generally greatest in high-voltage applications or when using very low $R_{DS(on)}$ FETs, which have larger Coss values.

$$\mathrm{Qtot} = \int_{-Vds}^{0} \left[\frac{\mathrm{Coss(0\ V)}}{(1-\mathrm{v})^{0.5}}\right] dv \qquad (15)$$

$$\text{P FETcoss} = \frac{\text{fsw} \times \text{Qtot} \times \text{Vds}}{2} \qquad (16)$$

Total FET losses can be approximated by summing Equation 13, Equation 14 and Equation 16.

Equation 17 reveals the diode losses simplify greatly. Be sure to select a diode rated for the secondary peak current, which is generally much greater than Iout.

$$\text{P Diode} = \frac{\text{Ipk} \times \frac{\text{Np}}{\text{Ns}} \times \text{t2} \times \text{fsw}}{2} \times \text{Vdiode} = \text{Iout} \times \text{Vdiode} \qquad (17)$$

Output capacitance is generally selected as the larger of Equations 18 or 19, which calculates capacitance based on ripple voltage and equivalent series resistance (Equation 18) or load transient response (Equation 19):

$$\text{Cout1 ripple} = \frac{\text{Iout\_max} \times (1-\text{D})}{\left(\text{Vout rip} - \text{Ipk} \times \frac{\text{Np}}{\text{Ns}} \times \text{Resr}\right) \times \text{fsw}} \qquad (18)$$

$$\text{Cout2 Itran} = \frac{\Delta\text{Iout}}{2\pi \times \Delta\text{Vout} \times \text{fBW}} \qquad (19)$$

where ΔIout is a change in output load current, ΔVout is the allowable output-voltage excursion and fBW is the estimated converter bandwidth.

Equation 20 calculates the output capacitor RMS current as:

$$\text{ICout rms} = \sqrt{\frac{\text{Ipk}^2 \times \left(\frac{\text{Np}}{\text{Ns}}\right)^2 \times t2 \times fsw}{3} - \text{Iout\_max}^2} \qquad (20)$$

Equations 21 and 22 estimate the input capacitor's parameters as:

$$\text{Cinmin} = \frac{\text{Ipk} \times \text{D}}{2 \times \text{fsw} \times \text{Vin rip}} \qquad (21)$$

$$\text{ICin rms} = \sqrt{\frac{\text{Ipk}^2 \times \text{D}}{3} - \left(\frac{\text{Pout\_max}}{\text{Vin} \times \eta}\right)^2} \qquad (22)$$

Equations 23, 24 and 25 summarize the three time intervals and their relationship:

$$\text{t1} = \sqrt{\frac{2 \times \text{Vout} \times \text{Iout} \times \text{Lpri}}{\text{Vin}^2 \times \text{fsw} \times \eta}} \qquad (23)$$

$$\text{t2} = \frac{\text{t1} \times \text{Vin}}{(\text{Vout} + \text{Vd}) \times \frac{\text{Np}}{\text{Ns}}} \qquad (24)$$

$$\text{t3} = \frac{1}{\text{fsw}} - \text{t1} - \text{t2} \qquad (25)$$

If you need additional secondary windings, Equation 26 easily calculates additional winding, Ns2:

$$\frac{\mathrm{Ns2}}{\mathrm{Ns1}} = \frac{\mathrm{Vout2+\ Vd2}}{\mathrm{Vout1 + Vd1}} \qquad (26)$$

where Vout1 and Ns1 are the regulated output voltage.

The transformer primary RMS current is the same as the FET RMS current in Equation 10; the transformer secondary RMS current is shown in Equation 27. The transformer core must be capable of handling Ipk without saturating. You should consider core losses too, but that is beyond the scope of this article.

$$\mathrm{Isec} = \mathrm{Ipk} \times \frac{\mathrm{Np}}{\mathrm{Ns}} \sqrt{\frac{\mathrm{t2} \times \mathrm{fsw}}{3}} \qquad (27)$$

The design of a DCM flyback is an iterative process; some initial assumptions, such as switching frequency, inductance or turn ratios may change based on later calculations, like power dissipations. But remain diligent – an optimized DCM flyback design can provide a low-power, compact and low-cost solution.