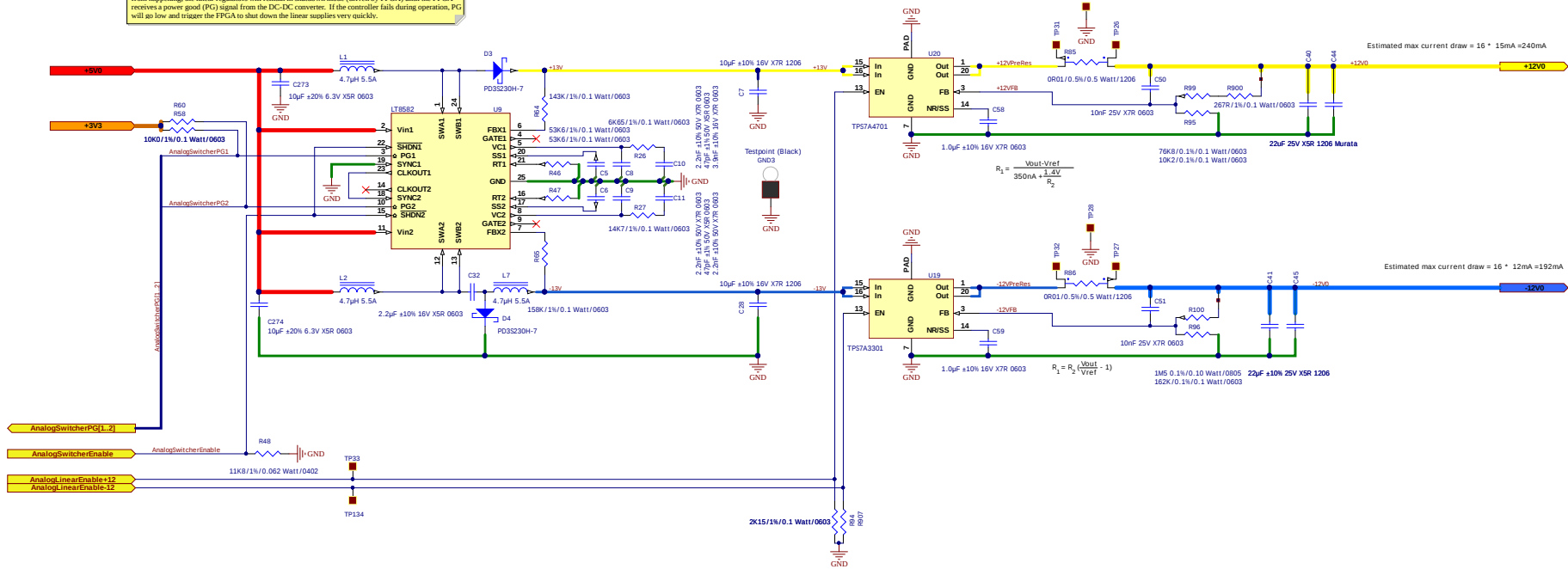


If an error occurs on the boost/inverting controller, the fail scenario would be that the -ve side output would be zero volts (because of DC blocking capacitor) and the positive side would be +4.3V (because of +5V passthrough of L11 and D3). This would cause DC offset on the op-amp outputs. To prevent this from happening, the linear regulators will remain in shutdown mode (driven by FPGA) until the FPGA receives a power good (PG) signal from the DC-DC converter. If the controller fails during operation, PG will go low and trigger the FPGA to shut down the linear supplies very quickly.



REV	DESCRIPTION	DATE
1	Initial Revision	

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Schematic Title Power		Revision -
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