Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

by Nicola Femia

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"There is nothing more practical than a good theory."

James C. Maxwell (1831-1879)

About the Author

Nicola Femia is Professor of Power Electronics at the University of Salerno, Italy, where he has founded the Power Electronics Research Group and the Power Electronics and Renewable Sources Laboratory. He is co-author of more than 180 scientific papers, one book and five patents. He has developed over 25 university and industry research projects on power electronics topics, and held over 50 invited lectures, courses and seminars on Power Electronics Design and Education in universities and industries over Europe, United States, China and India. In 2014 he has been Visiting Professor at the Electrical Engineering Department of Stanford University, Stanford, CA.

Introduction

This manual provides a guidance to a comprehensive hands-on learning experience on fundamentals of Power Electronics, tailored for Electrical Engineering and Electrical and Computer Engineering Undergraduate Programs. The education vision implemented in the laboratories anthology collected in the manual is founded on the intent of stimulating investigation and understanding capabilities of students, beyond the learning of technical topics. Problem-oriented theoretical models, circuit simulations and experimental tests are the ingredients of each laboratory, focusing on topics of wide interest in real world power electronics applications. The laboratories are inspired by the following key ideas:

1) whatever technical problem you need to solve regarding a physical device, circuit or system, there is always a good simplified theoretical model providing the key information, about what are the physical and functional factors majorly impacting the features of interest to the problem under investigation;

2) circuit simulators allow to implement models of different level of complexity to emulate the behavior of real devices, circuits and system, and help exploring their operability limits and observing the impact of model parameters and functional configurations on the resulting performances;

3) hands-on experimental tests and measurements are essential to validate and improve theoretical models, while understanding the impact of real physical parameters and functional features on the feasibility of targeted performance and reliability of devices, circuits and systems.

The combination of theory, simulations and experiments proposed in each laboratory engages the student into a virtuous learning loop, rich of observations and assessments, ending with a clear vision of a problem and of methods and tools to solve it. The laboratories, indeed, stimulate the students to interleave calculations, simulations and measurements, while changing model parameters based on observations of results, thus converging toward the improvement of models and the achievement of a desired real world behavior.

The laboratories are connected each other, forming four groups, which cover the fundamentals of DC-DC linear regulators, DC-DC buck regulators, DC-AC inverters, and AC-DC rectifiers. Each group of laboratories is performed by means of dedicated Multisim Live circuit schematics for simulations, and a dedicated section of the TI Power Electronics Board for experimental measurements. Although each lab is self-consistent, performing the entire sequence of laboratories dedicated to a given topology boosts the understanding of concepts and the achievement of a system level vision.

An important concept underlies the labs conception: power electronic circuits are systems made of single interconnected elements, conceived and configured to perform specific functional tasks and coordinated each other, to implement specified system features. Accordingly, the groups of laboratories from LAB1 to LAB4 and from LAB5 to LAB8 present and discuss a logical sequence of concepts and topics that guide the students step-by-step in understanding the transition from elements to systems, and from functions to features.

The four groups of labs offer also an opportunity to students to understand the manifold utilizations of a given device or concept over power electronics applications, to achieve different practical goals, or the same goal in different ways. This can be achieved, for example, through laboratories from LAB1 to LAB8, discussing the utilization of power MOSFETs either as variable resistors or as switches, to perform voltage regulation in linear and switching regulators, respectively, and through laboratories from LAB5 to LAB10, showing the utilization of pulse width modulation in DC-DC and DC-AC regulators, respectively. Crossed references of labs each other are included in the manual to highlight these connections.

The brief theory overview introducing each lab summarizes the main facts of interest to the topic under investigation, including simplified models tailored to the specific problem to be analyzed and solved. Going from a lab to the next one, the student learns that different simplified models can be used to represent a given device or system under different operating conditions. Students can use the models proposed in the labs theory overview, or they can replace them with the models discussed by instructors in the specific curriculum classes they teach.

This manual does not provide design rules and methodologies: indeed, the topics and the tools discussed throughout the labs intend to help students in achieving a good understanding of power electronics fundamentals, through the analysis of operation and performances of the elementary functional blocks building power supplies, thus preparing them to better assimilate the design topics taught by instructors in their classes.

Suggestions on possible expansion activities are also provided, to stimulate the exploration of further interesting aspects beyond the specific case studies discussed in each lab. Indeed, the anthology of labs proposed in the manual can be easily personalized and extended by instructors, also to cover topics regarding power semiconductors, magnetics, circuit theory, analog electronics, and control theory. Many test points and jumpers are available for this purpose in the TI Power Electronics Board, allowing to observe voltages and currents and to change the circuit configuration setup.

Learning Objectives

After completing the labs in this manual, you should have the ability to complete the following actions.

1. given a linear regulator, with specified components characteristics, you will be able to analyze and predict its behavior, under DC and AC operating conditions, in open-loop and closed-loop operation, by determining the values of voltages and currents of interest to evaluate static and dynamic performances, with specified units and accuracy;

2. given a buck regulator, with specified components characteristics, you will be able to analyze and predict its behavior, under DC and AC operating conditions, in open-loop and closed-loop operation, in continuous and discontinuous mode, by determining the values of voltages and currents of interest to evaluate the static and dynamic performances, with specified units and accuracy;

3. given a DC-AC pulse width modulated inverter, with specified components characteristics and modulation signals, you will be able to analyze and predict its behavior, under different load impedance conditions, by determining the amplitude of output current and voltage AC components, with specified units and accuracy:

4. given a high-frequency transformer and a square-wave inverter, with specified components characteristics and modulation signals, you will be able to analyze and predict its behavior, under different coils configurations, by determining the amplitude of input and output current and voltage AC components, with specified units and accuracy;

5. given an AC-DC rectifier, with specified components characteristics, you will be able to analyze and predict its behavior, under different input inductance and output capacitance conditions, by determining the amplitude of output current and voltage DC and AC components, with specified units and accuracy;

6. given a system comprises of an AC-DC rectifier with buck and linear post-regulators, with specified characteristics, you will be able to analyze and predict the behavior of the system, under different operating conditions, by determining the amplitude of input and output current and voltage DC and AC components of each stage, with specified units and accuracy.

Prerequisites

This lab manual was designed for students who have completed the following courses and have a working knowledge of the following hardware, software, and tools.

Completed Courses

1. *Introduction to Circuits*, or equivalent
2. *Semiconductor Devices*, or equivalent
3. *Introduction to Analog Electronics*, or equivalent

Hardware, Software, and Tool Knowledge

1. Oscilloscope
2. Function Generator
3. Digital Multimeter
4. Scientific Calculator

Organization of the Lab Manual

The manual is organized as a sequence of twelve labs, regarding four different power electronic topologies:

1-Linear Regulator

The four labs from Lab1 to Lab4 are dedicated to the linear regulator, focusing on the following topics:

Lab1: Linear Regulator in Open Loop DC Operation

The lab investigates the DC operation of a MOSFET as linear regulator, and the relationships among physical parameters and electrical variables determining the DC operating point

Lab2: Linear Regulator in Open Loop AC Operation

The lab investigates the AC operation of a MOSFET as linear regulator, and the relationships among physical parameters and electrical variables determining the effect of AC source perturbations on the output voltage

Lab3: Error Amplifier Operation

The lab investigates the operation of an error amplifier as feedback element, and the relationships among output voltage perturbations and the signal controlling the MOSFET gate drive voltage

Lab4: Linear Regulator in Closed Loop Operation

The lab investigates the impact of the closed loop feedback control on the capability of the linear regulator of maintaining the output voltage well regulated under DC and AC operating conditions, rejecting the source perturbations.

2-Buck Regulator

The four labs from Lab5 to Lab8 are dedicated to the buck regulator, focusing on the following topics:

Lab5: Buck Regulator Half-Bridge PWM Operation

The lab investigates the operation MOSFETs as switches, implementing the half-bridge used in buck regulator to convert a given DC input voltage into a lower DC output voltage

Lab6: Buck Regulator L-C Filter Operation

The lab investigates the operation of the L-C filter used to remove the high-frequency AC component generated by the MOSFET half-bridge of a buck regulator, and the relationships among physical and operating parameters determining the amplitude of AC ripple components of current and voltage.

Lab7: Buck Regulator in Discontinuous Mode Operation

The lab investigates the impact of a MOSFET-diode half-bridge on the operation of a buck regulator, and the relationships among physical and operating parameters determining the amplitude of AC ripple components of current and voltage an the voltage conversion ratio.

Lab8: Buck Regulator in Closed Loop Operation

The lab investigates the impact of the closed loop feedback control on the capability of the buck regulator of maintaining the output voltage well regulated under DC and AC operating conditions, rejecting the load perturbations.

3-DC-AC Inverter

Lab9 and Lab10 are dedicated to the single-phase DC-AC inverter and to the high-frequency transformer, focusing on the following topics:

Lab9: DC-AC PWM Inverter Operation

The lab investigates the operation of a MOSFETs full-bridge, driven by a sinusoidal pulsed width modulation, under different load impedance conditions, and the relationships among physical parameters and operating conditions determining the amplitude of output current and voltage AC components.

Lab10: High-Frequency Transformer Operation

The lab investigates the operation of a high-frequency transformer under square-wave voltage generated by a MOSFET full-bridge DC-AC inverter, and the relationships among physical parameters and operating conditions determining the output current and voltage and the amplitude of magnetizing current, under different coils configurations.

4-AC-DC Rectifier

Lab11 and Lab12 are dedicated to the single-phase AC-DC rectifier, focusing on the following topics:

Lab11: AC-DC Rectifier Operation

The lab investigates the operation of a single-phase diode full-bridge rectifier, under different input inductance and output capacitance conditions, and the relationships among physical parameters and operating conditions determining the amplitude of output voltage AC component.

Lab12: Post Regulators Operation

The lab investigates the operation of a system comprised of an AC-DC diode rectifier with a cascade of buck and linear post-regulators, and the relationships among physical parameters and operating conditions determining the behavior of the system and the amplitude of input and output current and voltage DC and AC components of each stage.

Lab Tools and Technology

Platform: NI ELVIS III
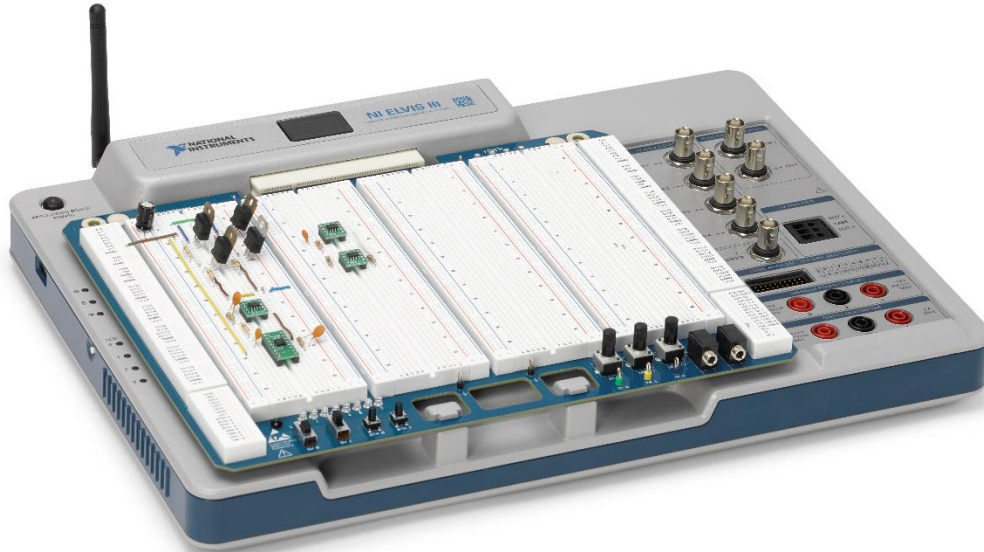
The NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) is an engineering laboratory solution for project-based learning that combines instrumentation and embedded design with a web-driven experience to create an active learning environment in the lab and studio and flipped classrooms, delivering a greater understanding of engineering fundamentals and system design. NI ELVIS addresses engineering curriculum by integrating project-based learning, teamwork, and design with course-specific application boards and labs developed by experts from education and industry. NI ELVIS, as a programmable platform, gives educators the ability to scale to future multidisciplinary applications driving student employability.

Learn more at http://www.ni.com/en-us/support/model.ni-elvis-iii.html

Hardware: TI Power Electronics Board
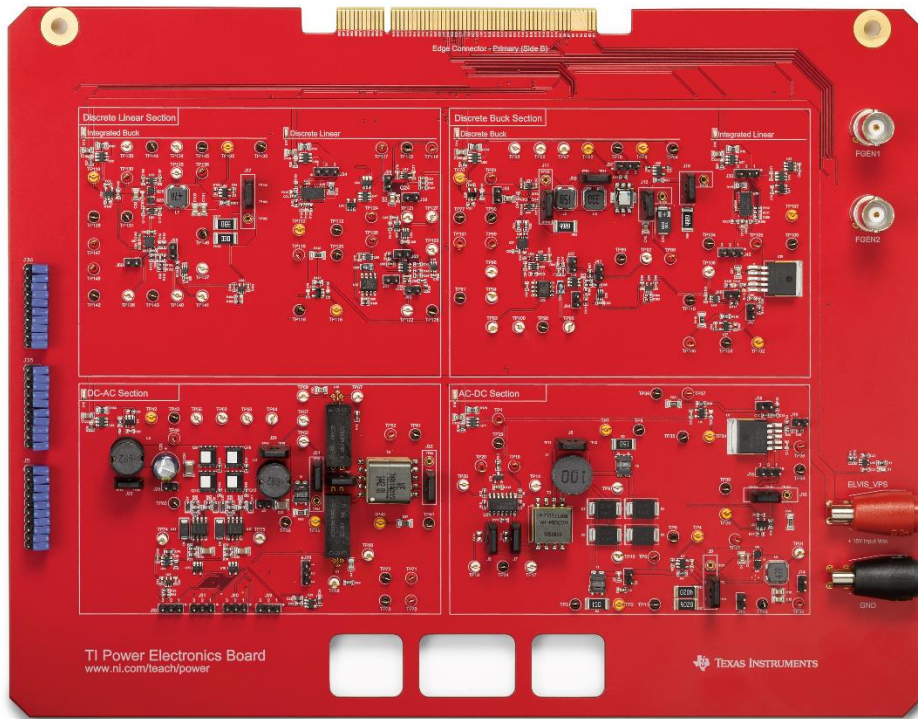
The TI Power Electronics Board is an application board for NI ELVIS III which provides a hands-on platform for learning power electronics and power management. Using functional blocks, students build their own buck converters, regulators, and both DC-AC and AD-DC converters. Students will gain an in-depth understanding of each component in a power electronics system and how it influences other components to create a cohesive system all while using industry-standard Texas Instruments circuits.

Warnings:

- Read carefully the instructions provided in each Lab about connections and setup of TI Power Electronics Board and NI ELVIS III instrumentation, and follow Lab steps.
- Compensate all the voltage probes used for measurements with the oscilloscope, before performing each Lab (see **http://www.ni.com/white-paper/14825/en/#toc4**).
- Connect the ground of the oscilloscope voltage probes to the nearest test point of the TI Power Electronics Board Section under test, with black plastic ring.

Learn more at http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

Software: Multisim Live
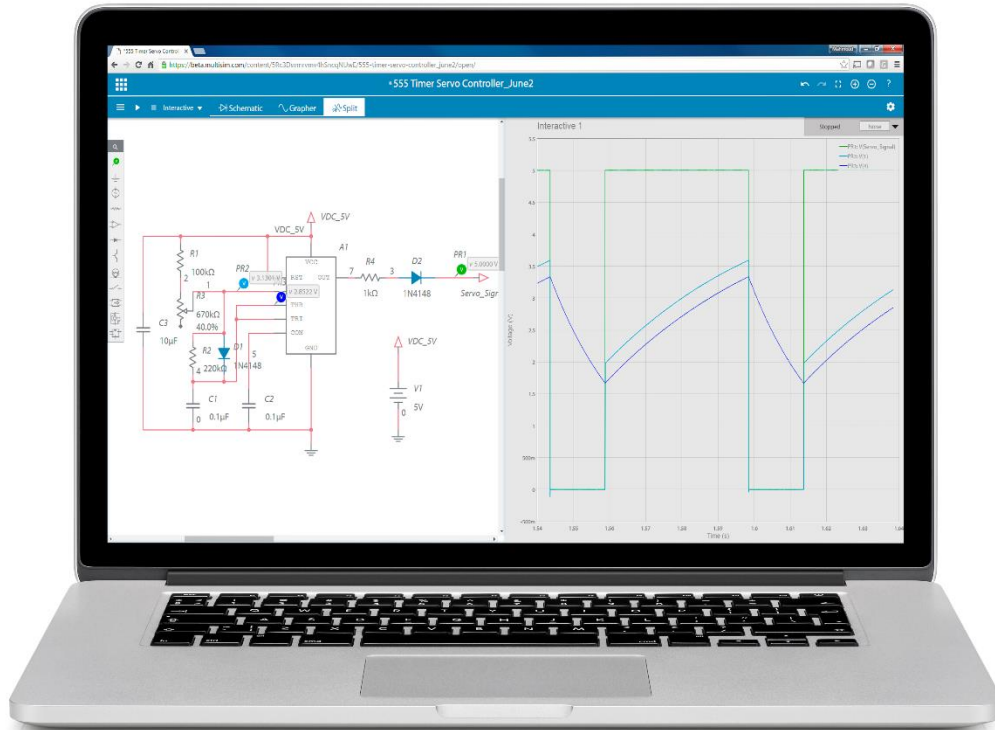
Multisim Live brings SPICE simulation to you anywhere, anytime with an interactive, online, touch-optimized environment that works on any device. With a database of over 30,000 community circuits, engineers, students, and makers can immediately turn inspiration into simulation.

Learn more at https://www.multisim.com/

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
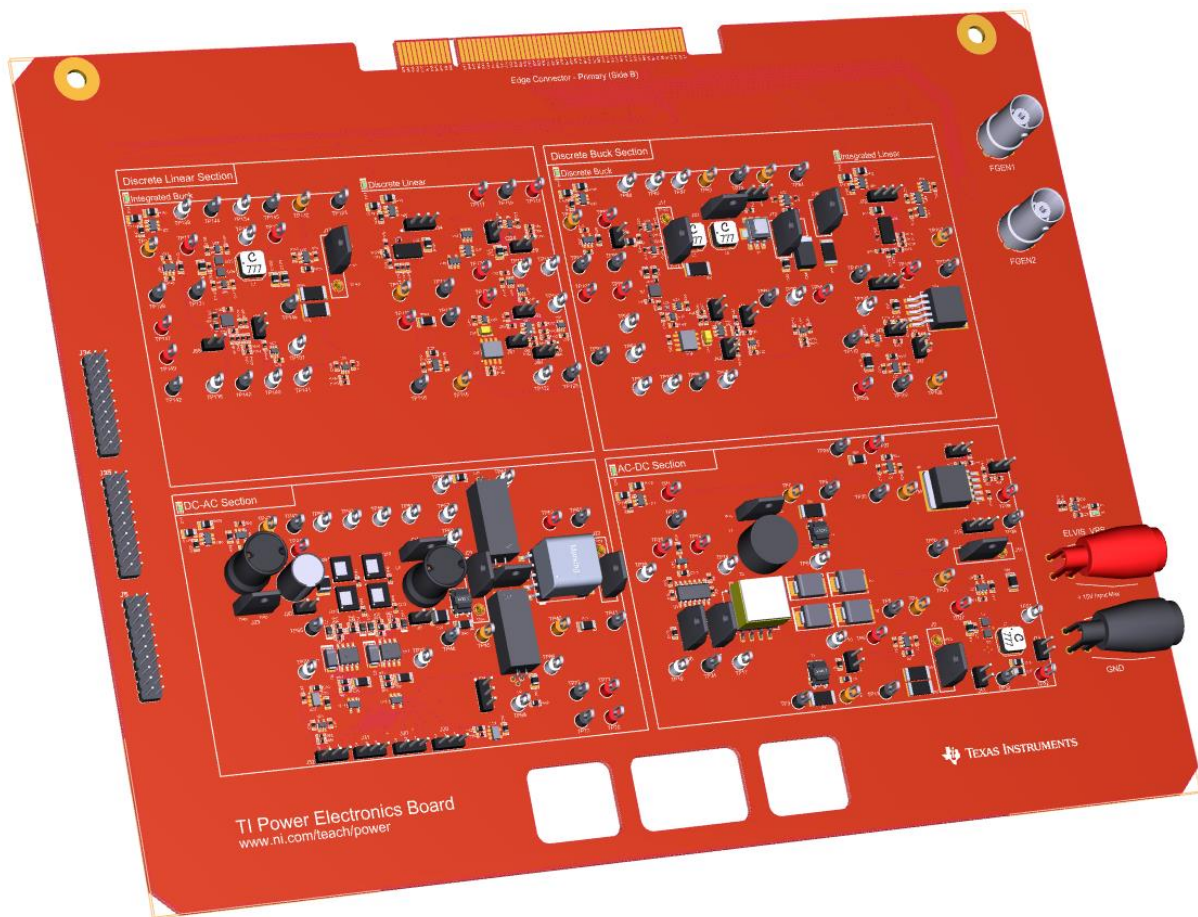
Lab 1: Linear Regulator
in Open Loop DC Operation

Lab 1: Linear Regulator in Open Loop DC Operation

The goal of this lab is to investigate the properties of a MOSFET in DC operation, when it works as a pass device in linear regulators. First, we review the equations describing the behavior of a MOSFET in DC operation, and discuss the impact of the gate-to-source voltage on the operating point. Next, we predict the MOSFET operating region and calculate the power losses and temperature under different conditions. Then, we simulate the MOSFET using its physical model. Finally, we perform lab experiments to estimate the real value of MOSFET parameters and compare their impact on the accuracy of theoretical and simulation predictions.
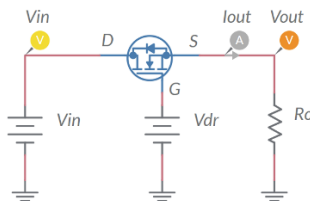
Figure 1-1. Linear Regulator

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given the parameters of a MOSFET, a source voltage and a load resistance, you will calculate the gate driver voltage required to achieve a desired output voltage, you will determine the MOSFET operating region and calculate its drain-to-source voltage and current, power losses and junction temperature, with specified units and accuracy, by applying the appropriate MOSFET equations
2. Given the parameters of a MOSFET, a source voltage, and a load resistance, you will determine the gate driver voltage required to achieve a desired output voltage by simulating the MOSFET operation, you will determine the MOSFET operating region and calculate its drain-to-source voltage and current, power losses and junction temperature, with specified units and accuracy, and you will determine the accuracy of theoretical predictions.
3. Given a real MOSFET, a DC power supply, a load resistor of given resistance, and a function generator, you will set experimentally the MOSFET gate driver voltage allowing to achieve a desired output voltage, you will record the measurement, with specified units and accuracy, you will compare the measured values with the simulations, and you will determine the accuracy of simulations.

Required Tools and Technology

Platform: NI ELVIS III
Instruments used in this lab:
   ● Function generator
   ● Digital multimeter
   ● Oscilloscope
   ● Power Supply
 	
Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.
	✓ Access Instruments
	  https://measurementslive.ni.com/
	✓ View User Manual
	  http://www.ni.com/en-us/support/model.ni-elvis-iii.html
	✓ View Tutorials
	  https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board	✓ View User Manual http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

Software: NI Multisim Live	✓ Access
	  https://www.multisim.com/
	✓ View Tutorial
	  https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility	✓ Download (Windows OS Only) http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a MOSFET as a linear regulator. This important feature is utilized in a large variety of low-power applications, where a well regulated DC voltage is required.

1-2 The linear regulator concept

Figure 1-2 shows a circuit composed of a voltage generator, V_{in}, a load resistor, R_o, and a variable resistor, R_{var}.
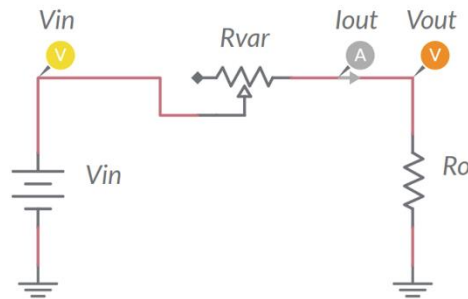
Figure 1-2. Resistive Voltage Divider

If the voltage V_{out} required by the load is lower than V_{in}, then the voltage drop across the variable resistor must equal the difference V_{in}-V_{out}. The value of the resistance R_{var} required to achieve the desired load voltage V_{out}, is given by Equation 1-1:

Equation 1-1
$$R_{var} = \frac{V_{in} - V_{out}}{V_{out}} R_o = \frac{V_{in} - V_{out}}{I_{out}}$$

The resistance R_{var} depends on the input voltage V_{in}, and on the load current, I_{out}: it must be adjusted to maintain the output voltage regulated at the desired value V_{out}, when V_{in} and I_{out} are subjected to time variations. This happens in many practical applications, where the source voltage V_{in} can be affected by disturbances (e.g. automotive power electronics) and the load can require a variable power (e.g. power signal amplifiers).

1-3 MOSFET operating as linear regulator

Figure 1-3 shows the basic circuit schematic of a linear regulator, using an N-channel MOSFET as a "pass device".
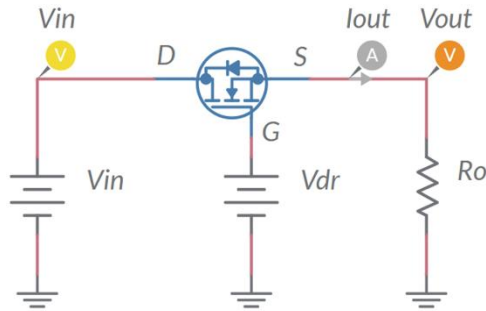
The linear regulator uses the MOSFET capability to emulate a variable resistor, whose resistance is driven by the gate-to-source voltage applied between the gate (G) and the source (S). The output voltage V_{out} can be regulated at the desired value by adjusting the gate-to-source voltage. The circuit driving the MOSFET gate-to-source voltage works as a source, providing a voltage V_{dr}. The voltage V_{dr} is applied to the gate terminal G and yields a gate-to-source voltage $V_{GS} = V_G - V_{out} = V_{dr} - V_{out}$. Equations 1-2 (also called MOSFET output characteristics) describe the MOSFET drain-to-source current in DC operation, as function of the drain-to-source voltage and gate-to-source voltage:

Equations 1-2

$$\text{cut-off region}: \quad V_{GS} < V_{th} \Rightarrow \quad I_{DS} = 0$$

$$\text{saturation region}: \quad V_{GS} > V_{th}, \quad V_{DS} > V_{GS} - V_{th} \Rightarrow \quad I_{DS} = \frac{\beta}{2}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$$\text{ohmic region}: \quad V_{GS} > V_{th}, \quad V_{DS} < V_{GS} - V_{th} \Rightarrow \quad I_{DS} = \frac{\beta}{2}V_{DS}[2(V_{GS} - V_{th}) - V_{DS}](1 + \lambda V_{DS})$$

V_{th} is the gate-to source threshold voltage, β is the trans-conductance coefficient, and λ is the channel-length modulation coefficient. Equations 1-2 highlight that, given the drain-to-source voltage V_{DS}, the current I_{DS} the MOSFET lets to pass from drain to source is determined by the gate-to-source voltage V_{GS}. The operating point of the MOSFET is determined by the combination of its own characteristics with the source and load parameters.

1-4 MOSFET DC operating point

The grey lines in Figure 1-4 are the plots of Equations 1-2, parameterized with respect to the gate-to-source voltage. The red line in Figure 1-4 is the locus of operating points of the MOSFET determined while varying the gate-to-source voltage, given the source voltage V_{in} and the load resistance R_{load}, while the green line is locus of the MOSFET DC operating points allowed by a given gate-to-source voltage $V_{GS}{}^*$.
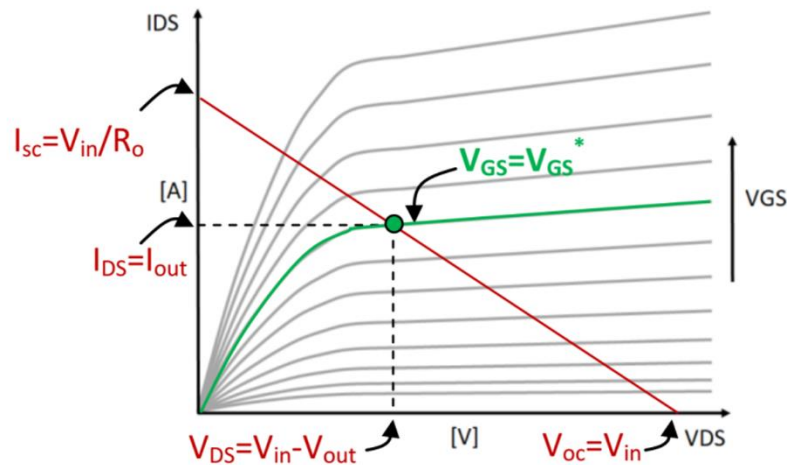
Figure 1-4. Determination of the MOSFET DC Operating Point.

The intersection of the red and green lines is the MOSFET DC operating point. It can be determined by means of the constraints given by Equations 1-3 to 1-5:

Equation 1-3
$$V_{DS} = V_{in} - V_{out}$$

Equation 1-4
$$V_{GS} = V_{dr} - V_{out}$$

Equation 1-5
$$I_{DS} = I_{out} = \frac{V_{out}}{R_o}$$

Combining Equations 1-2 to 1-5 allows determining the gate driver voltage V_{dr}, given the input voltage V_{in}, the load resistance R_o and the desired output voltage V_{out}. Neglecting the minor impact of the channel-length modulation coefficient λ in DC operation yields the simplified Equations 1-6 and 1-7:

saturation region (the equations are valid if $V_{DS} > V_{GS} - V_{th} \Rightarrow V_{in} > V_{dr} - V_{th}$):

Equation 1-6
$$V_{dr} = V_{th} + V_{out} + \sqrt{\frac{2V_{out}}{R_o \beta (1 + \lambda(V_{in} - V_{out}))}} \cong V_{th} + V_{out} + \sqrt{\frac{2V_{out}}{R_o \beta}}$$

ohmic region (the equations are valid if $V_{DS} < V_{GS} - V_{th} \Rightarrow V_{in} < V_{dr} - V_{th}$):

Equation 1-7
$$V_{dr} \cong V_{th} + \frac{V_{in} + V_{out}}{2} + \frac{V_{out}}{R_o \beta (V_{in} - V_{out})}$$

The gate driver voltage V_{dr} required to achieve the desired output voltage V_{out} is independent of the input voltage V_{in} when $V_{in} > V_{dr} - V_{th}$ (MOSFET operating in the saturation region), whereas it increases while the input voltage V_{in} decreases when $V_{in} < V_{dr} - V_{th}$ (MOSFET operating in the ohmic region). Equations 1-6 and 1-7 highlight that a MOSFET with a higher V_{th} requires a higher driver voltage V_{dr} to achieve the desired output voltage V_{out}. The minimum input voltage V_{inmin} allowing the output voltage regulation is determined by the gate driver voltage rating V_{drmax}. The difference $V_{inmin} - V_{out}$ is the "dropout voltage" of the linear regulator. *Low Dropout Regulators* (LDO) are characterized by a small dropout voltage.

1-5 MOSFET thermal properties

The MOSFET can operate at a maximum junction temperature rating T_{rating} of 150°C or 175°C, depending on its technology. Exceeding the maximum junction temperature may result in damage of the MOSFET and possible fault in the operation of the circuit where the MOSFET is used. The junction temperature depends on the MOSFET power loss, which can be calculated by means of Equation 1-8:

Equation 1-8
$$P_{loss} = V_{DS} I_{DS} = (V_{in} - V_{out}) \frac{V_{out}}{R_o}$$

Given the ambient temperature T_a, the MOSFET junction temperature T_j is given by Equation 1-9:

Equation 1-9
$$T_j = T_a + R_{\theta ja} P_{loss}$$

The coefficient $R_{\theta ja}$ is the thermal resistance of the MOSFET, determined by the package.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 Given the source voltage and load resistance, how does the MOSFET drain-to-source **current change** as the gate driver voltage increases?

    A. it increases
    B. it decreases
    C. it is not influenced

1-2 Given the source voltage and load resistance, how does the MOSFET drain-to-source **voltage change** as the gate driver voltage increases?

    A. it increases
    B. it decreases
    C. it not influenced

1-3 Given the desired output voltage and load resistance, how does the required MOSFET gate driver voltage change while the input voltage decreases, if the MOSFET operates in the saturation region?

    A. it increases
    B. it decreases
    C. it is not influenced

1-4 When does the MOSFET operate in the ohmic region as a linear regulator?

    A. never
    B. when the input voltage is much higher than the required output voltage
    C. when the input voltage is a little higher than the required output voltage

1-5 Given the source voltage and load resistance, how does the MOSFET power loss change as the gate driver voltage increases?

    A. increases
    B. not influenced
    C. non monotonic

2 Exercise

The Texas Instruments CSD15380F3 (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf) N-channel MOSFET Q1 used in the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III has the following nominal parameters:

- $V_{th} = 1.1V$ [the real value of V_{th} can range between 0.85V and 1.35]

- $\beta = 0.24A/V^2$ [the real value of β can range between 0.19V and 0.33]

- $\lambda = 0.02V^{-1}$ [the real value of λ can range between 0.01V and 0.05]

- $R_{\theta ja} = 255°C/W$ [the real value of $R_{\theta ja}$ is influenced by the device mounting]

Assume the following operating parameters:

- $V_{in} = 7V$

- $R_o = 120\Omega$

- $T_a = 30°C$

2-1 Using the rules and equations provided in the **Theory and Background** section, calculate the gate driver voltage V_{dr} required to achieve the values of output voltage listed in column 1 of Table 2-1, determine the status of the MOSFET (OFF = cut-off, SAT = saturation, OHM = ohmic), calculate the drain-to-source voltage and current, the power loss and the junction temperature of the MOSFET, with three decimal digits (for the temperature use one decimal digit), and report the results in Table 2-1.

Table 1-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

1	2	3	4	5	6	7
V_{out} [V]	status	V_{dr} [V]	V_{DS} [V]	I_{DS} [A]	P_{loss} [W]	T_j [°C]
1.5						
3.0						
4.5						
6.0						

3 Simulate

The simulations you will perform in this section allow you to analyze the impact of the gate driver voltage V_{dr} on the operating point of a MOSFET operating as a linear regulator. You will compare the results of the simulations with the results of calculations performed in the **Exercise** section, based on the simplified Equations 1-6 - 1-9, to verify the theoretical prediction and evaluate the impact of MOSFET parameters on the DC operating point.

3.1 Instructions

1. Open *Lab1 – MOSFET DC operation* from this file path:
   https://www.multisim.com/content/vuVttWyHxrRuPfki7F33Ad/lab-1-linear-regulator-open-loop-dc-operation/

   The circuit schematic for the analysis of MOSFET DC operating points is shown in Figure 3-1. The MOSFET is modeled by means of an *Analog Behavioral Modeling* current source (*ABM* current source). The *ABM* model implements the MOSFET Equations 1-2 provided in the **Theory and Background** section. The MOSFET parameters are set by means of the voltage sources *Vth*, *beta* and *lam* at the values used in the **Exercise** section.
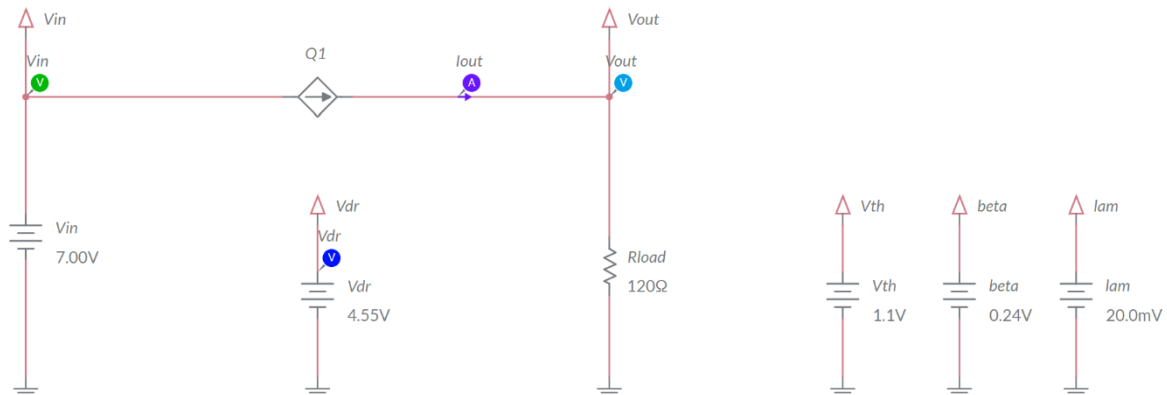
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of a Linear Regulator in Open Loop DC Operation

2. Select the *Interactive* simulation option and the *Schematic* visualization option.
3. Set the gate driver voltage V_{dr} at zero.

4. Run the simulation and increase the gate driver voltage (V_{dr}) until the number shown by the output voltage probe (V_{out}) equals the value of the output voltage indicated in the first column-first row of Table 3-1, with three decimal digits.
5. Record the value of the gate driver voltage in the second column of Table 3-1.
6. Repeat the simulation for all the values of the output voltage V_{out} listed in column 1 of Table 3-1.
7. Import in column 3 of table 3-1 the values of gate driver voltage reported in column 2 of Table 2-1 of **Exercise** section.
8. Calculate the % error ($V_{dr,cal}$-$V_{dr,sim}$)/$V_{dr,sim}$ x 100 between the values of the gate driver voltage V_{dr} obtained with calculations and simulations.
9. Calculate the power loss and the junction temperature of the MOSFET.
10. Calculate the % efficiency $\eta = P_{out}/P_{in}$ x 100= V_{out}/V_{in} x 100.

Table 3-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

1	2	3	4	5	6	7
V_{out} [V]	$V_{dr,sim}$ [V]	$V_{dr,cal}$ [V] from column 2 of Table 2-2	V_{dr} error [%]	P_{loss} [W]	T_j [°C]	η [%]
1.5						
3.0						
4.5						
6.0						

3-1   Does the maximum power loss correspond to the minimum efficiency?

A.   yes
B.   no
Please provide your comment _____

_____

3-2   What is the maximum V_{dr} % error between calculations and simulations?

A.   max % error <1%
B.   1% < max % error < 10%
C.   max % error >10%

3-3   Do you identify a trend in the V_{dr} error values vs the output voltage V_{out}?

      A.   yes
      B.   no
      Please provide your comment _____

_____

3-4   What is the possible origin of the error between V_{dr} calculations and simulations?

_____

Troubleshooting tips:
- If you get an error greater than 10% between simulation and calculation results, check the values of source voltage, load resistance and MOSFET parameters.
- If the simulation does not converge and you get some error message, reload *Lab1 – Linear Regulator in Open Loop DC Operation* from this file path: https://www.multisim.com/content/vuVttWyHxrRuPfki7F33Ad/lab-1-linear-regulator-open-loop-dc-operation/ and restart the simulation following the relevant instructions.

4 Implement

The **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 allows performing experiments on MOSFET DC Operation as linear regulator. The jumpers and test points used to setup the tests and measure the signals of interest are highlighted. The experiments you perform in this section allow you to observe the behavior of a real MOSFET in DC operation, to verify the effect of the gate driver voltage on the MOSFET status and operating condition. You will compare the experimental measurements with the results of simulations. Next, you will verify the compliance of the MOSFET simulation model with the real MOSFET behavior. Finally, you will determine possible adjustments of MOSFET model parameters to improve accuracy of simulations. The MOSFET Q24 of the linear regulator is a Texas Instruments CSD15380F3 (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf). [**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]
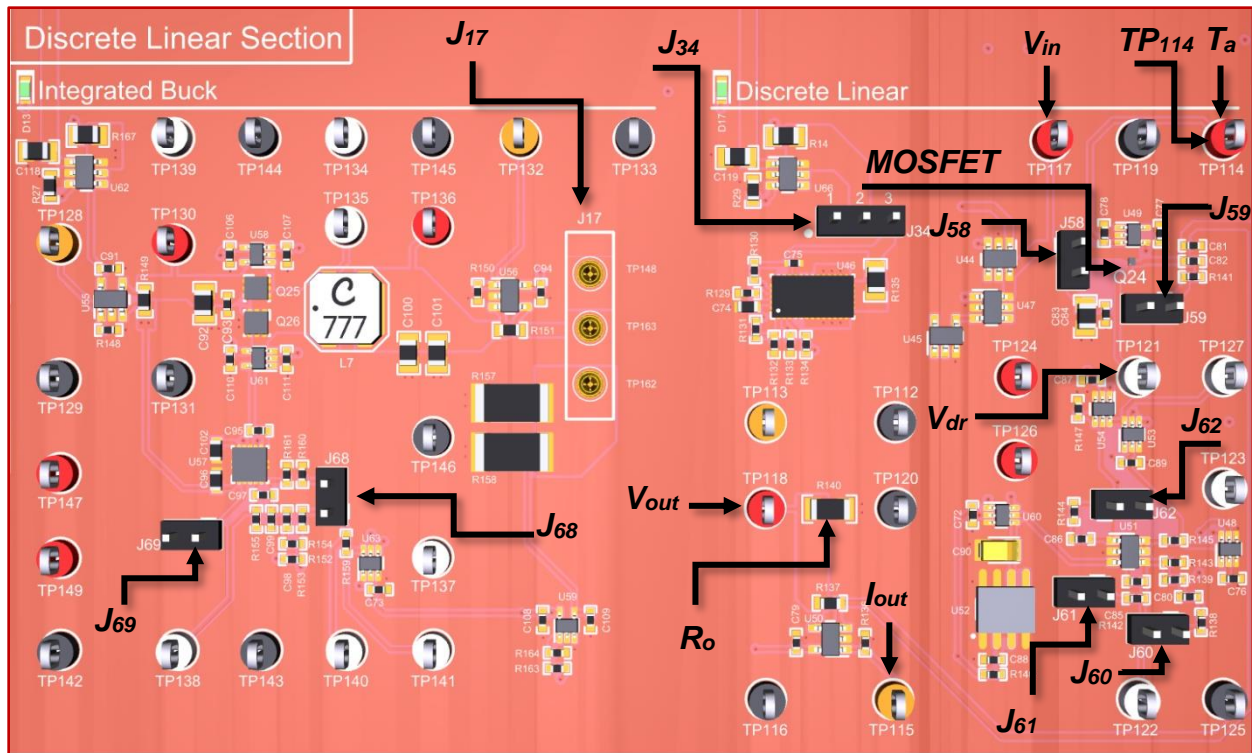
Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of a Linear Regulator in Open Loop DC Operation.

4-1 Instructions

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/

2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path： http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.

4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab1 – Linear Regulator in Open Loop DC Operation*.

5. Configure the jumpers of the board as indicated in Table 4-1.

6. Configure and connect the instruments as indicated in Tables 4-2 and 4-3.

Table 4-1 Jumpers setup

J17	J34	J58	J59	J60	J61	J62	J68	J69
short TP162-TP163	short 2-3	open	short	short	short	short	short	short

Table 4-2 Instruments Configuration and setup

Power Supply	Channel "+": Static, 7.00V, Channel "-": Inactive			
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 100us/div	*Acquisition*: average	*Measurements*: show
	Channel 1: ON • DC coupling • 1V/div • offset -4.0V • position -4.0V	*Channel 2*: ON • DC coupling • 1V/div • offset -4.0V • position -4.0V	*Channel 3*: ON • DC coupling • 1V/div • offset -4.0V • position -4.0V	*Channel 4*: OFF
Function Generator	*Channel 1*: Inactive *Channel 2*: Sine, Frequency 1Hz, Amplitude 0.00Vpp, DC offset 0.00V			
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: Automatic			

Table 4-3 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect Ch-1 to TP117 (V_{in}), connect Ch-2 to TP118 (V_{out}) connect Ch-3 to TP121 (V_{dr})
Function Generator	connect Ch-2 to FGEN2 BNC connector ($\rightarrow$TP121 = Discrete Linear V_{dr})
Digital Multimeter	connect Voltage input to TP115 (I_{out})

7. Run *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter*.
8. Adjust the *Power Supply* voltage until the RMS measurement of *Oscilloscope* Ch-1 (V_{in}) equals 7.00V [**Note:** in this experiment, use Volts, Ampères and Watts in voltage, current and power measurements and calculations, respectively, with three decimal digits].
9. Increase the DC offset of the *Function Generator* Ch-2 (V_{dr}) until the RMS measurement of the *Oscilloscope* Ch-2 (V_{out}) equals the value of the output voltage indicated in the first column-first row of Table 4-4. [**Note:** the maximum allowed value of gate driver voltage V_{dr} is $V_{dr,max}$ **= 6.5V**]
10. Read the RMS measurement of the *Oscilloscope* Ch-3 (V_{dr}) and the *Digital Multimeter* measurement (I_{out}), calculate the input power $P_{in} = V_{in}$ x I_{out}, and record the values in columns 2, 5 and 6 of Table 4-4, respectively.

11. Calculate the output power $P_{out} = V_{out} \times I_{out}$, and the % efficiency $\eta = P_{out}/P_{in} \times 100$, with one decimal digit, and report the result in columns 7 and 8 of Table 4-4, respectively.
12. Connect the *Digital Multimeter* to Test Point TP114, read the DC voltage measurement V_{TP114} in Volts, calculate the ambient temperature according to the formula $T_a = (V_{TP114} - 0.5V) \times 100$, calculate the MOSFET junction temperature according to the formula $T_j = T_a + (P_{in} - P_{out})R_{\theta ja}$, and report the result in column 9.
13. Repeat the measurements for all the values of the output voltage V_{out} listed in column 1 of Table 4-4.
14. Stop *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter*.
15. Import in column 3 of Table 4-4 the values of voltage V_{dr_sim} reported in column 2 of Table 3-1 of **Simulate** section.
16. Calculate the % error $(V_{dr,sim} - V_{dr,meas})/V_{dr,meas} \times 100$ between the values of the voltage V_{dr} obtained with simulations and measurements.

Table 4-4 DC operating point of the MOSFET, given the source voltage, load resistance and gate driver voltage

1	2	3	4	5	6	7	8	9
V_{out} [V]	$V_{dr,meas}$ [V]	$V_{dr.sim}$ [V] from column 2 of Tab 3-2	V_{dr} error [%]	I_{out} [A]	P_{in} [W]	P_{out} [W]	eff [%]	T_j [°C]
1.50								
3.00								
4.50								
6.00								

4-1 What is the maximum V_{dr} % error between simulations and measurements?

    A.   max % error <1%
    B.   1% < max % error < 10%
    C.   max % error >10%

4-2   What is the possible origin of the error between V_{dr} calculations and simulations?

_____

4-3   Did you to achieve the required output voltage with a gate driver voltage lower than

the maximum allowed value of 6.5V?

    A.   yes
    B.   no
    Please provide your comments: _____

_____

_____

_____

Troubleshooting tips:
- If the MOSFET does not work, or if the error between simulation and measurement is greater than 20%, verify the correct setup and connections of instruments, based on directions provided in Tables 4-1 and 4-2, and restart the experiment.

5 Analyze

5-1 Graph the values of voltage V_{dr} collected in columns 2 and 3 of Table 4-4 as a function of the required voltage V_{out}, including a legend that indicates which line style corresponds to which series (simulations, measurements).
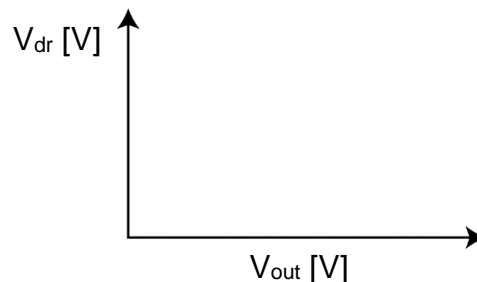
Figure 5-1 Simulated and Measured Values of Output Voltage V_{out} versus the Gate Driver Voltage V_{dr}.

5-2   Are the V_{dr} error values positive or negative?

      A.   always positive
      B.   always negative
      C.   either sign
      Please provide your comments: _____

_____

_____

_____

5-3   Do you see a trend in the V_{dr} error values vs the output voltage V_{out}?

      A.   increasing
      B.   decreasing
      C.   no precise trend
      Please provide your comments: _____

_____

_____

_____

5-4   Based on your observations and on the MOSFET properties discussed in the **Theory and Background** section, what parameter would you modify in the MOSFET model to reduce the error between measurements and simulations? How and why?

      A. V_{th}: _____

      B. β: _____

      C. λ: _____

5-5   Re-run the simulation by changing the parameters of MOSFET model, based on your answers to Question 5-5, and verify your predictions. Are the new simulation results closer to experimental ones? Do you infer a rule or a procedure to obtain the parameters of a MOSFET from experimental measurements?

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you learned and observed about the impact of MOSFET gate driver voltage and physical parameters on the linear regulator open loop DC operation. Explain why it is important to predict correctly the gate driver voltage value needed to achieve a desired value of the output voltage, and how the MOSFET parameters influence the value of gate driver voltage.

6-2   Expansion Activities

6-2-1. Investigate how the source voltage V_{in} influences the MOSFET operation, by determining the transition from saturation region to ohmic region. The investigation can be performed by means of simulations and experiments. In both cases, set the source voltage V_{in} at a given value (not exceeding 10V) and find the gate driver voltage V_{dr} that determines an output voltage V_{out} = V_{in}/2. Then, decrease the source voltage V_{in} in 100mV steps, while observing the output voltage V_{out}. You will observe no change in the output voltage until the input voltage reaches a certain value, below which you will see the output voltage to decrease. The change of behavior of the MOSFET is determined by the transition from the saturation to the ohmic region.

6-2-2. Repeat the Simulation 2 discussed in the **Simulate** section, by changing the voltage of sources *Vth*, *beta* and *lam* in the ranges indicated in Table 6-1, to investigate the sensitivity of the MOSFET DC operation point with respect to its model parameters.

Table 6-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

min V$_{th}$ [V]	max V$_{th}$ [V]	min beta [S]	max beta [S]	min lam [V^{-1}]	max lam [V^{-1}]
0.85	1.35	0.19	0.33	0.01	0.05

6-3 Resources for learning more

- This document provides the fundamentals of linear regulators:
  Linear Regulators: Theory of Operation and Compensation,
  http://www.ti.com/lit/an/snva020b/snva020b.pdf

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   A

1-2   B

1-3   C

1-4   C

1-5   C

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
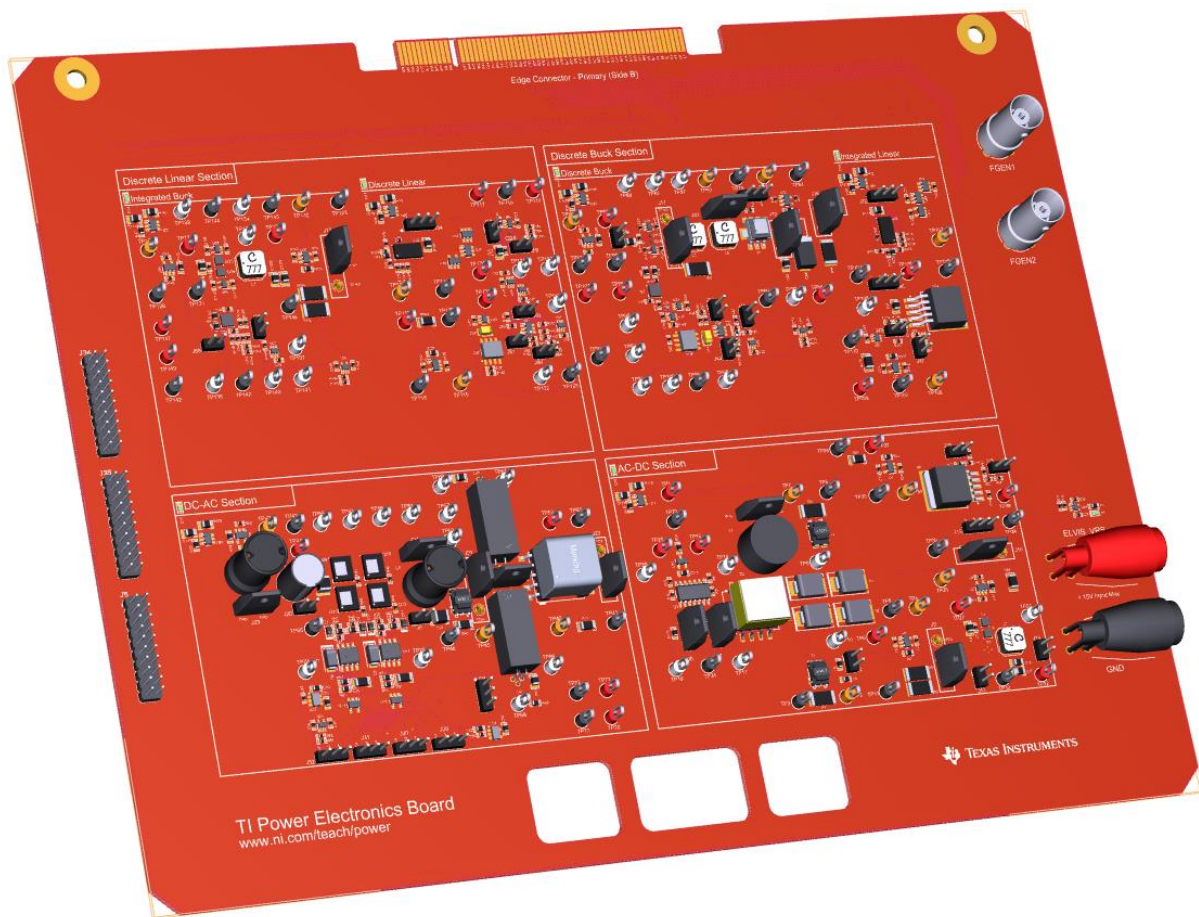
Lab 2: Linear Regulator in Open Loop AC Operation

Lab 2: Linear Regulator in Open Loop AC operation

The goal of this lab is to investigate the properties of a linear regulator in open loop AC operation. First, we will review the simplified equations describing the behavior of MOSFET in AC operation. Next, we will use this model to analyze and predict the sensitivity of the output voltage to AC perturbations injected on source and gate driver voltage, at different frequencies. Then, we will observe the response of a MOSFET to AC perturbations through simulations based on real MOSFET physical model. Finally, we will perform experimental measurements on a real MOSFET in AC operation, and will compare the results of calculations, simulations and measurements to verify the consistency of theoretical predictions.
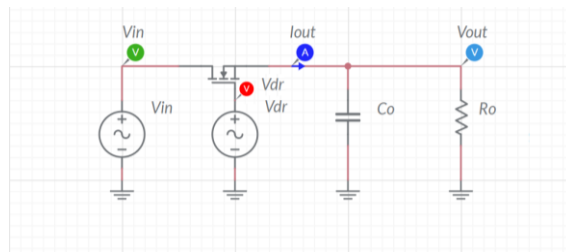
Figure 2-1 Linear Regulator

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a MOSFET, a load resistance, a DC source voltage, and a DC gate driver voltage, you will calculate the magnitude of the output voltage AC perturbation determined by AC perturbations injected on source and gate driver voltage, with specified units and accuracy, by applying the appropriate theoretical formulae.
2. Given a MOSFET, a load resistance, a DC source voltage, and a DC gate driver voltage, you will simulate the AC operation of the MOSFET to analyze the sensitivity of the output voltage with respect to AC perturbations injected by the source and gate driver voltage, with specified units and accuracy, to determine the accuracy of theoretical predictions.
3. Given a MOSFET, a dynamic power supply, a load resistor of given resistance, and a dynamic gate driver, you will analyze experimentally the output voltage AC perturbation determined by AC perturbations injected on source and gate driver voltage at different frequencies, with specified units and accuracy, to verify the consistency of theoretical predictions and simulations.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

✓ Access Instruments
https://measurementslive.ni.com/
✓ View User Manual
http://www.ni.com/en-us/support/model.ni-elvis-iii.html
✓ View Tutorials
https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

✓ View User Manual
http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

✓ Access
https://www.multisim.com/
✓ View Tutorial
https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

✓ Download (Windows OS Only)
http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by means of Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations on simulations and experiments
- ✓ Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental equations that are needed to analyze the AC operation of a MOSFET used in linear regulators applications. The AC response is an important feature of linear regulators, as it expresses the ability of the regulators to reject AC noise.

1-2 Linear Regulator in Open Loop AC Operation

Figure 1-2 shows a DC-DC linear regulator using a MOSFET as pass device, connected between a voltage source V_{in} and a load resistor R_o. The output voltage V_{out} is controlled by the MOSFET gate driver voltage V_{dr}. The capacitor C_o damps the AC output voltage perturbations.
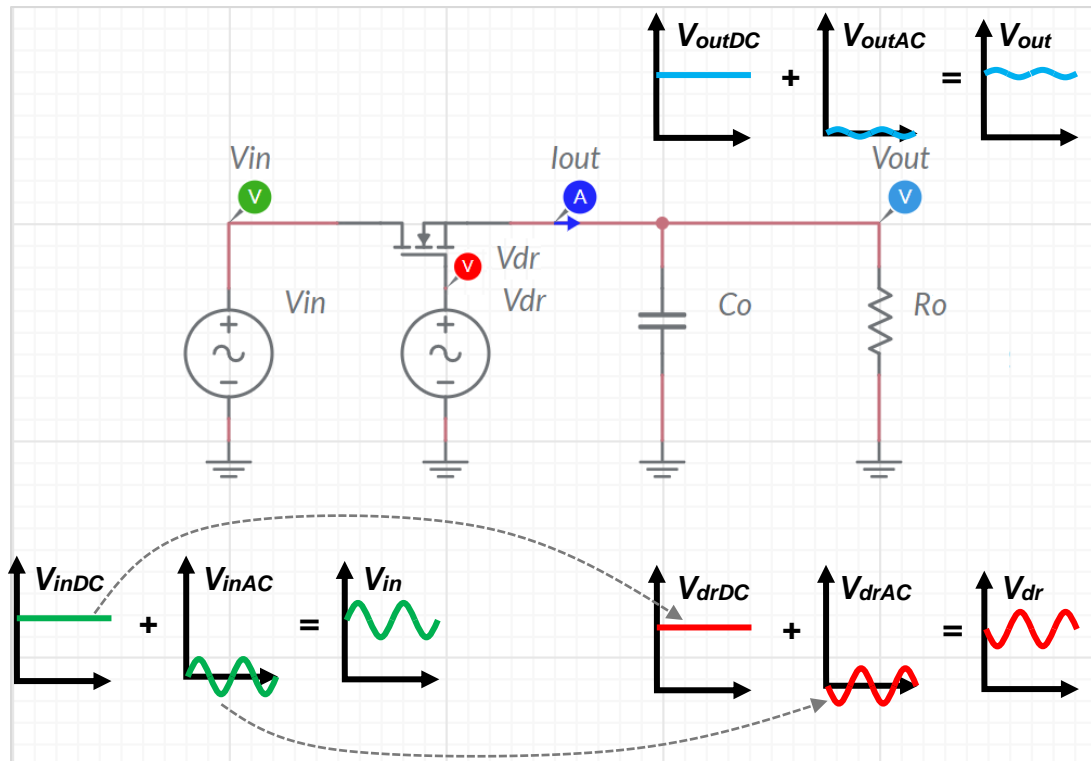
Figure 1-2. Linear Regulator in Open Loop AC Operation

In steady-state, given the DC component of source voltage V_{inDC}, the DC component of the gate driver voltage V_{drDC} can be adjusted to achieve the desired DC component value V_{outDC} of the output voltage. An AC perturbation $V_{inAC}sin(2\pi f{\cdot}t)$ of frequency f is applied to

the source voltage which causes an AC perturbation $V_{outAC}sin(2\pi f \cdot t + \varphi)$ on the output voltage, whose amplitude V_{outAC} and phase shift φ depend on MOSFET parameters, on C_o and R_o, and on frequency f. An AC perturbation $V_{drAC}sin(2\pi f \cdot t + \theta)$ injected on gate driver voltage at the same frequency f, with suitable amplitude V_{drAC} and phase shift θ, can cancel the output voltage AC perturbation.

1-3 Simplified Model of MOSFET in Open Loop AC Operation

A simplified model of a MOSFET in AC operation can be obtained by linearization of MOSFET drain-to-source DC current equations (see LAB1). The resulting simplified equations of the drain-to-source current I_{dsAC} are:

Equation 1-1 $I_{dsAC} = M_{in}V_{inAC} + M_{dr}V_{drAC} + M_{out}V_{outAC}$, *ohmic regio*n ($V_{inDC} < V_{drDC}$ - V_{th})

Equation 1-2 $I_{dsAC} = T_{in}V_{inAC} + T_{dr}V_{drAC} + T_{out}V_{outAC}$, *saturation regio*n ($V_{inDC} > V_{drDC}$ - V_{th})

$$M_{in} = \beta\left(V_{drDC} - V_{th} - V_{inDC}\right), \qquad M_{out} = -\beta\left(V_{drDC} - V_{th} - V_{outDC}\right), \qquad M_{dr} = \beta\left(V_{inDC} - V_{outDC}\right)$$

$$T_{in} = \tfrac{1}{2}\lambda\beta\left(V_{drDC} - V_{th} - V_{outDC}\right)^2, \quad T_{out} \cong -\beta\left(V_{drDC} - V_{th} - V_{outDC}\right), \quad T_{dr} \cong \beta\left(V_{drDC} - V_{th} - V_{outDC}\right)$$

where V_{th}, β, λ are the MOSFET gate-to-source threshold voltage, the transconductance coefficient and the channel-modulation coefficient, respectively. Equations 1-1 and 1-2 highlight that the AC response of the MOSFET depends on the DC operating point. Moreover, while the parameter β influences the output voltage sensitivity with respect to both V_{dr} and V_{in} (T_{in} and T_{dr} are both proportional to β), the parameter λ influences the output voltage sensitivity with respect to V_{in} (T_{in} is proportional to λ).

1-4 Open loop AC response of a linear regulator

The output voltage AC perturbation $V_{outAC}sin(2\pi ft + \varphi)$ of a linear regulator caused by the effect of AC perturbations $V_{inAC}sin(2\pi ft)$ and $V_{drAC}sin(2\pi ft + \theta)$ of source and gate driver voltages can be analyzed by using the circuit shown in Figure 1-3. The amplitude V_{outAC} of the output voltage perturbation is given by Equation 1-3:

Equation 1-3 $$V_{outAC} = I_{dsAC}\frac{R_o}{\sqrt{1+(2\pi C_o R_o f)^2}}$$

Merging Equations 1-1, 1-2 and 1-3 provides the expression of the ratio between the amplitude V_{outAC} of the AC output voltage perturbation and the amplitudes V_{inAC} and V_{drAC}:
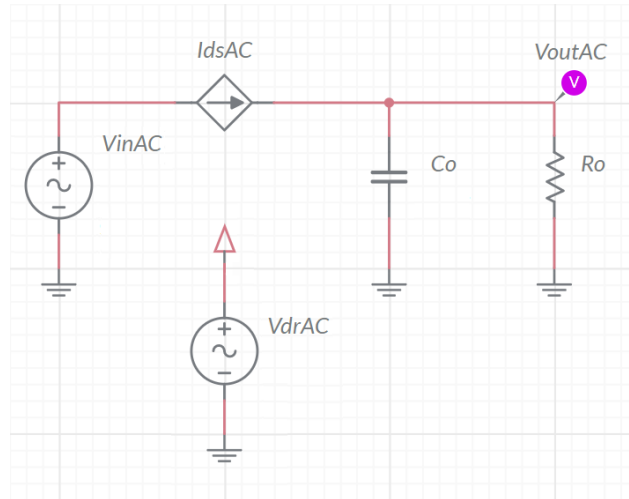
Figure 1-3. Simplified Circuit Model for the Analysis of Linear regulator in Open Loop AC Operation.

Equations 1-4

$$\left.\frac{V_{outAC}}{V_{inAC}}\right|_{V_{drAC}=0} = \begin{cases} \dfrac{M_{in}}{D_m} & ohmic\ region \\ \dfrac{T_{in}}{D_t} & saturation\ region \end{cases} \quad ; \quad \left.\frac{V_{outAC}}{V_{drAC}}\right|_{V_{inAC}=0} = \begin{cases} \dfrac{M_{dr}}{D_m} & ohmic\ region \\ \dfrac{T_{dr}}{D_t} & saturation\ region \end{cases}$$

$$f_m = \frac{1 - M_{out}R_o}{2\pi R_o C_o}, \quad D_m = 2\pi C_o \sqrt{f^2 + f_m^2} \quad (ohmic\ region)$$

$$f_t = \frac{1 - T_{out}R_o}{2\pi R_o C_o}, \quad D_t = 2\pi C_o \sqrt{f^2 + f_t^2} \quad (saturation\ region)$$

Equations 1-3 show that the sensitivity of the output voltage to AC source and gate driver voltage perturbations decreases as the frequency *f* increases. This means that the open loop linear regulator has a low-pass behavior. Moreover, the regulator has a different low-pass bandwidth, f_m and f_t, in the ohmic and saturation region respectively.

1-5 Effect of MOSFET capacitances.

The preceding simplified analysis neglects the impact of MOSFET capacitances. Therefore, Equations 1-6 and 1-7 are valid within a limited frequency range, whose boundary is influenced by the values of the MOSFET capacitances. Moreover, as the simplified model is based on linearization of MOSFET equations, the preceding analysis is more accurate if the amplitude of AC perturbations V_{inAC} and V_{drAC} is small (less than 10%) compared to the amplitude of DC components V_{inDC} and V_{drDC}.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 How is the amplitude of the AC output voltage perturbations correlated to the frequency of the AC source and gate driver voltage perturbations?
A. it is not correlated
B. it increases as the frequency increases
C. it decreases as the frequency increases

1-2 How is the sensitivity of the AC output voltage perturbations correlated to the DC operating point of the MOSFET?
A. it is not correlated
B. it is higher in the ohmic region
C. it is higher in the saturation region

1-3 How can you cancel the effects of AC source voltage perturbations on the output voltage?
A. by means of a MOSFET with a big threshold voltage V_{th}
B. by means of an appropriate AC perturbation injected on the gate driver voltage
C. by means of a MOSFET with a small trans-conductance coefficient β

1-4 If your answer to Question 1-3 is "B", what is the frequency of the AC perturbation to inject on the gate driver voltage?
A. the same of the AC source voltage disturbance
B. whatever
C. it depends on the DC output voltage

1-5 Is the accuracy of the simplified AC MOSFET model conditioned by the MOSFET AC operating conditions?
A. no
B. yes
if your answer is B, list the conditions ensuring better accuracy: _____

_____

_____

2 Exercise

The Texas Instruments CSD15380F3 (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf) N-channel MOSFET Q1 of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III has the following nominal parameters: V_{th} = 1.1V, β = 0.24A/V^2, λ =0.02V^{-1} [**Note:** if you have already performed **Lab1**, you can use the values of V_{th}, β and λ you have determined by means of the experiments]. Let us consider the following operating conditions and parameters:

A: V_{inDC} = 5.00V, V_{drDC} = 4.55V, V_{outDC} = 3.00V, R_o = 120Ω, C_o = 1μF.

B: V_{inDC} = 3.30V, V_{drDC} = 4.60V, V_{outDC} = 3.00V, R_o = 120Ω, C_o = 1μF.

2-1 Given the operating conditions A and B, for each value of the frequency f indicated in Table 2-1, use the equations provided in the **Theory and Background** section to:

- determine the MOSFET operating region (ohmic or saturation), calculate the relevant bandwidth f_m or f_t in kHz, with three decimal digits, and report the results in columns 2 and 5 of Table 2-1 (check the appropriate boxes), for case A and B respectively;

- calculate the amplitude in mV, with three decimal digits, of the AC output voltage perturbation V_{outAC} determined by an AC perturbation V_{inAC} = 100mV applied to the source voltage, and report the results in columns 3 and 6 of Table 2-1, for case A and B respectively;

- calculate the amplitude in mV, with three decimal digits, of the AC output voltage perturbation V_{outAC} determined by an AC perturbation V_{drAC} = 100mV applied to the gate driver voltage, and report the results in columns 4 and 7 of Table 2-1, for case A and B respectively;

2-2 Repeat the calculations with C_o = 11μF, and fill the relevant part of Table 2-2.

Table 1-1 Analysis of Linear Regulator in Open Loop AC operation, with C_o=1μF.

C_o=1μF	A: ☑ SAT ☐ OHM			B: ☐ SAT ☑ OHM		
1	2	3	4	5	6	7
f [kHz]	☐ f_m [kHz] ☑ f_t [kHz]	V_{outAC} [mV] V_{inAC}=100mV V_{drAC}=0	V_{outAC} [mV] V_{drAC}=100mV V_{inAC}=0	☑ f_m [kHz] ☐ f_t [kHz]	V_{outAC} [mV] V_{inAC}=100mV V_{drAC}=0	V_{outAC} [mV] V_{drAC}=100mV V_{inAC}=0
2						
10						
20						

$C_o=11\mu F$	A: ☑ SAT ☐ OHM			B: ☐ SAT ☑ OHM		
1	2	3	4	5	6	7
f [kHz]	☐ f_m [kHz] ☑ f_t [kHz]	V_{outAC} [mV] V_{inAC}=100mV V_{drAC}=0	V_{outAC} [mV] V_{drAC}=100mV V_{inAC}=0	☑ f_m [kHz] ☐ f_t [kHz]	V_{outAC} [mV] V_{inAC}=100mV V_{drAC}=0	V_{outAC} [mV] V_{drAC}=100mV V_{inAC}=0
2						
10						
20						

3 Simulate

The simulations you will perform in this section allow you to analyze AC perturbations on the output voltage of a MOSFET operating as linear regulator. You will observe the effects caused on the output voltage by AC perturbations injected on source voltage and on gate driver voltage. You will compare the results of the simulations with the results of calculations performed in the **Exercise** section, based on the simplified Equations 1-6 and 1-7, to verify the accuracy of theoretical calculations, and to observe the impact of the output capacitor on the AC perturbations of the output voltage.

3.1 Instructions

1. Open *Lab2 – Linear Regulator in Open Loop AC operation* from this file path:
   https://www.multisim.com/content/WxHkfMbLxCkJrJVMqPbX8Y/lab-2-linear-regulator-ac-open-loop-operation/
   The circuit schematic for the analysis of MOSFET AC operation is shown in Figure 3-1. The MOSFET is modeled by means of current source Q1, and its parameters are set by means of the voltage sources *Vth*, *beta* and *lam*, and correspond to the values used in the **Exercise** section. The parameters {*VA*, *Freq*, *VO*} of the voltage generators V_{in} and V_{dr} correspond to the parameters {V_{inAC}, *f*, V_{inDC}}, and {V_{drAC}, *f*, V_{drDC}}, respectively, as defined in the **Theory and Background** section.
2. Enter the values recorded in columns 3, 4, 6 and 7 of Table 2-1 of Exercise section in columns 3, 5, 7 and 9 of Table 3-1, respectively.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the switch S1 OPEN
5. Set the DC components V_{inDC} and V_{drDC} of source and gate driver voltage generators at values indicated for *Test A* in Table 3-1.
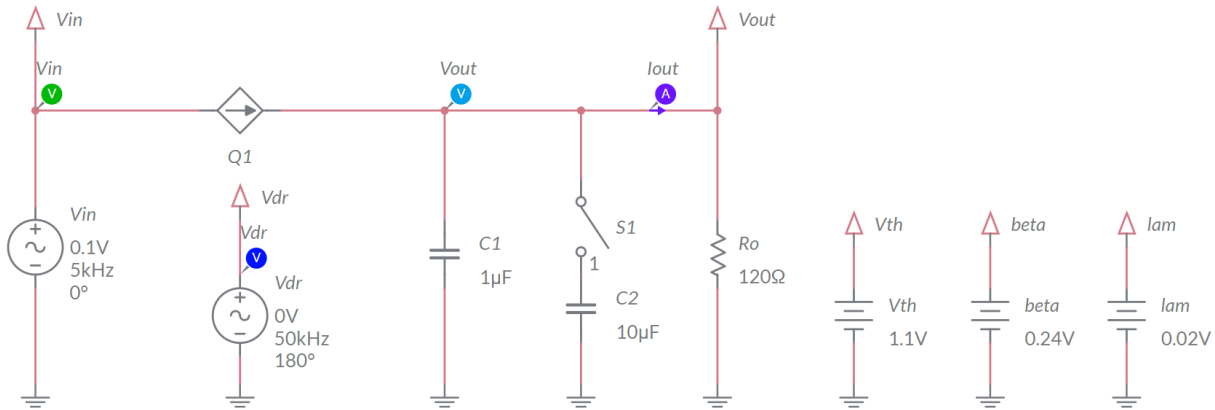
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Linear Regulator in Open Loop AC Operation.

6. Set the AC component of source voltage generator V_{in} with amplitude $V_{inAC} = 0.1\text{V}$.
7. Set the frequency of the AC component of source voltage generator V_{in} at the first value listed in column 1 of Table 3-1.
8. Set the AC component of gate driver generator V_{dr} with amplitude $V_{drAC}=0.0\text{V}$.
9. Run the simulation, read the measurement of peak-to-peak AC perturbation of the output voltage V_{pp} provided by the V_{out} voltage probe, calculate the amplitude $V_{outAC} = V_{pp}/2$ of the output voltage AC perturbation in mV, with two decimal digits resolution, and report the resulting value in column 2 of Table 3-1.
10. Repeat the step 9 for each value of the frequency listed in column 1.
11. Set the AC component of source voltage generator V_{in} with amplitude $V_{inAC} = 0\text{V}$.
12. Set the AC component of gate driver generator V_{dr} with amplitude $V_{drAC}=0.1\text{V}$.
13. Set the frequency of the AC component of gate driver generator V_{dr} at the first value listed in column 1 of Table 3-1.
14. Run the simulation, read the measurement of peak-to-peak AC perturbation of the output voltage V_{pp} provided by the V_{out} voltage probe, calculate the amplitude $V_{outAC} = V_{pp}/2$ of the output voltage AC perturbation in mV, with two decimal digits resolution, and report the resulting value in column 4 of Table 3-1.
15. Repeat the step 14 for each value of the frequency listed in column 1.
16. Set the DC components V_{inDC} and V_{drDC} of source and gate driver voltage generators at values indicated for **Test B** in Table 3-1.
17. Repeat the steps 6 to 15, and fill column 6 with values of V_{outAC} resulting from step 9 and column 8 with values of V_{drAC} resulting from step 14.
18. Set the switch S1 CLOSED, selecting the capacitor value, repeat the steps 5 to 17 and fill Table 3-2.

Table 3-1 Analysis of MOSFET in AC operation with $C_o=1\mu F$.

1	Test A: $V_{inDC} = 5.00V$, $V_{drDC} = 4.55V$				Test B: $V_{inDC} = 3.30V$, $V_{drDC} = 4.60V$			
	2	3	4	5	6	7	8	9
f [kHz]	V_{outAC} [mV] @ V_{drAC}=0 simulation	V_{outAC} [mV] from col.3 of Tab 2-1	V_{outAC} [mV] @ V_{inAC}=0 simulation	V_{drAC} [mV] from col.4 of Tab 2-1	V_{outAC} [mV] @ V_{drAC}=0 simulation	V_{outAC} [mV] from col.6 of Tab 2-1	V_{outAC} [mV] @ V_{inAC}=0 simulation	V_{drAC} [mV] from col.7 of Tab 2-1
2								
10								
20								

Table 3-2 Analysis of MOSFET in AC operation with $C_o=11\mu F$

1	Test A: $V_{inDC} = 5.00V$, $V_{drDC} = 4.55V$				Test B: $V_{inDC} = 3.30V$, $V_{drDC} = 4.60V$			
	2	3	4	5	6	7	8	9
f [kHz]	V_{outAC} [mV] @ V_{drAC}=0 simulation	V_{outAC} [mV] from col.3 of Tab 2-1	V_{drAC} [mV] @ V_{outAC}=0 simulation	V_{drAC} [mV] from col.4 of Tab 2-1	V_{outAC} [mV] @ V_{drAC}=0 simulation	V_{outAC} [mV] from col.6 of Tab 2-1	V_{drAC} [mV] @ V_{outAC}=0 simulation	V_{drAC} [mV] from col.7 of Tab 2-1
2								
10								
20								

3-1 Do the values of V_{outAC} obtained with simulations and calculations show the same trend?

A. yes
B. no
Please provide your comment: _____

_____

3-2 Is the difference between calculations and simulations bigger in test A or in test B?

A. bigger in test A
B. bigger in test B
C. almost the same in test A and test B
Please provide your comment: _____

_____

Troubleshooting tips:

- If the simulation does not converge and you get some error message, reload *Lab2 – Linear Regulator in Open Loop AC Operation* from this file path:
  https://www.multisim.com/content/WxHkfMbLxCkJrJVMqPbX8Y/lab-2-linear-regulator-ac-open-loop-operation/
  and restart the simulation, following the instructions.

4 Implement

The experiments in this section allow you to observe the behavior of a real MOSFET in AC operation, and to verify the effect of source and gate driver voltage AC perturbations on the output voltage. You will compare the measurements with calculations, to verify the consistency of the theoretical predictions. This experiment is performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1. The regulator uses the TI's CSD15380F3 MOSFET and OPA835IDBVR OPAMP and is powered by a TI's TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage. The AC disturbance on the input voltage of the Discrete Linear regulator is provided by the Integrated Buck regulator. The jumpers and test points used to setup the tests and to measure the signals are highlighted in Figure 4-1.

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Linear Regulator in Open Loop AC Operation

TI's devices datasheets are available at the following links:

CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf

OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf

TPS40303DRCR Buck Regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1   Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document:
   http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab2 – Linear Regulator in Open Loop AC Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.

Table 4-1 Jumpers setup

J17	J34	J58	J59	J60	J61	J62	J68	J69
short TP148-TP163	short 2-3	open	open	short	short	short	short	open

6. Connect the instruments as indicated in Table 4-2.

Table 4-2 Instruments connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP117 (Discrete Linear V_{in}) connect CH-2 to TP118 (Discrete Linear V_{out}) connect CH-3 to TP121 (Discrete Linear V_{dr}) connect CH-4 to TP141 (Integrated Buck V_{FB})
Function Generator	connect Ch-1 to FGEN1 BNC connector ($\rightarrow$TP141 = Integrated Buck V_{FB}) connect Ch-2 to FGEN2 BNC connector ($\rightarrow$TP121 = Discrete Linear V_{dr})

7. Configure and setup the instruments as indicated in Table 4-3 for *TEST A1*.

Table 4-3 Instruments initial configuration and setup

Power Supply	CH "+": Static, 7.00V, CH "-": Inactive			
Oscilloscope	*Trigger*: analog edge, CH1, set to 50%	*Horizontal*: 200us/div	*Acquisition*: average	*Measurements*: show
	CH-1: ON • DC coupling • 200mV/div • offset -5.0V	CH-2: ON • DC coupling • 50mV/div • offset -3.0V	CH-3: ON • DC coupling • 50mV/div • offset -4.8V	CH-4: ON • DC coupling • 50mV/div • offset -0.60V
Function Generator	***TEST A1 and A2***			
	CH-1: Sine, DC offset 600mV, Amplitude 0mV, Frequency 2kHz CH-2: Sine, DC offset 4.8V, Amplitude 0mV, Frequency 2kHz			
	TEST B1 and B2			
	CH-1: Sine, DC offset 830mV, Amplitude 0mV, Frequency 2kHz CH-2: Sine, DC offset 4.85V, Amplitude 0mV, Frequency 2kHz			
	notes:	- increasing the DC offset of CH-1 yields a decrease of V_{inDC} - increasing the DC offset of CH-2 yields an increase of V_{outDC}		

8. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
9. Read the RMS Measurements of the *Oscilloscope* CH-1 (V_{in}) and CH-2 (V_{out}) in Volts: the expected values are $V_{inDC} = 5.0V$ and $V_{outDC} = 3.0V$. Adjust the DC offset of *Function Generator* CH-1 and CH-2 until you read the expected values, with at least one decimal digit accuracy.
10. Set the *Function Generator* CH-1 with amplitude = 190mV.
11. Stop the scope and use the horizontal cursors on the scope CH-1 waveform to measure the peak-peak $V_{in,pk-pk}$ amplitude in milli Volts, with all decimal digits shown by the instrument, and report the result in column 2 of Table 4-4. [**Note:** a value $V_{in,pk-pk} = 1000mV$ is expected, resulting in $V_{inAC} = 500mV$. If needed, adjust the Amplitude of *Function Generator* CH-1 until you get $V_{in,pk-pk} = 1000mV\pm50mV$].
12. Measure the $V_{out,pk-pk}$ amplitude in milli Volts, with all decimal digits shown by the instrument, calculate $V_{outAC} = V_{out,pk-pk}/2$ and report the result in column 3 of Table 4-4.
13. Calculate the ratio V_{outAC}/V_{inAC}, with four decimal digits, and report the result in column 4 of Table 4-4.

14. Calculate the ratio V_{outAC}/V_{inAC} by means of Equations 1-4 provided in **Theory and Background** section, with four decimal digits, and report the result in column 5 of Table 4-4.
15. Repeat steps 11-14 for the other values of frequency f listed in column 1 of Table 4-4, by adopting the following setups of Function Generator CH-1: {Freq,Amp}= {10kHz,510mV}, {20kHz,980mV}.

Table 4-4 AC operation of the MOSFET in saturation region, with $C_o=1\mu F$.

	test A1 V_{inDC} = 5.0V, V_{drDC} = 4.8V, V_{outDC} = 3.0V V_{inAC} = 500mV (nominal), V_{drAC} = 0				test A2 V_{inDC} = 5.0V, V_{drDC} = 4.8V, V_{outDC} = 3.0V V_{inAC} = 0, V_{drAC} = 100mV (nominal)			
1	2	3	4	5	6	7	8	9
f [kHz]	V_{inAC} [mV] @ V_{drAC}=0	V_{outAC} [mV] @ V_{drAC}=0	V_{outAC}/V_{inAC} measured	V_{outAC}/V_{inAC} calculated	V_{drAC} [mV] @ V_{outAC}=0	V_{outAC} [mV] @ V_{outAC}=0	V_{outAC}/V_{drAC} measured	V_{outAC}/V_{drAC} calculated
2								
10								
20								

[**Note:** adjust the oscilloscope horizontal scale to fit waveforms frequency. Suggested: 200us/div for 2kHz, 50us/div for 10kHz, 20us/div for 20kHz]

16. Configure the instruments as indicated in Table 4-3 for **TEST A2**.
17. Read the RMS Measurement of the *Oscilloscope* CH-1 (V_{in}) and CH-2 (V_{out}) in Volts: the expected values are V_{inDC}=5.0V and V_{outDC}=3.0V. Adjust the DC offset of *Function Generator* CH-1 and CH-2 until you read the expected values, with at least one decimal digit of accuracy.
18. Set the Amplitude of *Function Generator* CH-2 at 200mV.
19. Measure the amplitude of $V_{dr,pk-pk}$ in milli Volts, with all decimal digits shown by the instrument, and report the result in column 6 of Table 4-4 [**Note:** a value $V_{dr,pk-pk}$ = 200mV is expected, resulting in V_{drAC} = 100mV. If needed, adjust the Amplitude of *Function Generator* CH-2 until you get $V_{dr,pk-pk}$ = 100mV±5mV].
20. Measure the amplitude of $V_{out,pk-pk}$, in milli Volts with all decimal digits shown by the instrument, calculate V_{outAC} = $V_{out,pk-pk}$/2 and report the result in column 7 of Table 4-4.
21. Calculate the ratio V_{outAC}/V_{drAC} and report the result in column 8 of Table 4-4.
22. Calculate the ratio V_{outAC}/V_{drAC} by means of Equations 1-4 provided in **Theory and Background** section, and report the result in column 9 of Table 4-4.
23. Repeat steps 1919-22 for all frequency values listed in column 1 of Table 4-4.
24. Set the *Oscilloscope* offsets as follows: CH-1: -3.3V, CH3: -4.85V, CH-4: -0.8V.
25. Configure the instruments as indicated in Table 4-3 for **TEST B1**

26. Repeat the steps 8-15 and report the results in Table 4-5, by adopting the following setup of *Function Generator* CH-1:

    {Freq,Am} {2kHz,40mV}, {10kHz,100mV}, {20kHz,200mV}.

27. Configure the instruments as indicated in Table 4-3 for **TEST B2**

28. Repeat the steps 17-23 and report the results in Table 4-5, by adopting the following setup of *Function Generator* CH-2:

    {Freq,Amp}= {2kHz,200mV}, {10kHz,200mV}, {20kHz,200mV}.

29. Stop *Power Supply*, *Function Generator* and *Oscilloscope*.

30. Short the jumper J59 to set C_o=11µF, repeat steps 8 to 30 and report the results in Tables 4-6 and 4-7.

Table 4-5 AC operation of the MOSFET in ohmic region, with C_o=1µF.

	test B1 V_{inDC} = 3.3V, V_{drDC} = 4.9V, V_{outDC} = 3.0V V_{inAC} = 100mV (nominal), V_{drAC} = 0				test B2 V_{inDC} = 3.3V, V_{drDC} = 4.9V, V_{outDC} = 3.0V V_{inAC} = 0, V_{drAC} = 100mV (nominal)				
1	2	3	4	5	6	7	8	9	
f [kHz]	V_{inAC} [mV] @ V_{drAC}=0	V_{outAC} [mV] @ V_{drAC}=0	V_{outAC} / V_{inAC} *measured*	V_{outAC} / V_{inAC} *calculated*	V_{drAC} [mV] @ V_{outAC}=0	V_{outAC} [mV] @ V_{outAC}=0	V_{outAC} / V_{drAC} *measured*	V_{outAC} / V_{drAC} *calculated*	
2									
10									
20									

Table 4-6 AC operation of the MOSFET in saturation region, with C_o=11µF.

	test A1 V_{inDC} = 5.0V, V_{drDC} = 4.8V, V_{outDC} = 3.0V V_{inAC} = 500mV (nominal), V_{drAC} = 0				test A2 V_{inDC} = 5.0V, V_{drDC} = 4.8V, V_{outDC} = 3.0V V_{inAC} = 0, V_{drAC} = 100mV (nominal)				
1	2	3	4	5	6	7	8	9	
f [kHz]	V_{inAC} [mV] @ V_{drAC}=0	V_{outAC} [mV] @ V_{drAC}=0	V_{outAC} / V_{inAC} *measured*	V_{outAC} / V_{inAC} *calculated*	V_{drAC} [mV] @ V_{outAC}=0	V_{outAC} [mV] @ V_{outAC}=0	V_{outAC} / V_{drAC} *measured*	V_{outAC} / V_{drAC} *calculated*	
2									
10									
20									

Table 4-7 AC operation of the MOSFET in ohmic region, with C_o=11µF.

	test B1 V_{inDC} = 3.3V, V_{drDC} = 4.9V, V_{outDC} = 3.0V V_{inAC} = 100mV (nominal), V_{drAC} = 0				test B2 V_{inDC} = 3.3V, V_{drDC} = 4.9V, V_{outDC} = 3.0V V_{inAC} = 0, V_{drAC} = 100mV (nominal)				
1	2	3	4	5	6	7	8	9	
f [kHz]	V_{inAC} [mV] @ V_{drAC}=0	V_{outAC} [mV] @ V_{drAC}=0	V_{outAC} / V_{inAC} *measured*	V_{outAC} / V_{inAC} *calculated*	V_{drAC} [mV] @ V_{outAC}=0	V_{outAC} [mV] @ V_{outAC}=0	V_{outAC} / V_{drAC} *measured*	V_{outAC} / V_{drAC} *calculated*	

2							
10							
20							

4-1　Do you observe the same trend in the measured and calculated ratio V_{outAC}/V_{inAC} as the frequency increases?

    A.　yes
    B.　no
    Please provide your comments: _____

_____

4-3　Is the sensitivity of the output voltage with respect to source voltage AC perturbations higher in the saturation or in the ohmic region?

    A.　higher in saturation region
    B.　higher in ohmic region
    C.　it depends on the frequency of AC disturbances

4-2　Do you observe the same trend in the measured and calculated ratio V_{outAC}/V_{drAC} as the frequency increases?

    A.　yes
    B.　no
    Please provide your comments: _____

_____

4-4　Is the sensitivity of the output voltage with respect to gate driver voltage AC perturbations higher in the saturation or in the ohmic region?

    A.　higher in saturation region
    B.　higher in ohmic region
    C.　it depends on the frequency of AC disturbances

Troubleshooting tips:
- If the MOSFET does not work as expected, verify the setup and connections of instruments provided in Tables 4-1, 4-2 and 4-3, and restart the experiment.

5 Analyze

5-1 Graph the values of ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} collected in columns 4 and 5 and in columns 8 and 9 of Table 4-4, respectively, as a function of the frequency f, including a legend that indicates which line style corresponds to which series (calculations, measurements).
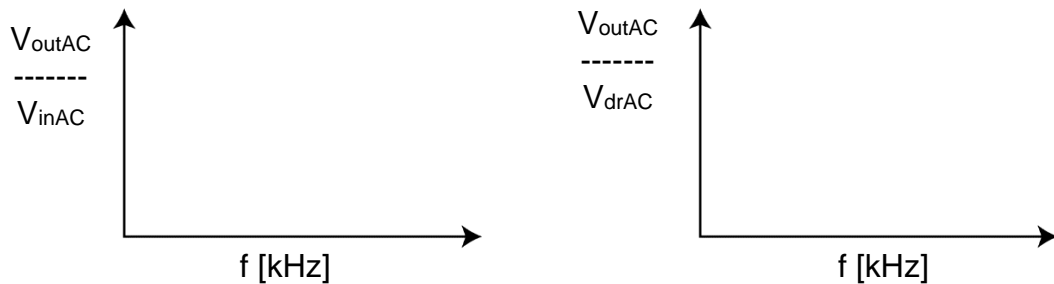
Figure 5-1 Calculated and Measured Values of Ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} Obtained while Varying the Frequency, with the MOSFET Operating in the Saturation Region

5-2 Graph the values of ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} collected in columns 4 and 5 and in columns 8 and 9 of Table 4-5, respectively, as a function of the frequency f, including a legend that indicates which line style corresponds to which series (calculations, measurements).
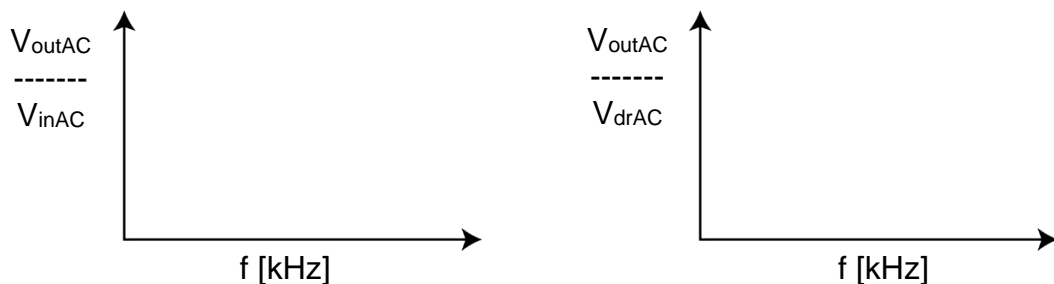
Figure 5-2 Calculated and Measured Values of Ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} Obtained while Varying the Frequency, with the MOSFET Operating in the Ohmic Region

5-3   In which operating region do you observe a bigger difference between calculated and measured values?

A.   saturation region
B.   ohmic region
C.   they are similar

5-4 Based on your answer to question 5-3, what can be the cause of the difference between calculated and measured values?

A. the accuracy of the MOSFET linearized model given by Equations 1-1 and 1-2 is poor when the amplitude of AC perturbations is not small compared to the DC component of the source and gate driver voltage

B. the MOSFET parameters V_{th}, β, λ used for calculations are not sufficiently accurate

C. other: _____

_____

5-5 Based on your answers to previous questions, what corrective actions would you take on the MOSFET parameters V_{th}, β, λ to improve the accuracy of calculations?

_____

_____

5-6 Repeat the calculations after making the actions you have proposed in you answer to Question 5-5, and verify your predictions. Are the new calculation results closer to experimental ones? Do you infer a practical guideline to obtain calculations better fitting experimental measurements?

_____

_____

5-7 Based on your observations, what operating region would you adopt to achieve a better noise immunity of the output voltage under AC source perturbations?

A. ohmic
B. saturation
C. either

why? _____

_____

6 Conclusion

6-1   Summary

Write a summary of what you learned and observed about the impact of the MOSFET DC bias point (saturation versus ohmic region) on its AC operation, regarding the sensitivity of the output voltage with respect to source and gate driver voltages AC perturbations. Explain why it is important to correctly determine the DC bias point of the MOSFET to predict its AC behavior by means of the mathematical model, and what are the main factors impacting the accuracy of theoretical calculations.

6-2   Expansion Activities

6-2-1. Investigate how the DC component of output voltage V_{outDC} influences the AC MOSFET operation, by repeating the previous calculations, simulations with Multisim Live circuit used in the **Simulate** section and measurements by means of the TI Power Electronics Board for NI ELVIS III used in the **Implement** section, with a different DC component of gate driver voltage V_{drDC}. You can analyze the operating conditions V_{outDC} = 1.5V (start with V_{drDC} = 2.9V, and adjust if needed) and V_{outDC} = 4.5V (start with V_{drDC} = 6.1V, and adjust if needed), with V_{inDC} = 7.0V. [Notes: 1) **do not exceed** 7V on V_{drDC}; 2) the **Theory and Background** section of **LAB1** provides the general equations allowing to set the DC component of gate driver voltage V_{drDC} required to achieve the desired DC output voltage V_{outDC}; 3) set the offset of the *Oscilloscope* Ch-2 equal to - V_{outDC}].

6-2-2. Perform **LAB1**, to learn more about linear regulator in open loop DC operation

6-2-3. Perform the following actions to analyze the complete open loop AC frequency response of a linear regulator, by means of Bode plots:

1. Take the Multisim Live circuit used in the **Simulate** section, and select the *AC Sweep* simulation option and the *Split* visualization option.
2. Double click on the voltage generator V_{in}, select the *AC analysis value* menu option, and set AC_mag = 0.1V
3. Double click on the voltage generator V_{dr}, select the *AC analysis value* menu option, and set AC_mag = 0V
4. Open the *Configuration Panel* and set Start freq. = 10Hz and Stop freq. = 1MHz
5. Double click on probes V_{in}, V_{dr}, I_{out} and uncheck the *Show plots* box
6. Run the simulation and watch the resulting AC Sweep plots.

The continuous line is the magnitude of the ratio V_{outAC}/V_{inAC}, while the dashed line is the phase shift between V_{outAC} and V_{inAC}, over the selected frequency range. These plots are the graphic visualization (Bode plots) of the Equations 1-6 provided in the **Theory and Background** section. You can repeat the simulation to generate the Bode plots of the ratio V_{outAC}/V_{drAC}, by exchanging the setup of V_{in} and V_{dr} generators and probes.

6-3   Resources for learning more

- This document provides the fundamentals of linear regulators:
  Linear Regulators: Theory of Operation and Compensation,
  http://www.ti.com/lit/an/snva020b/snva020b.pdf

Answer Key – Check Your Understanding Questions Only
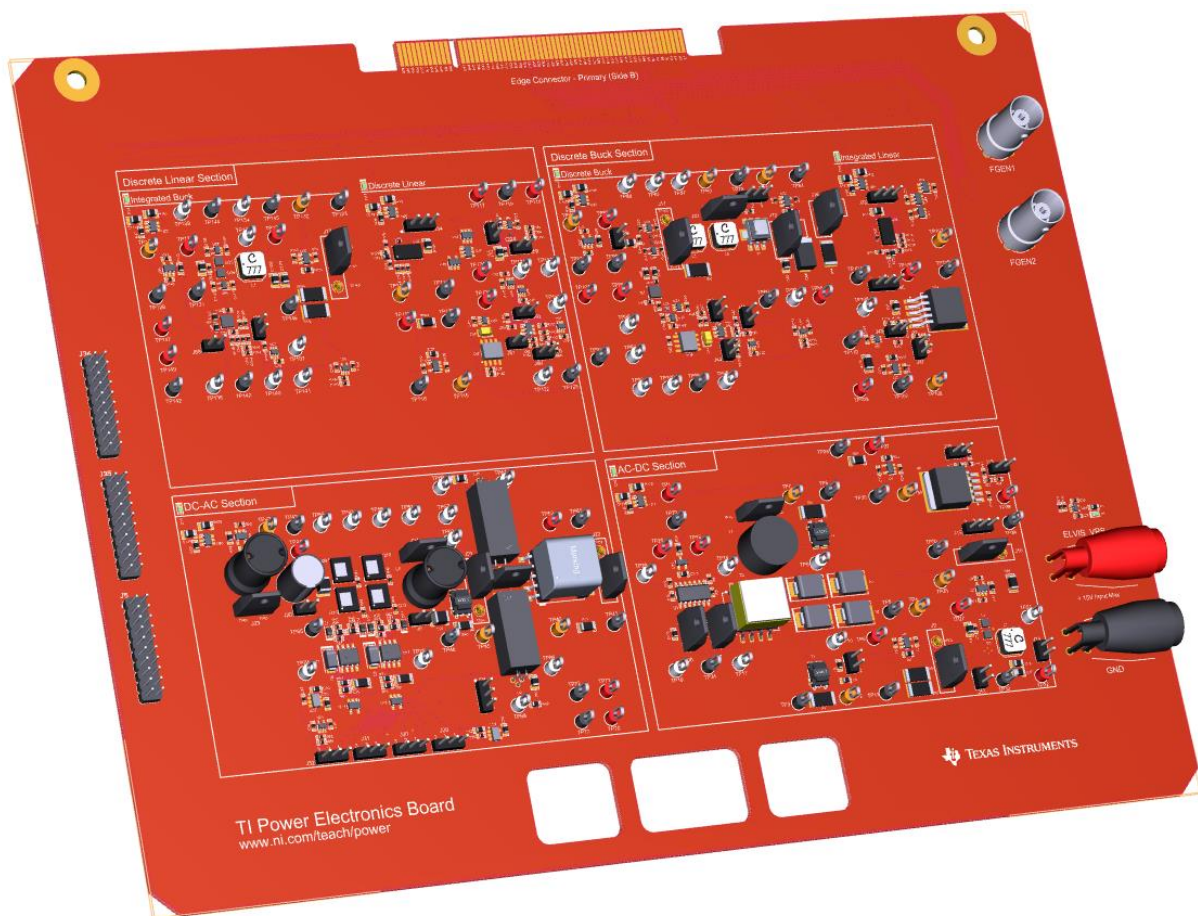
Check Your Understanding

1-1   C

1-2   B

1-3   B

1-4   A

1-5   B

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 3: Error Amplifier Operation

Lab 3: Error Amplifier Operation

The goal of this lab is to investigate the properties and the response of the error amplifier, which generates the MOSFET gate driver voltage in linear regulators. First, we will review the architecture and the simplified equations describing an error amplifier in DC and AC operation. Next, we will use the simplified error amplifier model to predict its AC gain. Then, we will simulate the response of the error amplifier to the perturbations of the output voltage with respect to the desired nominal value, in a linear regulator. Finally, we will perform experimental tests with a real error amplifier, and will compare the results of simulations and measurements to verify their consistency.
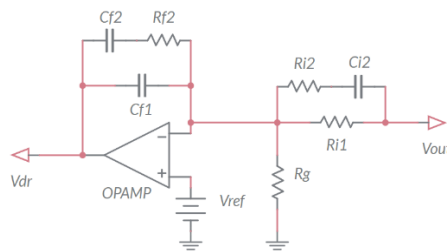
Figure 1-1. Error Amplifier.

Learning Objectives

After completing this lab, you should be able to complete the following activities.
1. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will calculate the magnitude of the error amplifier voltage determined by DC deviations and AC perturbations on the output voltage of the linear regulator, with specified units and decimal digits, by applying the appropriate theoretical formulae.
2. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will simulate the operation of the error amplifier to analyze the sensitivity of its voltage with respect to AC perturbations of the linear regulator output voltage, with specified units and decimal digits, to verify the consistency of theoretical predictions.
3. Given a real MOSFET operating as linear regulator, a DC power supply, a load resistor of given resistance, a function generator, and a real error amplifier, you will measure the DC and AC components of the error amplifier voltage determined by DC and AC perturbations of the linear regulator output voltage, with specified units and decimal digits, to verify the consistency of simulations and correct the model parameters.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

✓ Access Instruments
https://measurementslive.ni.com/
✓ View User Manual
http://www.ni.com/en-us/support/model.ni-elvis-iii.html
✓ View Tutorials
https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

✓ View User Manual
http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

✓ Access
https://www.multisim.com/
✓ View Tutorial
https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

✓ Download (Windows OS Only)
http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by means of Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations on simulations and experiments
- ✓ Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental equations used to analyze the DC and AC response of an error amplifier. The error amplifier is a fundamental part of linear regulators, as it drives the MOSFET gate voltage and regulates the output voltage.

1-2 Error Amplifier Architecture and Function

Figure 1-2 shows a linear regulator under open loop operation. The *error amplifier* consists of an operational amplifier (OPAMP), a voltage reference V_{ref}, and a group of capacitors $\{C_{f1}, C_{f2}, C_{i2}\}$ and resistors $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$. The function of the error amplifier is to sense the output voltage V_{out} and compare it to a desired DC nominal value $V_{outDC,nom}$, to generate a gate driver voltage V_{drEA} ensuring that $V_{out} = V_{outDC,nom}$. The capacitors $\{C_{f1}, C_{f2}, C_{i2}\}$ and the resistors $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$ determine the sensitivity of the error amplifier to the output voltage perturbations, and its capability to reject the effects of noise or undesired signals on the linear regulator output voltage.
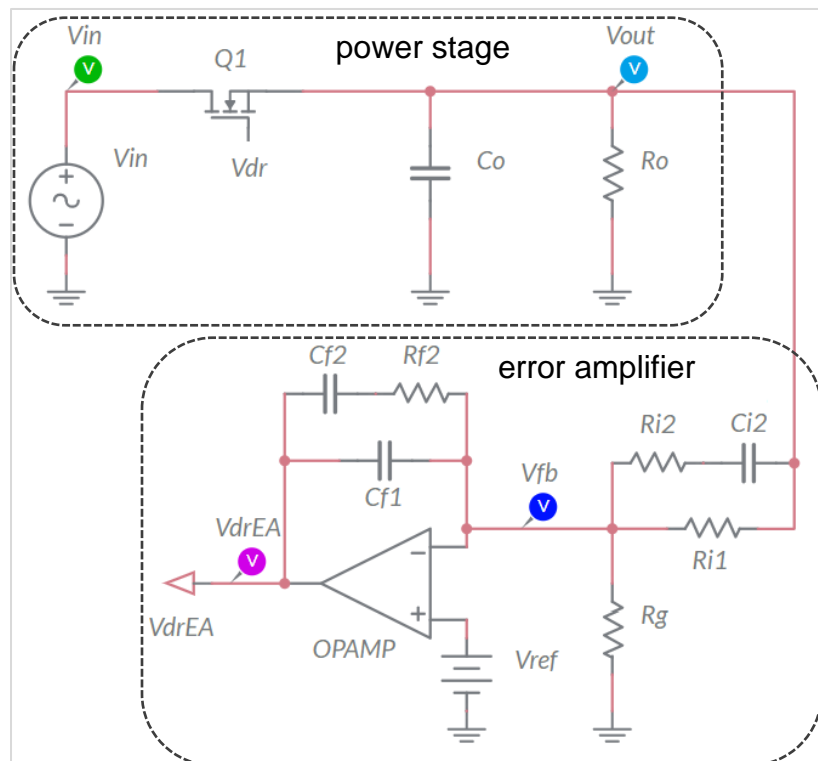
Figure 1-2. Error Amplifier in Open Loop Operation.

1-3 DC Analysis of the Error Amplifier

The MOSFET of the linear regulator shown in Figure 1-2 is driven by the generator V_{dr}. The DC output voltage V_{outDC} is determined by the DC source voltage V_{inDC} and by the DC gate driver voltage V_{drDC} (see **Lab1**). In DC steady-state operation, the capacitors C_{i2}, C_{f1} and C_{f2} are open, and the resistors R_g and R_{i1} form a *voltage divider sensor*, generating the feedback signal V_{fbDC}. If the OPAMP operates in its linear region, we have $V_{fbDC} \cong V_{ref}$, thus the DC output voltage fulfills Equation 1-1:

Equation 1-1
$$V_{outDC} = \left[1 + \frac{R_{i1}}{R_g}\right] V_{ref} = \frac{V_{ref}}{H}$$

where $H=R_g/(R_g+R_{i1})$. According to Equation 1-1, we can achieve a desired nominal DC output voltage $V_{outDC,nom} > V_{ref}$ with two resistances R_g and R_{i1} fulfilling Equation 1-2:

Equation 1-2
$$\frac{R_{i1}}{R_g} = \frac{V_{outDC,nom}}{V_{ref}} - 1$$

In DC operation, the error amplifier generates the MOSFET gate driver voltage $V_{drEA,DC}$ required to achieve the nominal value $V_{outDC,nom}$ (see **Lab1**):

Equation 1-3
$$V_{drDC,nom} = V_{th} + V_{outDC,nom} + \sqrt{\frac{2V_{outDC,nom}}{R_o \beta}}$$

If the DC output voltage deviates from the value $V_{outDC,nom}$, the error amplifier will generate a voltage given by

Equation 1-4
$$V_{drEA} = V_{drDC,nom} - G_{EA,DC}(V_{outDC} - V_{outDC,nom})$$

The coefficient $G_{EA,DC}$ is the error amplifier *open loop DC gain*. Based on Equation 1-4, if $V_{outDC} > V_{outDC,nom}$ the error amplifier decreases V_{drEA}, whereas if $V_{outDC} < V_{outDC,nom}$ the error amplifier increases V_{drEA}. We can achieve $V_{outDC} = V_{outDC,nom}$ only if $G_{EA,DC} = \infty$. In reality, $G_{EA,DC} = A_{dc}H$, where A_{dc} is the OPAMP DC open loop gain. An OPAMP with a higher DC open loop gain A_{dc} ensures a smaller steady-state error V_{outDC} - $V_{outDC,nom}$. The output voltage V_{dr} of the error amplifier is upper bounded by the OPAMP positive supply rail voltage V_{cc+}, and lower bounded by the negative supply rail voltage V_{cc-}. Therefore, Equation 1-4 is valid only if the OPAMP operates in the linear region, which happens when $V_{cc-} < A_{dc}H(V_{outDC,nom}$ - $V_{outDC}) < V_{cc+}$.

1-4 AC Analysis of the Error Amplifier

An AC perturbation $V_{inAC}sin(2\pi f \cdot t)$ injected on the source voltage generates an AC perturbation $V_{outAC}sin(2\pi f \cdot t + \varphi)$ on the output voltage (see **Lab2**). The error amplifier senses the output voltage AC perturbation and generates a signal $V_{drAC}sin(2\pi f \cdot t + \theta)$. The amplitude V_{drAC} depends on the amplitude V_{outAC} and frequency f of the AC output voltage perturbation. The AC gain $G_{EA,AC} = V_{drAC}/V_{outAC}$ of the error amplifier is given by:

Equation 1-5

$$G_{EA,AC} = \frac{V_{drAC}}{V_{outAC}} = \begin{cases} \dfrac{f_0}{f}\dfrac{1+f^2/f_Z^2}{1+f^2/f_P^2} & f > f_{LPF} \\ A_{dc}H & f < f_{LPF} \end{cases}$$

where $f_{LPF} = f_0/A_{dc}$. The pole frequencies f_0, f_P and the zero frequency f_Z influence the sensitivity of the error amplifier with respect to output voltage AC perturbations, and impact the stability of the regulator. They are set by means of the capacitors $\{C_{f1},C_{f2},C_{i2}\}$, and the resistors $\{R_g,R_{i1},R_{i2},R_{f2}\}$. Equation 1-5 highlights that the parameters f_0, f_P and f_Z are not influential on the error amplifier sensitivity at very low frequency. Normally, $f_Z < f_P$, and Equation 1-5 can be simplified as follows:

Equation 1-6

$$\frac{V_{drAC}}{V_{outAC}} \cong \begin{cases} [f<f_{LPF}] & [f_{LPF}<f<f_Z] & [f_Z<f<f_P] & [f>f_P] \\ A_{dc}H & \dfrac{f_0}{f} & \dfrac{f_0 f}{f_Z^2} & \dfrac{f_0 f_P^2}{f_Z^2 f} \end{cases}$$

The frequency f_0 determines the sensitivity of the error amplifier. A higher f_0 expands the range of frequency where the error amplifier is more sensitive to the output voltage AC perturbations. For the error amplifier shown in Figure 1-1 (known as *Type III* error amplifier) $f_0 =1/(R_{i1}(C_{f1}+C_{f2}))$. The sensitivity of the error amplifier decreases as the frequency f of the AC perturbation increases, except in the frequency range $[f_Z,f_P]$. The ratio f_P/f_Z is fixed based on *stability* requirements, and it is typically higher if f_0 is higher. The phase θ of the error amplifier output voltage $V_{drAC}sin(2\pi f \cdot t + \theta)$ is correlated to the phase φ of the linear regulator output voltage $V_{outAC}sin(2\pi f \cdot t + \varphi)$ by Equation 1-7:

Equation 1-7

$$\theta - \varphi = \begin{cases} -180° + 2\left[\arctan(f/f_Z) - \arctan(f/f_P)\right] - 90° & f > f_{LPF} \\ -180° & f < f_{LPF} \end{cases}$$

Based on Equations 1-5 and 1-7, if $f < f_{LPF}$ we have an *inverting error amplifier* with a very high gain, whereas if $f > f_{LPF}$ the gain decreases and the error amplifier voltage is expected to be delayed 270° with respect to the output voltage perturbation, except for $0.3f_Z<f<3f_P$.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What are the error amplifier parameters determining the nominal DC output voltage of a linear regulator?
    A. the frequencies of zero and poles
    B. the source voltage of the regulator
    C. the reference voltage and the resistors of the voltage divider sensor

1-2 What parameter of the OPAMP determines the magnitude of the linear regulator output voltage DC error?
    A. the DC open loop gain
    B. the positive supply voltage
    C. the low frequency pole

1-3 What is the amplitude of the error amplifier AC voltage correlated to the frequency of the linear regulator AC output voltage perturbations?
    A. it is not correlated
    B. it increases as the frequency increases
    C. it decreases as the frequency increases

1-4 What parameter of the error amplifier majorly impacts its sensitivity with respect to the linear regulator AC output voltage perturbations?
    A. the frequency of zero f_Z
    B. the frequency of pole f_0
    C. the reverence voltage V_{ref}

1-5 Based on your answer to Question 1-4, say what actions you would make to improve the sensitivity of the error amplifier:

_____

_____

_____

_____

2 Exercise

The error amplifier of the **Discrete Linear Section** in the TI Power Electronics Board for NI ELVIS III uses the TI's OPA835IDBVR OPAMP) and has the following nominal parameters (http://www.ti.com/lit/ds/symlink/opa835.pdf):

- $A_{dc}=10^6$, $V_{cc+}=5.5V$, $V_{cc-}=0V$.
- $R_g=26.1k\Omega$, $R_{i1}=39.2k\Omega$, $V_{ref}=1.024V$.
- $f_0 = 3.28kHz$, $f_Z = 5.44kHz$, $f_P = 172.95kHz$, $f_{LPF} = 3.28mHz$.

2-1 Given the parameters of the error amplifier, calculate the expected nominal value of the DC output voltage $V_{outDC,nom}$:

$V_{outDC,nom}$ = _____

2-2 What are the values of resistances R_g and R_{i1} required to achieve a nominal DC output voltage $V_{outDC,nom} = 3.3V$?

Given $R_g=26.1k\Omega$, $R_{i1,nominal}$ = _____

Given $R_{i1}=39.2k\Omega$, $R_{g,nominal}$ = _____

2-3 You have an AC perturbation $V_{outAC}sin(2\pi f\cdot t)$ on the output voltage of the linear regulator, which has an amplitude $V_{outAC} = 10mV$ and frequency f listed in Table 2-1. Calculate the ratio V_{drAC}/V_{outAC} and the expected value of the amplitude V_{drAC}, in milli Volts with one decimal digit, of the AC voltage $V_{drAC}sin(2\pi f\cdot t+\theta)$ generated by the error amplifier.

Table 1-1 Analysis of error amplifier voltage in AC operation.

f [Hz]	1	10	100	1000	10000	100000
V_{drAC}/V_{outAC}						
V_{drAC} [mV]						

2-4 Is the OPAMP able to generate all the V_{drAC} values you have collected in Table 2-1?

    A.   yes
    B.   no
    if your answer is B, when? why?: _____

_____

_____

3 Simulate

The simulations you will perform in this section will allow you to analyze the open loop behavior of an error amplifier. First, you will observe the voltage generated by the error amplifier, under different conditions determined by the deviations of the linear regulator output voltage with respect to the desired nominal value. Then, you will compare the results of the simulations with the results of calculations performed in the **Exercise** section, to verify the consistency of theoretical calculations and simulations.

3.1 Simulation 1: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path:
   https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/.
   The circuit is shown in Figure 3-1.
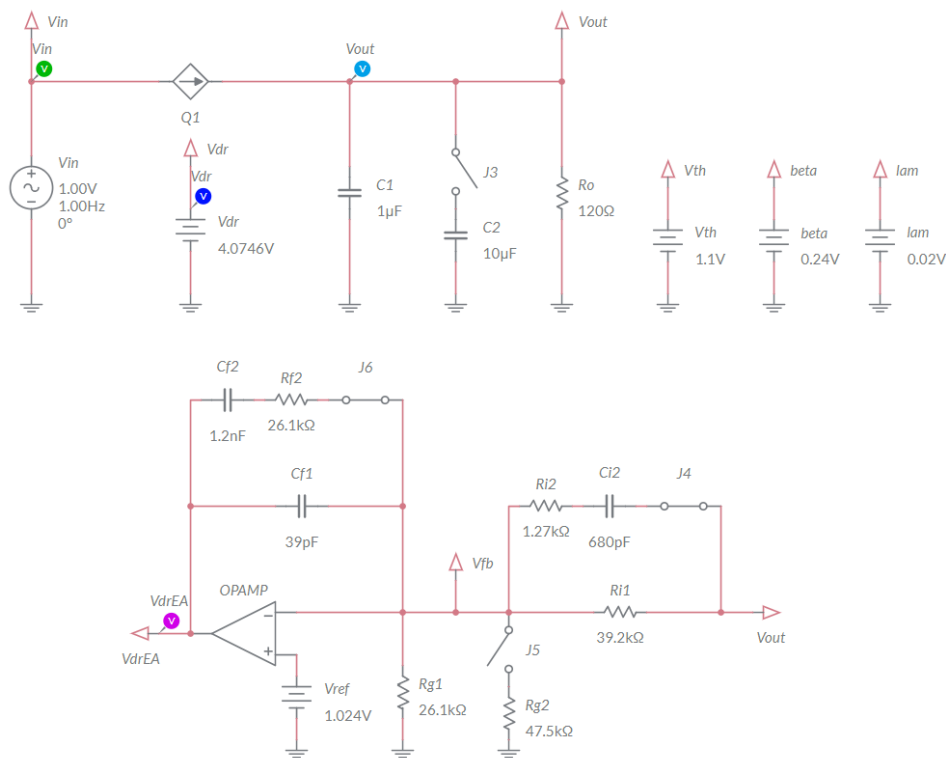
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Error Amplifier Operation.

In this simulation, you will observe the response of the error amplifier to deviations of the output voltage of the linear regulator with respect to the nominal value. For this

purpose, the error amplifier voltage V_{drEA} is not used directly as gate driver voltage. The generator V_{dr} is used indeed to set the desired DC output voltage V_{outDC} (see **Lab1**). Injecting an AC perturbation $V_{inAC}sin(2\pi f{\cdot}t)$ on source voltage V_{in} generates an AC perturbation $V_{outAC}sin(2\pi f{\cdot}t+\varphi)$ on the output voltage (see **Lab2**).The auxiliary generators Vth, *beta* and *lam* allow to set the MOSFET parameters $\{V_{th},\ \beta,\ \lambda\}$, respectively. The parameters $\{VA,\ Freq,\ VO\}$ of generators V_{in} and V_{dr} correspond to the parameters $\{V_{inAC},\ f,\ V_{inDC}\}$, and $\{V_{drAC},\ f,\ V_{drDC}\}$, respectively, as defined in the **Theory and Background** section. The capacitors $\{C_{f1},C_{f2},C_{i2}\}$, and the resistors $\{R_{g},R_{i1},R_{i2},R_{f2}\}$ are set so that the resulting error amplifier zero and poles are approximately f_0 = 3.28kHz, f_Z = 5.44kHz, f_P = 172.95kHz. The OPAMP parameters are $A_{dc}=10^6$, f_{OPAMP} = 30Hz, V_{cc+}=5.5V, V_{cc-}=0V.

2. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED in the simulation schematic.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Instantaneous* option box for voltage probes V_{in}, V_{out}, and V_{drEA} in the *Measurement labels* menu.
6. Calculate the nominal value $V_{outDC,nom}$ in Volts with three decimal digits, and report the result in Table 3-1.
7. Set *VA*=0, *Freq*=100Hz, *VO*=5V for the generator V_{in}, and *DC_mag* = 4.05V for the generator V_{dr}.
8. For each value of *DC_mag* of the DC voltage generator V_{dr} listed in Table 3-1, run the simulation, read the measurements of voltage probes V_{out} and V_{drEA} in Volts with three decimal digits and report the results in Table 3-1.

Table 3-1 Error Amplifier voltage as function of linear regulator output voltage V_{out}.

V_{drDC} (DC_mag) [V]	4.050	4.060	4.070	4.080	4.090	4.100
$V_{outDC,nom}$ [V]						
V_{outDC} [V]						
V_{outDC} - $V_{outDC,nom}$ [V]						
V_{drEA} [V]						

3-1-1 How does the error V_{outDC} - $V_{outDC,nom}$ vary as V_{dr} increases?

      A.   it increases
      B.   it decreases
      other: _____

_____

3-1-2 How does the error amplifier voltage V_{drEA} vary as V_{dr} increases?

      A.   it increases
      B.   it decreases
      other: _____

_____

3-1-3 Discuss the results of the error amplifier voltage V_{drEA}, based on the equations and relevant comments provided in the **Theory and Background** section:

_____

_____

_____

3-1-4 Set the values of the auxiliary generators $Vth = 1.35$, *beta* $= 0.33$ and *lam* $= 0.05$ in the circuit schematic, run the simulation and find the threshold value of V_{drDC} determining the transition of the error amplifier voltage V_{drEA} from V_{cc+} to V_{cc-}. Is this value greater or smaller than the threshold value of V_{drDC} from the Table 3-1?

      A.   greater
      B.   smaller
      why?: _____

_____

3.2 Simulation 2: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path:
2. Set the switches J3 and J5 OPEN, and the switches J4 and J6 to be CLOSED.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Periodic* option box for voltage probes V_{in}, V_{out}, and V_{drEA} in the *Measurement labels* menu.
6. Set *VA*=1V, *Freq*=1Hz, *VO*=5V for the generator V_{in}, and *DC_mag* = 4.0746V for the generator V_{dr} and run the simulation.
7. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{out} voltage probe and report the values of $V_{outDC} = V_{AV}$ (in Volts with three decimal digits) and V_{outAC} (in milli Volts with three decimal digits) in Table 3-2
8. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{drEA} voltage probe and report the values of $V_{drEA,DC} = V_{AV}$ (in Volts with three decimal digits) and $V_{drEA,AC}$ (in milli Volts with three decimal digits) in Table 3-2
9. Repeat steps 7-8 under V_{in} frequency and amplitude listed in Table 3-2.
10. Import in Table 3-2 the values of V_{drAC}/V_{outAC} recorded in Table 2-1 of **Exercise** section, for the corresponding frequencies.

Table 3-2 Error Amplifier response with C_o=1μF.

f [Hz] (V_{in} Freq)	1	10	100	1000	10000	100000
V_{inAC} [V] (V_{in} VA)	0.5	1	1	1	1	1
V_{drDC} [V] (V_{dr} DC_mag)	4.0746					
ML Simulation Max. Time Step	1e-5	1e-5	1e-5	1e-6	1e-7	1e-8
ML Grapher Horizontal Axis	500ms/div	50ms/div	5ms/div	500us/div	50us/div	5us/div
$V_{outDC,nom}$ [V]						
V_{outDC} [V]						
V_{outAC} [mV]						
$V_{drEA,DC}$ [V]						
$V_{drEA,AC}$ [mV]						
$V_{drEA,AC}/V_{outAC}$						
V_{drAC}/V_{outAC} from Table 2-1						

3-2-1 Do the values of $V_{drEA,AC}$ obtained with simulations show the same trend of V_{drAC} results obtained with calculations?

    A.   yes

    B.   no

    if your answer is B, highlight and discuss the differences: _____

_____

_____

3-2-2 How does the ratio V_{drAC}/V_{outAC} vary with the frequency?

    A.   it increases

    B.   it decreases

    C.   other

    if your answer is C, describe and discuss what you observe: _____

_____

_____

3-2-3 Should the error amplifier exhibit a different ratio V_{drAC}/V_{outAC} if the MOSFET parameters V_{th}, β and λ are changed?

    A.   yes

    B.   no

    why?: _____

_____

If you are not able to answer Question 3-2-3, change the value of the generators *Vth*, *lam* and *beta* in the circuit schematic and run the simulation. Analyze the results, read the **Theory and Background** section and then answer the question.

Troubleshooting tips:
- If the simulation does not run and you get some error message, reload *Lab3 – Error Amplifier Operation* from this file path: https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/ and restart the simulation, following the instructions.

4 Implement

The experiments of this section allow you to observe the behavior of a real error amplifier, and to verify the response of the error amplifier to DC and AC deviations of the output voltage of a linear regulator with respect to the desired nominal value. You will compare the experimental measurements with simulations, to verify their consistency and determine possible adjustments of MOSFET model parameters to improve the accuracy of simulations. The experiments are performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1, which uses the TI's CSD15380F3 MOSFET (pass device) and OPA835IDBVR OPAMP (error amplifier). The linear regulator is powered by a TI's TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage. The AC disturbance on the output voltage of the Discrete Linear regulator is generated by applying an AC signal to the linear regulator gate driver voltage. The error amplifier pole frequency f_0 is 3.3kHz when jumpers J60 and J62 are shorted, and 104kHz when jumpers J60 and J62 are open. The output capacitance C_o is 1µF with jumper J59 open, and 11µF with jumper J59 shorted. The nominal output voltage of the linear regulator is set at 2.5V with jumper J61 open, and at 3.3V with jumper J61 shorted.

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Error Amplifier Operation

TI's devices datasheets are available at the following links:

CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
TPS40303DRCR Buck Regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 General Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab3 – Error Amplifier Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect the instruments as indicated in Table 4-2.

Table 4-1 Jumpers setup

J17	J34	J58	J59	J60	J61	J62	J68	J69
short TP148-TP163	short 2-3	open	open	short	open	short	short	open

Table 4-2 Instruments connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP117 (input voltage V_{in}) connect CH-2 to TP118 (output voltage V_{out}) connect CH-3 to TP121 (gate driver voltage V_{dr}) connect CH-4 to TP123 (error amplifier voltage V_{drEA})
Function Generator	connect Ch-2 to FGEN2 BNC connector ($\rightarrow$TP121 = gate driver voltage V_{dr})

4-2 Experiment 1: Instructions

1. Use the instruments configuration and setup shown in Table 4-2-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-2-1 Instruments initial configuration and setup

Power Supply	CH "+": Static, 7.00V, CH "-": Inactive				
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 100us/div	*Acquisition*: average	*Measurements*: show	*Probe Attenuation*: 10x
	CH-1: ON • DC coupling • 2V/div • offset 0V	*CH-2*: ON • DC coupling • 20mV/div • offset -2.55V		*CH-3*: ON • DC coupling • 20mV/div • offset -4.35V	*CH-4*: ON • DC coupling • 2V/div • offset 0V
Function Generator	CH-1: Inactive CH-2: Sine, DC offset 3.9V, Amplitude 0mV, Frequency 1kHz				

3. Using horizontal cursors in Manual mode, read the average DC values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-2-2.

Table 4-2-2 Error Amplifier voltage as function of linear regulator output voltage V_{out}.

V_{drDC} [V] (Function Generator CH2 DC offset)	3.90	4.00	4.10	4.20	4.30	4.40
$V_{outDC,nom}$ [V]						
V_{dr} [V]						
V_{out} [V]						
V_{drEA} [V]						

4. Repeat the measurement for all the values of the driver voltage V_{drDC} indicated in Table 4-2-2, by changing the DC offset of *Function Generator* CH-2.
5. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-2-1 Do you observe a transition in the measured values of V_{drEA} from V_{cc+} to V_{cc-} like the one you have observed with the simulations?

A.   yes
B.   no
what is you comment? _____

_____

4-2-2 If your answer to Question 4-2-1 is A, does the threshold value of the gate driver voltage V_{dr} determine the transition of V_{drEA} of V_{drEA} from V_{cc+} to V_{cc-} the same you have observed with the simulations?

    A.   yes
    B.   no
    what is you comment? _____

_____

4-2-3 Based on your answer to Question 4-2-2, what parameter of the MOSFET model would you change to improve the accuracy of simulations? How and why?

    A. V_{th}: _____

    B. β: _____

    C. λ: _____

4-2-4 Run again the simulation by changing the parameters of MOSFET model and verify your predictions based on your answers to Question 4-2-3. Are the new simulation results closer to experimental ones? Do you infer a rule or a procedure to obtain the parameters of a MOSFET from experimental measurements?

_____

_____

_____

_____

4-3 Experiment 2: Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* and use the instruments configuration and setup shown in Table 4-3-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-3-1 Instruments initial configuration and setup

Power Supply	CH "+": Static, 7.00V, CH "-": Inactive				
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 200ms/div	*Acquisition*: average	*Measurements*: show	*Probe Attenuation*: 10x
	CH-1: ON • DC coupling • 1V/div • offset -4V	CH-2: ON • DC coupling • 10mV/div • offset -2.55V	CH-3: ON • DC coupling • 10mV/div • offset -4.175V	CH-4: ON • DC coupling • 1V/div • offset -3.5V	
Function Generator	CH-1: Inactive CH-2: Sine, DC offset 4.175V, Amplitude 20mV, Frequency 1Hz				

3. Using horizontal cursors in Manual mode, read the DC average values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-3-2.
4. Using cursors in Track mode, read the peak-peak values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, calculate the ratio $V_{drEA,AC}/V_{outAC}$, and report the values in Table 4-3-2.

Table 4-3-2 Error Amplifier response.

f [Hz] (FG CH-2 Frequency)	1	10	100	1000	10000	100000
suggested oscilloscope time/division	200ms/div	20ms/div	2ms/div	200µs/div	20µs/div	2µs/div
suggested oscilloscope CH-4 volt/division	1V/div	1V/div	100mV/div	10mV/div	10mV/div	10mV/div
suggested oscilloscope CH-4 offset	-3.5V	-3.5V	-5.54V	-5.54V	-5.54V	-5.54V
V_{drDC} [V] (FG CH-2 DC offset)	4.175	4.182	4.182	4.182	4.175	4.175
V_{drACpp} [mV] (FG CH-2 Amplitude)	20	20	20	20	20	20
V_{drACpp} [mV] (Scope CH-3 Volts pk-pk)						
$V_{outDC,nom}$ [V]						
V_{outDC} [V] (Scope CH-2 Average)						
$V_{outACpp}$ [mV] (Scope CH-2 Volts pk-pk)						
$V_{drEA,DC}$ [V] (Scope CH-4 Average)						
$V_{drEA,ACpp}$ [mV] (Scope CH-4 Volts pk-pk)						
$V_{drEA,ACpp}/V_{outACpp}$						
V_{drAC}/V_{outAC} from Table 3-2 (simulations)						

5. Repeat the measurement for all the values of Frequency, DC Offset and Amplitude of the driver voltage V_{dr} shown in Table 4-3-2, by changing the setup of *Function Generator* CH-2. [**Notes: 1)** if you don't see the CH-4 trace in the scope frame, decrease the DC offset V_{drDC}, with respect to the values shown in Table 4-3-2, in steps of -1mV, until the CH-4 sets in the frame; **2)** while measuring peak-peak voltage values, do not consider the high-frequency noise appearing as a rapid up-and-down swinging signal around the main sinusoidal waveform].
6. Enter in Table 4-3-2 the V_{drAC}/V_{outAC} values collected in Table 3-2.
7. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-3-1 Do you observe the same trend in the measured and simulated ratio V_{outAC}/V_{inAC} as the frequency increases?

    A.   yes
    B.   no
    if your answer is B, why? _____

_____

4-3-2 Should the error amplifier exhibit a different ratio V_{drAC}/V_{outAC} with $C_o = 11\mu F$?

    A.   yes
    B.   no
    why?: _____

_____

_____

Troubleshooting tips:
- If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

5 Analyze

5-1 Using the results collected in Table 4-3-2, calculate the ratios $G_{dr} = V_{outAC}/V_{drAC}$, $G_{EA} = V_{drEA,AC}/V_{outAC}$ and $T_{loop} = G_{EA}G_{dr} = V_{drEA,AC}/V_{drAC}$, report the results in Table 5-1, and graph the values of ratios G_{dr}, G_{EA} and T_{loop} as a function of the frequency f using a logarithmic scale for the horizontal axis and decibel scale for the vertical axis, including a legend that indicates which line style corresponds to which series (calculations, measurements).

Table 5-1 Error Amplifier response.

f [Hz]	1	10	100	1000	10000	100000
$G_{dr} = V_{outAC}/V_{drAC}$						
$G_{EA} = V_{drEA,AC}/V_{outAC}$						
$T_{loop} = V_{drEA,AC}/V_{drAC}$						
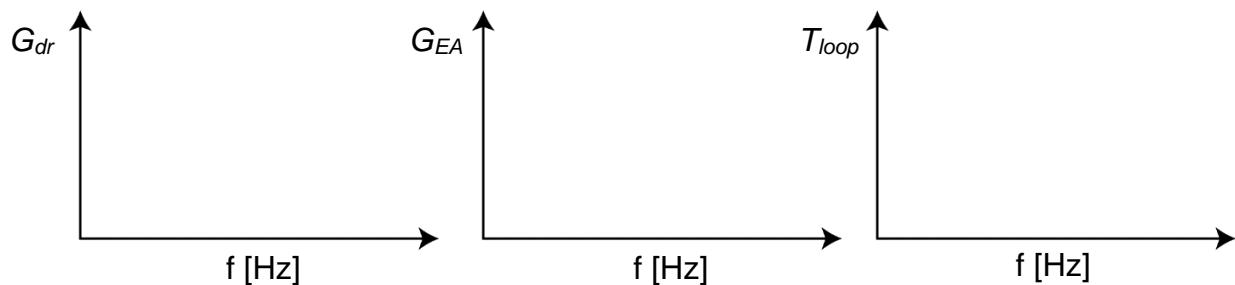
Figure 5-1 Calculated and measured values of ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} obtained while varying the frequency, with the MOSFET operating in the saturation region

The ratio G_{dr} is the open loop *control-to-output* gain of the linear regulator, which expresses the sensitivity of the output voltage with respect to the gate driver voltage perturbations (see **Lab2**). The ratio G_{EA} is the gain of the error amplifier, which expresses the sensitivity of the error amplifier voltage with respect to the output voltage perturbations (see **Theory and Background** section). The ratio T_{loop} is the loop gain of the linear regulator, which expresses the global sensitivity of the linear regulator to AC perturbations. A higher value of the loop gain involves a higher reactivity of the linear regulator to disturbances, which results in a more effective suppression of the disturbances and in a better output voltage regulation capability.

5-2   Based on the loop gain plot T_{loop} you have plotted in Figure 5-1, for what of the frequency values is the linear regulator better suppressing the disturbance effects?

A.   60Hz

B.   6kHz

C.   60kHz

5-3   Based on your observations and on the equations provided in the **Theory and Background** section, how would you modify the parameters f_0, f_Z, f_P and A_{dc} of the error amplifier to improve the disturbance suppression capability of the linear regulator?

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the AC response of the error amplifier of a linear regulator, regarding its sensitivity with respect to output voltage AC perturbations. Discuss the parameters influencing the AC response of the error amplifier, in what frequency range is it important to have a high error amplifier gain, why, and how you can achieve it.

6-2   Expansion Activities

6-2-1. Using the Multisim Live schematic of Figure 3-1, determine the frequency response of the linear regulator and of the error amplifier, by means of the *AC Sweep* option:
   a. Set the switches J4 and J6 to be closed.
   b. Replace the V_{dr} DC generator with an AC generator and set VO=4.0746V, Freq=1Hz, VA=0.1V.
   c. Set AC_mag = 0.1V in the *AC analysis value* menu option of the voltage generator V_{dr}.
   d. Set AC_mag = 0 V in the *AC analysis value* menu option of the voltage generator V_{in}.
   e. Set Start freq. = 1Hz and Stop freq. = 1MHz in the *Configuration Panel*.
   f. Set *Show plots* box unchecked on probe V_{in}.
   g. Run the simulation and watch the resulting AC Sweep plots (Bode plots). The continuous lines are the magnitudes of the ratios $G_{dr} = V_{outAC}/V_{drAC}$, $T_{loop} = G_{EA}G_{dr} = V_{drEA,AC}/V_{drAC}$, while the dashed line is the phase shift between V_{outAC} and $V_{drEA,AC}$ with respect to V_{drAC} over the selected frequency range.
   h. Verify that the plots follow the trend of results of Tables 3-2, 4-3-2 and 5-1.

6-2-2. Observe the behavior of an error amplifier with a higher gain, using the circuit schematic of Figure 3-1.

a. Open the switches J4 and J6. The resulting gain of the error amplifier will be:

Equation 6-2-1

$$G_{EA} = \frac{V_{drAC}}{V_{outAC}} = \begin{cases} \dfrac{f_0}{f} & f > f_{LPF} \\ A_{dc}H & f < f_{LPF} \end{cases}$$

The pole frequency f_0 of the error amplifier is now given by $f_0 = 1/(R_{i1}C_{f1}) = 104$kHz (*Type I* error amplifier), and consequently $f_{LPF} = 10.4$Hz.

b. Open switches J4 and J6.
c. Repeat the simulations in the test conditions listed in Table 3-2 (use *VA*=100mV with *Freq* = 1Hz, 10Hz, 100Hz, for generator V_{in}).
d. Compare and discuss the results of simulations obtained with the two different error amplifier setup.

6-2-1. Verify experimentally the effect of a higher error amplifier gain

a. Open the jumpers J60 and J62 in the **Discrete Linear Section** of TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
b. Test the regulator with Frequency = 10kHz, Amplitude = 30mVpp and DC offset = 4.328V on *Function Generator* CH-2, set the *Oscilloscope* CH-4 with AC coupling, 500mV/div, 0V offset, 50us/div.
c. Compare the error amplifier gain with the corresponding result reported in Table 4-3-2.

6-3   Resources for learning more

● This book provides the fundamentals of linear regulators control:
C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   C

1-2   A

1-3   C

1-4   B

1-5   Increase f_0, increase A_{dc}

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 4: Linear Regulator

in Closed Loop Operation

Lab 4: Linear Regulator in Closed Loop Operation

The goal of this lab is to analyze the closed loop operation of a linear regulator. We investigate the impact of the loop gain on the ability to reject noise and changes in the output voltage, which is the most important feature of linear regulators. First, we will review the principle of operation and the simplified model of a closed loop linear regulator. Next, we will use the simplified model to predict its response to AC perturbations and its accuracy to the reference signal. Then, we will simulate the linear regulator in DC and AC operation to evaluate the impact of the MOSFET and error amplifier parameters. Finally, we will perform experimental tests with a real linear regulator, and will compare the results of simulations and measurements to verify their consistency.
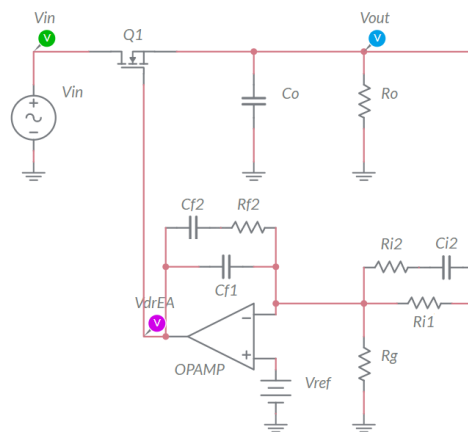
Figure 1-1. Closed Loop Linear Regulator.

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a linear regulator and its MOSFET and error amplifier characteristics, you will calculate the DC operating point and the AC response to input and reference voltage perturbations, with specified units and accuracy, by applying the appropriate theoretical formulae.

2. Given a linear regulator and its MOSFET and error amplifier characteristics, you will simulate the DC and AC operation with different error amplifier configurations, to determine the accuracy of theoretical model predictions, by comparing the appropriate sets of data and results

3. Given a real linear regulator, a dynamic power supply, and a function generator, you will measure the accuracy of the DC output voltage with respect to the desired nominal value, you will determine the AC response of the linear regulator, and you will determine the elements influencing the accuracy of simulations, by comparing the appropriate sets of data and results.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

✓ Access Instruments
https://measurementslive.ni.com/
✓ View User Manual
http://www.ni.com/en-us/support/model.ni-elvis-iii.html
✓ View Tutorials
https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

✓ View User Manual
http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

✓ Access
https://www.multisim.com/
✓ View Tutorial
https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

✓ Download (Windows OS Only)
http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by means of Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations on simulations and experiments
- ✓ Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental concepts and equations of a linear regulator in closed loop operation. We will discuss the impact of OPAMP and error amplifier characteristics on DC offset error and the noise rejection capability of the linear regulator.

1-2 Feedback Action of the Error Amplifier.

Figure 1-2 shows a linear regulator in closed loop operation. The error amplifier consists of the OPAMP, the voltage reference V_{ref}, the capacitors $\{C_{f1}, C_{f2}, C_{i2}\}$, and the resistors $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$. The error amplifier compares the output voltage V_{out} to the desired DC nominal value $V_{outDC,nom}$, and generates the gate driver voltage V_{drEA} ensuring that $V_{out} = V_{outDC,nom}$. Thanks to the error amplifier, the linear regulator is able to reject the AC noise, thus ensuring a well regulated low-noise output voltage, which is the most important feature of linear regulators. The components $\{C_{f1}, C_{f2}, C_{i2}\}$ and $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$ set the poles and zeros of the error amplifier, and determine its sensitivity to noise.
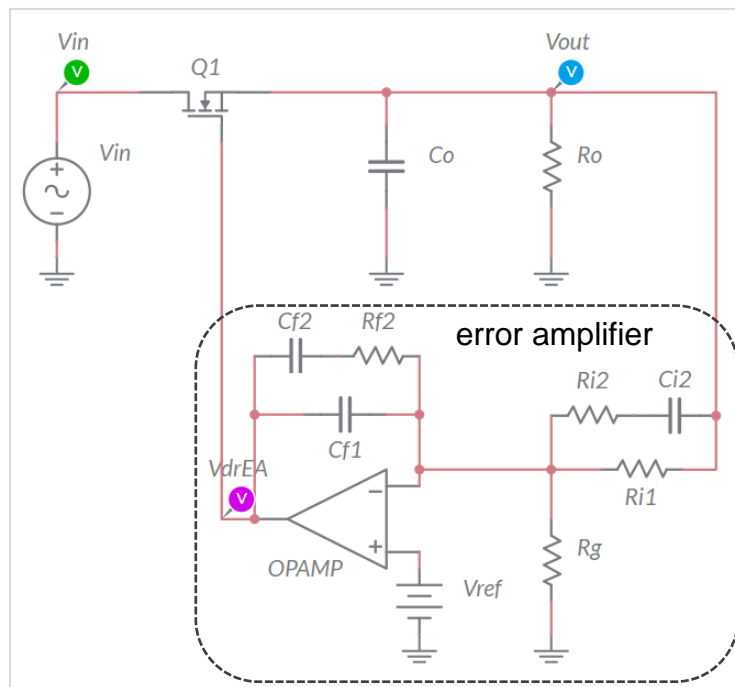
Figure 1-2. Linear Regulator in Closed Loop Operation.

1-3 Closed Loop DC Analysis of the Linear Regulator

The DC output voltage V_{outDC} of a linear regulator is determined by the DC source voltage V_{inDC} and by the DC gate driver voltage V_{drDC}. The MOSFET of a linear regulator normally operates in the saturation region, where we have:

Equation 1-3-1
$$V_{drDC} = V_{th} + V_{outDC} + \sqrt{\frac{2V_{outDC}}{R_o\beta(1+\lambda(V_{inDC}-V_{outDC}))}} \cong V_{th} + V_{outDC} + \sqrt{\frac{2V_{outDC}}{R_o\beta}}$$

V_{th}, β and λ are the MOSFET gate-to-source threshold voltage, transconductance and channel-length-modulation coefficient, respectively. The DC error amplifier voltage is:

Equation 1-3-2
$$V_{drDC} = A_{dc}(V_{ref} - V_{outDC}H)$$

where A_{dc} is the error amplifier DC gain and $H=(1+R_{i1}/R_g)^{-1}$ is the voltage sensor gain. Combining Equations 1-3-1 and 1-3-2 provides the linear regulator DC output voltage:

Equation 1-3-3
$$V_{outDC} \cong \frac{1}{(1+A_{dc}H)}\left[\sqrt{\frac{1}{2R_o\beta}+(A_{dc}V_{ref}-V_{th})(1+A_{dc}H)} - \frac{1}{\sqrt{2R_o\beta}}\right]$$

As the open loop DC gain A_{dc} of the OPAMP is normally very high (from 10^3 to 10^6), Equation 1-3-3 can be simplified as shown in Equation 1-3-4:

Equation 1-3-4
$$V_{outDC} \cong \frac{A_{dc}V_{ref}}{1+A_{dc}H}$$

An unlimited DC gain $A_{dc} = \infty$ would determine an output voltage V_{outDC} equal to:

Equation 1-3-5
$$V_{outDC,nom} = \frac{V_{ref}}{H}$$

Equations 1-3-4 and 1-3-5 highlight that the tolerance of V_{ref}, R_g and R_{i1} influence the output voltage nominal value $V_{outDC,nom}$. Based on Equations 1-3-4 and 1-3-5, the output voltage offset error of a linear regulator is given by Equation 1-6:

Equation 1-3-6
$$ERR_{DC} \cong \frac{A_{dc}V_{ref}}{1+A_{dc}H} - \frac{V_{ref}}{H}$$

1-4 Closed Loop AC Analysis of the Linear Regulator

The ratio between the amplitude of the AC perturbations on the output voltage of a linear regulator and the AC perturbations on the source voltage and gate driver voltage in open loop operation is given by Equation 1-4-1 (see **Lab2**):

Equations 1-4-1
$$\left.\frac{V_{outAC}}{V_{inAC}}\right|_{V_{drAC}=0} = G_{in} = \frac{\lambda \beta T_{dr}^2}{4\pi C_o \sqrt{f^2 + f_t^2}} \quad ; \quad \left.\frac{V_{outAC}}{V_{drAC}}\right|_{V_{inAC}=0} = G_{dr} = \frac{\beta T_{dr}}{2\pi C_o \sqrt{f^2 + f_t^2}}$$

$$T_{dr} = \sqrt{\frac{2\beta V_{outDC}}{R_o}} \, ; \qquad f_t = \frac{1 + T_{dr} R_o}{2\pi R_o C_o}$$

where λ is the MOSFET channel-modulation coefficient. The corner frequency f_t is the open loop bandwidth of the linear regulator. The error amplifier AC gain $G_{EA,AC}$ = V_{drAC}/V_{outAC} is given by the simplified Equation 1-4-2 (see **Lab3**):

Equation 1-4-2
$$G_{EA,AC} = \frac{V_{drAC}}{V_{outAC}} \cong \begin{cases} \dfrac{f_0}{f} & \dfrac{f_0}{A_{dc}} < f < f_0 \\[2ex] A_{dc} H & f < \dfrac{f_0}{A_{dc}} \end{cases}$$

Equation 1-4-2 highlights that a higher pole frequency f_0 increases the error amplifier sensitivity with respect to output voltage AC perturbations. Combining Equations 1-4-1 and 1-4-2 results in the simplified closed loop Equation 1-4-3:

Equation 1-4-3
$$G_{in,CL} = \frac{V_{outAC}}{V_{inAC}} \cong \frac{G_{in}}{G_{EA,AC} G_{dr}} = \frac{G_{in}}{T_{loop}} \qquad (\textit{valid for } f < f_0)$$

where T_{loop} = $G_{EA,AC} G_{dr}$ is the loop gain of the linear regulator, and the $G_{in,CL}$ gain expresses the noise rejection capability of the linear regulator. The inverse of $G_{in,CL}$ is the *Power Supply Rejection Ratio* (*PSRR*). From Equation 1-4-1 we see that the magnitude of the control-to-output gain G_{dr} is determined by the DC operating point, the MOSFET parameters, the load R_o and the capacitor C_o, and it is flat for frequency $f < f_t$. This results in a poor open loop noise rejection capability of the linear regulator at low frequency. From Equation 1-4-2 we see that the magnitude of the error amplifier gain is determined by the pole frequency f_0 and that it can be very high at low frequency, depending on the OPAMP DC open loop gain A_{dc} and on the setup of the pole frequency f_0. Equation 1-4-3 highlights that, given the DC operating conditions and the MOSFET characteristics, a high loop gain magnitude improves the linear regulator AC noise rejection capability. The loop gain of the linear regulator at low frequency is determined by the OPAMP dc open loop gain and by the error amplifier frequency pole frequency f_0.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What parameters of a linear regulator determine the nominal value of its DC output voltage?
  A. the MOSFET transconductance and gate-to-source threshold voltage
  B. the error amplifier pole and OPAMP dc gain A_d
  C. the reference voltage and the voltage sensor gain

1-2 What parameter of a linear regulator determine its DC output voltage offset error?
  A. the MOSFET transconductance β
  B. the error amplifier pole frequency f_0
  C. the OPAMP open loop dc gain A_{dc}

1-3 At what frequency is the open loop linear regulator more sensitive to AC noise?
  A. below the open loop bandwidth
  B. above the open loop bandwidth
  C. at any frequency

1-4 What parameters majorly influence the closed loop AC noise rejection capability of a linear regulator?
  A. the reference voltage and the voltage sensor gain
  B. the MOSFET transconductance and gate-to-source threshold voltage
  C. the error amplifier pole frequency f_0 and OPAMP dc gain A_{dc}

1-5 Based on your answers to Questions 1-1 to 1-4, what actions would you make to design a linear regulator with good DC accuracy and AC noise rejection capability?

_____

_____

_____

_____

2 Exercise

The **Discrete Linear Section** in the TI Power Electronics Board for NI ELVIS III is based on the following setup:

- MOSFET: TI's CSD15380F3, assume $V_{th} = 1.35V$, $\beta = 0.24A/V^2$, $\lambda = 0.05V^{-1}$
- OPAMP: TI's OPA835IDBVR, assume $A_{dc}=10^6$, $V_{cc+}=5.5V$, $V_{cc-}=0V$.
- VOLTAGE REFERENCE: TI's LM4140, assume $V_{ref}=1.024V\pm0.1\%$.
- ERROR AMPLIFER SETUP: $f_0 = 3.28kHz$, $R_{i1}=39.2k\Omega\pm1\%$, $R_g=26.1k\Omega\pm1\%$.

TI's devices datasheets are available at the following links:

- CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
- OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
- LM4140 VOLTAGE REFERENCE: http://www.ti.com/lit/ds/symlink/lm4140.pdf

2-1 Calculate the ideal, minimum and maximum values of the nominal value of the DC output voltage $V_{outDC,nom}$, in Volts with four decimal digits, considering the tolerances of parameters:

ideal $V_{outDC,nom}$ = 2.5219V ;   min $V_{outDC,nom}$ = 2.5297V ;   max $V_{outDC,nom}$ = 2.5956V.

2-2 Calculate the DC offset error of the output voltage, in micro Volts with three decimal digits, in the ideal, minimum and maximum nominal DC output voltage conditions determined with previous step 2-1:

ERR_{DC} @ min $V_{outDC,nom}$ = -6.573µV; ERR_{DC} @ max $V_{outDC,nom}$ = -6.252µV;
ERR_{DC} @ ideal $V_{outDC,nom}$ = -6.410µV;

2-3 Calculate the open loop bandwidth f_t of the linear regulator, in Hz, with $C_o=1µF$ and $C_o=11µF$, assuming $V_{inDC} = 5V$ and $V_{outDC} = 2.5V$:

f_t @ $C_o=1µF$ = 17250Hz ; f_t @ $C_o=11µF$ = 1568Hz

2-4 You have a source voltage with a 5V DC component and an AC noise $V_{inAC}sin(2\pi f \cdot t)$, where $V_{inAC} = 1V$ and the frequency f can have the values listed in Table 2-1. Assuming $V_{outDC} = 2.5V$ and $C_o=1µF$, calculate the ratio V_{outAC}/V_{inAC}, in the format XXX.XXXE-03, and the value of the amplitude V_{outAC} of the AC voltage $V_{outAC}sin(2\pi f \cdot t+\theta)$, in milli Volts with three decimal digits, under a) open loop and b) closed loop conditions, and report the results in Table 2-1.

Table 1-1 Analysis of linear regulator AC noise rejection capability in open loop and closed loop operation.

f [Hz]	10	100	1000
open loop V_{outAC}/V_{inAC}			
closed loop V_{outAC}/V_{inAC}			
open loop V_{outAC} [mV]			
closed loop V_{outAC} [mV]			

2-5   Based on the results of your calculations, do you observe and improvement in the AC noise rejection capability of the linear regulator in closed loop operation compared to open loop operation?

A.   yes

B.   no

Please provide your comments: _____

_____

2-6   What parameter would you change to improve the low frequency rejection capability, and how?

_____

_____

3 Simulate

The simulations you will perform in this section allow you to analyze the closed loop behavior of an error amplifier. First, you will observe the DC output voltage and determine the DC offset error with respect to the nominal value. Next, you will observe the error amplifier voltage and compare it with the theoretical value required to achieve the desired output voltage. Finally, you will analyze the impact of output capacitor and error amplifier setup on the AC noise rejection capability of the linear regulator in closed loop operation.

3.1 Simulation 1: Instructions

1. Open *Lab4 – Linear Regulator in Closed Loop Operation* from the file path: https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/

The circuit shown in Figure 3-1 is used for simulating the DC and AC linear regulator closed loop operation.
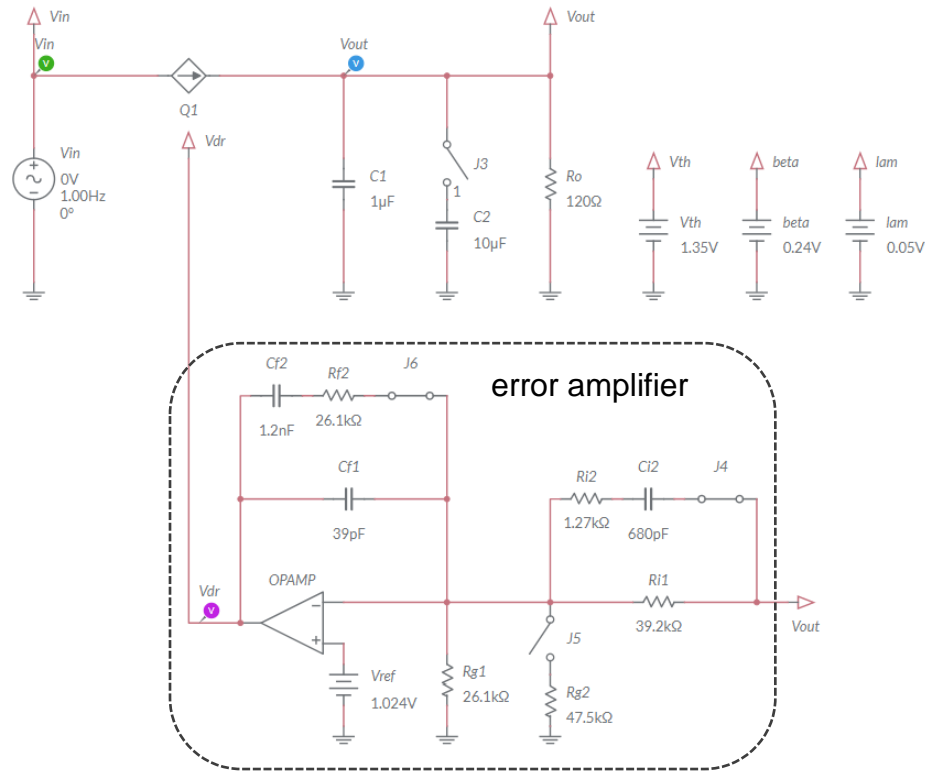
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Linear Regulator in Closed Loop Operation.

The error amplifier generates the gate driver voltage V_{dr}. The source voltage V_{in} includes a DC component and an AC perturbation. The parameters {*VA, Freq, VO*} of the generator V_{in} correspond to the parameters {V_{inAC}, *f*, V_{inDC}} as defined in the **Theory and Background** section. The auxiliary generators *Vth*, *beta* and *lam* allow to set the MOSFET parameters {V_{th}, β, λ}, respectively. The error amplifier pole frequency is $f_0 = 1/(R_{i1}(C_{f1}+C_{f2})) = 3.3$kHz with switches J4 and J6 closed (Type III error amplifier), and $f_0 = 1/(R_{i1}C_{f1}) = 104$kHz with jumpers J4 and J6 open (Type I error amplifier). The OPAMP is characterized by a dc gain $A_{dc}=10^6$.

2. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Instantaneous* option box for voltage probes V_{in}, V_{out}, and V_{dr} in the *Measurement labels* menu.

6. Calculate the nominal value $V_{outDC,nom}$ in Volts with three decimal digits, and report the result in Table 3-1.
7. Set *VA=0*, *Freq=10Hz* for the generator V_{in}.
8. For each value of DC source voltage V_{inDC} (*VO* voltage of the generator V_{in}) listed in Table 3-1, run the simulation, read the measurements of voltage probes V_{out} and V_{dr} in Volts with four decimal digits and report the results in Table 3-1.

Table 3-1 DC Output Voltage and Error Amplifier Voltage as function of DC Source Voltage.

V_{inDC} (VO) [V]	4.0	4.5	5.0	5.5	6.0
$V_{outDC,nom}$ [V]					
V_{outDC} [V]					
V_{drDC} [V]					

3-1-1 Does the DC output voltage V_{outDC} change as V_{inDC} increases?

A. yes

B. no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-1-2 Does the error amplifier voltage V_{dr} change as V_{inDC} increases?

A. yes

B. no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-1-3 What change do you expect in the simulation results if you open the switches J4 and J6? why?

_____

_____

3-1-4 What change do you expect in the simulation results if you close the switch J3 or J5? why?

_____

_____

3.2 Simulation 2: Instructions

1. Open *Lab4 – Linear Regulator in Closed Loop Operation* from the file path:
   https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/
2. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Periodic* option box for voltage probes V_{in}, V_{out}, and V_{dr} in the *Measurement labels* menu.
6. Set *VA*=1V, *Freq*=10Hz, *VO*=5V for the generator V_{in} and run the simulation.
7. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{out} voltage probe and report the values of $V_{outDC} = V_{AV}$ (in Volts with four decimal digits) and V_{outAC} (in milli Volts with three decimal digits) in Table 3-2.
8. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{dr} voltage probe and report the values of $V_{drDC} = V_{AV}$ (in Volts with four decimal digits) and V_{drAC} (in milli Volts with three decimal digits) in Table 3-2.
9. Repeat steps 7-8 under all V_{in} frequency and amplitude conditions of Table 3-2.

Table 3-2 Linear regulator AC response with C_o=1μF.

f [Hz] (V_{in} Freq)	10	100	1000
V_{inAC} [Hz] (V_{in} VA)	0.5	0.5	0.5
ML Simulation Max. Time Step	1e-5	1e-6	1e-7
ML Grapher Horizontal Axis	50ms/div	5ms/div	500us/div
$V_{outDC,nom}$ [V]			
V_{outDC} [V]			
V_{outAC} [mV]			
V_{drDC} [V]			
V_{drAC} [mV]			

3-2-1 Does the DC output voltage V_{outDC} change as the source voltage noise frequency increases?

A.   yes

B.   no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-2-2 Does the amplitude V_{outAC} of the AC output voltage noise change as the source voltage noise frequency increases?

A.   yes

B.   no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-2-3 What change do you expect if you open the switches J4 and J6? why?

_____

_____

3-2-4 What change do you expect if you close the switch J3 or J5? why?

_____

_____

Troubleshooting tips:

- If the simulation does not run and you get some error message, reload *Lab4 – Linear Regulator in Closed Loop Operation* from this file path: https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/ and restart the simulation, following the instructions.

4 Implement

The experiments of this section allow you to observe the behavior of a real linear regulator in closed loop operation. First, you will analyze the DC operating point of the linear regulator while varying the DC source voltage. Next, you will measure the AC output voltage generated by the AC noise of the source voltage. Finally, you will determine the impact of the error amplifier setup on the AC noise rejection capability of the linear regulator. The experiments are performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1, using the TI's CSD15380F3 MOSFET as pass device and TI's OPA835IDBVR OPAMP as error amplifier. The linear regulator is powered by a TI's TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage and an AC noise.
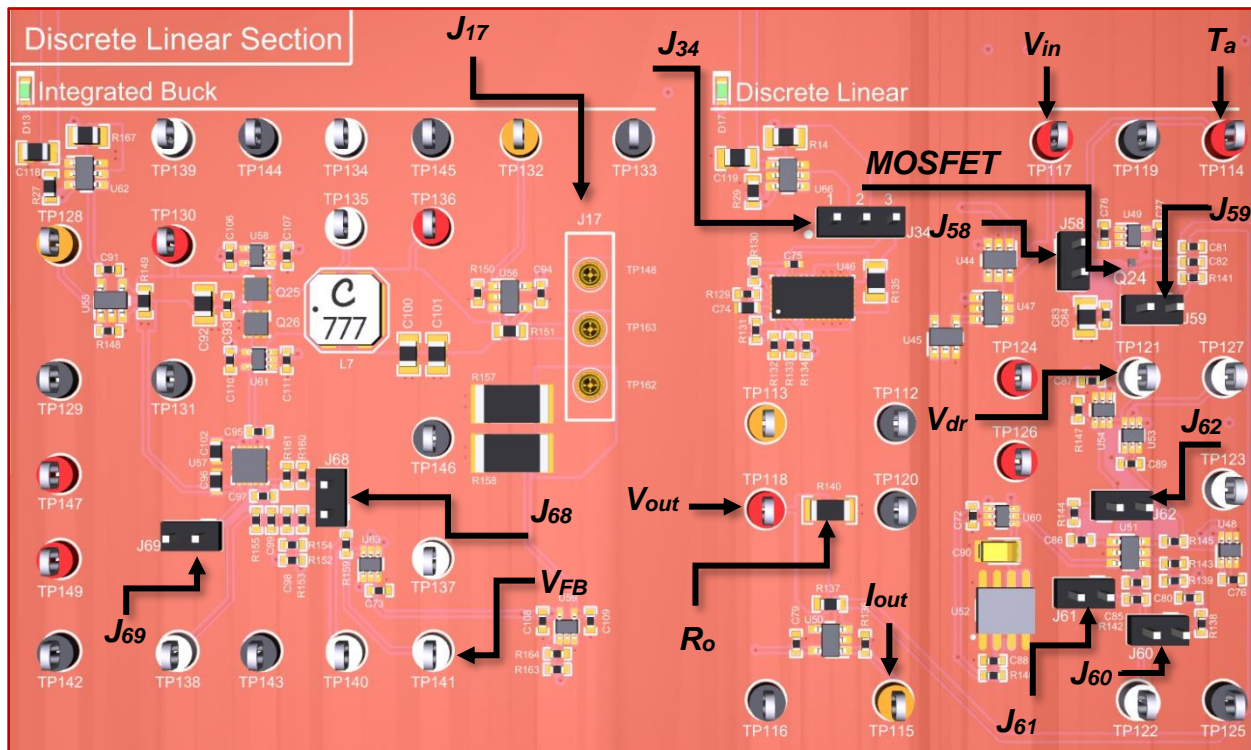
Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Linear Regulator in Closed Loop Operation

TI's devices datasheets are available at the following links:

CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
TPS40303DRCR Buck Regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf

The error amplifier pole frequency is $f_0 = 1/(R_{i1}(C_{f1}+C_{f2})) = 3.3$kHz with jumpers J60 and J62 shorted (Type III error amplifier), and $f_0 = 1/(R_{i1}C_{f1}) = 104$kHz with jumpers J60 and J62 open (Type I error amplifier). The output capacitance C_o is 1µF with jumper J59 open, and 11µF with jumper J59 shorted. The nominal output voltage is 2.5V with jumper J61 open, and 3.3V with jumper J61 shorted. [**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 General Instructions

1. Open *Variable Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open NI ELVIS III *PE Lab User Interface* (See Required Tools and Technology section for download instructions), and select *Lab4 – Linear Regulator in Closed Loop Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect the instruments as indicated in Table 4-2.

Table 4-1 Jumpers setup

J17	J34	J58	J59	J60	J61	J62	J68	J69
short TP148-TP163	short 2-3	open	open	short	open	short	short	open

Table 4-2 Instruments connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP117 (input voltage V_{in}), connect CH-2 to TP118 (output voltage V_{out}), connect CH-3 to TP121 (gate driver voltage V_{dr})
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP137 = Integrated Buck output voltage control)

4-2 Experiment 1: Instructions

1. Use the instruments configuration and setup shown in Table 4-2-1.

Table 4-2-1 Instruments initial configuration and setup

Power Supply	CH "+": Static, 7.00V, CH "-": Inactive				
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 100us/div	*Acquisition*: average	*Measurements*: show	*Probe Attenuation*: 10x
	CH-1: ON • DC coupling • 2V/div • offset 0V	CH-2: ON • DC coupling • 2V/div • offset 0V		CH-3: ON • DC coupling • 2V/div • offset 0V	CH-4: OFF
Function Generator	CH-1: Sine, DC offset 735mV, Amplitude 0mV, Frequency 10Hz CH-2: Inactive				

2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
3. Read the average DC values of the *Oscilloscope* CH-2 (V_{out}) and CH-3 (V_{dr}) and CH-4 (V_{drEA}), using the cursors in Track mode, and report the values in Table 4-2-2, with two decimal digits.
4. Repeat the measurement for all the values of the driver voltage V_{drDC} indicated in Table 4-2-2, by changing the DC offset of *Function Generator* CH-2.
5. Import in Table 4-2-2 the DC values of V_{outDC} and V_{drDC} collected in Table 3-1, in Volts with two decimal digits.
6. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

Table 4-2-2 Linear regulator DC output voltage and gate driver voltage as function of DC input voltage.

Function Generator CH1 DC offset [mV]	735	670	600	540	470
$V_{outDC,nom}$ [V]					
V_{inDC} [V]					
V_{outDC} [V]					
V_{outDC} [V] from Table 3-1					
V_{drDC} [V]					
V_{drDC} [V] from Table 3-1					

4-2-1 Is the DC output voltage V_{outDC} trend, as V_{inDC} increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

    A.   yes
    B.   no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

_____

_____

4-2-2 Is the gate driver voltage V_{drDC} trend, as V_{inDC} increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

    A.   yes
    B.   no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

_____

_____

4-2-3 Based on your answer to Questions 4-2-1 and 4-2-2, what parameter of the linear regulator model would you change to improve the accuracy of simulations? How and why?

_____

_____

4-3 Experiment 2: Instructions

    1. Open *Power Supply*, *Function Generator* and *Oscilloscope* and use the instruments configuration and setup shown in Table 4-3-1.

Table 4-3-1 Instruments initial configuration and setup

Power Supply	*CH "+"*: Static, 7.00V, *CH "-"*: Inactive				
Oscilloscope	*Trigger*: CH-1 Analog edge, set to 50%	*Horizontal*: 50ms/div	*Acquisition*: average	*Measurements*: show	*Probe Attenuation*: 10x
	CH-1: ON • DC coupling • 2V/div • offset -0V	*CH-2*: ON • DC coupling • 10mV/div • offset -2.55V	*CH-3*: ON • DC coupling • 10mV/div • offset -4.25V	*CH-4*: OFF	
Function Generator	*CH-1*: Sine, DC offset 610mV, Amplitude 135mV, Frequency 10Hz *CH-2:* Inactive				

2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
3. Read the DC average values of the *Oscilloscope* CH-2 (V_{out}) and CH-3 (V_{dr}) and report the values in Table 4-3-2, with two decimal digits.
4. Read the peak-peak values of the *Oscilloscope* CH-2 (V_{out}) and CH-3 (V_{dr}) with two decimal digits, divide by 2 and report the values in Table 4-3-2.
5. Repeat the measurement for all the values of Frequency, DC Offset and Amplitude of the *Function Generator* CH-1 indicated in Table 4-3-2
6. Import in Table 4-3-2 the values of V_{outDC} and V_{drDC} collected in Table 3-2, in Volts with two decimal digits, and the values of V_{outAC} and V_{drAC} collected in Table 3-2, in milli Volts with the same decimal digits of the corresponding measured data.
7. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

Table 4-3-2 Error Amplifier response.

Function Generator CH-1 Frequency [Hz]	10	100	1000
Function Generator CH-1 Amplitude [mV]	135	135	150
Function Generator CH-1 DC offset [mV]	600	600	600
$V_{outDC,nom}$ [V]			
Scope CH-2 Average V_{outDC} [V]			
V_{outDC} from Table 3-2 [V]			
Scope CH-2 Volts Vpk-pk/2 = V_{outAC} [mV]			
V_{outAC} from Table 3-2 [mV]			
Scope CH-3 Average V_{drDC} [V]			
V_{drDC} from Table 3-2 [V]			
Scope CH-3 Volts Vpk-pk/2 = V_{drAC} [mV]			
V_{drAC} from Table 3-2 [mV]			

4-3-1 Is the AC output voltage V_{outAC} trend, as the frequency f increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

    A.   yes

    B.   no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

_____

_____

4-3-2 Is the gate driver voltage V_{drAC} trend, as V_{inAC} increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

    A.   yes

    B.   no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

_____

_____

4-3-3 Based on your answer to Questions and 4-3-1 and 4-3-2, what parameter of the linear regulator model would you change to improve the accuracy of simulations? How and why?

_____

_____

Troubleshooting tips:
- If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

5 Analyze

5-1 Using the results collected in Table 4-3-2, calculate the value in decibel of the Power Supply Rejection Ratio $PSRR_{dB} = 20\log_{10}(V_{inAC}/V_{outAC})$, with one decimal digit, at each frequency and report the results in Table 5-1. Graph the $PSRR_{dB}$ values as a function of the frequency f using a logarithmic scale for the horizontal axis and decibel scale for the vertical axis. Include a legend that indicates which line style corresponds to which series (calculations, measurements).

Table 5-1 Closed Loop Power Supply Rejection Ratio.

f [Hz]	10	100	1000
$PSRR_{db} = 20\log10(V_{inAC}/V_{outAC})$			
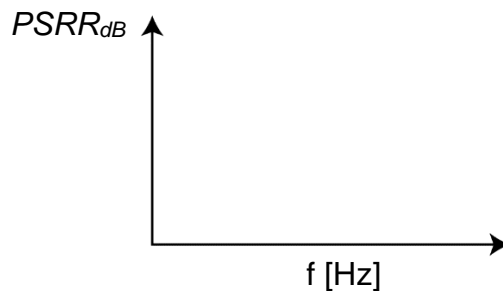
Figure 5-1 PSRR Values Obtained with Different Setup of the Closed Loop Linear Regulator.

5-2   Based on your learning, discuss the trend of $PSRR_{db}$ you observe and indicate what parameter of the linear regulator would you change to improve PSRR at high frequency:

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the closed loop operation of a linear regulator, regarding its DC accuracy and noise rejection capability with respect to source voltage AC perturbations. Discuss the conditions and the parameters influencing the closed loop response of the linear regulator, and how you can improve the Power Supply Rejection Ratio.

6-2   Expansion Activities

6-2-1. The parameters V_{th}, β and λ of the MOSFET model are characterized by a tolerance determined by manufacturing processes, and they depend on the MOSFET junction temperature. Assuming that:

- the value of V_{th} can range between 0.85V and 1.35

- the value of β can range between 0.19V and 0.33

- the value of λ can range between 0.01V and 0.05

a. Determine the combination of values of MOSFET parameters that would improve the linear regulator PSRR.
b. Use Multisim Live simulation circuit schematic of Figure 3-1 to verify your prediction.

6-2-2. Determine the frequency response of the linear regulator with respect to the reference voltage V_{ref} with the simulation circuit schematic of Figure 3-1, by using the *AC Sweep* option.

a. Set the switches J4 and J6 to be closed.
b. Replace the V_{ref} DC generator with an AC generator and set VO=1.024V, Freq=1Hz, VA=0.1V.
c. Set AC_mag = 0.1V in the *AC analysis value* menu option of the voltage generator V_{ref}.
d. Set AC_mag = 0 V in the *AC analysis value* menu option of the voltage generator V_{in}.
e. Set Start freq. = 1Hz and Stop freq. = 1MHz in the *Configuration Panel*.
f. Set *Show plots* box unchecked on probe V_{in}.
g. Run the simulation and watch the resulting AC Sweep plots (Bode plots). The continuous line is the magnitude of the ratios $T_{ref} = V_{outAC}/V_{refAC}$, while the dashed line is the phase shift between V_{outAC} with respect to V_{refAC}.

The response should be flat up to a certain frequency. That frequency is the closed loop bandwidth of the linear regulator, which is the frequency range wherein the regulator is able to track accurately the reference voltage, while exhibiting a good PSRR. A wide bandwidth is a highly valuable feature of a linear regulator.

6-2-3. Analyze the effect of output capacitance on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.

    a. Short the jumper J59 to set the output capacitance at 11µF.
    b. Repeat Experiment 2, following the relevant instructions.
    c. Calculate the value in decibel $PSRR_{dB}$ = $20\log_{10}(V_{inAC}/V_{outAC})$ at each frequency.
    d. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.

6-2-4. Analyze the effect of error amplifier setup on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.

    a. Open the jumpers J60 and J62 to set the frequency pole f_0 at 104kHz.
    b. Repeat Experiment 2, following the relevant instructions.
    c. Calculate the value of the $PSRR_{dB}$ = $20\log_{10}(V_{inAC}/V_{outAC})$ at each frequency.
    d. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.

6-2-5. Analyze the effect of output voltage setup on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.

    a. Short the jumper J61 to set the nominal output voltage at 3.3V.
    b. Repeat Experiment 2, following the relevant instructions. [**Note:** set the offset of *Oscilloscope* CH-2 at -3.45V and CH-3 at -5.25V]
    c. Calculate the value of the $PSRR_{dB}$ = $20\log_{10}(V_{inAC}/V_{outAC})$ at each frequency.
    d. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.

6-3 Resources for learning more

- This book provides the fundamentals of linear regulators control:
  C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   C

1-2   C

1-3   A

1-4   C

1-5   high f_0, high A_{dc}

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 5: Buck Regulator

Half-Bridge PWM Operation

Lab 5: Buck Regulator Half-Bridge PWM Operation

The goal of this lab is to investigate the behavior of MOSFETs when configured as a half-bridge in Pulse Width Modulation (PWM) operation. The PWM MOSFETs half-bridge is the main functional element of the buck converter, the most diffused high-efficiency step-down DC-DC regulator topology. First, we review the principle of operation and fundamental equations of the MOSFET in the half-bridge configuration and of the PWM modulator. Next, we predict the theoretical average output voltage of the half-bridge considering the impact of MOSFETs resistance. Then, we simulate the MOSFET half-bridge and PWM modulator and we verify the theoretical predictions in different operating conditions. Finally, we perform lab experiments to measure the real values of output voltage and duty-cycle, determine the buck regulator conversion ratio, evaluate the MOSFETs loss and resistance and determine the efficiency of the regulator.
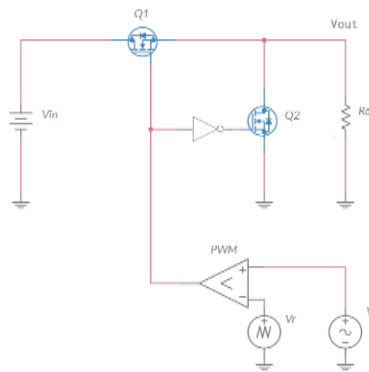
Figure 1-1. MOSFETs in Half-Bridge Configuration

Learning Objectives
After completing this lab, you should be able to complete the following activities.
1. Given a MOSFET half-bridge, a PWM modulator, a source voltage, and a load resistance, you will calculate the PWM control voltage required to achieve a desired output voltage and the conversion efficiency of the half-bridge in different operating conditions, with specified units and accuracy.
2. Given a MOSFET half-bridge, a PWM modulator with a triangular carrier signal and a DC control voltage, you will simulate the half-bridge behavior to verify the consistency of theoretical predictions, by comparing the simulated and the calculated output voltage under the same source voltage and a load resistance conditions.
3. Given a real MOSFET half-bridge, a PWM modulator, a DC power supply, a load resistor, and a two channel function generator, you will determine the PWM control voltage needed to achieve a desired output voltage, the duty-cycle, the efficiency and the MOSFET on-state resistance, with specified units and accuracy.

Required Tools and Technology

Platform: NI ELVIS III Instruments used in this lab: ● Function generator ● Digital multimeter ● Oscilloscope ● Power Supply **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.	✓ Access Instruments https://measurementslive.ni.com/ ✓ View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html ✓ View Tutorials https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M
Hardware: TI Power Electronics Board	✓ View User Manual http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
Software: NI Multisim Live	✓ Access https://www.multisim.com/ ✓ View Tutorial https://www.multisim.com/get-started/
Software: TI Power Electronics Configuration Utility	✓ Download (Windows OS Only) http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a PWM modulated MOSFET half-bridge. This important element is used in a large variety of switching power supply applications, ensuring high-efficiency DC-DC voltage conversion.

1-2 MOSFET half-bridge in PWM operation.

Figure 1-2 shows a couple of MOSFETs Q_1 and Q_2 in half-bridge configuration, controlled by a PWM modulator. The MOSFETs operate as switches. The *carrier* signal V_r, and the *control* signal V_c determine the status of the PWM comparator output. When $V_r < V_c$, the PWM comparator output is high, the Gate Driver sets gate signals G1 and G2 respectively high and low, and Q1 conducts whereas Q2 is open. When $V_r > V_c$, the PWM comparator output is low, the Gate Driver sets gate signals G1 and G2 respectively low and high, and Q1 is open whereas Q2 conducts. This results in a square-wave half-bridge output voltage V_{out}, as shown in Figure 1-2 [**Note:** the edges of the square-wave voltage V_{out} in a real PWM modulated half-bridge are delayed with respect to the crossing of V_c and V_r signals]. The switching frequency $f_s = 1/T_s$ is determined by the period T_s of the signal V_r.
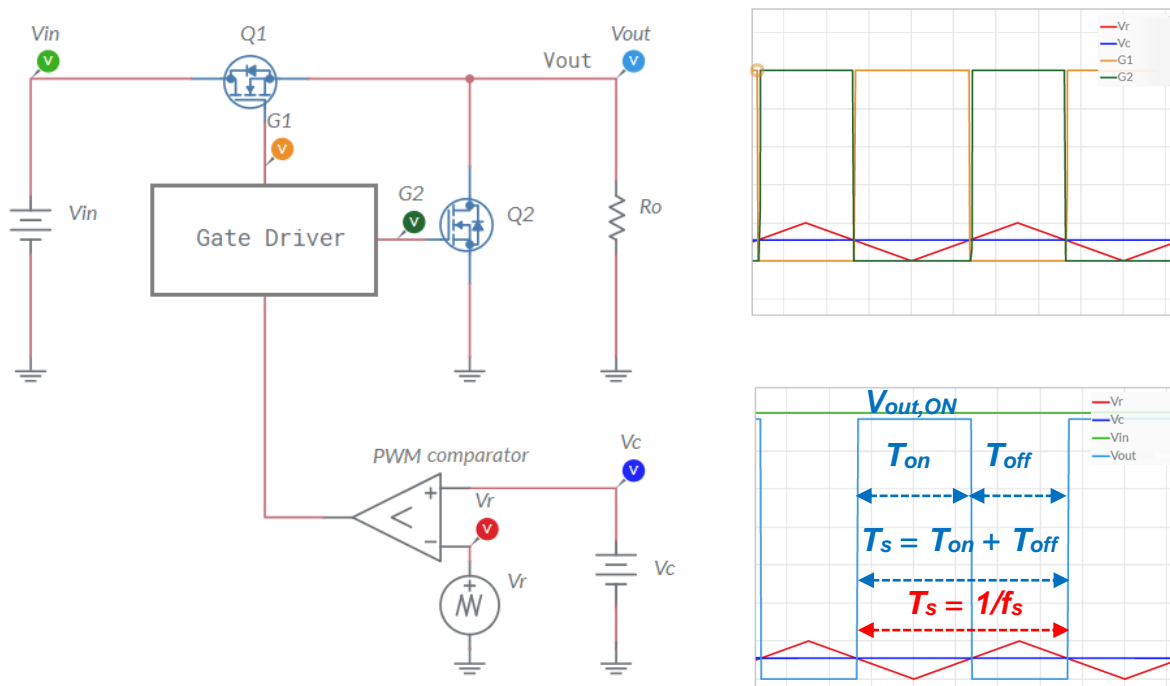
Figure 1-2. MOSFET Half-Bridge in PWM Operation.

The amplitude $V_{out,ON}$ of the square-wave voltage V_{out} is determined by the input voltage V_{in} and by the MOSFET characteristics. During the time the gate signal of a MOSFET is high, the gate-drive circuitry drives the device to the ohmic region, where it behaves like a resistor (see **Lab1**). The MOSFET drain-to-source on-state resistance $R_{DS(on)}$ in the ohmic region is inversely proportional to the gate-to-source voltage, and depends on the temperature, as shown in Figure 1-3.
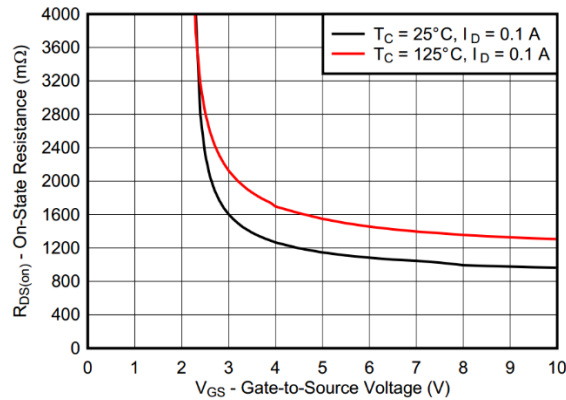
Figure 1-3. MOSFET On-State Resistance as Function of Gate-to-Source Voltage (Texas Instruments CSD15380F3).

An approximated analytical expression of the on-state resistance $R_{DS(on)}$ of a MOSFET is given by Equation 1-1:

Equation 1-1
$$R_{DS(on)} = \frac{1}{\beta(V_{gs} - V_{th})}$$

where V_{gs} is the gate-to-source voltage applied to the MOSFET, V_{th} is its gate-to-source voltage threshold, and β is its trans-conductance coefficient (see **Lab1**).

1-3 Average Output Voltage of MOSFET Half-Bridge

The voltage V_{out} applied to the load resistor R_o is given by Equation 1-2:

Equation 1-2
$$V_{out} = \begin{cases} V_{out,ON} = \dfrac{R_o}{R_o + R_{DS(on)}^{Q1}} V_{in} & t \in T_{on} \\[2mm] V_{out,OFF} = 0 & t \in T_{off} \end{cases}$$

where T_{on} is the interval of time where $V_r < V_c$, T_{off} is the interval of time where $V_r > V_c$, and $T_{on} + T_{off} = T_s$. The ratio $D = T_{on}/T_s$ is the PWM duty-cycle D. The duty-cycle D is determined by ratio between the control signal and the peak-peak amplitude of the triangular carrier signal, and is given by:

Equation 1-3
$$D = \begin{cases} 0 & V_c \leq 0 \\ \dfrac{V_c}{V_{rpp}} & 0 < V_c < V_{rpp} \\ 1 & V_c \geq V_{rpp} \end{cases}$$

Based on Equation 1-2, the average voltage applied to the load resistor $V_{out,AV}$ is:

Equation 1-4
$$V_{out} = \frac{R_o}{R_o + R_{DS(on)}^{Q1}} D V_{in}$$

Based on Equations 1-3 and 1-4, the average output voltage $V_{out,AV}$ can range from 0 to $V_{in}R_o/(R_o+R_{DS(on)}^{Q1}) < V_{in}$. From Equation 1-4 we can derive the value of the control signal V_c required to achieve a desired nominal average output voltage $V_{out,nom}$:

Equation 1-5
$$V_c = \left(1 + \frac{R_{DS(on)}^{Q1}}{R_o}\right) \frac{V_{rpp} V_{out,nom}}{V_{in}}$$

1-4 MOSFET Power Loss and Half-Bridge Conversion Efficiency

The conduction average power loss of MOSFET Q1 is given by:

Equation 1-6
$$P_{Q1} = D R_{DS(on)}^{Q1} \frac{V_{in}^2}{(R_{DS(on)}^{Q1} + R_o)^2}$$

The maximum MOSFET power loss is given by $P_{Q1max}=(150°C-T_a)/R_{\theta ja}$, where T_a and $R_{\theta ja}$ are the ambient temperature and the MOSFET thermal resistance, respectively. The average power P_{Ro} delivered to the load resistor R_o and the resulting percent efficiency $\eta_\%$ of the MOSFET half-bridge are given by:

Equation 1-7
$$P_{Ro} = D R_o \frac{V_{in}^2}{(R_{DS(on)}^{Q1} + R_o)^2}$$

Equation 1-8
$$\eta_\% = \frac{R_o}{R_o + R_{DS(on)}^{Q1}} x100$$

Equation 1-7 highlights that the MOSFET half-bridge can achieve a very high efficiency if the resistance $R_{DS(on)}^{Q1}$ of MOSFET Q1 is very low. According to the MOSFET on-state resistance of Figure 1-3, a higher value of the gate-driver voltage can help reducing the on-state resistance.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What functional element is used to change the average output voltage of a MOSFET half-bridge?
    A. the MOSFET gate driver
    B. the PWM modulator
    C. the voltage source

1-2 How is average output voltage of the half-bridge related to the source voltage?
    A. it is always lower
    B. it is always higher
    C. it can be higher or lower

1-3 Given the source voltage and the load resistance, how can we change the value of the average output voltage of the half-bridge?
    A. by varying the gate-driver voltage
    B. by varying the PWM modulator control voltage
    C. by varying the gate-driver voltage and the PWM modulator control voltage

1-4 Is the average output voltage of the half-bridge influenced by the switching frequency?
    A. yes
    B. no
    C. it depends on the MOSFET on-state resistance

1-5 What factor is mainly influencing the efficiency of the half-bridge?
    A. the duty-cycle
    B. the carrier peak-peak voltage
    C. the MOSFET power loss

1-6 How can we reduce the MOSFET conduction power loss?
    A. by increasing the PWM comparator control voltage
    B. by increasing the gate-driver voltage
    C. by decreasing the gate-driver voltage

2 Exercise

The two TI's CSD15380F3 (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf) N-channel MOSFETs Q1 and Q2 used in the Discrete Buck Section of the TI Power Electronics Board for NI ELVIS III have the following nominal parameters: $V_{th} = 1.1$V, $\beta = 0.24$A/V^2, $\lambda = 0.02$V^{-1}. The negative input of the PWM modulator is connected to a voltage source generating a triangular waveform, with 2µs period T_s, equal rise and fall time, 1V peak-peak voltage, while the positive input is connected to a DC voltage source. The MOSFETs Gate Driver provides a 5V gate-to-source voltage V_{dr}.

2-1 Assuming $V_{in} = 7$V, use the rules and equations provided in the **Theory and Background** section to calculate:

- the MOSFET on-state resistance $R_{DS(on)}$, in Ohms with three decimal digits:
  $R_{DS(on)} = $ _____
- the control voltage, in Volt with three decimal digits, required to achieve an average output voltage $V_{out,AV} = 2.5$V, for all the values of load resistance R_o listed in Table 2-1, and the corresponding % efficiency, with one decimal digit.

Table 1-1 PWM control voltage and efficiency as function load resistance

R_o [Ω]	20	50	100	120	150	200
V_c [V]						
η [%]						

2-2 Assuming $R_o = 50\Omega$, use the equations provided in the **Theory and Background** section to calculate the control voltage, in Volt with three decimal digits, required to achieve an average output voltage $V_{out,AV} = 2.5$V, for all the values of source voltage V_{in} listed in Table 2-1, and the corresponding % efficiency, with one decimal digit.

Table 2-2 PWM control voltage and efficiency as function input voltage

V_{in} [Ω]	1	2	3	4	5	6
V_c [V]						
η [%]						

3 Simulate

The goal of the simulations you will perform in this section is to analyze the operation of a MOSFET half-bridge controlled by a PWM modulator. You will verify the consistency of the PWM modulator control voltage calculated in the **Exercise** Section, by observing the average voltage at the output of the half-bridge, under different source voltage and load resistance conditions.

3-1 General Instructions

1. Open *Lab5 – Buck Regulator Half-Bridge PWM Operation* from this file path:
   https://www.multisim.com/content/sRY9ZW7saFpr4MKWu2a5A5/lab-5-buck-regulator-mosfets-pwm-operation/
   The circuit schematic for the analysis of the PWM modulated MOSFET half-bridge is shown in Figure 3-1. The MOSFETs are modeled by means of two *Single Pole Single Throw (SPST)* switches, characterized by 1.068Ω ON resistance and 1MΩ OFF resistance. The gate driver block includes time delays *td1* and *td2* and gates AND1 and AND2 to prevent cross conduction of the MOSFETs Q1 and Q2.
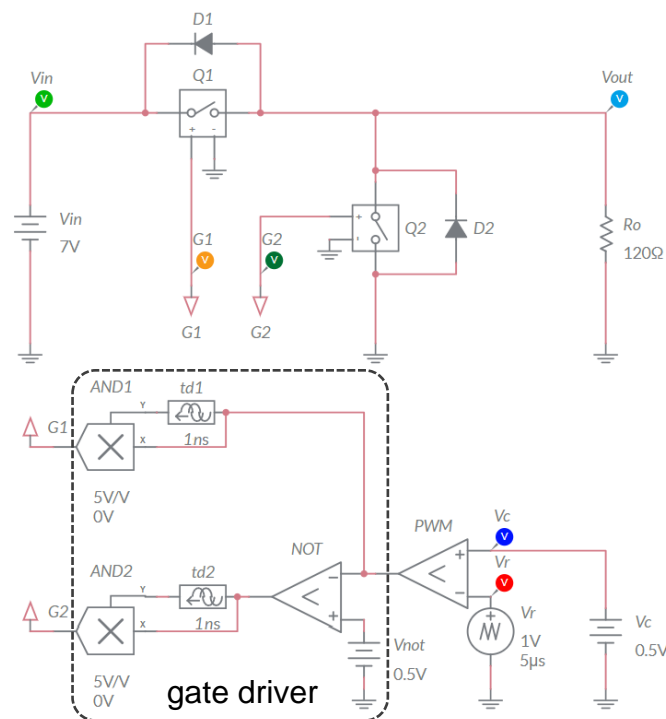
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of a buck regulator in open loop DC Operation

3-1-1 Simulation 1 Instructions

1. Select *Interactive* simulation and *Split* visualization options.
2. Check the *Periodic* option box for voltage probe V_{out} in *Measurement labels* menu.
3. Import in Table 3-1 the values of PWM control voltage V_c you have calculated and reported in Table 2-1 of **Exercise** section for each value of the load resistance R_o;
4. Set the simulation circuit parameters as follows:
   - V_{in}: *DC_mag* = 7.0V;
   - V_r: *VA* = 1V, *Per* = 5µs, *TF* = 2.5µs, Offset 0V;
   - R_o: 20Ω;
   - V_c: *DC_mag* = value of V_c corresponding to R_o equal to 20Ω.
5. Run the simulation, read the average value V_{AV} displayed by the output voltage probe V_{out}, in Volt with three decimal digits, and report the result in Table 3-1.
6. Export the *Grapher image* and save it as `Lab 5 - Buck Regulator_ Half-Bridge PWM Operation-Grapher_xx_yy.png`, where xx is the R_o value and yy is the V_c value.
7. Repeat steps 6-7 for all the values of R_o and V_c listed in Table 3-1.
8. Stop the simulation

Table 3-1 Average output voltage in load resistance and PWM control voltage matched conditions

R_o [Ω]	20	50	100	120	150	200
V_c [V] from Table 2-1						
$V_{out,AV}$ [V]						

3-1-2 Simulation 2 Instructions

1. Check the *Periodic* and the *Instantaneous* option boxes for voltage probe V_{out} in *Measurement labels* menu.
2. Import in Table 3-2 the values of PWM control voltage V_c you have calculated and reported in Table 2-2 of **Exercise** section for each value of the source voltage V_{in};
3. Set the simulation circuit parameters as follows:
   - R_o: 50Ω;
   - V_r: *VA* = 1V, *Per* = 5µs, *TF* = 2.5µs, Offset 0V;
   - V_{in}: *DC_mag* = 1.0V;
   - V_c: *DC_mag* = value of V_c corresponding to V_{in} equal to 1V.
4. Run the simulation, read the average value V_{AV} displayed by the output voltage probe V_{out}, in Volt with three decimal digits, and report the result in Table 3-1 [**Note:**

if the V_{AV} value is not displayed, read the v (instantaneous) value displayed by the output voltage probe V_{out}].

5. Export the *Grapher image* and save it as `Lab 5 - Buck Regulator_ Half-Bridge PWM Operation-Grapher_xx_yy.png`, where xx is the V_{in} value and yy is the V_c value.
6. Repeat steps 6-7 for all the values of V_{in} and V_c listed in Table 3-1.
7. Stop the simulation

Table 3-2 PWM control voltage required to set 2.5V output voltage as a function of source voltage.

V_{in} [Ω]	1	2	3	4	5	6
V_c [V] from Table 2-2						
$V_{out,AV}$ [V]						

3-1   Does the average output voltage match the required value in all the source voltage and load resistance conditions?

A.   yes
B.   no
Please provide your comments: _____

_____

3-2   From the images you have saved in step 5, does the duty-cycle of the square-wave output voltage V_{out} always increase as the control voltage V_c increases?

A.   yes
B.   no
Please provide your comments: _____

_____

Troubleshooting tips:
● If the simulation does not converge and you get some error message, reload *Lab5 – Buck Regulator Half-Bridge PWM Operation* from this file path https://www.multisim.com/content/sRY9ZW7saFpr4MKWu2a5A5/lab-5-buck-regulator-half-bridge-pwm-operation/ and restart the simulation following the instructions.

4 Implement

The experiments you perform in this section allow you to observe the behavior of a real MOSFET half-bridge in PWM operation. You will measure the ON and OFF times, voltages and currents characterizing the operation of the half-bridge under different conditions. Then, you will calculate the duty-cycle and the efficiency. Finally, you will estimate the MOSFETs on-state resistance. The **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments. [**Note:** The maximum input voltage V_{in} is 12V]. A 50Ω resistance R_o can be connected to the output of the Half-bridge (test point TP87) by means of the Jumper J11. The TI's CSD15380F3 half-bridge MOSFETs are characterized by a typical 1.2Ω on-state resistance at 4.5V gate-to-source voltage, 25°C and 0.1A, and a thermal resistance of 255°C/W. The PWM modulator is based on TI's TLV7011DPWR comparator, while the half-bridge MOSFET gate driver is a TI's TPS51601ADRBR.
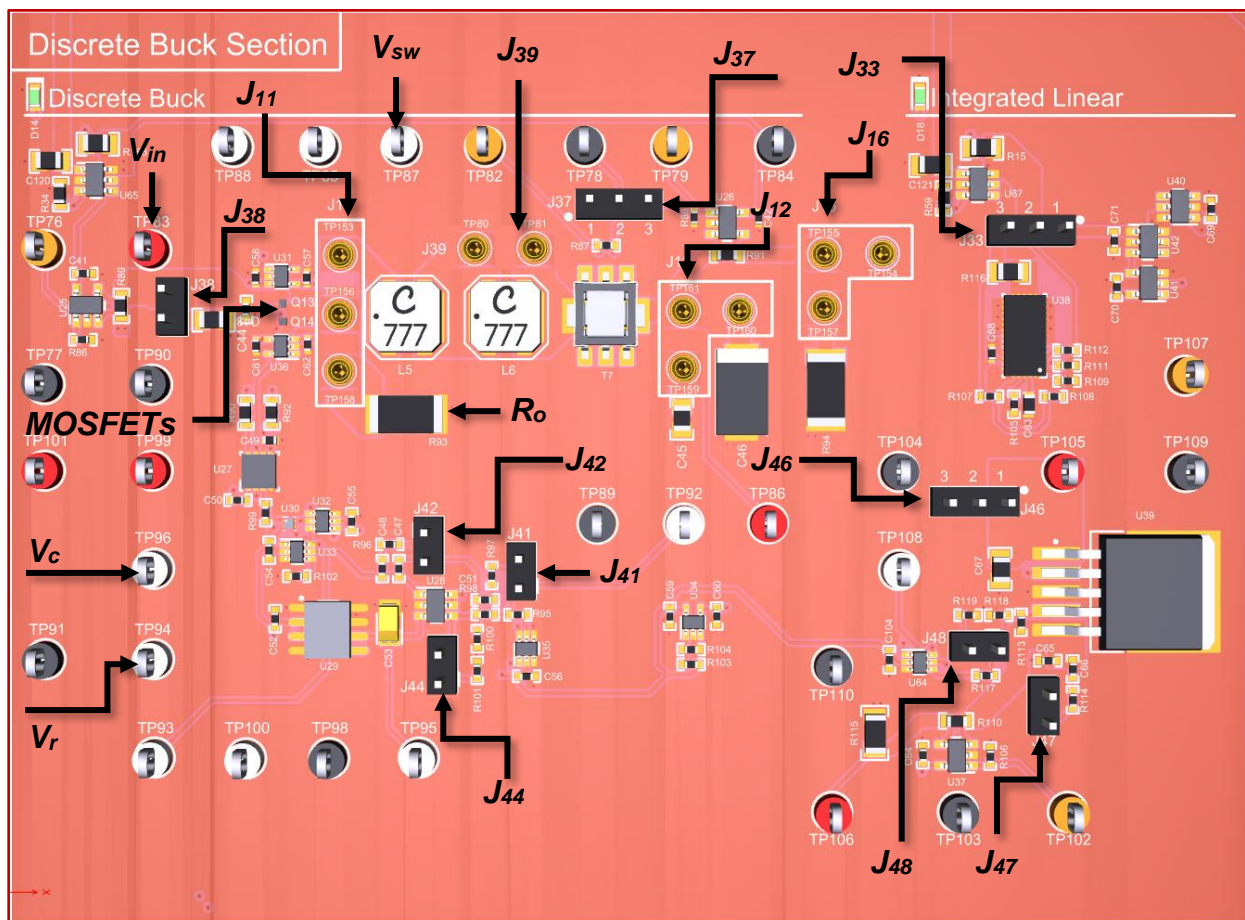
Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Buck Section Used for the Analysis of MOSFET Half-Bridge PWM Operation.

The datasheets of TI's components are available at these links:

- CSD15380F3 MOSFET: (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf)
- TLV7011DPWR COMPARATOR: (http://www.ti.com/lit/ds/symlink/tlv7011.pdf)
- TPS51601ADRBR GATE DRIVER: (http://www.ti.com/lit/ds/symlink/tps51601a.pdf).

The PWM modulator triangular carrier signal V_r and control signal V_c are available at test points TP94 and TP96, respectively. [**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 Instructions

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter* using Measurements Live. For help on launching instruments, refer to this help document: `http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/`
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: `http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html`
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab5 – Buck Regulator Half-Bridge PWM Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect and configure the instruments as indicated in Tables 4-2 and 4-3.

Table 4-1 Jumpers setup

J11		J12	J16	J37	J38	J39
short TP156-TP158		open	open	short 1-2	short	open
J41	J42	J33	J44	J46	J47	J48
short	short	short 2-3	open	short 2-3	short	open

Table 4-2 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP83 (V_{in}), connect CH-2 to TP87 (V_{sw}) connect CH-3 to TP94 (V_r), connect CH-4 to TP96 (V_c)
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP94 = V_r) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP96 = V_c)
Digital Multimeter	connect Voltage input to TP87 (V_{sw}), or to TP76 (I_{in}), as per instructions

Table 4-3 Instruments Configuration and setup

Power Supply	Channel "+": Static, 7.00V, Channel "-": Inactive			
Oscilloscope	Trigger: Analog Edge, CH-2, set to 50%	Horizontal: 2us/div	Acquisition: average	Measurements: show
	Channel 1: ON • DC coupling • 1V/div • offset 0V	Channel 2: ON • DC coupling • 2V/div • offset 0V	Channel 3: ON • DC coupling • 1V/div • offset 0V	Channel 4: ON • DC coupling • 1V/div offset 0V
Function Generator	Channel 1: Triangle, Frequency 200kHz, Amplitude 1Vpp, DC offset 0.5V Channel 2: Sine, Frequency 1Hz, Amplitude 0Vpp, DC offset 0V			
Digital Multimeter	Measurement mode: DC voltage; Range: Automatic			

7. Run *Oscilloscope*, *Digital Multimeter*, *Function Generator* and *Power Supply*.
8. Connect the *Digital Multimeter* input to TP87 (V_{sw})
9. Adjust the *Function Generator* CH-2 DC offset until the measurement of *Digital Multimeter* equals 4.000V, with three decimal digits, and then record the resulting value of the control voltage V_c, in Volt with three decimal digits, in Table 4-4.
10. Using **Theory and Background** equations, calculate the value, in Volt with three decimal digits, of the control voltage required to achieve the same average output voltage, and report the result in Table 4-4.
11. Use the horizontal cursors to measure the values of ON time, T_{on}, and OFF time, T_{off}, in micro seconds with two decimal digits, and report the results in Table 4-4.
12. Calculate the percent duty-cycle $D = T_{on} / (T_{on} + T_{off})$ x 100, with no decimal digits, and report the value in Table 4-4.
13. Use the vertical cursors to measure the values of output voltage $V_{out,ON}$ and $V_{out,OFF}$ during the ON time and OFF time, in Volt with at least two decimal digits, and report the results in Table 4-4.
14. Calculate the average output power $P_{out,AV} = D(V_{out,ON})^2/R_o$, in Watt with three decimal digits, and report the result in Table 4-4.
15. Connect *Digital Multimeter* to TP76 to measure the average input current $I_{in,AV}$, read the measurement in Volt (the current sensor on board has 1V/A gain), with three decimal digits, and report the result in Table 4-4.
16. Use the vertical cursors to measure the average value of input voltage $V_{in,AV}$, in Volt with three decimal digits, calculate the average input power $P_{in,AV} = V_{in,AV}$ x $I_{in,AV}$, in Watt with three decimal digits, and report the result in Table 4-4.

17. Calculate the percent efficiency $\eta = P_{out} / P_{in}$ x 100, with one decimal digit, and report the result Table 4-4.
18. Calculate the value of the load resistor current $I_{o,ON} = V_{out,ON} / R_o$ during the ON time T_{on}, in Ampère with three decimal digits, and report the results in Table 4-4.
19. Calculate the on-state resistance of MOSFET Q1 (high side) $R_{ds(on)} = (V_{in} - V_{out,ON}) / I_{o,ON}$, in Ohm with no decimal digits, and report the result in Table 4-4.
20. Using Equation 1-6, calculate the power loss P_{Q1} of the MOSFET Q1 (high side), in Watt with three decimal digits, and report the result in Table 4-4.
21. Repeat the steps 8-20 for all the values of output voltage V_{out} listed in Table 4-4.
22. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.

Table 4-4 Half-Bridge PWM operation.

$V_{out,AV}$ [Ω]	4	5	6
V_c [V]			
V_c [V] from Theory			
T_{ON} [µs]			
T_{OFF} [µs]			
duty-cycle [%]			
$V_{out,ON}$ [V]			
$V_{out,OFF}$ [V]			
$P_{out,AV}$ [W]			
$I_{in,AV}$ [A]			
$P_{in,AV}$ [W]			
η [%]			
$I_{o,ON}$ [A]			
Q1 $R_{ds(on)}$ [Ω]			
Q1 P_{loss} [W]			

4-1   Are the values of the control voltage you have set to achieve the desired output voltage higher or lower than the calculated values?

A.   higher
B.   lower
C.   other: _____

Please provide your comment: _____

_____

4-2   How does the efficiency change as the output voltage increases?

      A.   it increases
      B.   it decreases
      C.   other: _____

      Please provide your comment: _____

_____

Troubleshooting tips:
- If the MOSFET half-bridge does not work, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiment.

5 Analyze

5-1 Graph the values of the voltage conversion ratio $M = V_{out,AV}/V_{in}$ between the average output voltage $V_{out,AV}$ collected in Table 4-4 and the average input voltage V_{in}, as function of the percent duty-cycle D:
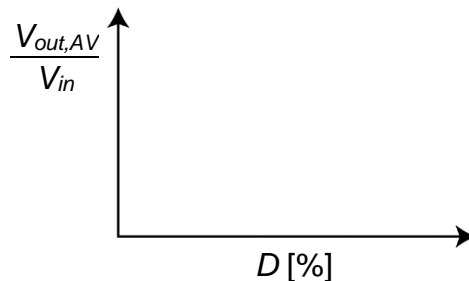
Figure 5-1 Voltage Conversion Ratio of the Half-Bridge as Function of Duty-Cycle.

5-2   Describe the trend of the conversion ratio M you observe, and discuss it based on ***Theory and Background*** equations:

_____

_____

5-3 Graph the values of the % efficiency as function of the average output voltage $V_{out,AV}$ collected in Table 4-4:

η [%]

V_{out} [V]
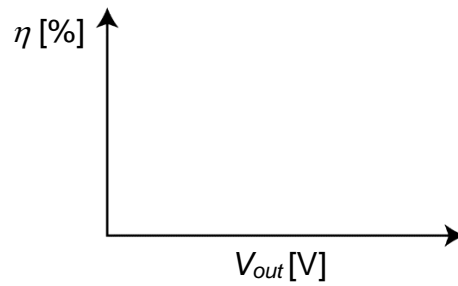
Figure 5-2 Efficiency of the Half-Bridge as Function of Output Voltage.

5-4   Describe the trend of the efficiency you observe, and discuss it based on ***Theory and Background*** equations:

_____

_____

5-5 Graph the values of the MOSFET on-state resistance $R_{ds(on)}$ as function of the power loss P_{loss} collected in Table 4-4:

$R_{ds(on)}$ [Ω]

P_{loss} [W]
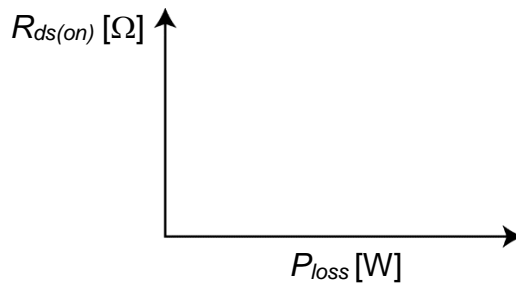
Figure 5-3 MOSFET On-State Resistance as function of power loss.

5-6   Describe the trend of the MOSFET on-state resistance you observe, and discuss it based on ***Theory and Background*** equations:

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the operation of a PWM MOSFET half-bridge, and the impact of the MOSFET on-state resistance on its overall performances. Explain the limits of operation in terms of admissible ranges of values of input and output voltage and current, considering the inherent properties of the half-bridge, of the PWM modulator and of the MOSFETs.

6-2   Expansion Activities

6-2-1. Investigate how the switching frequency influences the PWM operation, by means of simulations and measurements.

- Simulations
    a. Set the source voltage V_{in} at 7V and the PWM control voltage V_c between 0 and V_{rpp}.
    b. Set the load resistance R_o to 50Ω, which is equal to the value of the load resistance used on the **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III.
    c. Set the frequency, amplitude and offset of the triangular carrier signal V_r at 100kHz, 1Vpp and 0.5V respectively.
    d. Set the DC magnitude of the control signal V_c at 0.5V.
    e. Run the simulation, watch and record the average output voltage while increasing the frequency of the triangular carrier signal in 100kHz steps, up to 1MHz.
       You should observe that the frequency does not influence the PWM modulator and the average output voltage.

- Measurements
    a. Follow the instructions provided in *Section 4.1* to setup the **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III.
    b. Set the *Power Supply* voltage at 7V.
    c. Set the frequency, amplitude and offset of the *Function Generator* CH-1 (V_r) at 100kHz, 1Vpp and 0.5V respectively.
    d. Set the frequency, amplitude and offset of the *Function Generator* CH-2 (V_c) at 1Hz, 0Vpp and 0.5V respectively.

e. Run the experiment, watch and record the average output voltage while increasing the frequency of the *Function Generator* CH-1 in 100kHz steps, up to 1MHz.
Due to delay times and other properties of the real PWM modulator and of MOSFET gate drivers, you may observe a change in the average output voltage as the frequency increases. Describe and discuss the differences you observe between simulations and measurements

6-2-2. Run the ***Lab1 – Linear Regulator in Open-Loop DC Operation***, and compare the efficiency performance of a linear regulator to the efficiency performance of the MOSFET half-bridge under similar input and output conditions. The MOSFET of in the Discrete Linear Regulator is the same component used in the half-bridge of the **Discrete Buck Section**.

6-4 Resources for learning more

- This book provides the fundamentals of switching regulators:
  S. Maniktala, *Switching Power Supplies A - Z,* Newness

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   B

1-2   A

1-3   B

1-4   A

1-5   C

1-6   B

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
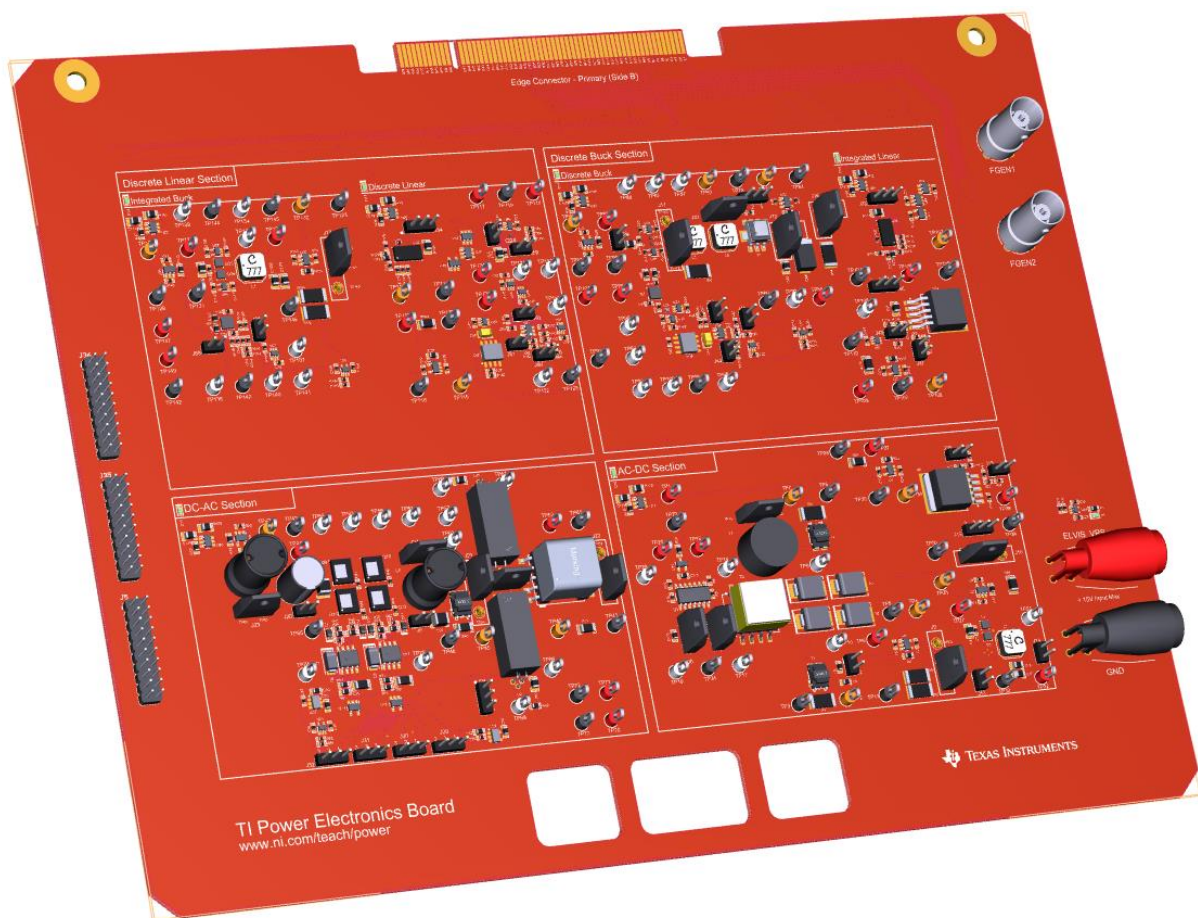
Lab 6: Buck Regulator:

L-C Filter Operation

Lab 6: Buck Regulator L-C Filter Operation

The goal of this lab is to investigate the L-C filter operation in a Buck regulator. In particular, we analyze the behavior of the L-C filter subjected to the square-wave voltage generated by a PWM modulated MOSFETs half-bridge. First, we review the function and the principle of operation of the inductor and of the capacitor in the L-C filter of a buck regulator, to predict the inductor current ripple and the output voltage ripple. Then, we simulate a buck regulator comprised of a MOSFET half-bridge, a PWM modulator, an L-C filter and a load resistor, to verify the consistency of theoretical predictions under different operating conditions. Finally, we perform lab experiments to measure the average output voltage, current and voltage ripple, and efficiency of a buck regulator in open loop operation, and to estimate the parameters of the L-C filter.
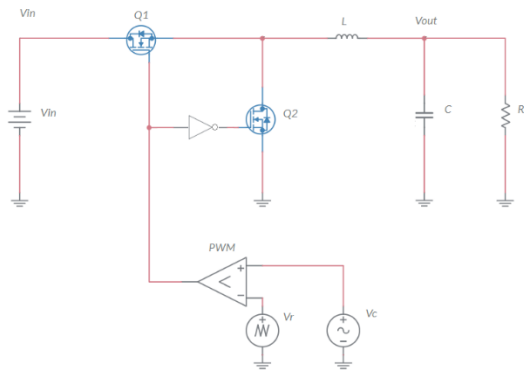
Figure 1-1 Buck Regulator with L-C Filter

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a PWM modulated MOSFET half-bridge, an L-C filter, a source voltage, and a load resistance, you will calculate the peak-peak amplitude of inductor ripple current and output ripple voltage, and the converter efficiency, with specified units and accuracy, by applying the appropriate theoretical equations.
2. Given a PWM modulated MOSFET half-bridge, an L-C filter, a source voltage, and a load resistance, you will simulate the L-C filter behavior to verify the consistency of theoretical predictions, by comparing the simulated and the calculated output voltage under the same operating conditions.
3. Given a real PWM modulated MOSFET half-bridge, an L-C filter, a source voltage, a load resistance, and a two channel function generator, you will measure the converter efficiency and the peak-peak amplitude of inductor ripple current and output ripple voltage, and you will determine the parameters of the inductor and of the capacitor, with specified units and accuracy.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

- ✓ Access Instruments
  https://measurementslive.ni.com/
- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ni-elvis-iii.html
- ✓ View Tutorials
  https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

- ✓ Access
  https://www.multisim.com/
- ✓ View Tutorial
  https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

- ✓ Download (Windows OS Only)
  http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

  Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of the L-C filter in a Buck regulator. The L-C filter is an important functional element of DC-DC voltage regulators, as it integrates energy transfer and noise filtering features.

1-2 Ideal L-C filter operation in the Buck Regulator.

Figure 1-2 shows a MOSFETs half-bridge controlled by a Pulse Width Modulation (PWM) comparator. The carrier signal V_r, and the control signal V_c determine the status of the PWM comparator output. During the time T_{on} we have $V_r < V_c$ and the PWM comparator output is high. Therefore, the Gate Driver sets gate signals G1 and G2 respectively high and low, thus Q1 conducts and Q2 is open. During the time T_{off} we have $V_r > V_c$ and the PWM comparator output is low. Therefore, the Gate Driver sets gate signals G1 and G2 respectively low and high, thus Q1 is open and Q2 conducts. This results in the square-wave half-bridge output voltage V_{out} shown in Figure 1-2. The switching frequency $f_s = 1/T_s$ is determined by the period T_s of the triangular signal V_r.
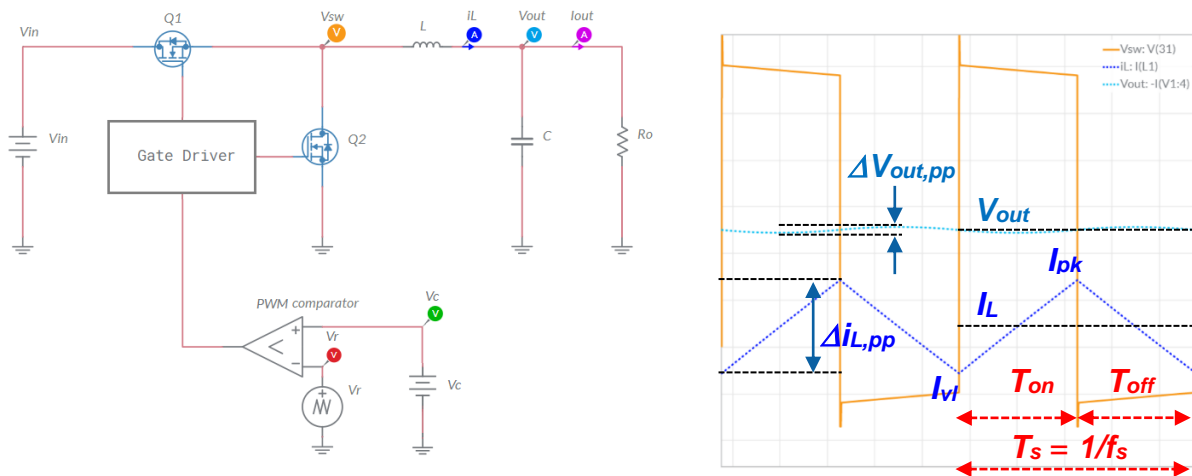
Figure 1-2. Buck Regulator L-C Filter Operation.

The typical waveforms of output voltage and the inductor current of buck regulator in open loop DC operation are shown in Figure 1-2. The peak-peak amplitude of the output voltage AC component $\Delta V_{out,pp}$, defined as *output ripple voltage*, is normally very small

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compared to the average DC component V_{out} (typically, $\Delta V_{out,pp}$ is about 1% of V_{out}), and the output voltage waveform is almost flat. The average DC component I_L of the inductor current equals the average load current $I_{out} = V_{out} / R_o$, as the DC current of the output capacitor is zero. The voltage V_{sw} of the half-bridge is a square wave, switching between V_{in} during the MOSFET Q1 on time T_{on} and zero during the MOSFET Q1 off time T_{off} (see **Lab5** for more details about half-bridge PWM operation). As a consequence, the inductor voltage is a square wave too, switching between V_{in} - V_{out} and - V_{out}. The resulting AC component of the inductor current, defined as *inductor ripple current*, is the triangular waveform with peak-peak amplitude $\Delta i_{L,pp}$ shown in Figure 1-2. The capacitor bypasses the inductor ripple $\Delta i_{L,pp}$. Due to the low pass nature of the L-C filter, the DC average value V_{out} of the capacitor voltage equals the average value of the half-bridge square-wave voltage, $V_{out} = V_{sw,DC} = V_{in} \times D$, where D is the duty-cycle of the half-bridge, defined as $D = T_{on} / (T_{on} + T_{off}) \cong V_{out}/V_{in}$ (see **Lab5**). The resulting theoretical peak-peak amplitudes of inductor ripple current and output ripple voltage are given by Equations 1-1:

Equations 1-1
$$\Delta i_{L,pp} = \frac{D(V_{in} - V_{out})}{f_s L} = \frac{V_{out}(V_{in} - V_{out})}{V_{in} f_s L} \qquad \Delta V_{out,pp} = \frac{\Delta i_{L,pp}}{8 f_s C}$$

where f_s is the switching frequency, L is the inductance of the inductor and C is the capacitance of the capacitor. The peak-peak amplitude of inductor ripple current $\Delta i_{L,pp}$ is normally comparable to the DC component I_L (typically, it is about 50% of I_L). Equations 1-1 and 1-2 show that:

a. given the switching frequency f_s, the DC input voltage V_{in} and the DC output voltage V_{in}, the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ is bigger if the inductance L is smaller;

b. given the switching frequency f_s and the inductor ripple current $\Delta i_{L,pp}$, the peak-peak amplitude of the capacitor ripple voltage $\Delta V_{out,pp}$ is bigger if the capacitance C is smaller;

c. given the DC input voltage V_{in}, the DC output voltage V_{in}, the inductance L and the capacitance C, the peak-peak amplitude of inductor ripple current $\Delta i_{L,pp}$ and capacitor ripple voltage $\Delta V_{out,pp}$ is smaller if the switching frequency is higher.

From Equations 1-1 we can derive the values of the inductance L and capacitance C needed to obtain a desired inductor ripple current $\Delta i_{L,pp}$ and capacitor ripple voltage $\Delta V_{out,pp}$, given the DC input voltage V_{in}, the DC output voltage V_{in} and the switching frequency f_s:

Equations 1-2
$$L = \frac{V_{out}(V_{in} - V_{out})}{V_{in} f_s \Delta i_{L,pp}} \qquad C = \frac{\Delta i_{L,pp}}{8 f_s \Delta V_{out,pp}}$$

1-3 Effects of MOSFET, inductor and capacitor resistance.

Real MOSFETs, inductors and capacitors have a parasitic resistance, causing power losses and influencing the inductor ripple current and capacitor ripple voltage. The ohmic power losses of MOSFET, inductor and capacitor are given by Equations 1-3:

$$P_{Q1} = R_{ds(on)}^{Q1} D I_L^2 \alpha; \; P_{Q2} = R_{ds(on)}^{Q2}(1-D)I_L^2\alpha; \; P_L = R_L I_L^2 \alpha; \; P_C = R_C \frac{\Delta i_{Lpp}^2}{12}; \; \alpha = \left(1 + \frac{\Delta i_{Lpp}^2}{12 I_L^2}\right)$$

where $R_{ds(on)}^{Q1}$ and $R_{ds(on)}^{Q2}$ are the On-State resistances of MOSFETs Q_1 and Q_2 (see **Lab5**), while R_L and R_C are the inductor and capacitor resistances. The theoretical value of ripple current $\Delta i_{L,pp}$ given by Equations 1-1 can be used in Equations 1-3 to estimate power losses. The resulting efficiency η of the buck regulator is given by Equation 1-4:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}; \qquad P_{out} = \frac{V_{out}^2}{R_o} \qquad P_{loss} = P_{Q1} + P_{Q2} + P_L + P_C$$

The values of $\Delta i_{L,pp}$ and $\Delta v_{out,pp}$ including the effects of losses are given by:

$$\Delta i_{L,pp} \cong \frac{V_{out}(V_{in} - V_{out} - (R_{ds(on)}^{Q1} + R_L)I_{out})}{\eta V_{in} f_s L}$$

1-4 Ripple voltage of ceramic and electrolytic capacitors.

Given the inductor ripple current, the output ripple voltage is determined by the characteristics of the capacitor. Figure 1-3 shows the typical waveforms of ripple voltage generated by ceramic and electrolytic capacitors, the two types of capacitors majorly used in switching regulators applications.
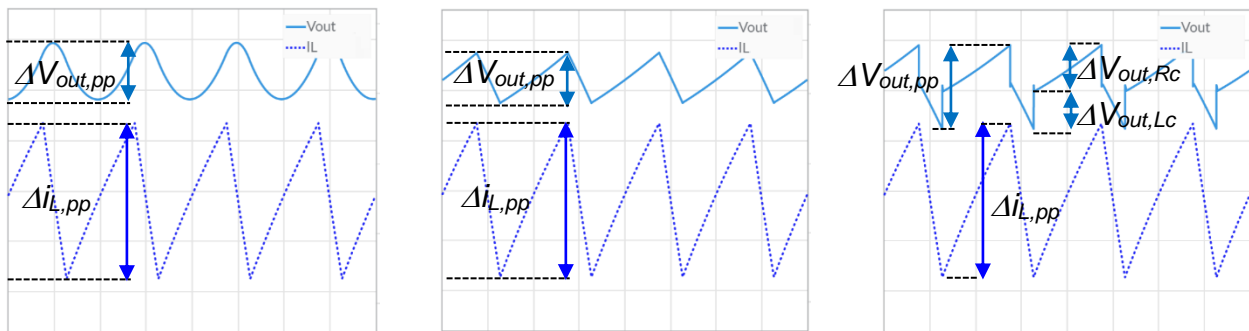
Figure 1-3. Output Ripple Voltage Waveforms for (a) Ceramic Capacitor, (b) Electrolytic Capacitor, (c) Electrolytic Capacitor with Effect of Parasitic Inductance.

The ripple voltage of ceramic capacitors is mainly determined by their capacitance (Figure 1-3(a)). The ripple voltage of electrolytic capacitors is mainly determined by their resistance (Figure 1-3(b)), and is influenced by their parasitic inductance L_c, which generates an additional

square-wave ripple $\Delta V_{out,Lc}$ (Figure 1-3(c)). The simplified Equations 1-6 can be used to calculate the amplitude of peak-peak ripple voltage of ceramic and electrolytic capacitors:

Equations 1-6
$$\Delta V_{out,pp} \cong \begin{cases} \dfrac{\Delta i_{L,pp}}{8 f_s C} & \text{ceramic capacitors} \quad \left(R_C = \dfrac{1}{2\pi f_s C} \right) \\[2ex] \Delta V_{out,Rc} + \Delta V_{out,Lc} = R_c \Delta i_{L,pp} + \dfrac{L_c}{L} V_{in} & \text{electrolytic capacitors} \quad \left(R_C \ ? \ \dfrac{1}{2\pi f_s C} \right) \end{cases}$$

A more general formula of output ripple voltage can be derived for other types of capacitors having a resistance R_C comparable to the reactance $1/(2\pi f_s C)$.

1-5 MOSFETs switching losses.

The MOSFETs Q_1 and Q_2 of the half-bridge generate *switching losses* during their on-off and off-on commutations, given by Equation 1-7:

Equations 1-7
$$P_{Q1,sw} \cong \begin{cases} \frac{1}{2}(V_{in} + V_F) f_s (I_{vl} t_{sw,on} + I_{pk} t_{sw,off}) & I_{vl} > 0 \\[1ex] \frac{1}{2}(V_{in} + V_F) f_s I_{pk} t_{sw,off} & I_{vl} \leq 0 \end{cases} \qquad P_{Q2,sw} \cong \begin{cases} 0 & I_{vl} \geq 0 \\[1ex] \frac{1}{2}(V_{in} + V_F) f_s |I_{vl}| t_{sw,off} & I_{vl} < 0 \end{cases}$$

where $I_{vl} = I_L - \Delta i_{L,pp}/2$ and $I_{vl} = I_L + \Delta i_{L,pp}/2$, V_F is the forward voltage of MOSFETs body diodes, $t_{sw,on}$ and $t_{sw,off}$ are the times the MOSFET needs to turn on and turn off, respectively,. The MOSFET $t_{sw,on}$ and $t_{sw,off}$ times depend on MOSFET parasitic capacitances, gate-to-source voltage threshold V_{th}, transconductance coefficient β (see **Lab1**) and gate driver voltage V_{dr}. The switching losses $P_{Q1,sw}$ can be added to the losses in Equation 1-5 to obtain a more accurate estimation of efficiency. The switching losses are important if the MOSFETs $t_{sw,on}$ and $t_{sw,off}$ switching times are long (this happens in MOSFETs with current ratings in the range of tens of Ampère, which are characterized by big parasitic capacitances) and if the switching frequency is high (this happens in buck regulators operating in the range of tens to hundreds milli Ampère, where the switching frequency can be high in the MHz range).

1-6 Inductor core losses.

Inductors are composed of a copper wire coil wounded around a magnetic core. The copper coil determines the resistance R_L of the inductor, which causes ohmic losses. The magnetic core also generates power loss, which is modeled by the Steinmetz Equation 1-8:

Equation 1-8
$$P_{L,core} \cong K_{fe} f_s^x \Delta i_{L,pp}^y$$

where the parameters K_{fe}, x and y depend on the material, shape and size of the magnetic core. The inductor core loss can influence the converter efficiency for high switching frequency and high ripple operating conditions.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What parameter determines the inductor ripple current in the buck regulator?
  A. the capacitance
  B. the inductance
  C. the average output current

1-2 What parameter determines the output ripple voltage in the buck regulator?
  A. the average output voltage
  B. the inductance
  C. the capacitance

1-3 What is the effect on the inductor ripple current and output ripple voltage in the buck regulator determined by an increase of the switching frequency?
  A. both ripples increase
  B. both ripples decrease
  C. the inductor ripple current increases and the output capacitor voltage decreases

1-4 What is the effect of a higher inductor resistance on the buck converter efficiency?
  A. the efficiency increases
  B. the efficiency decreases
  C. there is no effect

1-5 Does the resistance of the capacitor influence the amplitude of the inductor ripple current?
  A. yes
  B. it depends on the average output voltage
  C. no

1-6 What parameter does majorly influence the amplitude of output voltage ripple if an electrolytic capacitor is used?
  A. the switching frequency
  B. the resistance of the capacitor
  C. the load current

2 Exercise

TI's CSD15380F3 (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf) MOSFET is used for Q_1 and Q_2 in the **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III. The MOSFET has the following nominal parameters: V_{th} = 1.1V, β = 0.24A/V^2, λ = 0.02V^{-1}. The MOSFET is also characterized by the following parameters under the operating conditions determined by the setup of the **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III: $R_{ds(on)}$ = 1.2Ω, $t_{sw,on} \cong$ 0.2ns, $t_{sw,off}$ =0.3ns. The inductor can be set with the following two options: (a) L=15µH, R_L=140mΩ, (b) L=48µH, R_L=400mΩ, and the capacitor can be set with the following two options: (a) C=100µF, R_c=55mΩ, (b) C=10µF, R_c=5mΩ.

2-1 Assuming V_{in}= 7V, V_{out}= 5.0V, f_s = 200kHz, and selecting option (b) for the inductor setup and option (b) for the capacitor setup, use the equations provided in the **Theory and Background** section to calculate:

- the average inductor ripple current, in milli Ampère with one decimal digit:
  I_L = _____
- the peak-peak amplitude of the ideal inductor ripple current, in milli Ampère with one decimal digit: $\Delta i_{L,pp(ideal)}$ = _____
- the peak-peak amplitude of the ideal output ripple voltage, in milli Volt with one decimal digit: $\Delta v_{o,pp(ideal)}$ = _____

2-2 Using the results of ripple calculations from 2-1 and equations provided in the **Theory and Background** section, calculate the power loss of MOSFETs Q_1 and Q_2, inductor and capacitor, in milli Watt with three decimal digits, and report the results in Table 2-1:

Table 1-1 Power losses of MOSFETs, inductor and capacitor of Buck Regulator in DC Operation.

	MOSFET Q_1 ohmic loss	MOSFET Q_1 switching loss	MOSFET Q_2 ohmic loss	MOSFET Q_2 switching loss	inductor ohmic loss	capacitor ohmic loss
loss [mW]						

2-3 Using the results obtained from previous point 2-1, and the equations provided in the **Theory and Background** section, calculate the efficiency $\eta = P_{out} / (P_{out}+P_{loss})$, with three decimal digits, the peak-peak inductor ripple current and the average input current $I_{in} = P_{in}/V_{in} = (P_{out}+P_{loss}) / V_{in}$, in milli Ampère with one decimal digit:

η = _____ $\Delta i_{L,pp(real)}$ = _____

I_{in} = _____

3 Simulate

The goal of the simulations in this section is to analyze the operation of the L-C filter of a Buck Regulator under DC open loop conditions. You will verify the consistency of the perk-peak amplitude of inductor ripple current and output ripple voltage and of efficiency calculated in the **Exercise** Section. You will also observe the inductor current and output voltage waveforms under different operating conditions.

3-1 Instructions

1. Open *Lab6 – Buck Regulator L-C Filter Operation* from this file path:
   https://www.multisim.com/content/bdUiT8S52XAVbZkFwhgY44/lab
   -6-buck-regulator-l-c-filter-operation/. The circuit schematic for the analysis of the Buck Regulator L-C filter operation is shown in Figure 3-1.
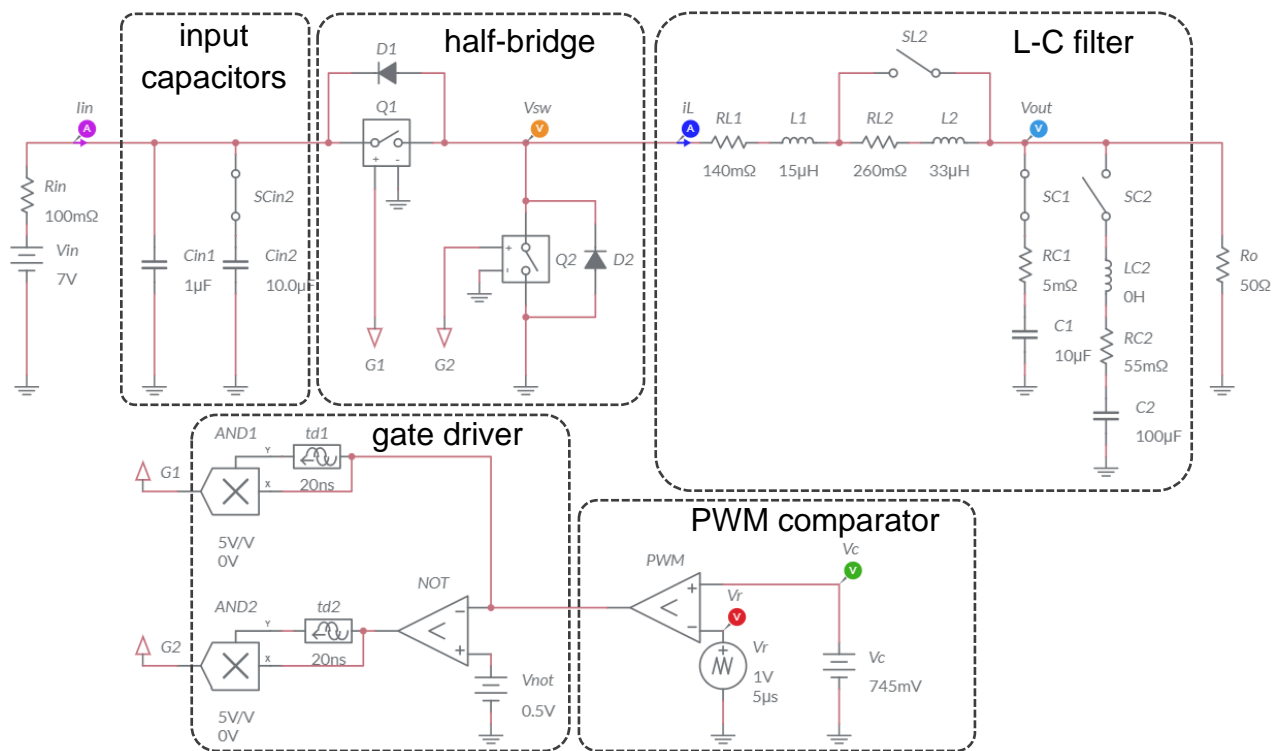
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Buck Regulator L-C Filter.

The L-C filter is configurable by means of switches SL1, SC1 and SC2 as follows:

- SL2 closed: $L = L_1 = 15\mu H$, $R_L = R_{L1} = 140m\Omega$;
- SL2 open: $L = L_1 + L_2 = 48\mu H$, $R_L = R_{L1} + R_{L2} = 400m\Omega$;
- SC1 closed, SC2 open: $C = C_1 = 10\mu F$, $R_c = R_{C1} = 5m\Omega$;
- SC2 closed, SC1 open: $C = C_2 = 100\mu F$, $R_c = R_{C2} = 55m\Omega$.

[**Notes: 1)** the input capacitors C_{in1} and C_{in2} are normally included in buck regulators to obtain an input current I_{in} with a small amplitude ripple; **2)** the model of capacitor C_2 includes a parasitic inductance L_{C2} initially set at 0H].

2. Set SL2 to be OPEN, SC1 to be CLOSED, SC2 to be OPEN and SCin2 to be CLOSED.
3. Select *Interactive* simulation and *Split* visualization options.
4. Check the *Periodic* option box for voltage probe V_{out} and current probes i_L and I_{in} in *Measurement labels* menu.
5. Set the simulation circuit parameters as follows:
   - V_{in}: *DC_mag* = 7.0V;
   - V_r: *VA* = 1V, *Per* = 5µs, *TF* = 2.5µs, Offset 0V;
   - R_o: 50Ω;
   - V_c: *DC_mag* = 745mV
6. Run the simulation and wait until it ends.
7. Read the average value V_{AV} displayed by the output voltage probe V_{out}, in Volt with four decimal digits, and report the result in Table 3-1.
8. Read the peak-peak value V_{pp} displayed by the output voltage probe V_{out}, in milli Volt with one decimal digit, and report the result in Table 3-1.
9. Read the average value I_{AV} displayed by the inductor current probe i_L, in milli Ampère with one decimal digit, and report the result in Table 3-1.
10. Read the peak-peak value I_{pp} displayed by the inductor current probe i_L, in milli Ampère with one decimal digit, and report the result in Table 3-1.
11. Read the average value I_{AV} displayed by the input current probe I_{in}, in milli Ampère with one decimal digit, and report the result in Table 3-1.
12. Calculate the efficiency η = ($V_{out}I_{out}$) / ($V_{in}I_{in}$), with three decimal digits, and report the result in Table 3-1.
13. Import in Table 3-1 the values of V_{out}, $\Delta V_{out,pp}$, I_{out}, $\Delta i_{L,pp}$, I_{in} and η obtained in the **Exercise** calculations

Table 3-1 L-C filter operation and converter efficiency with L = 48µH, R_L = 400mΩ; C = 10µF, R_c = 5mΩ.

	V_{out} [V]	$\Delta V_{out,pp}$ [mV]	$I_L = I_{out}$ [mA]	$\Delta i_{L,pp}$ [mA]	I_{in} [mA]	η
from simulations						
from calculations						

14. Enter the simulation results from Table 3-1 in the first row of Table 3-2.
15. Re-run the simulation using the switch setups listed in Table 3-2, and report the resulting values of V_{out}, $\Delta V_{out,pp}$, I_{out}, $\Delta i_{L,pp}$, I_{in} and η.

Table 3-2 L-C filter operation and converter efficiency under different filter setup.

	SL2	SC1	SC2	V_{out} [V]	$\Delta V_{out,pp}$ [mV]	$I_L = I_{out}$ [mA]	$\Delta i_{L,pp}$ [mA]	I_{in} [mA]	η
(a)	open	closed	open	5.0084	8.8	100.3	140.4	74.6	0.962
(b)	closed	closed	open	5.0570	28.0	101.1	445.6	78.5	0.930
(c)	open	open	closed	5.0072	7.8	101.2	140.3	75.3	0.961
(d)	closed	open	closed	5.0560	25.0	102.2	444.4	79.3	0.930

3-1   Do the simulations match the calculations in Table 3-1?

A.   yes

B.   no

Please provide your comments: _____

_____

3-2   Is the peak-peak amplitude of the output ripple voltage small compared to the average output voltage?

A.   yes

B.   no

why? _____

_____

3-3   What switch setup determines the smallest peak-peak amplitude of inductor ripple current in Table 3-2?

(a)   ☐

(b)   ☐

(c)   ☐

(d)   ☐

why? _____

_____

3-3   What switch setup determines the biggest peak-peak amplitude of output ripple voltage in Table 3-2?

(a)   ☐
(b)   ☐
(c)   ☐
(d)   ☐
why? _____

_____

Troubleshooting tips:
- If the simulation does not converge and you get some error message, reload *Lab6 – Buck Regulator L-C Filter Operation* from this file path https://www.multisim.com/content/sRY9ZW7saFpr4MKWu2a5A5/lab-5-buck-regulator-half-bridge-pwm-operation/ and restart the simulation following the instructions.

4 Implement

The experiments in this section allow you to observe the behavior of the L-C filter of a buck regulator in steady-state operation. You will measure the peak-peak amplitudes of inductor ripple current and output ripple voltage, under different conditions. Then, you will use the measurements to estimate the inductance of the inductor, and the capacitance, the resistance and the parasitic inductance of capacitors. Finally, you will measure the efficiency of the buck regulator. The **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments. [**Note:** The max input voltage V_{in} is 12V]. A 50Ω resistance R_o can be connected to the output of the L-C filter by means of the Jumper J16. The TI's CSD15380F3 half-bridge MOSFETs are characterized by a typical 1.2Ω on-state resistance at 4.5V gate-to-source voltage. The PWM modulator uses a TI's TLV7011DPWR comparator, and the half-bridge MOSFET gate driver is a TI's TPS51601ADRBR. The links to the datasheets are available below:

- CSD15380F3 MOSFET: (http://www.ti.com/lit/ds/symlink/csd15380f3.pdf)
- TLV7011DPWR COMPARATOR: (http://www.ti.com/lit/ds/symlink/tlv7011.pdf)
- TPS51601ADRBR GATE DRIVER: (http://www.ti.com/lit/ds/symlink/tps51601a.pdf).

The L-C filter is configurable by means of jumpers J39 and J12 as follows:

- J39 closed: $L = 15\mu H$, $R_L = 140m\Omega$;
- J39 open: $L = 48\mu H$, $R_L = 400m\Omega$;

- J12 shorting TP161-TP159: $C = 10\mu F$, $R_c = 5m\Omega$ (ceramic capacitor);
- J12 shorting TP161-TP160: $C = 100\mu F$, $R_c = 55m\Omega$ (electrolytic capacitor).
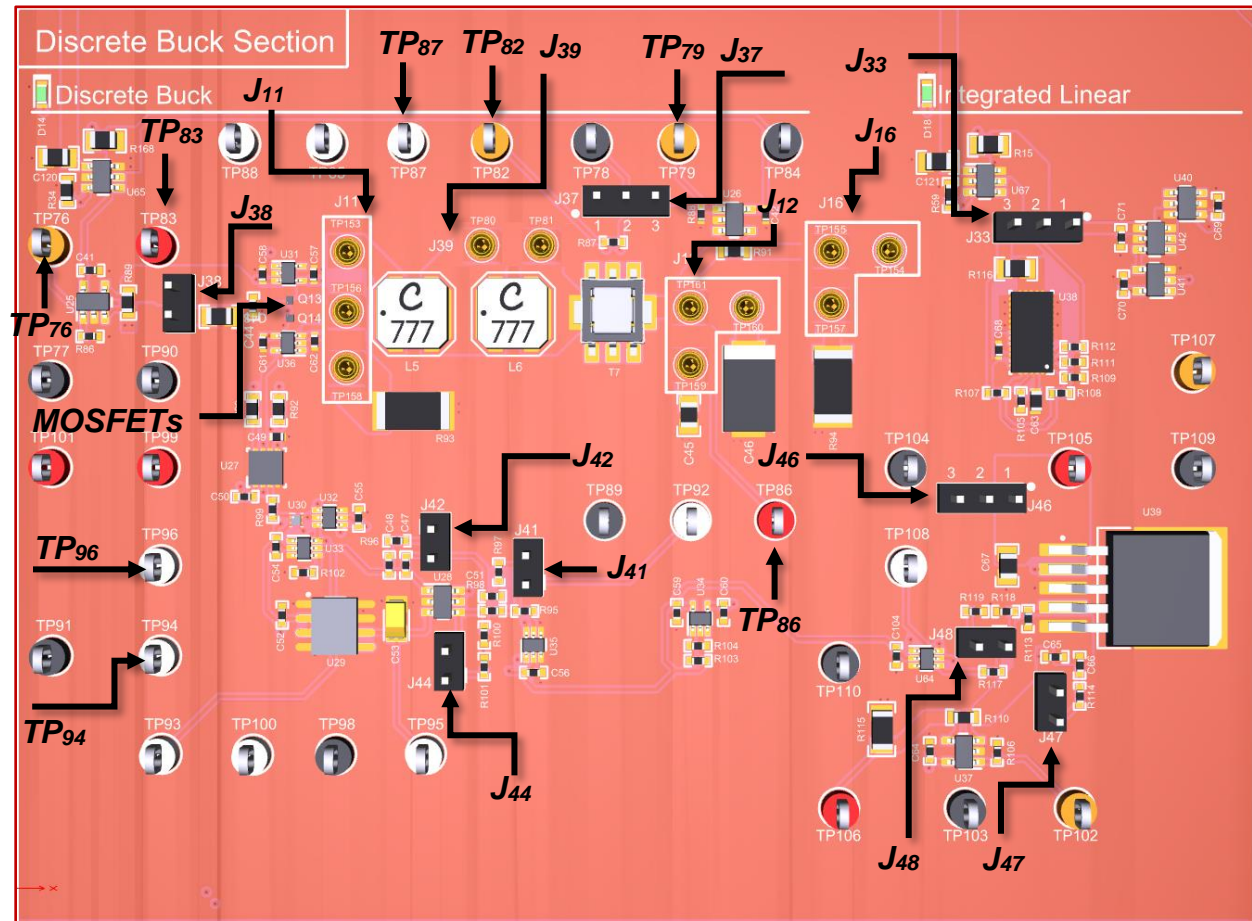
Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Buck Section Used for the Analysis of Buck Regulator L-C Filter Operation.

The board uses a current sensing transformer and a resistor (T7 and R87 shown in Figure 4-1) to sense the inductor ripple current. The transformer generates a voltage test point TP82, that can be measured by means of a voltage probe. As the voltage-to-current transconductance of the sensing transformer is 0.5, dividing the voltage measured at test point TP82 by 2 provides the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$. [**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 General Instructions

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter* using Measurements Live. For help on launching instruments, refer to this help

document:

2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.

4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab6 – Buck Regulator L-C Filter Operation*.

4-2 Experiment 1 Instructions

1. Configure the jumpers of the board as indicated in Table 4-2-1.
2. Connect and configure the instruments as indicated in Tables 4-2-2 and 4-2-3.

Table 4-2-1 Jumpers setup

J11	J12	J16	J33	J37	J38
short TP156-TP153	short TP160-TP161	short TP155-TP157	short 2-3	short 1-2	short
J39	J41	J42	J44	J46	J47	J48
open	short	short	short	short 2-3	short	open

Table 4-2-2 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP83 (V_{in}), connect CH-2 to TP86 (V_{out}) connect CH-3 to TP87 (V_{sw}), connect CH-4 to TP82 (I_L)
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP94 = PWM comparator V_r) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP96 = PWM comparator V_c)
Digital Multimeter	connect Voltage input to TP86 (V_{out}), TP82 (I_L) or TP76 (I_{in}), as per instructions

Table 4-2-3 Instruments Configuration and setup

Power Supply	Channel *"+"*: Static, 7.00V, Channel *"-"*: Inactive			
Oscilloscope	*Trigger*: Analog Edge, CH-3, set to 50%	*Horizontal*: 2us/div	*Acquisition*: average	*Measurements*: show
	Channel 1: ON • DC coupling • 1V/div • offset -4V	*Channel 2*: ON • DC coupling • 10mV/div • offset -5.0V	*Channel 3*: ON • DC coupling • 1V/div • offset -4V	*Channel 4*: ON • DC coupling • 100mV/div offset 0V
Function Generator	*Channel 1*: Triangle, Frequency 200kHz, Amplitude 1Vpp, DC offset 0.5V			

	Channel 2: Sine, Frequency 1Hz, Amplitude 0Vpp, DC offset 855mV
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: Automatic

3. Using the *Oscilloscope* cursors in *Manual Mode*:
   - measure the peak-peak amplitude of the output ripple voltage $\Delta v_{out,pp}$ on CH-2, in milli Volt with one decimal digit of accuracy, and report the result in Table 4-2-4 [**Notes: 1)** if the ripple voltage waveform is as shown in Figure 1-3(c), measure the amplitude of the steep front $\Delta v_{out,Lc}$ and the amplitude of the rising ramp portion $\Delta v_{out,Rc}$ separately; **2)** neglect the high-frequency noise, and measure the peak-peak amplitude of the ripple voltage waveforms as shown in Figure 1-3];
   - measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on CH-4, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-2-4.
4. Connect *Digital Multimeter* to TP79, measure the average output current I_{out}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-2-4;
5. Connect *Digital Multimeter* to TP76, measure the average input current I_{in}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-2-4;
6. Calculate the efficiency $\eta = (V_{out}I_{out})/(V_{in}I_{in})$, with three decimal digits, and report the result in Table 4-2-4.
7. Calculate the inductance of the inductor $L = V_{out}(V_{in}-V_{out}-(R_{dson}+R_L)I_{out})/(\eta V_{in}f_s\Delta i_{L,pp})$, in micro Henry with three decimal digits, and report the result in Table 4-2-4;
8. If the ripple voltage waveform looks like in Figure 1-3(a), calculate the capacitance of the capacitor $C = \Delta i_{L,pp}/(8f_s\Delta v_{out,pp})$, in micro Farad with three decimal digits, and report the result in Table 4-2-4.
9. If the ripple voltage waveform looks like in Figure 1-3(b), calculate the resistance of the capacitor $R_C = \Delta V_{out,pp}/\Delta i_{L,pp}$, in milli Ohm with no decimal digits, and report the result in Table 4-2-4.
10. If the ripple voltage waveform looks like in Figure 1-3(c), calculate the parasitic inductance of the capacitor $L_C = L\Delta V_{out,Lc}/V_{in}$, in nano Henry with no decimal digits, and the resistance of the capacitor $R_C = \Delta V_{out,Rc}/\Delta i_{L,pp}$, in milli Ohm with no decimal digits, where L is the inductance of the inductor from step 7, and report the results in Table 4-2-4.
11. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.
12. Repeat the steps 3-14 for all the jumpers setups listed in Table 4-2-4.

Table 4-2-4 L-C filter operation and converter efficiency under different filter setup.

	J12	J39	η	$\Delta i_{L,pp}$ [mA]	$\Delta V_{out,pp}$ [mV]	$\Delta V_{out,Lc}$ [mV]	$\Delta V_{out,Rc}$ [mV]	L [µH]	C [µF]	R_c [mΩ]	L_c [nH]
(a)	short TP159-TP161	open									
(b)	short TP159-TP161	closed									
(c)	short TP160-TP161	open									
(d)	short TP160-TP161	closed									

4-2-1 Are the values of inductance *L* of the inductor determined from experimental measurements close to the nominal values?

  A.   yes
  B.   no
  C.   other: _____

  Please provide your comments: _____

  _____

4-2-2 Is the shape of the output ripple voltage the same for the two capacitors?

  A.   yes
  B.   no
  C.   other: _____

  Please provide your comments: _____

  _____

4-2-3 Given an inductor setup, what is the capacitor determining the biggest peak-peak amplitude of the output ripple voltage?

  A.   the 10µF capacitor
  B.   the 100µF capacitor
  C.   other: _____

  Please provide your comments: _____

  _____

4-2-4 For what capacitor did you observe the shape of the output ripple voltage waveform showing the effect of parasitic inductance?

    A.   the 10µF capacitor
    B.   the 100µF capacitor
    C.   other: _____

    Please provide your comments: _____

_____

4-2-5 Does the parasitic inductance of the capacitor change with the setup of the main inductor?

    A.   yes
    B.   no
    C.   other: _____

    Please provide your comments: _____

_____

4-3 Experiment 2 Instructions

1. Configure the jumpers of the board as indicated in Table 4-3-1.

Table 4-3-1 Jumpers setup

J11	J12	J16	J33	J37	J38
short TP156-TP153	short TP159-TP161	short TP155-TP157	short 2-3	short 1-2	short
J39	J41	J42	J44	J46	J47	J48
short	short	short	short	short 2-3	short	open

2. Connect and configure the instruments as indicated in Tables 4-3-2 and 4-3-3.

Table 4-3-2 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP83 (V_{in}), connect CH-2 to TP86 (V_{out}) connect CH-3 to TP87 (V_{sw}), connect CH-4 to TP79 (I_L)
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP94 = PWM comparator V_r) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP96 = PWM comparator V_c)
Digital Multimeter	connect Voltage input to TP86 (V_{out})

Table 4-3-3 Instruments Configuration and setup

Power Supply	Channel "+": Static, 7.00V, Channel "-": Inactive			
Oscilloscope	Trigger: Analog Edge, CH-3, set to 50%	Horizontal: 2us/div	Acquisition: average	Measurements: show
	Channel 1: ON • DC coupling • 1V/div • offset -4V	Channel 2: ON • DC coupling • 1V/div • offset -4V	Channel 3: ON • DC coupling • 1V/div • offset -4V	Channel 4: ON • DC coupling • 500mV/div offset 0V
Function Generator	Channel 1: Triangle, Frequency 200kHz, Amplitude 6.0Vpp, DC offset 3.0V Channel 2: Sine, Frequency 1Hz, Amplitude 0Vpp, DC offset 1.0V			
Digital Multimeter	Measurement mode: DC voltage; Range: Automatic			

3. Set the *Function Generator* CH-2 DC offset to 1.0V (PWM control voltage V_c).
4. Run *Oscilloscope*, *Digital Multimeter*, *Function Generator* and *Power Supply*.
5. Read the *Digital Multimeter* measurement of output voltage V_{out}, in Volt with three decimal digit of accuracy, and report the result in Table 4-3-4.
6. Repeat step5, setting the *Function Generator* CH-2 DC offset to the values of the PWM control voltage V_c listed in Table Table 4-3-4, and report the results in Table 4-3-4.
7. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.
8. Using the equations provided in **Theory and Background** Section, calculate the duty-cycle D, with tree decimal digits of accuracy, the theoretical output voltage V_{out}, in Volt with three decimal digits of accuracy, for each value of the PWM control voltage V_c, and report the results in Table 4-3-4.

Table 4-3-4 Output Voltage of Buck Regulator under Different Duty-Cycle Conditions.

V_c [V]	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0
D									
V_{out} [V] (measured)									
V_{out} [V] (calculated)									

4-3-1 Are the measurements and calculations trends consistent?

    A.   yes

    B.   no

    C.   other: _____

    Please provide your comments: _____

_____

4-3-2 Are the measured values of average output voltage greater or lower than the calculated values?

    A.   greater
    B.   lower
    C.   other: _____

Please provide your comments: _____

_____

Troubleshooting tips:

- If the regulator does not work, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiment.

5 Analyze

5-1 Using the results collected in Table 4-2-4, analyze the values of efficiency versus peak-peak amplitude of inductor ripple current, and discuss the correlation among these values based on *Theory and Background* equations:

_____

_____

_____

5-2 Using the results collected in Table 4-3-4, graph the values of voltage conversion ratio $M = V_{out}/V_{in}$, as function of the duty-cycle D, comparing measurements and calculations:
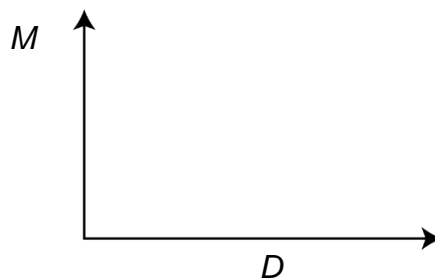
Figure 5-1 Voltage Conversion Ratio of Buck Regulator as Function of Duty-Cycle.

5-3   Discuss the differences between calculated and measured data, based on *Theory and Background* equations:

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the buck regulator L-C filter operation, discussing the impact of the inductor an capacitor parameters on the peak-peak amplitude of inductor ripple current and output ripple voltage, and on the buck regulator efficiency.

6-2   Expansion Activities

6-2-1. Investigate the influence of switching frequency on L-C filter operation, by means of TI Power Electronics Board for NI ELVIS III of Figure 4-1.
   a. Use the same connections and configurations indicated in Tables 4-1 and 4-2.
   b. Use the jumpers configuration adopted for test (d) of Table 4-4.
   c. Set the Frequency of *Function Generator* CH-1 at 250kHz.
   d. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
   e. Using the *Oscilloscope* cursors in *Manual Mode*:
   - measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on CH-4, in milli Ampère with one decimal digit of accuracy, and report the result in Table 6-1;

   - measure the peak-peak amplitude of the output ripple voltage $\Delta v_{out,pp}$ on CH-2, in milli Volt with one decimal digit of accuracy, and report the result in Table 6-1.

   f. Repeat step e. for all the values of the Frequency of *Function Generator* CH-1 listed in Table 6-1.
   g. Stop *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 6-1 Peak-peak amplitude of inductor ripple current and output ripple voltage versus the switching frequency

f [kHz]	250	300	350	400	450	500
$\Delta i_{L,pp}$ [mA]						
$\Delta v_{out,pp}$ [mV]						

6-1 Analyze the values of peak-peak amplitude of inductor ripple current and output ripple voltage as the switching frequency increases and discuss them based on **_Theory and Background_** equations:

_____

_____

_____

6-2-2. Investigate the influence of input voltage on L-C filter operation, by means of TI Power Electronics Board for NI ELVIS III of Figure 4-1.
   a. Use the same connections and configurations indicated in Tables 4-2-1 and 4-2-2.
   b. Use the jumpers configuration adopted for test (c) of Table 4-2-4.
   c. Set the voltage of _Power Supply_ at 6.0V.
   d. Run _Oscilloscope_, _Function Generator_ and _Power Supply_.
   e. Using the _Oscilloscope_ cursors in _Manual Mode_:
   - measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on CH-4, in milli Ampère with one decimal digit of accuracy, and report the result in Table 6-2;
   - measure the peak-peak amplitude of the output ripple voltage $\Delta v_{out,pp}$ on CH-2, in milli Volt with one decimal digit of accuracy, and report the result in Table 6-2.
   f. Repeat step e. for all the values of the _Power Supply_ voltage listed in Table 6-2.
   g. Stop _Power Supply_, _Function Generator_ and _Oscilloscope_.

Table 6-2 Peak-peak amplitude of inductor ripple current and output ripple voltage versus the input voltage

V_{in} [V]	6.0	6.5	7.0	7.5	8.0	8.5
$\Delta i_{L,pp}$ [mA]						
$\Delta v_{out,pp}$ [mV]						

6-2 Analyze the values of peak-peak amplitude of inductor ripple current and output ripple voltage as the input voltage increases and discuss them based on **_Theory and Background_** equations:

_____

_____

_____

6-2-3. Verify the influence of parasitic inductance on the output ripple voltage waveform and peak-peak amplitude, using the Multisim Simulation Schematic of Figure 3-1.

a. Follow the simulation instructions provided in Section 3-1.
b. Before running the simulation, set the switches SL2, SC1 and SC2 corresponding to filter configuration (c) or (d) of Table 4-4, and set the value of the inductance LC2 in series to the capacitor C2 equal to the corresponding value L_c recorded in Table 4-4.
c. Run the simulation, and measure the peak-peak amplitude or output ripple voltage using the *Grapher* cursor on the output voltage trace
d. Compare the result with the corresponding measured value recorded in Table 4-4.

6-3   Resources for learning more

● This book provides the fundamentals of switching regulators:
S. Maniktala, *Switching Power Supplies A - Z,* Newness

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   B

1-2   C

1-3   B

1-4   B

1-5   C

1-6   B

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
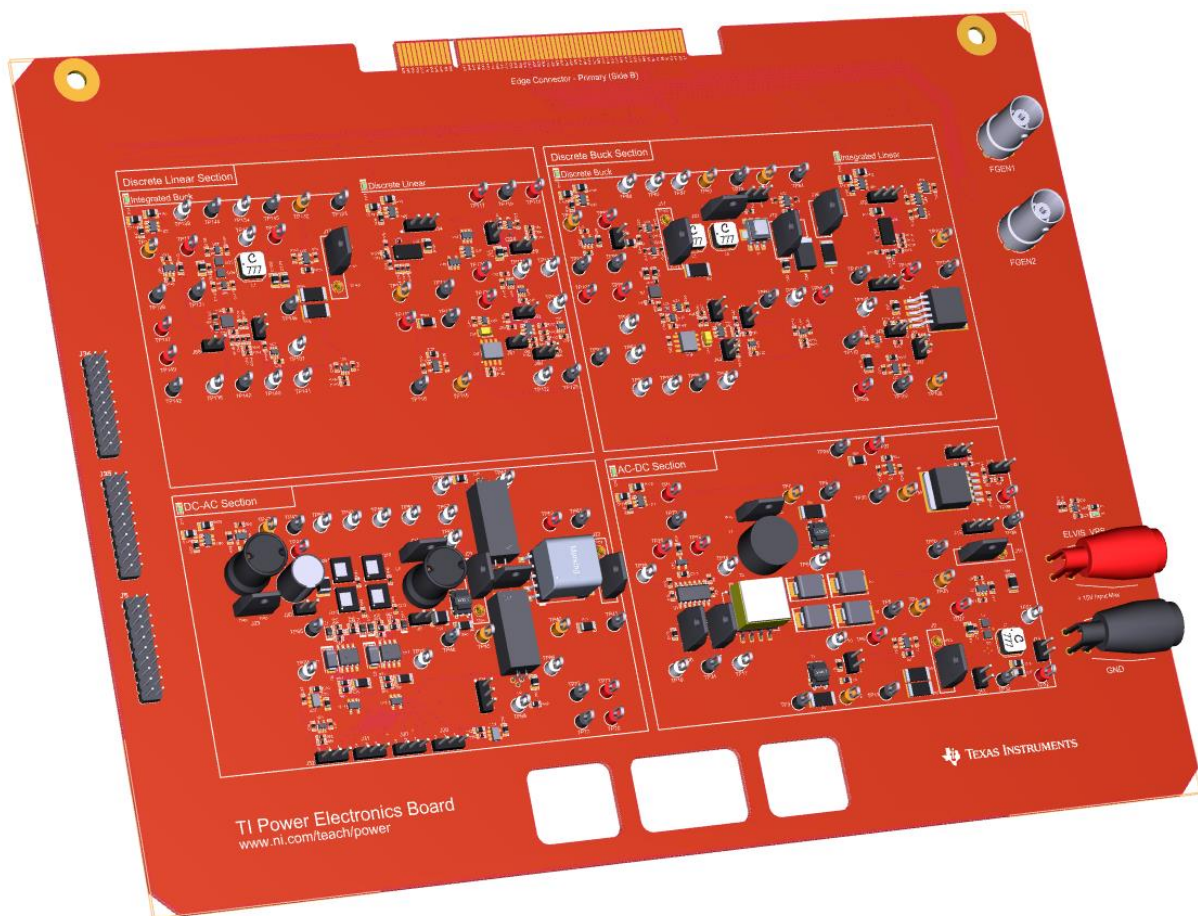
Lab 7: Buck Regulator

in Discontinuous Mode Operation

Lab 7: Buck Regulator in Discontinuous Mode Operation

The goal of this lab is to investigate the discontinuous mode operation of Buck regulator. In particular, we analyze the influence of inductance, load current and switching frequency on the steady-state behavior of the buck regulator, when the half-bridge uses a MOSFET and a diode. First, we review the principle of operation of the buck regulator in discontinuous mode operation, and determine the amplitude of inductor ripple current and source-to-output conversion ratio. Next, we simulate the buck regulator, to verify the impact of parameters on discontinuous mode operation. Finally, we perform lab experiments on a real buck converter to observe the current and voltage waveforms in discontinuous mode, and calculate the voltage conversion ratio.
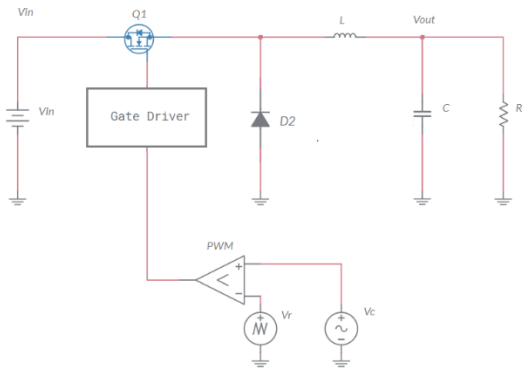
Figure 1-1 Buck Regulator with MOSFET-Diode Half-Bridge

Learning Objectives

After completing this lab, you should be able to complete the following activities.
1. Given a buck regulator implemented with a MOSFET-diode half-bridge, you will calculate the peak-peak amplitude of inductor ripple current, with specified units and decimal digit accuracy, and determine the discontinuous mode operation, by applying the appropriate theoretical equations.
2. Given a buck regulator implemented with a MOSFET-diode half-bridge, you will simulate the regulator to verify the impact of inductance on discontinuous mode operation, and verify the consistency of theoretical predictions.
3. Given a real buck regulator implemented with a MOSFET-diode half-bridge, you will observe the inductor current and switching node waveforms to detect the discontinuous mode operation, measure the ripple current and voltage conversion ratio, with specified units and decimal digits accuracy, and verify the consistency of calculations and simulations.

Required Tools and Technology

Platform: NI ELVIS III Instruments used in this lab: • Function generator • Digital multimeter • Oscilloscope • Power Supply **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.	✓ Access Instruments https://measurementslive.ni.com/ ✓ View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html ✓ View Tutorials https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M
Hardware: TI Power Electronics Board	✓ View User Manual http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
Software: NI Multisim Live	✓ Access https://www.multisim.com/ ✓ View Tutorial https://www.multisim.com/get-started/
Software: TI Power Electronics Configuration Utility	✓ Download (Windows OS Only) http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts of buck regulator in discontinuous mode, and discuss the influence of switching frequency, inductance of the L-C filter and load current.

1-2   Buck Regulator Continuous and Discontinuous Mode.

Figure 1-2 shows a buck regulator with a half-bridge comprised of the MOSFET Q1 and the diode D2, defined as *freewheeling diode*. The half-bridge is controlled by a Pulse Width Modulation (PWM) comparator (see **Lab5** for PWM modulation). During the time T_{on}, the MOSFET Q1 turns ON, the diode D2 is interdicted, and the inductor current rises. During the time T_{off}, the MOSFET Q1 turns OFF, the diode D2 conducts and the inductor current falls. If the inductor current is positive when the next switching cycle starts, the buck regulator operates in *continuous mode* (**CCM**) (see **Lab6** for CCM operation). If the inductor current crosses zero before the next switching cycle starts, the diode D2 turns off and the buck regulator operates in *discontinuous mode* (**DCM**). When this happens, the inductor current stays zero during the time T_{idle}, until the next switching cycle starts. The resulting waveforms for continuous and discontinuous operation mode are shown in Figure 1-2.
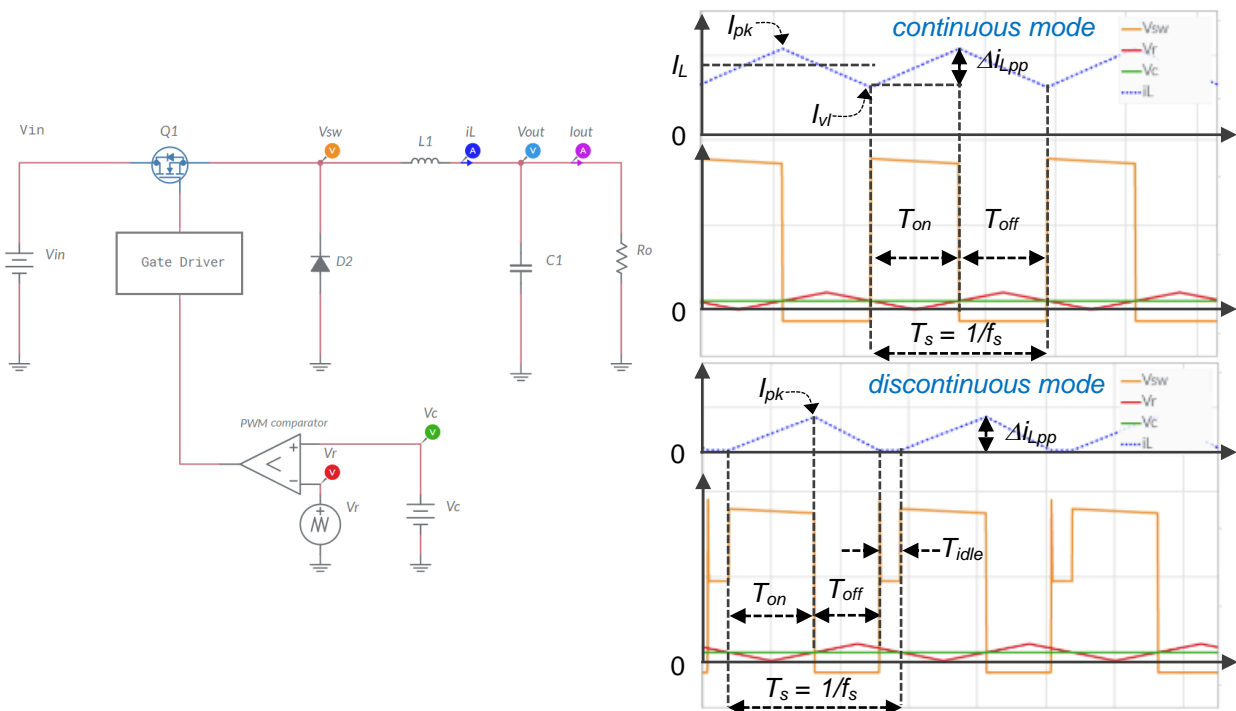
igure 1-2. Buck Regulator in Continuous and Discontinuous Operation Mode.

1-3   Factors Determining Discontinuous Mode.

The buck regulator operates in continuous mode if the peak-peak amplitude of the inductor ripple current is lower than 2 times the DC component of the inductor current:

Equation 1-1
$$\Delta i_{Lpp} = \frac{(V_{in} - V_{out})DT_s}{L} < 2I_L$$

where L is the inductance of the inductor, T_s is the switching period fixed by the triangular carrier signal V_r, R_o is the load resistance and D is the duty-cycle (see **Lab5**), given by:

Equation 1-2
$$D = \frac{T_{on}}{T_s} = \frac{V_c}{V_{rpp}}$$

Considering that $I_L = I_{out} = V_{out}/R_o$ and $V_{out} \cong DV_{in}$ in continuous mode, neglecting losses (see **Lab6** for power losses), Equation 1-1 can be simplified as shown below:

Equation 1-3
$$D > 1 - \frac{2Lf_s}{R_o}$$

From Equation 1-3, the condition for the buck regulator operating in discontinuous mode is:

Equation 1-4
$$D < 1 - \frac{2Lf_s}{R_o}$$

Equation 1-4 highlights that the factors determining the discontinuous operation mode are:

- a big load resistance R_o;
- a low switching frequency f_s;
- a small inductance L;
- a small duty-cycle D.

1-4   Voltage Conversion Ration of Buck Regulator in Discontinuous Mode.

The source-to-output voltage conversion ratio of buck regulator in discontinuous mode (neglecting power losses) is given by Equation 1-5 (see **Section 6-3** reference):

Equation 1-5
$$\frac{V_{out}}{V_{in}} = \frac{2}{1 + \sqrt{1 + \frac{8Lf_s}{R_o D^2}}}$$

Equation 1-5 highlights that in discontinuous mode, given the input voltage V_{in}, the duty-cycle D needs to be changed as the load resistance varies, to obtain a desired output voltage V_{out}.

1-5   Power Losses in Discontinuous Mode.

The MOSFET Q1, the inductor L and the freewheeling diode $D2$ cause power losses, which affect the operation of the buck regulator. The influence of MOSFET Q1 and inductor L on peak-peak amplitude of inductor ripple current is given by Equation 1-6:

Equation 1-6
$$\Delta i_{Lpp} = I_{pk} = \frac{(V_{in} - V_{out} - (R_{dson} + R_L)I_{out})DT_s}{L}$$

where R_{dson} and R_L are the MOSFET on-state resistance and the inductor resistance, respectively. The conduction time T_{off} of the freewheeling diode is given by Equation 1-7:

Equation 1-7
$$T_{off} = \frac{I_{pk}L}{V_{out} + V_F + R_L I_{out}} = \frac{(V_{in} - V_{out} - (R_{dson} + R_L)I_{out})DT_s}{V_{out} + V_F + R_L I_{out}}$$

where V_F is the forward voltage of freewheeling diode $D2$. The resulting conduction power losses of MOSFET ($P_{Q1,cond}$), inductor ($P_{L,cond}$), and freewheeling diode ($P_{D2,cond}$) are given by Equations 1-8:

Equation 1-8
$$P_{Q1,cond} = R_{ds(on)}^{Q1} I_{pk}^2 \frac{T_{on}}{3T_s}; \quad P_{L,cond} = R_L I_{pk}^2 \frac{T_{on} + T_{off}}{3T_s}; \quad P_{D2,cond} = \tfrac{1}{2} V_F I_{pk} T_{off} f_s$$

The MOSFET causes a switching loss during the on-off commutation, given by Equation 1-9:

Equations 1-9
$$P_{Q1,sw} \cong \tfrac{1}{2}(V_{in} + V_F)f_s I_{pk} t_{sw,off}$$

where $t_{sw,off}$ is the time the MOSFET needs to turn off, which depends on MOSFET parasitic capacitances, gate-to-source voltage threshold V_{th}, transconductance coefficient β (see **Lab1** and **Lab5**) and gate driver voltage V_{dr}. The inductor is affected by magnetic core power loss, which is modeled by the Steinmetz Equation 1-10:

Equation 1-10
$$P_{L,core} \cong K_{fe} f_s^x \Delta i_{L,pp}^y$$

where the parameters K_{fe}, x and y depend on material, shape and size of magnetic core. The resulting efficiency of the buck regulator in discontinuous mode is given by Equation 1-11:

Equation 1-11
$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}; \quad P_{out} = \frac{V_{out}^2}{R_o}; \quad P_{loss} = P_{Q1,cond} + P_{Q1,sw} + P_{L,cond} + P_{L,core} + P_{D2,cond}$$

[**Note:** Some ringing can be observed in the experimental waveform on inductor current during the idle time, caused by the resonance between the inductor and the parasitic capacitances of half-bridge MOSFET and diode].

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What implementation of a buck regulator could determine the discontinuous mode?
   A. the use of a PWM modulator with high peak-peak triangular carrier signal
   B. the use of a MOSFET-diode half-bridge
   C. the use of a ceramic output capacitor

1-2 How do you detect discontinuous mode operation in a buck regulator?
   A. by observing the inductor current, to verify if it crosses zero
   B. by observing the capacitor voltage, to verify if it looks triangular
   C. by observing the source voltage, to verify if it has spikes

1-3 What factor can determine discontinuous mode operation in buck regulator?
   A. a low source voltage
   B. a high inductance
   C. a high load resistance

1-4 What would you do to prevent discontinuous mode if the buck regulator has a high resistance load?
   A. increase the inductance of the inductor
   B. decrease the switching frequency
   C. increase the source voltage

1-5 What would you do to prevent discontinuous mode if the buck regulator has a small inductance?
   A. increase the switching frequency
   B. decrease the capacitance of the capacitor
   C. increase the peak-peak amplitude of PWM triangular carrier signal

1-6 What is the effect of discontinuous mode operation on the voltage conversion ratio of buck regulator?
   A. it results lower than continuous mode operation
   B. it results dependent on the capacitance of output capacitor
   C. it results dependent on load resistance

2 Exercise

In the **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III, the inductor can be configured with the following two options:

option 1: $L=15\mu H$

option 2: $L=48\mu H$

Assuming $V_{in} = 7V$, $V_{rpp} = 6V$, $T_s = 5\mu s$, $V_c = 3V$ and $R_o = 50\Omega$, determine:

a. the operation mode of the buck regulator:

- with inductor option 1:   continuous mode ☐   discontinuous mode ☐;
- with inductor option 2:   continuous mode ☐   discontinuous mode ☐;

b. the value of output voltage V_{out}, in Volt with three decimal digits of accuracy:

- with inductor option 1: $V_{out} = $ _____
- with inductor option 2 $V_{out} = $ _____

c. the minimum value of switching frequency allowing to operate in continuous mode, in kilo Hertz with one decimal digit of accuracy:

- with inductor option 1: $f_{s,min} = $ _____
- with inductor option 2: $f_{s,min} = $ _____

d. the minimum value of duty-cycle D_{min} allowing to operate in continuous mode, with three decimal digits of accuracy, and the corresponding value $V_{c,min}$ of the PWM control voltage, in Volt with three decimal digits of accuracy:

- with inductor option 1: $D_{min} = $ _____; $V_{c,min} = $ _____;
- with inductor option 2: $D_{min} = $ _____; $V_{c,min} = $ _____;

e. the maximum value of load resistance allowing to operate in continuous mode, in Ohm with one decimal digit of accuracy:

- with inductor option 1 $R_{o,max} = $ _____;
- with inductor option 2: $R_{o,max} = $ _____;

3 Simulate

The goal of the simulations in this section is to analyze the discontinuous mode operation of a buck regulator. You will verify the consistency of theoretical predictions of the **Exercise** Section, and observe the inductor current waveform under different parameters configurations, affecting the operation mode.

3-1 General Instructions

1. Open *Lab7 – Buck Regulator in Discontinuous Mode Operation* from this file path:
   https://www.multisim.com/content/JzTGExaCRiRHvZpqWseVnL/lab-7-buck-regulator-in-discontinuous-mode-operation/.

   The circuit schematic for the analysis of the buck regulator in discontinuous mode is shown in Figure 3-1.
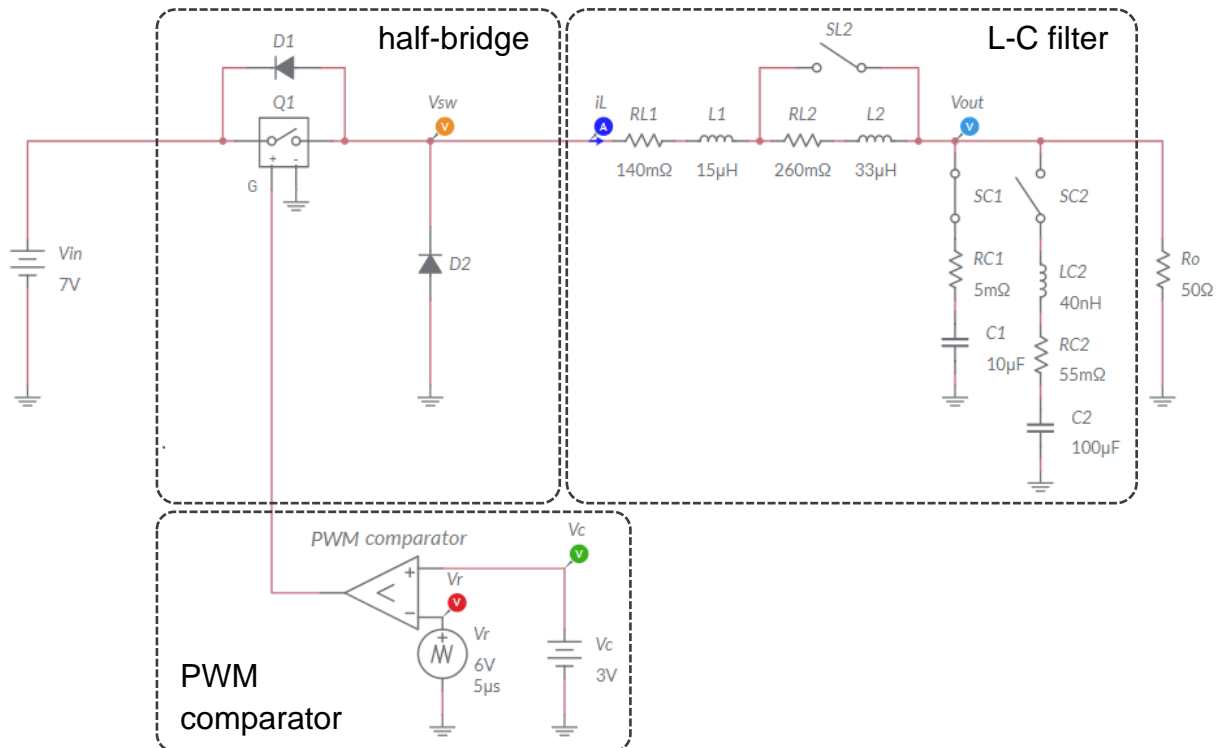
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Buck Regulator in Discontinuous Mode.

The MOSFET is modeled by means of a *Single Pole Single Throw (SPST)* switch, characterized by 1.2Ω ON resistance and 1MΩ OFF resistance. D1 represents the MOSFET body-diode, while D2 is the freewheeling diode. The L-C filter is configurable by means of switches SL1, SC1 and SC2 as follows:

- SL2 closed: $\qquad$ $L = L_1 = 15\mu H$, $R_L = R_{L1} = 140m\Omega$;
- SL2 open: $\qquad$ $L = L_1 + L_2 = 48\mu H$, $R_L = R_{L1} + R_{L2} = 400m\Omega$;
- SC1 closed, SC2 open: $\qquad$ $C = C_1 = 10\mu F$, $R_c = R_{C1} = 5m\Omega$;
- SC2 closed, SC1 open: $\qquad$ $C = C_2 = 100\mu F$, $R_c = R_{C2} = 55m\Omega$.

[**Note:** the series L_{C2}-R_{C2}-C_2 models an electrolytic capacitor with parasitic inductance L_{C2}, while the series R_{C1}-C_1 models a ceramic capacitor].

3-2 Simulation 1 Instructions

1. Set SL2 to be CLOSED, SC1 to be CLOSED and SC2 to be OPEN.
2. Select *Interactive* simulation and *Split* visualization options.
3. Check the *Periodic* option box for voltage probe V_{out} and current probes i_L in *Measurement labels* menu.
4. Set the simulation circuit parameters as follows:
   - V_{in}: *DC_mag* = 7.0V;
   - V_r: *VA* = 6V, *Per* = 5µs, *TF* = 2.5µs, Offset 0V;
   - R_o: 50Ω;
   - V_c: *DC_mag* = 3.0V
5. Run the simulation and wait until it ends.
6. Read the average value V_{AV} displayed by the output voltage probe V_{out}, in Volt with four three digits, and report the result in Table 3-1.
7. Read the average value I_{AV} displayed by the inductor current probe i_L, in milli Ampère with one decimal digit, and report the result in Table 3-1.
8. Read the peak-peak value I_{pp} displayed by the inductor current probe i_L, in milli Ampère with one decimal digit, and report the result in Table 3-1.
9. Set SL2 to be OPEN and repeat steps 5-8.
10. Import in Table 3-1 the values of V_{out} you have calculated in the **Exercise** in step "b".

Table 3-1 Buck Regulator in Discontinuous Mode

	V_{out} [V] from Exercise step "b".	V_{out} [V]	I_L [mA]	$\Delta i_{L,pp}$ [mA]
L = 15µH				
L = 48µH				

3-2-1 What operation mode do you detect?

A. continuous mode

B. discontinuous mode

why? _____

_____

3-2-2 Are simulations consistent with calculations?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

3-2-3 Is the peak-peak amplitude of the inductor ripple current greater than two times the average inductor current? Is this consistent with the operation mode?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

3-2-4 What inductor determines the smallest peak-peak amplitude of inductor ripple current?

    A.   L = 15µH

    B.   L = 48µH

    why? _____

    _____

3-2-5 What is the value of the switching node voltage V_{sw} of the half-bridge during the idle time T_{idle}?

    A. $V_{sw} = V_{in}$

    B. $V_{sw} = V_{out}$

    why? _____

    _____

3-3 Simulation 3 Instructions

1. Set SL2 to be OPEN, SC1 to be CLOSED and SC2 to be OPEN.
2. Select *Interactive* simulation and *Split* visualization options.

3. Check the *Periodic* option box for voltage probe V_{out} and current probes i_L in *Measurement labels* menu.
4. Set the simulation circuit parameters as follows:
   - V_{in}: *DC_mag* = 7.0V;
   - R_o: 50Ω;
   - V_c: *DC_mag* = 3.0V
5. Take the minimum value of switching frequency $f_{s,min}$ allowing to operate in continuous mode with the inductor option L = 48µH calculated in **Exercise** Section in step "c".
6. Choose a value of switching frequency $f_s > f_{s,min}$, calculate its period $T_s > 1/f_s$ and set the parameters of the triangular carrier signal generator V_r in the circuit schematic as follows:
   - V_r: *VA* = 6V, *Per* = T_s, *TF* = T_s/2, Offset 0V;
7. Run the simulation and wait until it ends.

3-3-1 What operation mode do you detect?

A.   continuous mode
B.   discontinuous mode
Please provide your comments: _____

_____

3-3-2 If your answer to question 3-3-1 is "B", what change would you make in the simulation parameters to achieve continuous mode operation? why?

_____

_____

Troubleshooting tips:
- If the simulation does not converge and you get some error message, reload *Lab7 – Buck Regulator in Discontinuous Mode Operation* from this file path https://www.multisim.com/content/JzTGExaCRiRHvZpqWseVnL/lab-7-buck-regulator-in-discontinuous-mode-operation/ and restart the simulation following the instructions.

4 Implement

The experiments in this section allow you to observe the behavior of the buck regulator in discontinuous mode operation. You will measure the average output voltage, the inductor peak-peak ripple current and average current under different conditions. Then, you will use the measurements to verify the consistency of theoretical predictions. Finally, you will measure the voltage conversion ratio of the buck regulator in discontinuous mode. The **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments.
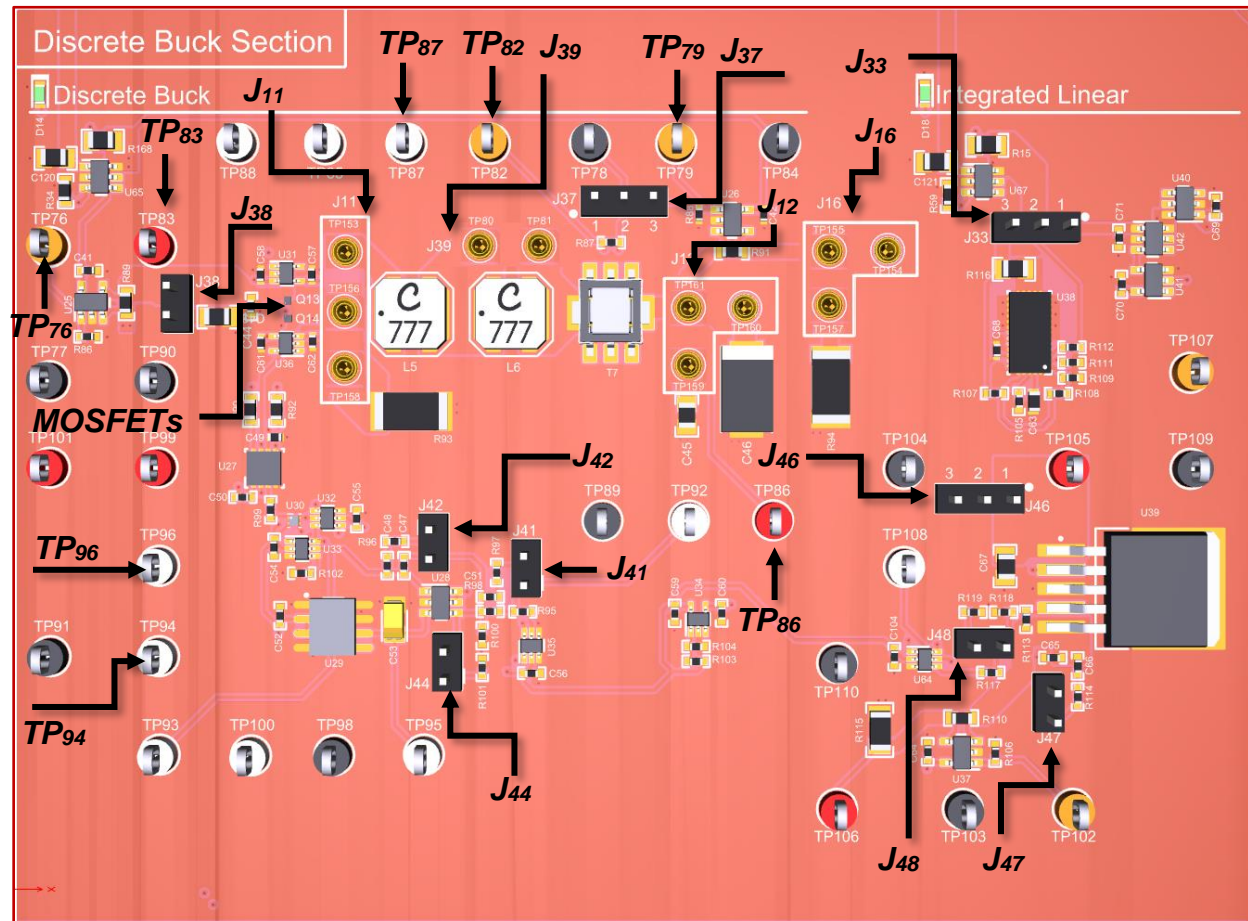
Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Buck Section Used for the Analysis of Buck Regulator in Discontinuous Mode Operation.

The half-bridge uses two TI's CSD15380F3 MOSFETs. Its output can be connected to the L-C filter by means of the Jumper J11. The L-C filter is configurable as follows:

- **J39 closed**: $L = 15\mu H$, $R_L = 140m\Omega$; **J39 open**: $L = 48\mu H$, $R_L = 400m\Omega$;
- **J12 shorting TP161-TP159**: $C = 10\mu F$, $R_c = 5m\Omega$ (ceramic capacitor);
- **J12 shorting TP161-TP160**: $C = 100\mu F$, $R_c = 55m\Omega$ (electrolytic capacitor).

A 50Ω resistance R_o can be connected to the output of the L-C filter by means of the Jumper J16. The current shunt monitor INA139NA/3K senses the average DC output current, which can be measured at test point TP79 with a 1:1 Ampère/Volt transduction gain. The board uses a current sensing transformer and a resistor (T7 and R87 shown in Figure 4-1) to sense the inductor ripple current. The transformer generates a voltage at test point TP82, that can be measured by means of a voltage probe. As the voltage-to-current transconductance of the sensing transformer is 0.5, dividing the voltage measured at test point TP82 by 2 provides the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$. The MOSFET gate driver TPS51601ADRBR features two optional configurations:

- **FCCM**: the gate drive signals of both MOSFET Q1 and Q2 are enabled;
- **SKIP**: the gate drive signal of low side MOSFET Q2 is disabled

When the gate driver is configured for **FCCM** operation (Forced Continuous Conduction Mode), the buck regulator operates in continuous mode under all operating conditions determined by the source, switching frequency, inductance and load. When the gate driver is configured for **SKIP** operation, the body diode of low side MOSFET operates as the freewheeling diode in the MOSFET-diode half-bridge, and the buck regulator can operate in discontinuous mode. The links to datasheets are available below:

- CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf;
- OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf;
- TLV7011DPWR COMPARATOR: http://www.ti.com/lit/ds/symlink/tlv7011.pdf;
- TPS51601ADRBR GATE DRIVER: http://www.ti.com/lit/ds/symlink/tps51601a.pdf;
- INA139NA/3K CURRENT MONITOR: http://www.ti.com/lit/ds/symlink/ina139.pdf.

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1. General Instructions

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter* using Measurements Live. For help on launching instruments, refer to this help document: `http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/`

2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: `http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html`

3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.

4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab7 – Buck Regulator in Discontinuous Mode Operation*.

5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect and configure the instruments as indicated in Tables 4-2 and 4-3.

Table 4-1 Jumpers setup

J11	J12	J16	J33	J37	J38
short TP156-TP153	short TP159-TP161	short TP155-TP157	short 2-3	short 1-2	short
J39	J41	J42	J44	J46	J47	J48
short	short	short	short	short 2-3	short	open

Table 4-2 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP94 (V_r), connect CH-2 to TP86 (V_{out}) connect CH-3 to TP96 (V_c), connect CH-4 to TP82 (Δi_{Lpp})
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP94 = PWM comparator V_r) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP96 = PWM comparator V_c)
Digital Multimeter	connect Voltage input to TP86 (V_{out}), TP79 (I_L) or TP76 (I_{in}), as per instructions

Table 4-3 Instruments Configuration and setup

Power Supply	*Channel "+"*: Static, 7.00V, *Channel "-"*: Inactive			
Oscilloscope	*Trigger*: Analog Edge, CH-1, set to 50%	*Horizontal*: 2us/div	*Acquisition*: average	*Measurements*: show
	Channel 1: ON • DC coupling • 2V/div • offset -8V	*Channel 2*: ON • DC coupling • 2V/div • offset 0.0V	*Channel 3*: ON • DC coupling • 2V/div • offset -8V	*Channel 4*: ON • DC coupling • 500mV/div offset 0V
Function Generator	*Channel 1*: Triangle, Frequency 200kHz, Amplitude 6.0Vpp, DC offset 3.0V *Channel 2*: Sine, Frequency 1Hz, Amplitude 0Vpp, DC offset 3.0V			
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: Automatic			

4-2. Experiment 1 Instructions

1. Connect the *Digital Multimeter* to TP86 (V_{out}).
2. Run *Oscilloscope*, *Digital Multimeter*, *Function Generator* and *Power Supply*.
3. Read the *Digital Multimeter* measurement of output voltage V_{out}, in Volt with three decimal digit of accuracy, and report the result in Table 4-4.

4. Using the *Oscilloscope* cursors in *Track Mode*, measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on CH-4, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-4.
5. Connect *Digital Multimeter* to TP79, measure the average output current I_{out}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-4;
6. Connect *Digital Multimeter* to TP76, measure the average input current I_{in}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-4;
7. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.
8. Import in Table 4-4 the values of V_{out}, I_L and $\Delta i_{L,pp}$ collected in Table 3-1 for L=15µH.
9. Set jumper J39 to be open, repeat the steps 1-7 and report the results in Table 4-4.
10. Import in Table 4-4 the values of V_{out}, I_L and $\Delta i_{L,pp}$ collected in Table 3-1 for L=48µH.

Table 4-4 Buck Regulator in Discontinuous Mode

	V_{out} [V] measured	V_{out} [V] simulated	I_L [mA] measured	I_L [mA] simulated	$\Delta i_{L,pp}$ [mA] measured	$\Delta i_{L,pp}$ [mA] simulated
L = 15µH						
L = 48µH						

4-2-1 Do you detect discontinuous mode operation from measurements? how?

A.   yes

B.   no

Please provide your comments: _____

_____

4-2-2 Does the inductor ripple current waveform look similar to the theoretical plots of Figure 2-1?

A.   yes

B.   no

Please provide your comments: _____

_____

4-2-3 Are the measurements consistent with simulations?

A.   yes

B.   no

Please provide your comments: _____

_____

4-3. Experiment 2 Instructions

1. Set jumper J39 to be shorted.
2. Connect the *Digital Multimeter* to TP86 (V*out*).
3. Set the *Function Generator* CH-2 DC offset to 1.0V (PWM control voltage V_c).
4. Run *Oscilloscope*, *Digital Multimeter*, *Function Generator* and *Power Supply*.
5. Read the *Digital Multimeter* measurement of output voltage V*out*, in Volt with three decimal digit of accuracy, and report the result in Table 4-5.
6. Using the *Oscilloscope* cursors in *Track Mode*, measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on CH-4, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-5.
7. Connect *Digital Multimeter* to TP79, measure the average output current I_{out}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-4;
8. Connect *Digital Multimeter* to TP76, measure the average input current I_{in}, in milli Ampère with one decimal digit of accuracy, and report the result in Table 4-4;
9. Repeat steps 5-8, setting the *Function Generator* CH-2 DC offset to the values of the PWM control voltage V_c listed in Table 4-5, and report the results in Table 4-4.
10. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.
11. Using the equations provided in **Theory and Background** Section, calculate the duty-cycle *D*, with tree decimal digits of accuracy, the theoretical output voltage *Vout*, in Volt with three decimal digits of accuracy, and the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$, in milli Alpère with one decimal digit of accuracy, for each value of the PWM control voltage V_c, and report the results in Table 4-5 [**Note:** check the value of load resistance R_o by calculating the ratio V_{out}/I_{out} of measured output voltage and current].
12. Calculate the efficiency $\eta = (V_{out}I_{out})/(V_{in}I_{in})$, with three decimal digits, for each value of the PWM control voltage V_c, and report the result in Table 4-4.

Table 4-5 Output Voltage of Buck Regulator in Discontinuous Mode Operation under Different Duty-Cycle Conditions.

V_c [V]	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0
D									
V_{out} [V] (measured)									
V_{out} [V] (calculated)									
Δi_{Lpp} [mA] (measured)									
Δi_{Lpp} [mA] (calculated)									
I_{in} [mA] (measured)									
I_{out} [mA] (measured)									
efficiency η (measured)									

4-3-1 Are the measurements and calculations trends consistent?

    A.   yes

    B.   no

    C.   other: _____

    Please provide your comments: _____

    _____

4-3-2 Are the measured values of average output voltage and peak-peak amplitude of inductor ripple current greater or lower than the calculated values?

    A.   greater

    B.   lower

    C.   other: _____

    Please provide your comments: _____

    _____

4-3-3 What is the trend of the efficiency as the duty-cycle increases?

    A.   it increases

    B.   it decreases

    C.   other: _____

    Please provide your comments: _____

    _____

4-3-4 What is the trend of the peak-peak amplitude of inductor ripple current as the duty-cycle increases?

    A.   it increases

    B.   it decreases

    C.   other: _____

    Please provide your comments: _____

    _____

Troubleshooting tips:

- If the regulator does not work, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiment.

5 Analyze

5-1   Using the results collected in Table 4-5, graph the values of the measured and calculated voltage conversion ratio $M_{DCM} = V_{out}/V_{in}$, as function of the duty-cycle D:
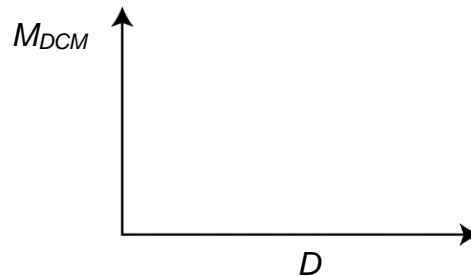
Figure 5-1 Voltage Conversion Ratio of Buck Regulator in Discontinuous Mode Operation as Function of Duty-Cycle.

5-2   Describe the trend of the conversion ratio M you observe, and discuss the differences between measurements and calculations, based on **Theory and Background** equations:

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the buck regulator in discontinuous mode operation. Discuss the factors that can determine the transition of the buck regulator from continuous mode to discontinuous mode, and the main differences between performances in continuous and discontinuous mode operation.

6-2 Expansion Activities

6-2-1. Investigate the influence of inductance and switching frequency on discontinuous mode operation, by means of TI Power Electronics Board for NI ELVIS III of Figure 4-1, following the instructions below.

a. Use connections and setups indicated in Tables 4-1, 4-2 and 4-3.
b. Set the Frequency of *Function Generator* CH-1 at 250kHz.
c. Run *Oscilloscope*, *Digital Multimeter*, *Function Generator* and *Power Supply*
d. Using the *Oscilloscope* cursors in *Manual Mode*:

- measure the peak-peak amplitude of the inductor ripple current $\Delta i_{L,pp}$ on the *Oscilloscope* CH-4, in milli Ampère with one decimal digit of accuracy, divide by 2 and report the result in Table 6-1; Ampère with one decimal digit of accuracy
- measure the average inductor current I_L on *Digital Multimeter*, in Ampère with one decimal digit of accuracy, and report the result in Table 6-1.
- check the box in Table 6-1 corresponding to the operation mode you detect.

e. Repeat step d. for all the values of the Frequency of *Function Generator* CH-1 listed in Table 6-1.
f. Stop *Power Supply*, *Function Generator*, *Digital Multimeter* and *Oscilloscope*.
g. Set the jumper J39 to be OPEN, repeat steps b. to f., and report the results in Table 6-1

Table 6-1 Buck Regulator Operation Mode under Different Switching Frequency and Inductance Conditions

	f [kHz]	250	300	350	400	450	500
J39 short L = 15µH	$\Delta i_{L,pp}$ [mA]						
	I_L [mA]						
	operation mode	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM
J39 open L = 48µH	$\Delta i_{L,pp}$ [mA]						
	I_L [mA]						
	operation mode	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM	☐ CCM ☐ DCM

6-1 Analyze the values of peak-peak amplitude of inductor ripple current and average inductor current as the switching frequency increases, and discuss the differences between the two inductor setups based on ***Theory and Background*** equations:

_____

_____

_____

6-2-3. Compare the voltage conversion ratio of buck regulator in continuous mode and discontinuous mode operation.

    a. Run *Experiment 2* of **Lab6**, import in the graph of Figure 5-1 the values of the voltage conversion ratio $M_{CCM} = V_{out}/V_{in}$ of buck regulator in continuous mode operation, as function of the duty-cycle D, and discuss the differences of the voltage conversion ratio between the continuous and discontinuous mode of operation:

_____

_____

_____

6-3   Resources for learning more

- This book provides the fundamentals of switching regulators:
  S. Maniktala, *Switching Power Supplies A - Z*, Newness

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   B

1-2   A

1-3   C

1-4   A

1-5   A

1-6   C

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
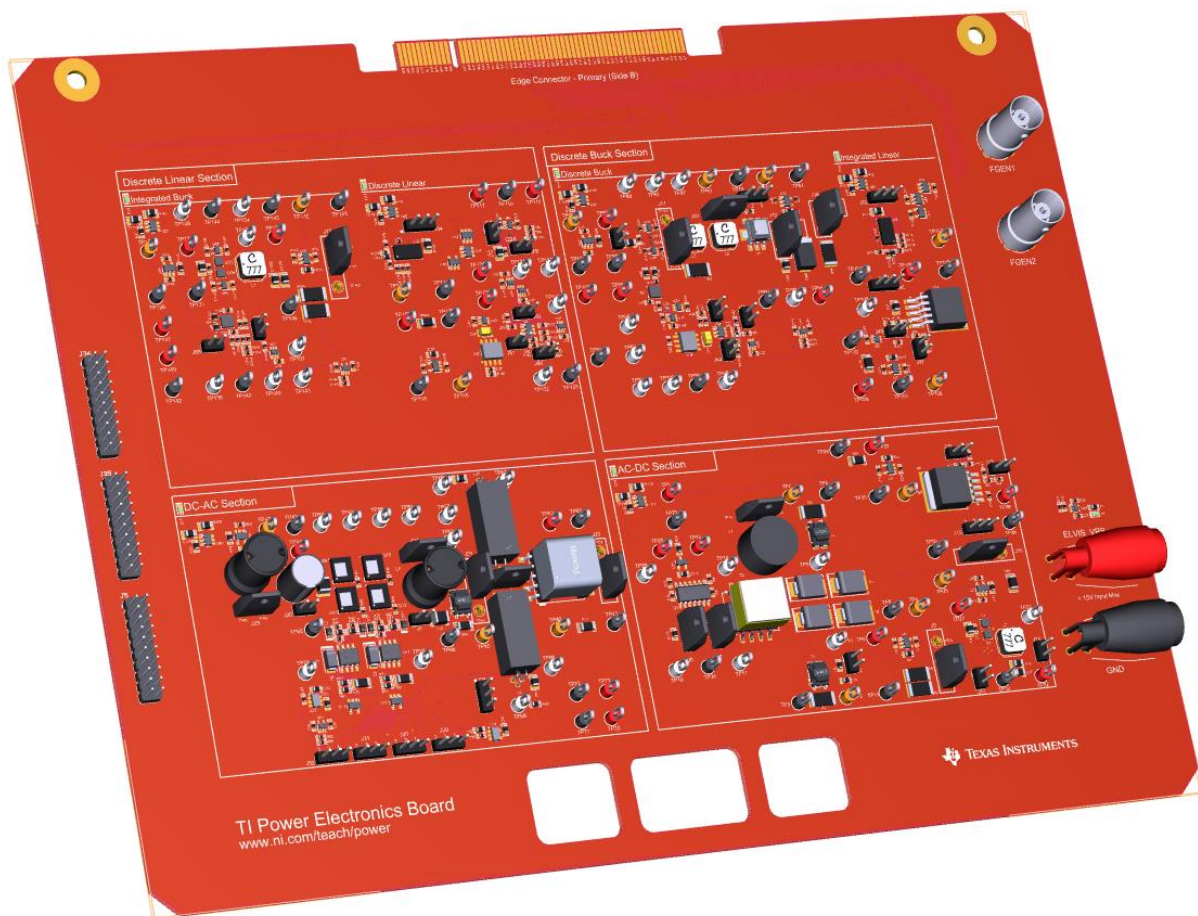
Lab 8: Buck regulator

in Closed Loop Operation

Lab 8: Buck Regulator in Closed Loop Operation

The goal of this lab is to analyze the closed loop operation of a buck regulator. We investigate the impact of the error amplifier on the output voltage DC regulation, and on the capability of rejecting output voltage AC perturbations caused by load current noise, which is one of the most important features of buck regulators. First, we will review the simplified DC and AC model of a closed loop buck regulator. Next, we will predict its Dc accuracy and AC response to load perturbations. Then, we will simulate the buck regulator in DC and AC operation to verify the DC regulation capability. Finally, we will perform experiments to observe the response of a real buck regulator to AC load perturbations, and will compare the results of calculations, simulations and measurements to verify their consistency.
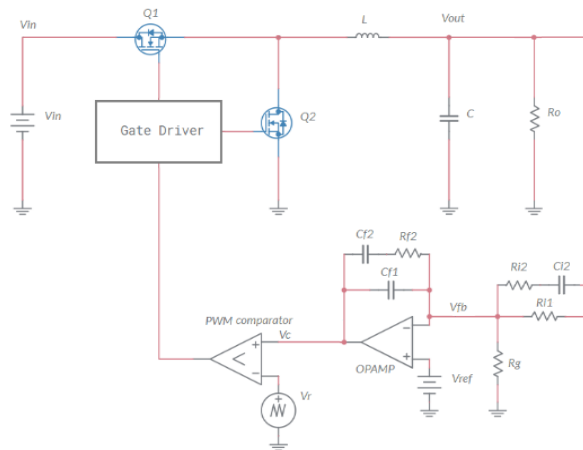
Figure 1-1. Closed Loop Buck Regulator.

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a buck regulator and the characteristics of its L-C filter and error amplifier, you will calculate the DC operating point and the AC response to load perturbations, with specified units and accuracy, by applying the appropriate theoretical formulae.
2. Given a buck regulator and the characteristics of its L-C filter and error amplifier, you will simulate its DC operation for different source voltage values, to determine the accuracy of theoretical model predictions, with specified units and accuracy, by comparing the appropriate sets of data and results
3. Given a real buck regulator, a power supply and a dynamic load, you will measure the accuracy of the DC output voltage with respect to the desired nominal value, and the amplitude of output voltage AC perturbations caused by AC load current perturbations, with specified units and accuracy.

Required Tools and Technology

Platform: NI ELVIS III
 	
Instruments used in this lab:
   • Function generator
   • Digital multimeter
   • Oscilloscope
   • Power Supply
 	
Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.
	✓ Access Instruments
	   https://measurementslive.ni.com/
	✓ View User Manual
	   http://www.ni.com/en-us/support/model.ni-elvis-iii.html
	✓ View Tutorials
	   https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board	✓ View User Manual http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

Software: NI Multisim Live	✓ Access
	   https://www.multisim.com/
	✓ View Tutorial
	   https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility	✓ Download (Windows OS Only) http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by means of Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations on simulations and experiments
- ✓ Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction.

In this section, we review the basic concepts and equations of a buck regulator in closed loop operation (see the reference given in section 6-3 to learn more). We discuss the impact of the L-C filter and of the error amplifier on DC offset error and the capability of the buck regulator to attenuate the effects of AC load current perturbations.

1-2 Feedback Action of the Error Amplifier.

Figure 1-2 shows a buck regulator in closed loop operation. The error amplifier consists of the OPAMP, the voltage reference V_{ref}, the capacitors $\{C_{f1}, C_{f2}, C_{i2}\}$, and the resistors $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$. The error amplifier compares the output voltage V_{out} to the desired DC nominal value $V_{outDC,nom}$, and generates the PWM control signal V_c ensuring that $V_{out} = V_{outDC,nom}$. Thanks to the error amplifier, the buck regulator generates a well regulated output voltage, rejecting the effects of load changes, which is one of the most important feature of buck regulators. The components $\{C_{f1}, C_{f2}, C_{i2}\}$ and $\{R_g, R_{i1}, R_{i2}, R_{f2}\}$ set the poles and zeros of the error amplifier, and determine its sensitivity to output voltage changes (See **Lab 3** for error amplifier operation).
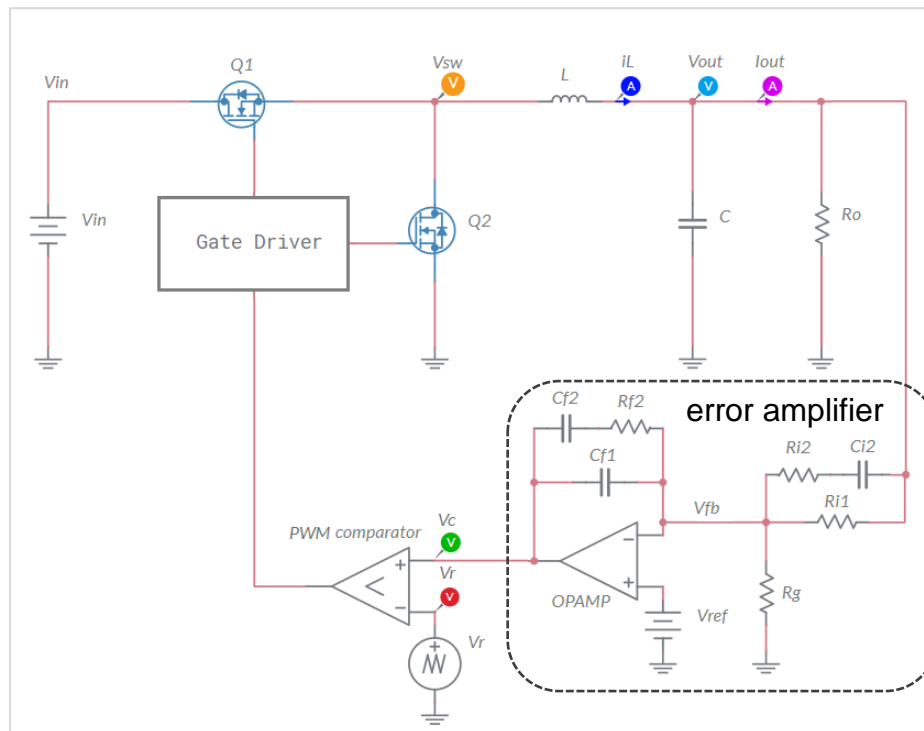
Figure 1-2. Buck Regulator in Closed Loop Operation.

1-3 Closed Loop DC Analysis of the Buck Regulator

The DC output voltage V_{outDC} of a buck regulator is determined by the DC source voltage V_{inDC} and by the DC PWM control voltage V_{cDC}. For a buck regulator with efficiency η, it is:

Equation 1-3-1
$$V_{outDC} = \frac{D}{\eta} V_{in} = \frac{V_{cDC}}{\eta V_{rpp}} V_{inDC}$$

where D is the duty-cycle of the MOSFET half-bridge, and V_{rpp} is the peak-peak amplitude of the triangular carrier signal of the PWM comparator (see **Lab5**). The error amplifier determines the DC PWM control voltage V_{cDC}, given by Equation 1-3-2:

Equation 1-3-2
$$V_{cDC} = A_{dc}(V_{ref} - V_{outDC}H)$$

where A_{dc} is the error amplifier DC gain and $H=(1+R_{i1}/R_g)^{-1}$ is the voltage sensor gain (see **Lab3**). Combining Equations 1-3-1 and 1-3-2 provides the buck regulator DC output voltage:

Equation 1-3-3
$$V_{outDC} = \frac{A_{dc}V_{ref}V_{in}}{\eta V_{rpp} + A_{dc}V_{in}H}$$

An unlimited DC gain $A_{dc} = \infty$ would determine an output voltage $V_{outDC,nom}$ equal to:

Equation 1-3-4
$$V_{outDC,nom} = \frac{V_{ref}}{H}$$

Based on Equations 1-3-3 and 1-3-4, the output voltage DC offset error of a buck regulator is given by Equation 1-3-5:

Equation 1-3-5
$$ERR_{DC} \cong \frac{A_{dc}V_{ref}V_{in}}{\eta V_{rpp} + A_{dc}V_{in}H} - \frac{V_{ref}}{H}$$

The tolerance of resistances R_{i1} and R_g and of the voltage reference V_{ref} influence the nominal value $V_{outDC,nom}$ given by Equation 1-3-4 and the DC offset error given by Equation 1-3-5. Typically, the accuracy of the voltage divider resistances and of the reference voltage is about 1% (See **Lab4** for effects of parameters tolerances on the DC operation of an error amplifier).

1-4 Open Loop Output Impedance of the Buck Regulator

AC load current perturbations are frequent in applications where loads are logic devices, like microprocessors. A load current AC perturbation $I_{outAC}sin(2\pi ft)$ causes an AC perturbation $V_{outAC}sin(2\pi ft+\theta)$ in the output voltage of the buck regulator. In open loop operation, the ratio $Z_{out,OL}$ between the amplitude of the output voltage V_{outAC} and load current AC perturbation I_{outAC} is defined as *open loop output impedance*, and is given by Equation 1-4-1:

Equation 1-4-1

$$\frac{V_{outAC}}{I_{outAC}}\bigg|_{open\ loop} = Z_{out,OL} = R_{DC}\frac{N_L(f)N_C(f)}{M(f)}$$

$$N_L(f) = \sqrt{\left(1+\frac{f^2}{f_L^2}\right)}; \quad N_C(f) = \sqrt{\left(1+\frac{f^2}{f_C^2}\right)}; \quad M(f) = \sqrt{\left(1-\frac{f^2}{f_n^2}\right)^2 + \frac{f^2}{Q^2 f_n^2}};$$

$$R_{DC} = R_L + DR_{ds(on)}^{Q1} + (1-D)R_{ds(on)}^{Q2}; \quad f_L = \frac{R_L}{2\pi L}; \quad f_C = \frac{1}{2\pi R_C C}; \quad f_n = \frac{1}{2\pi\sqrt{LC}}; \quad Q = R_o\sqrt{\frac{C}{L}}$$

where L and R_L are the inductance and resistance of the inductor, C and R_c are the capacitance and resistance of the capacitor, $R_{ds(on)}^{Q1}$ and $R_{ds(on)}^{Q2}$ are the on-state resistances of half-bridge MOSFETs, D is the duty-cycle, and R_o is the DC load resistance. Normally, $f_L < f_n < f_c$. From Equation 1-4-1 it follows that a low output impedance is a desirable feature of a buck regulator, as it involves a better rejection capability of AC load current perturbations. At high frequency, the output impedance is equal to the resistance of the capacitor, $Z_{out,OL} \cong R_C$. At low frequency, the output impedance is equal to the sum of inductor and MOSFETs resistance, $Z_{out,OL} \cong R_{DC}$.

1-5 Error Amplifier Gain

The buck regulator capability to reject the effects of AC load current perturbations improves in closed loop operation, thanks to the feedback action of the error amplifier. When the error amplifier senses an AC perturbation of amplitude V_{outAC} in the output voltage, it generates an AC signal of amplitude $V_{cAC} = G_{ea}V_{outAC}$, where G_{ea} is the *error amplifier gain*, given by Equation 1-5-1, for the error amplifier configuration of Figure 1-2:

Equation 1-5-1

$$G_{ea}(f) = \frac{V_{cAC}}{V_{outAC}} = \begin{cases} \dfrac{f_0}{f}\dfrac{1+f^2/f_Z^2}{1+f^2/f_P^2} & f > \dfrac{f_0}{A_{dc}} \\[4mm] A_{dc}H & f < \dfrac{f_0}{A_{dc}} \end{cases}$$

The frequencies f_0, f_P and f_Z are set by capacitances $\{C_{f1},C_{f2},C_{i2}\}$ and resistances $\{R_g,R_{i1},R_{i2},R_{f2}\}$, and determine the sensitivity of the error amplifier with respect to AC perturbations of the output voltage.

1-6 Control-to-Output Gain of the Buck Regulator

The AC perturbation V_{cAC} generated by the error amplifier determines an additional AC perturbation in the output voltage, whose magnitude is given by Equation 1-6-1:

Equation 1-6-1
$$\frac{V_{outAC}}{V_{cAC}} = G_c(f) = \frac{V_{inDC}}{V_{rpp}} \frac{N_c(f)}{M(f)}$$

where $N_c(f)$ and $M(f)$ are given in Equation 1-4-1. The function G_c is defined as *control-to-output gain* of the buck regulator. The AC perturbation generated by the error amplifier attenuates the effect of the perturbation caused by the AC load current perturbation.

1-7 Loop Gain of the Buck Regulator

The product $T = G_c G_{ea}$ is defined as *loop gain* of the buck regulator, expressing the closed loop sensitivity of buck regulator to AC perturbations. A high loop gain T involves a higher sensitivity to AC perturbations and a higher efficacy of the buck regulator in attenuating them (see also **Lab4** for loop gain). Equation 1-6-1 highlights that the control-to-output gain is equal to V_{inDC}/V_{rpp} at low frequency, while it decreases as frequency increases. Equation 1-5-1 highlights that a higher pole frequency f_0 increases the error amplifier sensitivity with respect to output voltage AC perturbations. However, the frequency f_0 has to be limited to prevent instability, which causes uncontrollable high frequency noise in the output voltage. Therefore, the loop gain T can be high only at low frequency. The *loop gain cross-over frequency f_{co}* is the upper bound of the frequency range where the magnitude of loop gain T is greater than 1, and is determined by the error amplifier poles f_0, f_P and zero f_Z.

1-8 Closed Loop Output Impedance of the Buck Regulator

The *closed loop output impedance $Z_{out,CL}$* of the buck regulator is given by the simplified Equation 1-8-1:

Equation 1-8-1
$$\left. \frac{V_{outAC}}{I_{outAC}} \right|_{closed\ loop} = Z_{out,CL} \cong \begin{cases} \dfrac{Z_{out,OL}}{G_{ea}(f)G_c(f)} = \dfrac{R_L V_{rpp}}{V_{inDC}} \dfrac{N_L(f)}{G_{ea}(f)} & f < f_{co} \\ \\ Z_{out,OL} & f > f_{co} \end{cases}$$

According to Equation 1-8-1, the closed loop output impedance $Z_{out,CL}$ of the buck regulator is lower than the open loop output impedance $Z_{out,OL}$ below the cross-over frequency, where $G_{ea}(f)G_C(f) > 1$. Therefore, given the control-to-output gain $G_C(f)$, the buck regulator has better rejection capability of AC load current perturbing effects at frequencies where the error amplifier gain is higher. The error amplifier gain at low frequency is mainly determined by the pole frequency f_0 and by OPAMP DC open loop gain A_{dc}.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What parameters of a buck regulator determine the nominal value of its DC output voltage?
    A. the inductance and capacitance of the L-C filter
    B. the reference voltage and the voltage sensor gain
    C. the error amplifier pole and OPAMP dc gain A_{dc}

1-2 What parameter of a buck regulator determines its DC output voltage offset error?
    A. the inductance L
    B. the OPAMP open loop dc gain A_{dc}
    C. the error amplifier pole frequency f_0

1-3 What parameter of a buck regulator determines the open loop output impedance of the buck regulator at low frequency?
    A. the inductance of the inductor
    B. the capacitance pf the capacitor
    C. the resistance of the inductor

1-4 What parameters majorly influence the closed loop output impedance of the buck regulator at low frequency?
    A. the error amplifier pole frequency f_0 and OPAMP dc gain A_{dc}
    B. the MOSFET half-bridge gate driver voltage
    C. the reference voltage and the voltage sensor gain

1-5 Based on your answers to Questions 1-1 to 1-4, what would you do to design a buck regulator with higher DC accuracy and low output impedance?

_____

_____

_____

_____

2 Exercise

The **Discrete Buck Section** in the TI Power Electronics Board for NI ELVIS III is based on the following setup:

- MOSFETs: TI's CSD15380F3, assume $V_{th} = 1.35$V, $\beta = 0.24$A/V^2, $\lambda = 0.05$V^{-1}
- OPAMP: TI's OPA835IDBVR, assume $A_{dc}=10^6$, $V_{cc+}=5.5$V, $V_{cc-}=0$V.
- VOLTAGE REFERENCE: TI's LM4140, assume $V_{ref}=1.024$V.
- ERROR AMPLIFER SETUP: $f_0 = 4.06$kHz.

The TI's devices datasheets are available at the following links:

- CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
- OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
- LM4140 VOLTAGE REFERENCE: http://www.ti.com/lit/ds/symlink/lm4140.pdf

The voltage divider is configurable as follows:

- (a) $R_{i1}=39.2$kΩ, $R_g=18.2$kΩ;　(b) $R_{i1}=39.2$kΩ, $R_g=10.2$kΩ

The L-C filter is configurable as follows:

- (a) $L = 15$µH, $R_L = 140$mΩ;　(b) $L = 48$µH, $R_L = 400$mΩ;
- (a) $C = 10$µF, $R_c = 5$mΩ;　(b) $C = 100$µF, $R_c = 55$mΩ.

2-1 Calculate the nominal value of the DC output voltage $V_{outDC,nom}$, in Volts with three decimal digits, and the DC offset error, in microvolts with one decimal digit, with voltage divider options (a) and (b) :

- (a): $V_{outDC,nom}$ = _____;　ERR_{DC} = _____
- (b): $V_{outDC,nom}$ = _____;　ERR_{DC} = _____

2-2 You have a buck regulator powered by a 7V DC source voltage and generating a 5V DC output voltage for a 120Ω DC load resistance R_o. The load is subjected to an AC perturbation $I_{outAC}sin(2\pi ft)$, where the frequency f can have the values listed in Table 2-1. Assume the inductor configuration (b) and the capacitor configuration (a). Calculate the open and closed loop output impedance $Z_{out,OL}$ and $Z_{out,CL}$ in Ohms with three decimal digits, and report the results in Table 2-1.

Table 1-1 Output Impedance of a buck regulator in open loop and closed loop operation.

f [Hz]	1	10	100	1000	10000
$Z_{out,OL}$					
$Z_{out,CL}$					

2-3 Based on the results of your calculations, do you see an improvement in the AC load current perturbation rejection capability of the buck regulator in closed loop operation compared to open loop operation?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

2-4 What parameter would you change to further improve the low frequency rejection capability, and how?

    _____

    _____

3 Simulate

The simulations you will perform in this section allow you to analyze the closed loop behavior of buck regulator. You will observe the DC output voltage while varying the DC source voltage, to verify the regulation capability of the feedback control loop. You will analyze the PWM control voltage generated by the error amplifier and compare it with the ratio between the DC output and source voltages.

3.1 Instructions

1. Open *Lab8 – Buck Regulator in Closed Loop Operation* from the file path: https://www.multisim.com/content/WSHeUkuHMCHHnyeEu2MHxZ/lab-8-buck-regulator-in-closed-loop-operation/.

   The circuit used for simulating the DC and AC buck regulator closed loop operation is shown in Figure 3-1. The error amplifier generates the PWM control voltage V_c. The load is a DC resistance $R_o = 240\Omega$. The error amplifier poles and zero frequencies are $f_0 = 120\text{Hz}$, $f_z = 4.276\text{kHz}$ and $f_P = 153.9\text{kHz}$, with switches Sf2 and Si2 closed. The OPAMP is characterized by a dc gain $A_{dc}=10^6$. The DC voltage source V_{in} is characterized by a parasitic resistance $R_{in} = 100\text{m}\Omega$.
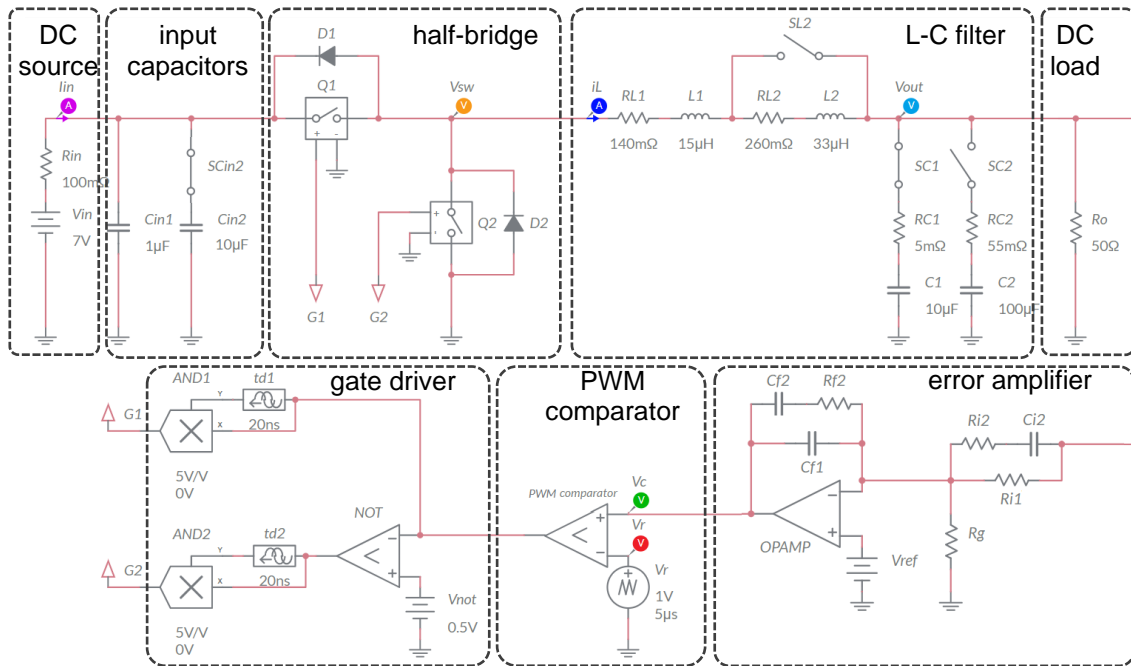
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Buck Regulator in Closed Loop Operation.

2. Set switches SCin2 and SC1 to be CLOSED, and switches SL2 and SC2 to be OPEN.
3. Set the *initial voltage* of capacitor *C1* to 5V.
4. Select the *Interactive* simulation option and the *Split* visualization option.
5. Set the *Maximum Time Step* and *Maximum Initial Step* to 10ns, and *End time* to 2ms in the *Simulation settings* menu;
6. Check the *Periodic* option box for voltage probes V_{in}, V_{out}, and V_c in the *Measurement labels* menu.
7. Import in Table 3-1 the nominal value $V_{outDC,nom}$ in Volts with three decimal digits, calculated in the ***Exercise*** Section 2-1.
8. Set *DC_mag* = 6.0V for generator V_{in}.
9. Run the simulation and wait until it ends.
10. Read the average value V_{AV} displayed by the output voltage probe V_{out}, in Volt with three decimal digits, and report the result in Table 3-1.
11. Read the average value V_{AV} displayed by the PWM control voltage probe V_c, in Volt with three decimal digits, calculate the ratio V_c/V_{rpp} and report the result in Table 3-1, with three decimal digits.
12. Calculate the ratio V_{outDC}/V_{inDC} with three decimal digits and report the result in Table 3-1.
13. Repeat steps 9-12 for each value of DC source voltage V_{inDC} (*VO* voltage of the generator V_{in}) listed in Table 3-1.

V_{inDC} [V]	6.0	6.5	7.0	7.5	8.0	8.5	9.0
$V_{outDC,nom}$ [V]							
V_{outDC} [V]							
V_{cDC}/V_{rpp} [V]							
V_{outDC}/V_{inDC}							

3-1-1 Does the DC output voltage V_{outDC} change as V_{inDC} increases?

A.   yes
B.   no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-1-2 Does the PWM control voltage V_{cDC} change as V_{inDC} increases?

A.   yes
B.   no

Discuss the results based on the **Theory and Background** section equations:

_____

_____

3-1-3 How is the ratio V_{cDC}/V_{rpp} correlated to the ratio V_{outDC}/V_{inDC}? why?

_____

_____

3-1-4 What change do you expect in the simulation results if you close the switch SC2 and open the switch SC1? why?

_____

_____

Troubleshooting tips:

● If the simulation does not run and you get some error message, reload *Lab8 – Buck Regulator in Closed Loop Operation* from this file path: https://www.multisim.com/content/WSHeUkuHMCHHnyeEu2MHxZ/lab-8-buck-regulator-in-closed-loop-operation/ and restart the simulation, following the instructions.

4 Implement

The experiments of this section allow you to observe the behavior of a real buck regulator in closed loop operation. First, you will analyze the DC operating point of the buck regulator while varying the DC source voltage. Next, you will measure the AC output voltage perturbation generated by an AC load current perturbation. The **Discrete Buck Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments.
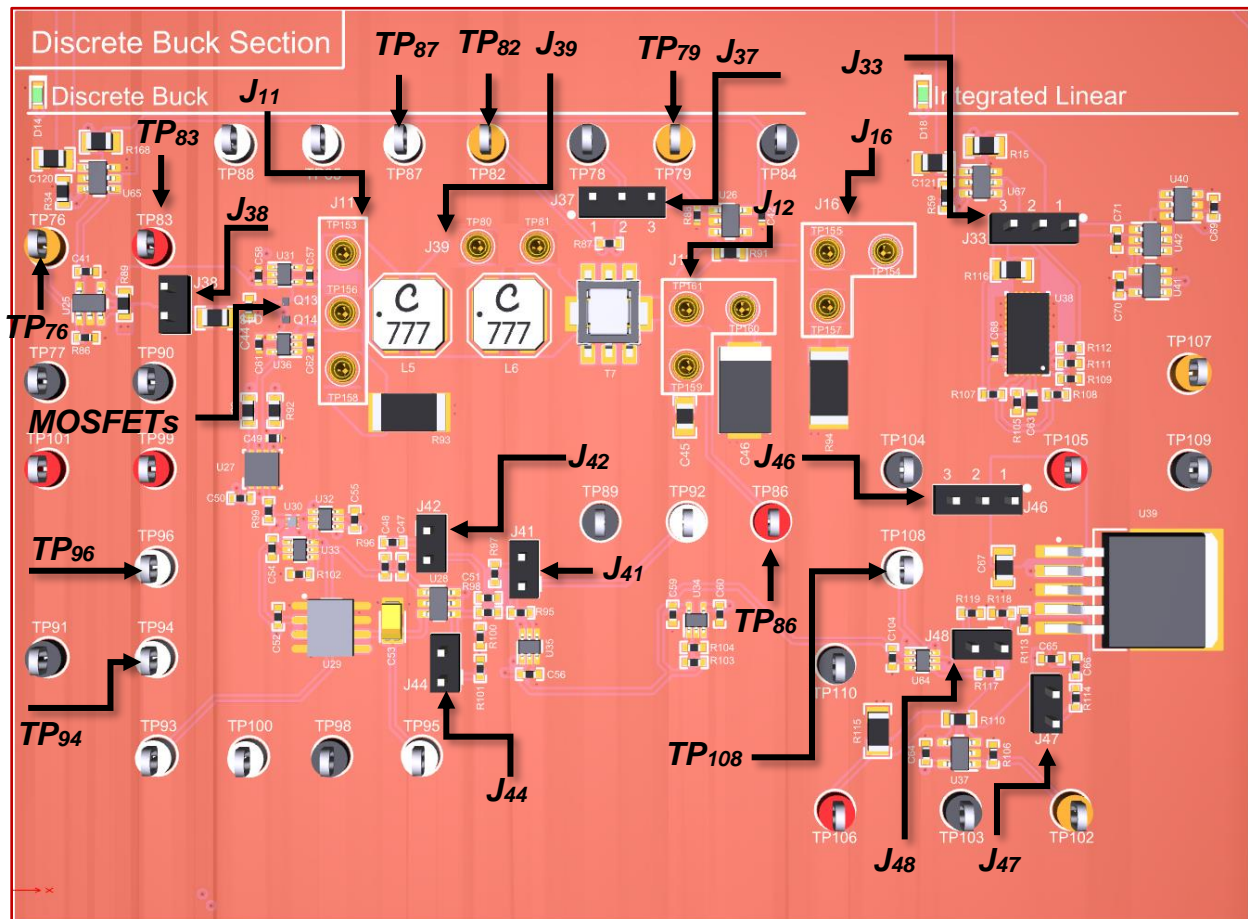

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Buck Section Used for the Analysis of Buck Regulator in Closed Loop Operation

The half-bridge MOSFETs is implemented with TI's CSD15380F3, the error amplifier OPAMP is TI's OPA835IDBVR, the PWM comparator uses a TI's TLV7011DPWR, the gate driver is a TI's TPS51601ADRBR. The INA139NA/3K current shunt monitor senses the low frequency output current, which can be measured at test point TP79 with a 1:1 Ampère/Volt transduction gain. The links to datasheets are available below:

- CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf;
- OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf;
- TLV7011DPWR COMPARATOR: http://www.ti.com/lit/ds/symlink/tlv7011.pdf;
- TPS51601ADRBR GATE DRIVER: http://www.ti.com/lit/ds/symlink/tps51601a.pdf;
- INA139NA/3K CURRENT MONITOR: http://www.ti.com/lit/ds/symlink/ina139.pdf.

The MOSFETs on-state resistance is 1.2Ω at 4.5V gate-to-source voltage. The half-bridge is connected to the L-C filter through jumper J11. The output of the L-C filter is connected to the input of an **Integrated Linear Regulator**, which operates as a dynamic load, through jumper J16. The L-C filter is configurable by means of jumpers J39 and J12 as follows:

- **J39 closed**: $L = 15\mu H$, $R_L = 140m\Omega$; **J39 open**: $L = 48\mu H$, $R_L = 400m\Omega$;
- **J12 shorting TP161-TP159**: $C = 10\mu F$, $R_c = 5m\Omega$ (ceramic capacitor);
- **J12 shorting TP161-TP160**: $C = 100\mu F$, $R_c = 55m\Omega$ (electrolytic capacitor).

The error amplifier poles and zero frequencies are set to $f_0 = 120Hz$, $f_z = 4.27kHz$ and $f_P = 153.9kHz$, with jumpers J41 and J42 closed. [**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components].

4-1 General Instructions

1. Open *Variable Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab8 – Buck Regulator in Closed Loop Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.

Table 4-1 Jumpers configuration

J11	J12	J16	J33	J37	J38
short TP156-TP153	short TP159-TP161	short TP155-TP154	short 2-3	short 1-2	short
J39	J41	J42	J44	J46	J47	J48
open	short	short	short	short 1-2	short	open

4-2 Experiment 1 Instructions

1. Connect the instruments as indicated in Table 4-2-1.

Table 4-2-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP83 (V_{in}), connect CH-2 to TP86 (V_{out}) connect CH-3 to TP93 (V_c), connect CH-4 to TP87 (V_{sw})
Function Generator	connect CH-1 to FGEN1 BNC connector (TP94 = Buck PWM comparator V_r) connect CH-2 to FGEN2 BNC connector (TP108 = Linear Feedback V_{FB})

2. Configure and setup the instruments as indicated in Table 4-2-2.

Table 4-2-2 Instruments Configuration and setup for Experiment 1

Power Supply	Channel "+": Static, 7.00V, Channel "-": Inactive			
Oscilloscope	Trigger: analog edge, CH-4, set to 50%	Horizontal: 200ms/div	Acquisition: average	Measurements: show
	Channel 1: ON • DC coupling • 2V/div • offset 0.0V	Channel 2: ON • DC coupling • 2V/div • offset 0.0V	Channel 3: ON • DC coupling • 2V/div • offset -8.0V	Channel 4: ON • DC coupling • 2V/div offset 0.0V
Function Generator	Channel 1: Triangle, Frequency 500kHz, Amplitude 6Vpp, DC offset 3.0V Channel 2: Sine, Frequency 1Hz, Amplitude 0.0Vpp, DC offset -2.0V			

3. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
4. Using the *Oscilloscope* cursors in Track mode, read the average DC values of the CH-2 (V_{out}), in Volt with two decimal digits, and report the value in Table 4-2-3.
5. Using the *Oscilloscope* cursors in Track mode, read the average DC values of the CH-3 (V_c), in Volt with two decimal digits, divide it by the triangular carrier peak-peak amplitude V_{rpp} = 6V, and report the result, with two decimal digits, in Table 4-2-3.
6. Repeat the measurements and calculations for all the values of the source voltage V_{inDC} indicated in Table 4-2-3, by changing the DC voltage of *Power Suppy*.
7. Import in Table 4-2-3 the DC values of V_{outDC} and V_{cDC}/V_{rpp} collected in Table 3-1, with two decimal digits.
8. Stop *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-2-3 DC Output Voltage and Error Amplifier Voltage as function of DC Source Voltage.

V_{inDC} [V]	6.0	6.5	7.0	7.5	8.0	8.5	9.0
$V_{outDC,nom}$ [V]							
V_{outDC} [V] measured							
V_{outDC} [V] from Table 3-1							
V_{cDC}/V_{rpp} [V] measured							
V_{cDC}/V_{rpp} [V] from Table 3-1							

4-2-1 Does the DC output voltage V_{outDC} vary as V_{inDC} increases?

    A.   yes

    B.   no

Discuss the differences between simulations and experiments based on the **Theory and Background** section equations:

_____

_____

4-2-2 What is the trend of the ratio V_{cDC}/V_{rpp} as V_{inDC} increases? why?

_____

_____

4-2-3 Based on your answer to Questions and 4-1-1 and 4-1-2, what parameter of the buck regulator model would you change to improve the accuracy of simulations? How and why?

_____

_____

_____

4-3 Experiment 2 Instructions

1. Connect the instruments as indicated in Table 4-3-1.

Table 4-2-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP83 (V_{in}), connect CH-2 to TP86 (V_{out}) connect CH-3 to TP93 (V_c), connect CH-4 to TP79 (I_{out})
Function Generator	connect CH-1 to FGEN1 BNC connector (TP94 = Buck PWM comparator V_r) connect CH-2 to FGEN2 BNC connector (TP108 = Linear Feedback V_{FB})
Digital Multimeter	connect Voltage input to TP79 (I_{out})

2. Use the instruments configuration and setup shown in Table 4-3-1.

Table 4-3-1 Instruments Configuration and setup for Experiment 2

Power Supply	*Channel "+"*: Static, 7.00V, *Channel "-"*: Inactive			
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 200µs/div	*Acquisition*: average	*Measurements*: show
	Channel 1: ON • DC coupling • 2V/div • offset 0.0V	*Channel 2*: ON • DC coupling • 10mV/div • offset -5.0V	*Channel 3*: ON • DC coupling • 10mV/div • offset -4.33V	*Channel 4*: ON • DC coupling • 10mV/div offset 0.0V
Function Generator	*Channel 1*: Triangle, Frequency 500kHz, Amplitude 6Vpp, DC offset 3.0V *Channel 2*: Sine, Frequency 1Hz, Amplitude 1Vpp, DC offset 550mV			
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: Automatic			

3. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
4. Read the DC average of output voltage V_{outDC} and PWN control signal V_{cDC} on the *Oscilloscope* CH-2 (V_{out}) and CH-3 (V_c), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-3-2.
5. Read the peak-peak amplitude of output voltage ΔV_{outpp} and PWN control signal ΔV_{cpp} on the *Oscilloscope* CH-2 (V_{out}) and CH-3 (V_c), in milli Volts with all decimal digits shown by the instrument, and report the values in Table 4-3-2.
6. Calculate the error amplifier gain $G_{ea} = \Delta V_{cpp}/\Delta V_{outpp}$, in with three decimal digits, and report the result in Table 4-3-2.

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7. Read the DC average output current I_{outDC} on *Digital Multimeter*, in milli Volt, with one decimal digit, and report the value in Table 4-3-2 in mA with one decimal digit.
8. Read the peak-peak amplitude of output current ΔI_{outpp} on the *Oscilloscope* CH-4 (I_{out}), in milli Volt with all decimal digits shown by the instrument, and report the value in milli Ampère in Table 4-3-2.
9. Calculate the output impedance $Z_{out,CL} = \Delta V_{outpp}/\Delta I_{outpp}$, in Ohm with three decimal digits, and report the result in Table 4-3-2.
10. Repeat the steps 2-6 for all the values of Frequency of the *Function Generator* CH-2 indicated in Table 4-3-2.
11. Stop *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-3-2 Buck Regulator Closed Loop Output Impedance.

Function Generator CH-2 Frequency [Hz]	1	10	100	1000
$V_{outDC,nom}$ [V]				
V_{outDC} [V]				
ΔV_{outpp} [mV]				
V_{cDC} [V]				
ΔV_{cpp} [mV]				
$G_{ea} = \Delta V_{cpp}/\Delta V_{outpp}$				
I_{outDC} [mA]				
ΔI_{outpp} [mA]				
$Z_{out,CL} = \Delta V_{outpp}/\Delta I_{outpp}$ [Ω]				

4-3-1 Discuss the trend you observe in the values of the error amplifier gain as the frequency f increases, based on **Theory and Background** section concepts:

_____

_____

4-3-1 Discuss the trend you observe in the values of the closed loop output impedance as the frequency f increases, based on **Theory and Background** section concepts:

_____

_____

4-3-3 Based on your answer to Questions and 4-3-1 and 4-3-2, what parameter of the buck regulator would you change to reduce the output impedance? How and why?

_____

_____

Troubleshooting tips:
- If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

5 Analyze

5-1 Re-calculate the theoretical values of error amplifier gain G_{ea} and of closed loop output impedance $Z_{out,CL}$, based on **Theory and Background** equations, using the values of switching frequency (f_s=500kHz) and peak-peak amplitude of the PWM triangular carrier signal (V_{rpp}=6Vpp) adopted for the Experiment 2 of Section 4-2. Graph the resulting values versus the frequency f, together with the experimental values of G_{ea} and $Z_{out,CL}$ collected in Table 4-3-3. Include a legend indicating which line style corresponds to which series (calculations, measurements).

Table 5-1 Closed Loop Power Supply Rejection Ratio.

Frequency [Hz]	1	10	100	1000
theoretical G_{ea}				
experimental G_{ea}				
theoretical $Z_{out,CL}$ [Ω]				
experimental $Z_{out,CL}$ [Ω]				
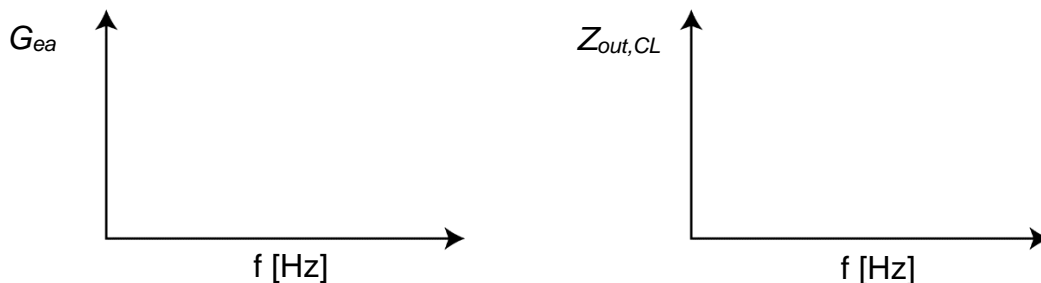
Figure 5-1 Theoretical and Experimental Values of Error Amplifier Gain and Closed Loop Output Impedance of Buck Regulator.

5-2   Discuss the differences you observe between the experimental and theoretical values of error amplifier gain G_{ea} and of closed loop output impedance $Z_{out,CL}$. Based on your learning, assess what parameters majorly influence the two functions G_{ea} and $Z_{out,CL}$, and indicate what parameter would you change to improve the accuracy of the theoretical predictions.

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the closed loop operation of a buck regulator, concerning its DC accuracy and rejection capability of load current AC perturbations. Discuss the conditions and the parameters influencing the closed loop operation of the buck regulator, and discuss why and how can you reduce the output impedance of buck regulator.

6-2   Expansion Activities

6-2-1. Investigate the influence of switching frequency on closed loop output impedance of buck regulator, by means of TI Power Electronics Board for NI ELVIS III of Figure 4-1.
   a. Follow general instructions provided in Section 4-1.
   b. Follow the instructions for Experiment 2 provided in Section 4-3.
   c. Set the switching frequency to 200kHz by means of the Frequency of *Function Generator* CH-1.
   d. Run the experiment and report the resulting values of closed loop output impedance in Table 6-1.
   e. Repeat step d. for all the values of the switching frequency listed in Table 6-1.

Table 6-1 Buck Regulator Closed Loop Output Impedance under different switching frequency conditions

load current AC frequency [Hz]	1	10	100	1000
$Z_{out,CL}$ @ f_s = 200kHz [Ω]				
$Z_{out,CL}$ @ f_s = 400kHz [Ω]				
$Z_{out,CL}$ @ f_s = 600kHz [Ω]				
$Z_{out,CL}$ @ f_s = 800kHz [Ω]				

6-1 Analyze the values of closed loop output impedance as the switching frequency increases and discuss them based on *Theory and Background* equations:

_____

_____

_____

6-2-2. Investigate the influence of the L-C filter setup on closed loop output impedance of buck regulator, by means of TI Power Electronics Board for NI ELVIS III of Figure 4-1.
   a. Follow general instructions provided in Section 4-1.
   b. Follow the instructions for Experiment 2 provided in Section 4-3.
   c. Import in Table 6-2 the values of closed loop output impedance recorded in Table 4-3-2 for Experiment 2, relevant to the setup of jumper J39 open ($L = 48\mu H$, $R_L = 400m\Omega$) and jumper J12 shorting TP161-TP159 ($C = 10\mu F$, $R_c = 5m\Omega$).
   d. Short the jumper J39 to set $L = 15\mu H$, $R_L = 160m\Omega$, run the experiment and report the resulting values of closed loop output impedance in Table 6-1.
   e. Open the jumper J39 to set $L = 48\mu H$, $R_L = 400m\Omega$, short TP161-TP160 with jumper J12 to set $C = 100\mu F$, $R_c = 55m\Omega$, run the experiment and report the resulting values of closed loop output impedance in Table 6-2.
   f. Short the jumper J39 to set $L = 15\mu H$, $R_L = 160m\Omega$, run the experiment and report the resulting values of closed loop output impedance in Table 6-2.

Table 6-2 Buck Regulator Closed Loop Output Impedance under different L-C filter setup conditions

load current AC frequency [Hz]	1	10	100	1000
$Z_{out,CL}$ @ $L = 48\mu H$, $C = 10\mu F$ [Ω]				
$Z_{out,CL}$ @ $L = 15\mu H$, $C = 10\mu F$ [Ω]				
$Z_{out,CL}$ @ $L = 48\mu H$, $C = 100\mu F$ [Ω]				
$Z_{out,CL}$ @ $L = 15\mu H$, $C = 100\mu F$ [Ω]				

6-2 Analyze the values of closed loop output impedance for the different L-C filter configurations and discuss them based on *Theory and Background* equations:

_____

_____

_____

6-3 Resources for learning more

- This book provides the fundamentals of switching regulators:
  S. Maniktala, *Switching Power Supplies A - Z,* Newness

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   B

1-2   B

1-3   C

1-4   A

1-5   high f_0, high A_{dc}

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III
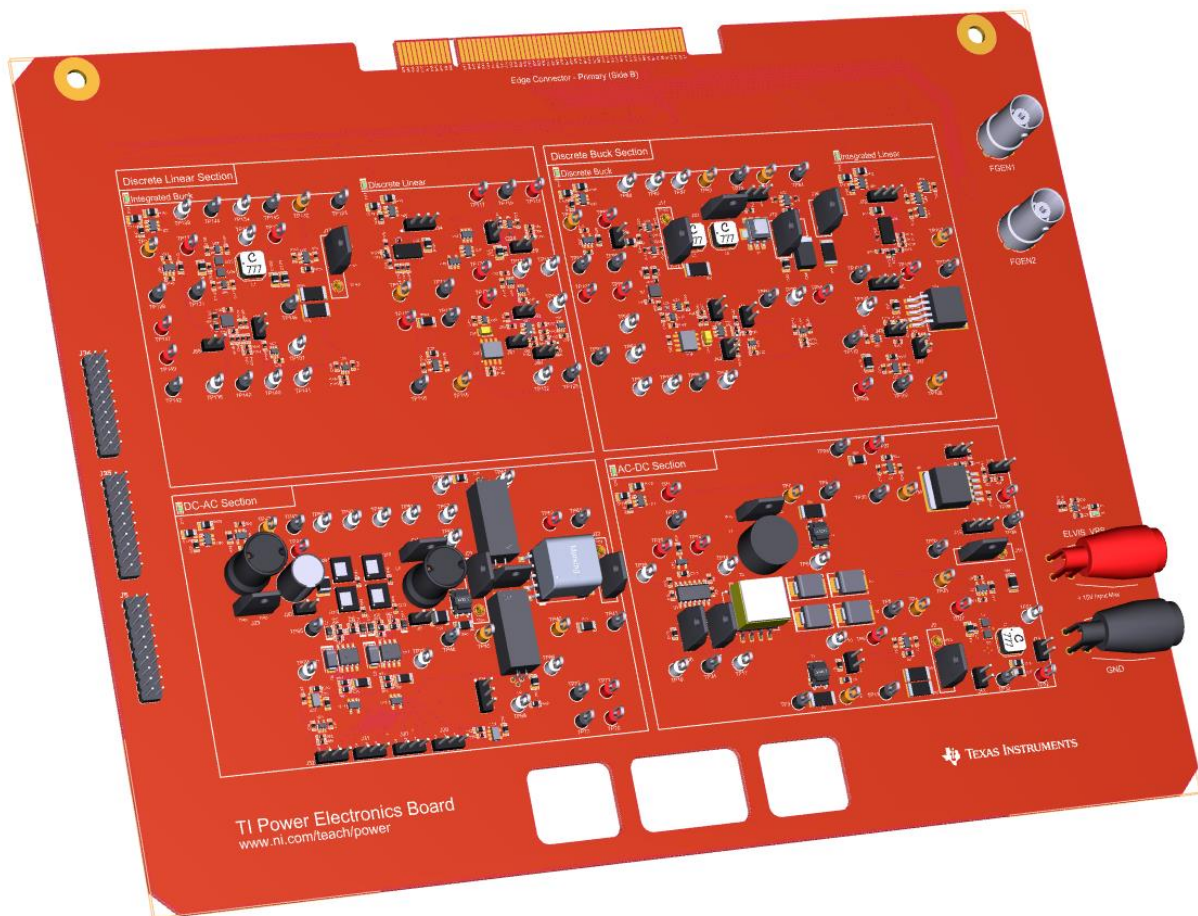
Lab 9: DC-AC

PWM Inverter Operation

Lab 9: DC-AC PWM Inverter Operation

The goal of this lab is to investigate the behavior of a DC-AC Pulse Width Modulated (PWM) Inverter, which is widely used in variable frequency AC drives for induction motors. First, we review the principle of operation and the main waveforms of a PWM Inverter, based on a MOSFET full-bridge converter topology. Next, we analyze the effect of L-C filter by means of simulations. Finally, we perform lab experiments to obseve the AC output voltage and perform ripple voltage measurements.
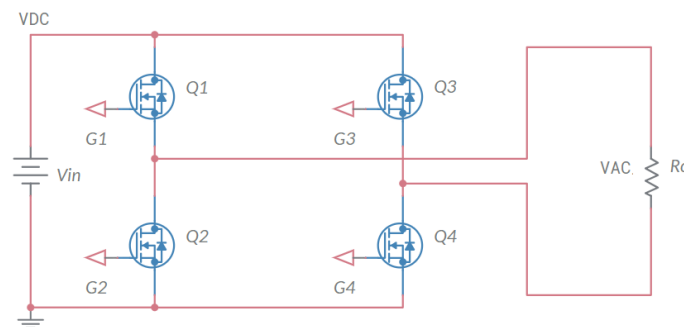
Figure 1-1. DC-AC Inverter

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a DC-AC PWM Inverter, with specified modulation and switching PWM signals setup, you will calculate the amplitude of sinusoidal and ripple components of AC current and voltage, with specified units and accuracy, and determine the L-C output filter parameters needed to limit the amplitude of ripple components below given limits, under different switching frequency operating conditions.

2. Given a DC-AC PWM Inverter, you will simulate its operation under different PWM signals and L-C filter setup, to analyze the amplitude of sinusoidal and ripple components of AC current and voltage, and verify their consistency with theoretical predictions.

3. Given a real DC-AC PWM Inverter with configurable PWM signals and L-C output filter, you will observe the AC load voltage waveform, and measure the amplitude of sinusoidal and ripple components, with specified units and accuracy, under different L-C output filter and PWM signals setup.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

✓ Access Instruments
https://measurementslive.ni.com/
✓ View User Manual
http://www.ni.com/en-us/support/model.ni-elvis-iii.html
✓ View Tutorials
https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMlWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

✓ View User Manual
http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

✓ Access
https://www.multisim.com/
✓ View Tutorial
https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

✓ Download (Windows OS Only)
http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a single-phase DC-AC PWM inverter based on a MOSFET full-bridge. First, we analyze the principle of operation and the resulting AC voltage waveform. Next, we discuss the filtering effect of load inductance. Finally, we analyze the effect of an L-C filter.

1-2 DC-AC Inverters Fundamentals

An ideal DC-AC inverter converts a DC voltage V_{DC} into an AC sinusoidal voltage $V_{AC}(t)$, as shown in Figure 1-2.
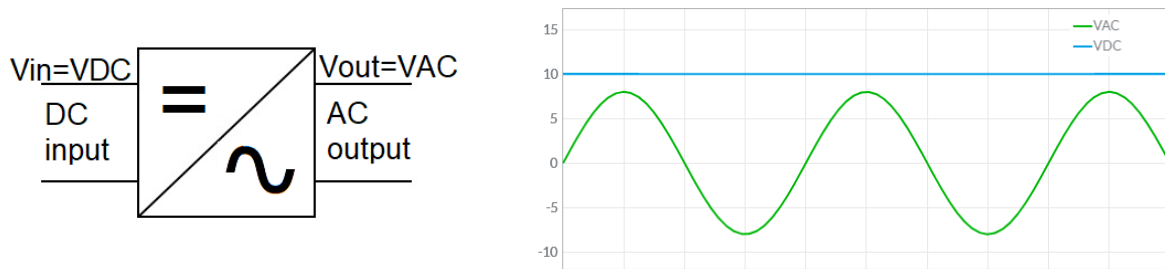
Figure 1-2. Inverter Input and Output waveforms.

The ideal output AC voltage of a DC-AC inverter is given by Equation 1-1:

Equation 1-1
$$V_{AC,ideal}(t) = kV_{DC}\cos(2\pi f_m t)$$

where f_m is the desired frequency and k is a constant. The DC-AC conversion can be performed by means of several circuit topologies and control techniques, providing an AC voltage characterized by different levels of accuracy with respect to the ideal sinusoid of Equation 1-1. The output of a real DC-AC inverter is given by Equation 1-2:

Equation 1-2
$$V_{AC,real}(t) = kV_{DC}\cos(2\pi f_m t) + \sum_{n=1}^{\infty} A_n \cos(2\pi n f_m t + \theta_n)$$

where the magnitude A_n of the harmonics is determined by the circuit topology and modulation technique. Harmonics are undesired high-frequency effects determined by DC-AC inverter operation. They must be kept with levels that are compatible with a correct and safe operation of load and source, and ensure that the electro-magnetic emission limits imposed by Electro Magnetic Compatibility (EMC) regulations are met.

1-3 DC-AC PWM Inverter.

Figure 1-2 shows a DC-AC Pulse Width Modulated (PWM) inverter.

(a) DC-AC PWM Inverter With Ohmic Load

(b) Half-Bridge Q1-Q2 Voltage $V_{AC\_p}(t)$

(c) Half-Bridge Q3-Q42 Voltage $V_{AC\_n}(t)$

(d) Load AC Voltage $V_{AC}(t) = V_{AC\_p}(t) - V_{AC\_n}(t)$
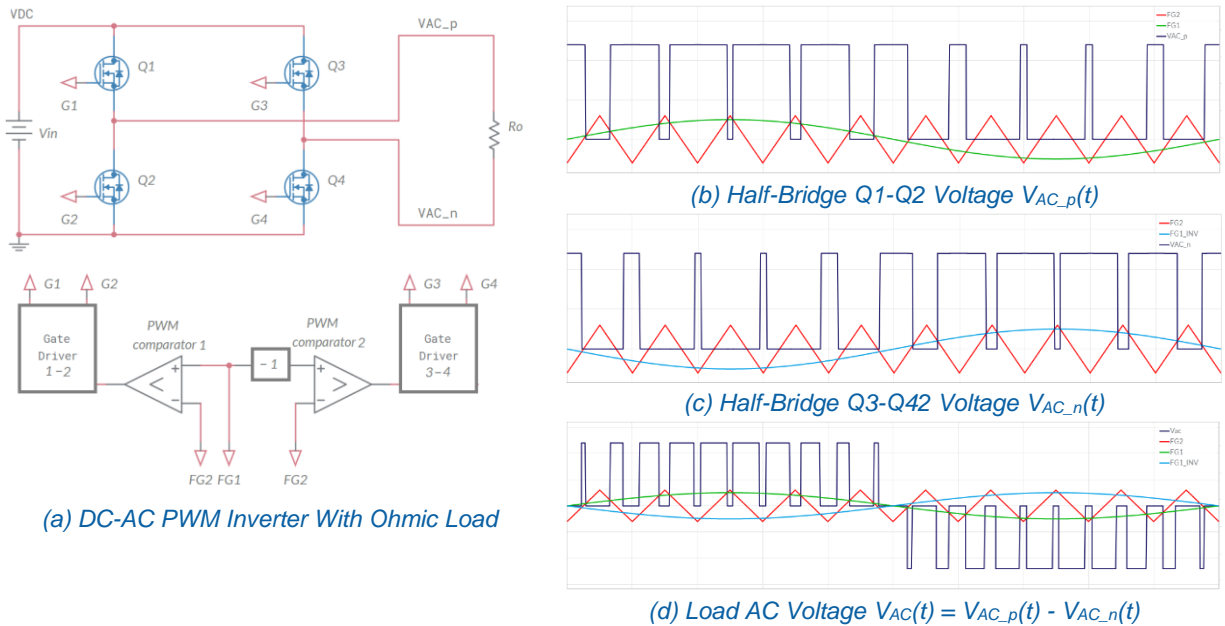
Figure 1-2. MOSFET Full-Bridge Inverter.

The MOSFET full bridge is comprised of two half-bridges. The half-bridge Q1-Q2 operates in PWM mode (see **Lab5**), driven by PWM comparator 1. As shown in Figure 1-2(b), the signal $FG1(t) = V_{ref}\cos(2\pi f_m t)$, of period $T_m = 1/f_m$, is the *modulation reference* for the output voltage $V_{AC}(t)$. The triangular waveform $FG2(t)$, of period $T_s = 1/f_s$, is the *modulation carrier*. Normally the *switching frequency* f_s is much greater than the *modulation frequency* f_m. For AC frequency $f = 50$Hz, the PWM switching frequency f_s can be 5kHz. The resulting output voltage $V_{AC\_p}(t)$ of the half-bridge Q1-Q2 is the modulated square pulses train shown in Figure 1.2(b). The half-bridge Q3-Q4 also operates in PWM mode, driven by PWM comparator 2, with an inverter reference signal $FG1\_INV(t) = - FG1(1)$ (see Figure 1-2(c)). The resulting output voltage $V_{AC\_n}(t)$ of the half-bridge Q3-Q4 is the modulated square pulses train shown in Figure 1.2(b). The resulting voltage $V_{AC}(t) = V_{AC\_p}(t) - V_{AC\_n}(t)$ applied to load resistor R_o is the sequence of square pulses of amplitude V_{DC} shown in Figure 1-2(d). The width of pulses is modulated by the reference sinusoidal signal $FG1(t)$. If the PWM triangular carrier has a peak-peak amplitude V_{rpp}, the average $V_{AC,av}(t)$ of the AC voltage $V_{AC}(t)$ over each half switching period $T_s/2$ is given by Equation 1-3:

Equation 1-3
$$V_{AC,av}(t) = \frac{2}{T_s}\int_{t_0}^{t_0+T_{s/2}} V_{AC}(t)dt \cong D(t)V_{DC}; \qquad D(t) = \frac{2V_{ref}}{V_{rpp}}\sin(2\pi f_m t)$$

where $D(t)$ is the *modulation duty-cycle* of the DC-AC PWM inverter output voltage.

1-4 Impact of Load Inductance.

Figure 1-3(b) shows the current waveform of an AC ohmic load. Many AC loads, like induction motors, are ohmic-inductive. If the PWM switching frequency f_s is sufficiently high, the L-R low pass nature of the load determines the current waveform shown in Figure 1-3(c).

(b) Ohmic Load Voltage and Current

(a) DC-AC PWM Inverter With Ohmic-Inductive Load

(c) Ohmic-Inductive Load Voltage and Current
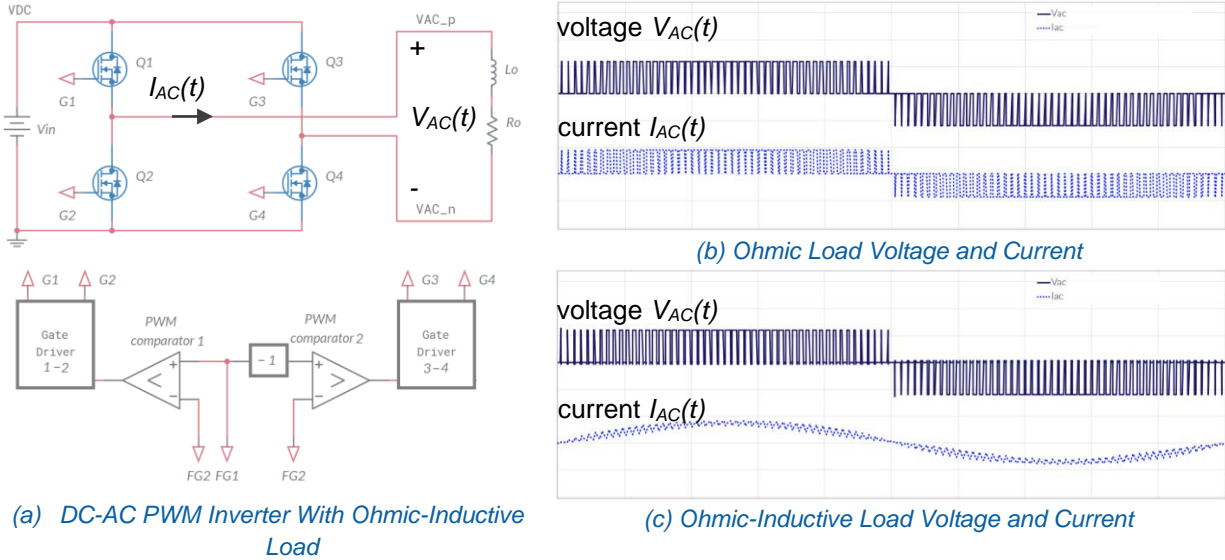
Figure 1-3. AC Currents of Ohmic and Ohmic-Inductive Loads Powered by a DC-AC PWM Inverter.

The current of the ohmic-inductive load exhibits a sinusoidal component at modulation frequency f_m of the reference signal and a triangular ripple component at PWM switching frequency f_s. The sinusoidal component is given by Equation 1-4:

Equation 1-4
$$I_{AC}(t) = \frac{V_{DC}}{Z_{f_m}} D(t); \qquad Z_{f_m} = \sqrt{R_o^2 + (2\pi f_m L_o)^2}$$

The peak-peak amplitude of the switching frequency ripple component is time varying, and is given by Equation 1-5 (see **Lab6**):

Equation 1-5
$$\Delta I_{AC,pp}(t) = \frac{V_{DC} - R_o I_{AC}(t)}{2L_o f_s} D(t) = \frac{V_{ref} V_{DC}}{L_o f_s V_{rpp}} \left(1 - \frac{2V_{ref} R_o}{Z_{f_m} V_{rpp}} \sin(2\pi f_m t) \right) \sin(2\pi f_m t)$$

From Equation 1-5, the amplitude of the peak-peak ripple component $\Delta I_{AC,pp}(t)$ is maximum at the instant t_{max} given by Equation 1-6:

Equation 1-6
$$if \ \frac{Z_{f_m} V_{rpp}}{4R_o V_{ref}} \leq 1: \ t_{max} = \frac{T_m}{2\pi} \arcsin\left(\frac{Z_{f_m} V_{rpp}}{4R_o V_{ref}} \right); \quad if \ \frac{Z_{f_m} V_{rpp}}{4R_o V_{ref}} > 1: \ t_{max} = \frac{T_m}{4}$$

The maximum amplitude of peak-peak AC ripple component is given by Equation 1-7:

Equation 1-7
$$if \ \frac{Z_{f_m} V_{rpp}}{4R_o V_{ref}} \leq 1: \ \Delta I_{AC,ppmax} = \frac{V_{DC} Z_{f_m}}{8R_o L_o f_s}; \quad if \ \frac{Z_{f_m} V_{rpp}}{4R_o V_{ref}} > 1: \ \Delta I_{AC,ppmax} = \frac{V_{ref} V_{DC}}{L_o f_s V_{rpp}} \left(1 - \frac{2V_{ref} R_o}{Z_{f_m} V_{rpp}} \right)$$

1-5 DC-AC PWM Inverter with L-C Filter.

If an ohmic load requires an AC voltage with low harmonic content, the modulated square wave voltage generated by the MOSFET full-bridge must be filtered by means of an L-C filter (insight the same concept in **Lab6**), resulting in the waveforms shown in Figure 1-4.

(a) DC-AC PWM Inverter With L-C Filter

(b) Voltage and Current Waveforms without C_o

(c) Voltage and Current Waveforms with C_o
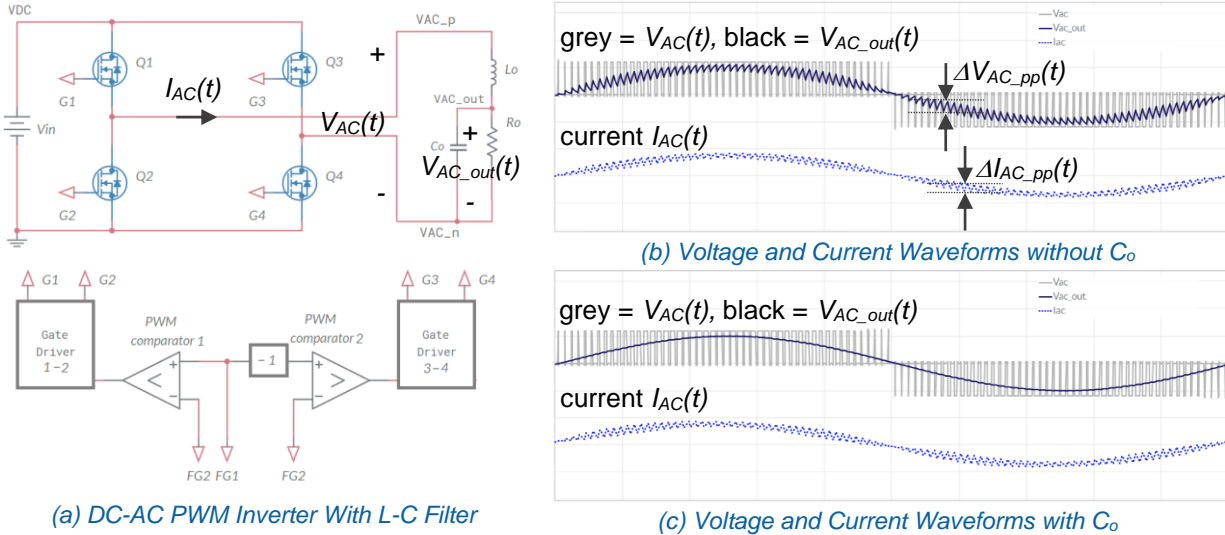
Figure 1-4. AC Currents of an Ohmic Load Powered by a DC-AC PWM Inverter with L-C Filter.

As discussed in Section 1-4, the current of an ohmic-inductive load has a sinusoidal component at frequency f_m of the reference signal and a triangular ripple component at switching frequency f_s. Adding an inductor L_o in series to an ohmic load R_o determines the same effect of an ohmic-inductive load. The inductance L_o needed to keep the peak-peak amplitude of AC ripple component below a given limit $\Delta I_{AC\_out,pp max}$, is given by Equation 1-7:

Equation 1-7
$$L_o = \frac{V_{DC}}{4 f_s \Delta I_{AC\_out,pp max}}$$

Without a parallel capacitor, the resulting maximum peak-peak amplitude of ripple voltage on load resistor R_o will be $\Delta V_{AC\_out,pp max} = R_o \Delta I_{AC\_out,pp max}$. The maximum peak-peak amplitude of load ripple voltage with a parallel capacitor of capacitance C_o is given by Equation 1-8:

Equation 1-8
$$\Delta V_{AC\_out,pp max} = \frac{\Delta I_{AC\_out,pp max}}{8 f_s C_o}$$

From Equation 1-8, the capacitance C_o needed to keep the maximum peak-peak amplitude of switching frequency load ripple voltage below a given limit $\Delta V_{AC\_out,pp max}$ is given by Equation 1-9:

Equation 1-9
$$C_o = \frac{\Delta I_{AC\_out,pp max}}{8 f_s \Delta V_{AC\_out,pp max}}$$

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What is the function of a DC-AC inverter?
   A. to convert a DC source voltage into an AC load voltage
   B. to invert the flow of energy between a DC source and a DC load
   C. to invert the polarity of a DC source voltage

1-2 How can we achieve the conversion of a DC voltage into an AC voltage?
   A. by means of a transformer
   B. by means of a MOSFETs full-bridge
   C. by means of a diodes full-bridge

1-3 What type of AC waveform we obtain with a DC-AC PWM inverter?
   A. a sinusoid with a triangular ripple component
   B. a sinusoid with a DC component
   C. a train of square pulses

1-4 What type of AC load powered by DC-AC PWM inverter absorbs a quasi-sinusoidal current?
   A. an ohmic-capacitive load
   B. an ohmic-inductive load
   C. an ohmic load

1-5 How do we obtain a sinusoidal AC voltage for an ohmic load from a DC-AC PWM inverter?
   A. by mean of an L-C filter
   B. by means of capacitors in parallel to the MOSFETs
   C. by means of an inductor in series to the source

1-6 How do the values of the inductance and capacitance of the L-C filter of a DC-AC PWM inverter, needed to limit the amplitude of AC current and voltage ripple components, change as the PWM switching frequency increases?
   A. they increase
   B. they decrease
   C. they do not depend on the PWM switching frequency

2 Exercise

The MOSFET full-bridge of the DC-AC Inverter Section of the TI Power Electronics Board for NI ELVIS III can be connected to a 50Ω load resistor R_o through an L-C filter, comprised of a 6.8mH series inductor L_o and a 10µF parallel capacitor C_o.

2-1 Assuming that the DC source provides a DC voltage V_{DC} = 10V, the PWM modulator triangular carrier has a 5kHz switching frequency f_s and a 6.0V peak-peak amplitude V_{rpp}, the AC reference voltage has a 50Hz modulation frequency f_m and 2.5V amplitude V_{ref}, use the rules and equations provided in the **Theory and Background** section to calculate:

- the amplitude of AC sinusoidal component $I_{AC}(t)$ of the series R_o-L_o at modulation frequency f_m, in Ampère with three decimal digits of accuracy:
  I_{AC} = _____
- the maximum peak-peak amplitude of AC ripple component $\Delta I_{AC,pp}(t)$ of the series R_o-L_o at switching frequency f_s, in Ampère with three decimal digits of accuracy, and the ratio between the instant t_{max} where that maximum is reached and the modulation period T_m, with two decimal digits:
  $\Delta I_{AC,pp}$max = _____ t_{max}/T_m = _____
- the maximum peak-peak amplitude of AC ripple component $\Delta V_{AC\_out,pp}(t)$ of voltage on ohmic load resistor R_o at switching frequency f_s, in Volt with three decimal digits of accuracy:
  $\Delta V_{AC,pp}$max = _____

2-2 Assuming R_o= 50Ω, for the values of switching frequency f_s listed in Table 2-1, use the equations provided in the **Theory and Background** section to calculate:

- the L-C filter inductance L_o needed to limit the maximum peak-peak amplitude of AC current ripple component $\Delta I_{AC,pp}$max to 50mA, in milli Henry with two decimal digits of accuracy;
- the L-C filter capacitance C_o needed to limit the maximum peak-peak amplitude of AC voltage ripple component $\Delta V_{AC\_out,pp}$max to 100mV, in micro Farad with two decimal digits of accuracy.

Table 1-1 Inductance and Capacitance of L-C filter as Function of PWM Switching Frequency f_s.

f_s [kHz]	1	5	10	50
L_o [mH]				
C_o [µF]				

3 Simulate

The goal of the simulations you will perform in this section is to analyze the operation of a DC-AC PWM Inverter. You will observe the AC voltage and current waveforms under different operating conditions, to verify the impact of PWM switching frequency and the consistency of the theoretical model.

3-1 Instructions

1. Open *Lab9 – DC-AC PWM Inverter Operation* from this file path:
   https://www.multisim.com/content/kTPAgYp6A2aPhxtxVMBdMd/lab-9-dc-ac-inverter-pwm-operation/
   The circuit schematic for the analysis of the DC-AC PWM inverter is shown in Figure 3-1. The MOSFETs are modeled by means of two *Single Pole Single Throw (SPST)* switches. The gate drivers include time delays *td1–td4* and gates A1–A4 to prevent cross conduction of the MOSFETs. The switches *JLo* and *JCo* allow the output L-C filter configuration. An input L-C filter is also included, which can be configured by means of switches *JLin* and *JCin*. Voltage-Controlled sources *AC_probe* and *AC_out_probe* allow AC differential voltage measurements.
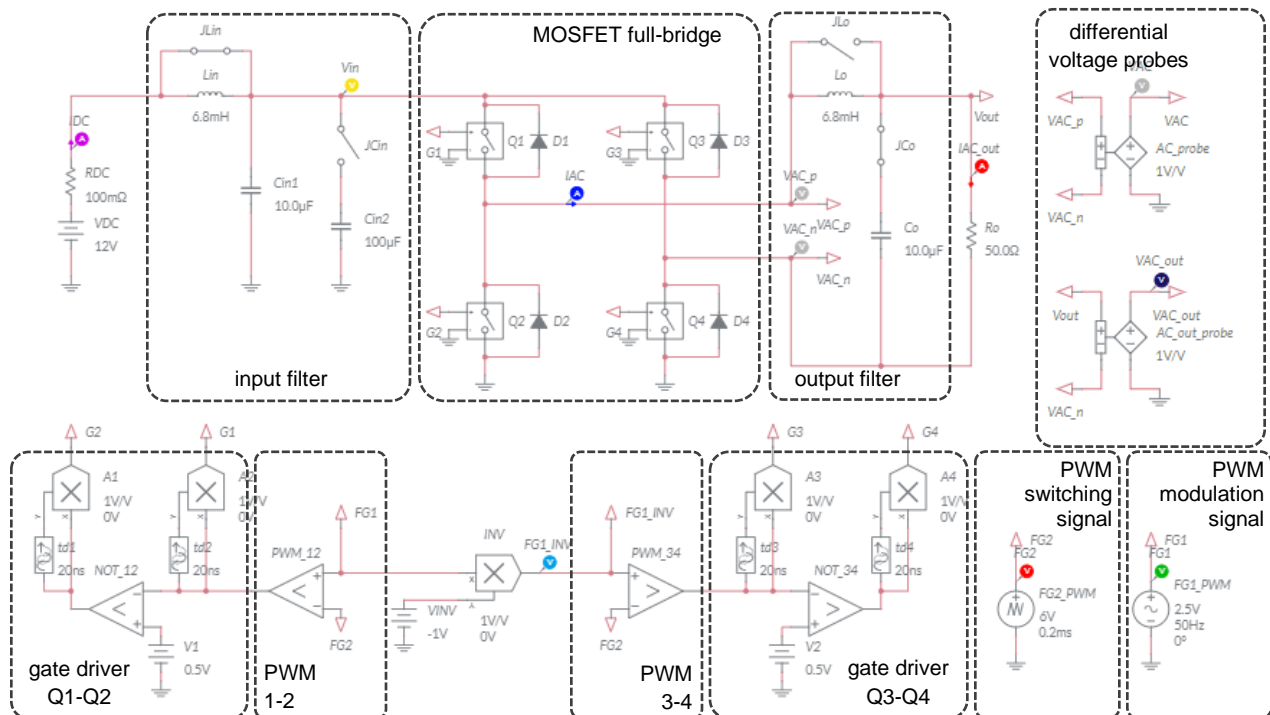
Figure 3-1. Multisim Live Circuit Schematic for the Analysis of the DC-AC PWM Inverter Operation.

3-1-1 Simulation 1 - PWM inverter operation with ohmic load.

1. Set the switches as indicated in Table 3-1-1.

Table 3-1-1 Switches Setup for Simulation 1

JLin	JCin	JLo	JCo
shorted	open	shorted	open

2. Set the circuit parameters as follows:
   - *FG1 (sinusoidal modulation signal)*: *VA* = 2.5V, *Freq* = 50Hz, Offset 0.0V;
   - *FG2 (triangular switching signal)*: *VA* = 6V, *Per* = 500µs, *TF* = 250µs, Offset -3V;
3. Double click on probes *FG1*, *VAC_out* and *IAC_out,* and check the *Show plot* option box. Uncheck the *Show plot* option box for all the other probes.
4. *Interactive* simulation and *Grapher* visualization options.
5. Run the simulation and wait until it stops.

3-1-1 Is the waveform of AC voltage of load resistor *VAC_out* a train of square pulses, whose width is proportional to the instant value of the modulation sinusoid *FG1*?

    A.   yes
    B.   no
Please provide your comments: _____

_____

3-1-2 Are the waveforms of load resistor voltage and current *VAC_out* and *IAC_out* similar?

    A.   yes
    B.   no
Please provide your comments: _____

_____

3-2-1 Simulation 2 - PWM inverter operation with ohmic load and series filter inductor.

1. Set the switches as indicated in Table 3-2-1.

Table 3-2-1 Switches Setup for Simulation 1

JLin	JCin	JLo	JCo
shorted	open	open	open

2. Set the circuit parameters as follows:
    - *FG1 (sinusoidal modulation signal)*: *VA* = 2.5V, *Freq* = 50Hz, Offset 0.0V;
    - *FG2 (triangular switching signal)*: *VA* = 6V, *Per* = 500µs, *TF* = 250µs, Offset -3V;
3. Double click on probes *FG1*, *VAC, VAC_out* and *IAC_out,* and check the *Show plot* option box. Uncheck the *Show plot* option box for all the other probes.
4. Select *Interactive* simulation and *Grapher* visualization options.
5. Run the simulation and wait until it stops.

3-2-1 Do the waveforms of AC voltage *VAC_out* and current *IAC_out* of load resistor show a sinusoidal component at modulation frequency f_m and a ripple component at switching frequency f_s?

    A.   yes
    B.   no
    Please provide your comments: _____

_____

3-2-2 Is the peak-peak amplitude of AC voltage *VAC_out* and current *IAC_out* ripple component variable during the modulation period T_m?

    A.   yes
    B.   no
    Please provide your comments: _____

_____

3-2-2 Detect the instant t_{max} where the peak-peak amplitude of AC voltage *VAC_out* and current *IAC_out* ripple component reach the maximum and calculate the ratio t_{max}/T_m. Is the result consistent with the value calculated by means of *Equation 1-6* provided in the **Theory and Background** Section?

    A.   yes
    B.   no
    Please provide your comments: _____

_____

3-3-1 Simulation 3 - PWM inverter operation with ohmic load and L-C Filter.
1. Set the switches as indicated in Table 3-3-1.

Table 3-3-1 Switches Setup for Simulation 1

JLin	JCin	JLo	JCo
shorted	open	open	shorted

2. Set the circuit parameters as follows:
   - *FG1 (sinusoidal modulation signal)*: *VA* = 2.5V, *Freq* = 50Hz, Offset 0.0V;
   - *FG2 (triangular switching signal)*: *VA* = 3V, *Per* = 500µs, *TF* = 250µs, Offset -3V;
3. Double click on probes *FG1*, *VAC*, *IAC*, *VAC_out* and *IAC_out,* and check the *Show plot* option box. Uncheck the *Show plot* option box for all the other probes.
4. Select *Interactive* simulation and *Grapher* visualization options.
5. Run the simulation and wait until it stops.

3-3-1 Is the peak-peak amplitude of ripple components of load voltage and current at switching frequency f_s lower than in Simulation 2?

   A.   yes
   B.   no
   Please provide your comments: _____

   _____

3-3-2 Is the peak-peak amplitude of AC ripple component at switching frequency f_s bigger in current *IAC* or in current *IAC_out*?

   A.   bigger in current *IAC*
   B.   bigger in current *IAC_out*
   C.   other: _____

   _____

   Please provide your comments: _____

   _____

Troubleshooting tips:

   If the simulation does not converge and you get some error message, reload *Lab9 – DC-AC PWM Inverter Operation* from this file path https://www.multisim.com/content/kTPAgYp6A2aPhxtxVMBdMd/lab-9-dc-ac-inverter-pwm-operation/ and restart the simulation following the instructions.

4 Implement

The experiments you perform in this section allow you to observe the voltage and current waveforms of a real DC-AC PWM inverter operation, under different operating conditions. The **DC-AC Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments. The full-bridge uses four TI's CSD16322Q5C MOSFETs, two TI's TLV7011DPWR comparators and two TI's UCC27712DR MOSFET drivers. The full-bridge AC output can be connected to a 50Ω resistance R_o, by means of the Jumper J21. The jumpers J24 and J27 allow to connect a 6.8mH inductor in series and a 10µF in parallel to the load resistor R_o, respectively. The modulation sinusoidal signal *FG1* and the triangular switching signal *FG2* are available at test points TP71 and TP70, respectively. The datasheets of TI's components are available at these links:

- CSD16322Q5C MOSFET: (http://www.ti.com/lit/ds/symlink/csd16322q5c.pdf)
- TLV7011DPWR COMPARATOR: (http://www.ti.com/lit/ds/symlink/tlv7011.pdf)
- UCC27712DR GATE DRIVER: (http://www.ti.com/lit/ds/symlink/ucc27712.pdf).
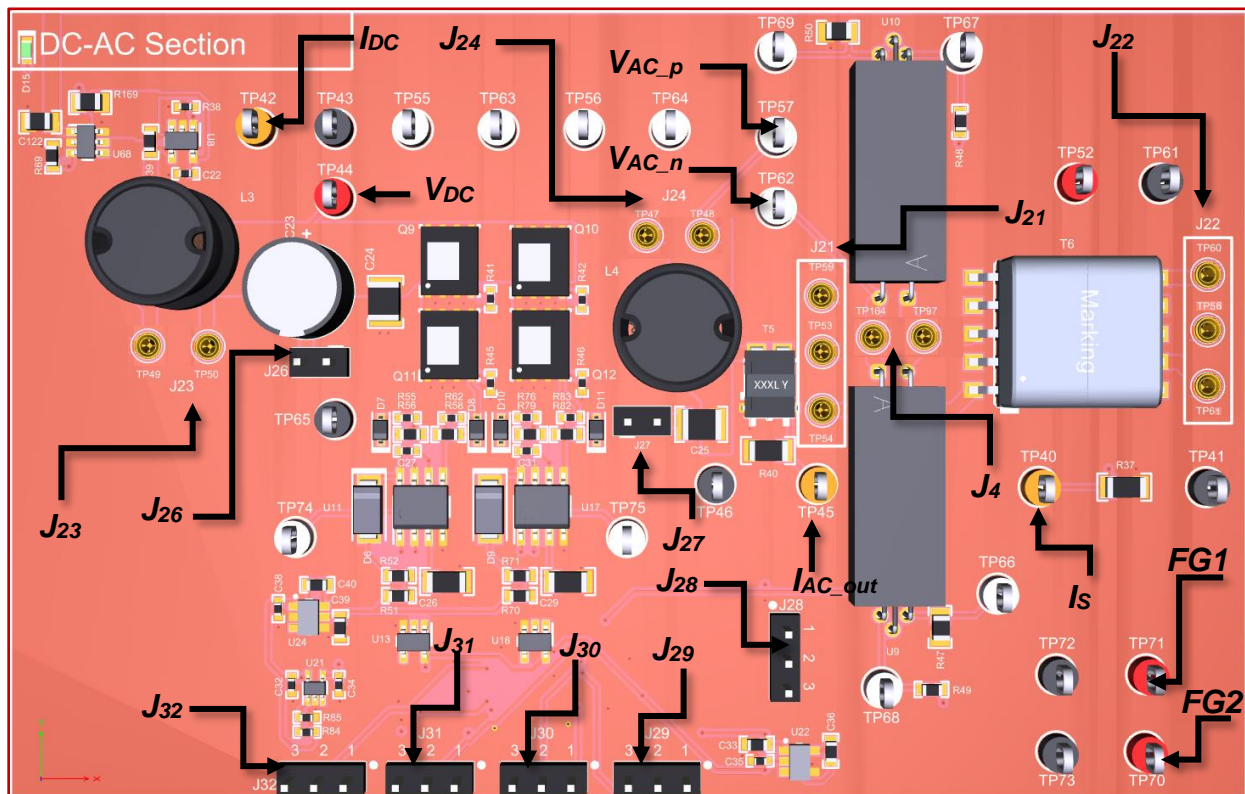

Figure 4-1. TI Power Electronics Board for NI ELVIS III – DC-AC Section Used for the Analysis of MOSFET DC-AC PWM Inverter Operation.

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 Instructions

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Pattern Generator* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/

2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.

4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab9 – DC-AC PWM Inverter Operation*.

5. Connect and configure the instruments as indicated in Tables 4-1 and 4-2. [**Note:** the AC load voltage can be observed on the *Oscilloscope* Math channel, which provides the difference between CH-1 (V_{AC_p}) and CH-2 (V_{AC_n})]

Table 4-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP57 (V_{AC_p}), connect CH-2 to TP62 (V_{AC_n}) connect CH-3 to TP70 (*FG2*), connect CH-4 to TP71 (*FG1*)
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP71 = *FG1*) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP70 = *FG2*)
Pattern Generator	connect TRIG to DIO 0 (red) and GND (black) using a BNC-to-Alligator Cable

Table 4-2 Instruments Configuration and setup

Power Supply	*Channel "+"*: Static, 10.00V, *Channel "-"*: Inactive				
Oscilloscope	*Trigger*: Analog Edge, CH-4, set to 50%	*Horizontal*: 2ms/div	*Acquisition*: average	*Measurements*: hide	
	Channel 1: ON • DC coupling • 5V/div • offset 15V	*Channel 2*: ON • DC coupling • 5V/div • offset 0V	*Channel 3*: ON • DC coupling • 1V/div • offset 0V	*Channel 4*: ON • DC coupling • 1V/div • offset 0V	*Math*: ON • CH1-CH2 • 5V/div • offset -15V
Function Generator	*follow instructions provided below*				
Pattern Generator	*follow instructions provided below*				

6. Configure the jumpers of the board as indicated in Table 4-3.

Table 4-3 Jumpers Setup

J21	J22	J23	J24	J26	J27
short TP53-TP59	open	shorted	shorted	shorted	open
J4	**J28**	**J29**	**J30**	**J31**	**J32**
shorted	short 2-3	short 2-3	short 2-3	short 1-2	short 2-3

7. Perform the Experiments 1 to 5 in the sequence they are presented.

4-2 Experiment 1 - PWM inverter operation with ohmic load, 50Hz modulation frequency and 500Hz switching frequency.

1. On *Channel 1* of the *Function Generator*:
   a. select *Custom* and use the file selector to select the TDMS waveform *Lab9_FG1_sinusoidal_50Hz_450mVpp_25kSps*;
   b. set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 25kS/s, set *Generation mode* to *Loop*.
2. On *Channel 2* of the *Function Generator*:
   a. select *Custom* and use the file selector to select the TDMS waveform *Lab9_FG2_triangular_500Hz_1Vpp_25kSps*;
   b. set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 25kS/s, set *Generation mode* to *Loop*.
3. On *Logic Analyzer and Pattern Generator*:
   a. click on *"+"* in the *Pattern Generator* section;
   b. click on *Signal* to add a new signal to the *Pattern Generator*;
   c. check the box next to *Logic 0* to add the line and click on the whitespace in the instrument;
   d. set *Status* to *On*, set *Mode* to *Clock*, set *Frequency* to 1Hz, set *Duty cycle* to 50%.

4. Run *Oscilloscope, Pattern Generator*, *Function Generator* and *Power Supply*.

5. Stop *Power Supply, Function Generator, Pattern Generator* and *Oscilloscope*.

6. You should see on the *Oscilloscope* the 50Hz sinusoidal modulation waveform on CH4 and the 500Hz triangular switching waveform on CH3.

4-2-1 Please describe the waveforms you observe on *Oscilloscope* CH-1 and CH-2:

_____

_____

4-2-2 Please describe the waveforms you observe on *Oscilloscope* Math channel:

_____

_____

4-2-3 Is the waveform of the load voltage observed on Math channel corresponding to your expectation, based on **Theory and Background** learning and simulations?

A.   yes
B.   no

Please provide your comments: _____

_____

_____

4-3   Experiment 2 - PWM inverter operation with ohmic load, 50Hz modulation frequency and 2kHz switching frequency.

1   On *Channel 2* of the *Function Generator*:
   a. select *Custom* and use the file selector to select the TDMS waveform *Lab9_FG2_triangular_2kHz_1Vpp_25kSps*;
   b. set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 25kS/s, set *Generation mode* to *Loop*.

2   Run *Oscilloscope, Pattern Generator*, *Function Generator* and *Power Supply*.

3   Stop *Power Supply, Function Generator, Pattern Generator* and *Oscilloscope*.

4   You should see on the *Oscilloscope* the 50Hz sinusoidal modulation waveform on CH4 and the 2kHz triangular switching waveform on CH3.

4-3-1 Please describe the waveforms you observe on *Oscilloscope* CH-1 and CH-2:

_____

_____

4-3-2 Please describe the waveforms you observe on *Oscilloscope* Math channel:

_____

_____

4-3-3 Does the waveform of the load voltage you observe on Math channel complies with your expectation, based on **Theory and Background** learning and simulations?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

    _____

[**Note:** the *Oscilloscope* sampling rate is 25kS/s when the time base is set to 2ms/div: as a result, you will not see sharp rise and fall edges in all the square pulses on CH1, CH2 and Math channel, unlike you did with 500Hz switching frequency. To see the sharp edges of square pulses of the load voltage you can set the *Oscilloscope* time base to 200µs/div, run the *Oscilloscope*, *Function Generator* and *Power Supply*, stop the *Oscilloscope* and observe the Math channel. You will see just few pulses, instead of an entire modulation period of the waveform]

4-4 Experiment 3 - PWM inverter operation with ohmic load and series inductor.

1. Set the jumper J24 to be OPEN.
2. Run *Oscilloscope, Pattern Generator*, *Function Generator* and *Power Supply*.
3. Stop *Power Supply, Function Generator, Pattern Generator* and *Oscilloscope*.

4-4-1 Does the waveform of the load voltage you observe on Math channel comply with your expectation, based on **Theory and Background** learning and simulations?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

    _____

4-4-2 Is there a sinusoidal component at modulation frequency in the load voltage waveform?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-4-3 Is there a triangular component at switching frequency in the load voltage waveform?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-4-4 Does the peak-peak amplitude of the triangular component at switching frequency show a maximum over the modulation period? where? what is its value?

    A.   yes:

    it is located at $t_{max}/T_m =$ _____ , and its value is $\Delta V_{AC\_out,pp}\text{max}@fs$ [mV] = _____

    B.   no

    Please provide your comments: _____

    _____

    [**Note:** the *Oscilloscope* sampling rate is 25kS/s when time base is set to 2ms/div: the resulting measurement of the peak-peak amplitude of the triangular component at switching frequency $\Delta V_{AC\_out,pp}\text{max}@fs$ can be not accurate. To improve the measurement accuracy, you can reduce the *Oscilloscope* time base to 200µs/div]

4-5 Experiment 4 - PWM inverter operation with ohmic load, series inductor and parallel capacitor.

1. Set the jumper J27 to be SHORTED.
2. Run *Oscilloscope, Pattern Generator*, *Function Generator* and *Power Supply*.
3. Stop *Power Supply, Function Generator, Pattern Generator* and *Oscilloscope*.
4. Using the *Oscilloscope* cursors on the Math channel, measure the peak-peak amplitude of the load voltage waveform at the modulation frequency f_m, in Volts with one decimal digit: $V_{AC\_out,pp}@fm =$ _____;

4-4-1 Does the waveform of the load voltage you observe on Math channel complies with your expectation, based on **Theory and Background** learning and simulations?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-4-2 Is the sinusoidal component at modulation frequency in the load voltage waveform the same you have observed in Experiment 3?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-4-3 Does the peak-peak amplitude of the triangular component at switching frequency show a maximum over the modulation period? where? what is its value?

    A.   yes:

    it is located at $t_{max}/T_m =$ _____ , and its value is $\Delta V_{AC\_out,pp}\text{max}@fs$ [mV] = _____

    B.   no

    Please provide your comments: _____

    _____

    [**Note:** the *Oscilloscope* sampling rate is 25kS/s when time base is set to 2ms/div: the resulting measurement of the peak-peak amplitude of the triangular component at switching frequency $\Delta V_{AC\_out,pp}\text{max}@fs$ can be not accurate. To improve the measurement accuracy, you can reduce the *Oscilloscope* base to 200µs/div]

4-6 Experiment 5 - PWM inverter operation with ohmic load and series inductor, under different switching frequency conditions.

1. Set the jumpers J24 and J27 to be OPEN.
2. Run *Oscilloscope, Pattern Generator*, *Function Generator* and *Power Supply*.
3. Stop *Power Supply, Function Generator, Pattern Generator* and *Oscilloscope*.
4. Using the *Oscilloscope* Cursors on the Math channel, measure the peak-peak amplitude $V_{AC\_out,pp}@fm$ of the load voltage waveform at the modulation frequency f_m, in Volts with one decimal digit, and the maximum peak-peak amplitude of the load ripple voltage $\Delta V_{AC\_out,pp}\text{max}@fs$ at the switching frequency f_s, in Volts with two decimal digits, and report the results in Table 4-5-1.
   [**Note:** the *Oscilloscope* sampling rate is 25kS/s when time base is set to 2ms/div: the resulting measurement of the peak-peak amplitude of the triangular component at switching frequency $\Delta V_{AC\_out,pp}\text{max}@fs$ can be not accurate. To improve the measurement accuracy, you can reduce the *Oscilloscope* time base to 200µs/div].
5. Repeat step 2-3 for all the values of switching frequency listed in Table 4-5-1, by uploading on *Channel 2* of the *Function Generator* the TDMS waveforms:

a. *Lab9_FG2_triangular_3kHz_1Vpp_25kSps*,
　　b. *Lab9_FG2_triangular_4kHz_1Vpp_25kSps,*
　　c. *Lab9_FG2_triangular_5kHz_1Vpp_25kSps,*

6. Report the results in the Table 4-5-1.
7. Using the equations provided in **Theory and Background** Section, calculate the theoretical values of the maximum peak-peak amplitude of the load ripple voltage $\Delta V_{AC\_out,pp\max@fs}$, in Volt with two decimal digits, and report the results in Table 4-5-1.

Table 4-5-1 Amplitudes of Load Voltage Sinusoidal and Ripple Components as Function of Switching Frequency

f_s [kHz]	2	3	4	5
$V_{AC\_out,pp@fm}$ [V]				
$\Delta V_{AC\_out,pp\max@fs}$ [V] @ 2ms/div				
$\Delta V_{AC\_out,pp\max@fs}$ [V] @ 200µs/div				
$\Delta V_{AC\_out,pp\max@fs}$ [V] calculated				

4-5-1　Are the measured values of peak-peak amplitude of the triangular component at switching frequency consistent with calculations?

　　A.　yes
　　B.　no
　　Please provide your comments: _____

　　_____

Troubleshooting tips:
● If the DC-AC PWM inverter does not work, or the waveforms look much different with respect to simulations, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiments.

5 Analyze

5-1 Compare the Oscilloscope waveforms to the simulated waveforms, and discuss their similarities and differences based on *Theory and Background* equations:

_____

_____

_____

6 Conclusion

6-1 Summary

Write a summary of what you observed and learned about the operation of a DC-AC PWM Inverter, and discuss the impact of switching frequency, inductance and capacitance on the resulting load voltage waveform.

6-2 Expansion Activities

Investigate the DC source current determined by the operation of a DC-AC PWM Inverter, by means of Multisim Live simulations.

6-2-1. Open *Lab9 – DC-AC PWM Inverter Operation* from this file path:
`https://www.multisim.com/content/kTPAgYp6A2aPhxtxVMBdMd/lab-9-dc-ac-inverter-pwm-operation/`
The switches JCin and JLin allow connecting the additional 100µF parallel capacitor and 6.8mH series inductor to the DC source. These two component help filtering the switching frequency ripple current component of the AC current I_{AC}.

6-2-2. Set the switches as indicated in Table 6-2-1.

Table 6-2-1 Switches Setup

JLin	JCin	JLo	JCo
shorted	open	open	open

  a. Set the circuit parameters as follows:
   - *FG1 (sinusoidal modulation signal)*: *VA* = 2.5V, *Freq* = 50Hz, Offset 0.0V;
   - *FG2 (triangular switching signal)*: *VA* = 6V, *Per* = 200µs, *TF* = 100µs, Offset -3V;
  b. Double click on probes *IDC, FG1*, *VAC* and *IAC,* and check the *Show plot* option box. Uncheck the *Show plot* option box for all the other probes.

c. Select *Interactive* simulation and *Grapher* visualization options.
d. Run the simulation and wait until it stops.
e. Export the grapher image as .png format file, or the grapher data as .csv format file.
f. Set the jumper JCin to be CLOSED and repeat steps f-g.
g. Set the jumpers JCin to be OPEN and JLin to be OPEN, and repeat steps f-g.
h. Compare the switching ripple components of the DC source current I_{DC} waveforms you have obtained with the three different simulations.

6-4   Resources for learning more

- These book provides the fundamentals of DC-AC Inverters:
  - P.Krein, *Elements of Power Electronics*, Oxford Press
  - N.Mohan, T.M.Undeland, W.P.Robbins, *Power Electronics: Converters, Applications and Design*, John Wiley & Sons

Answer Key – Check Your Understanding Questions Only
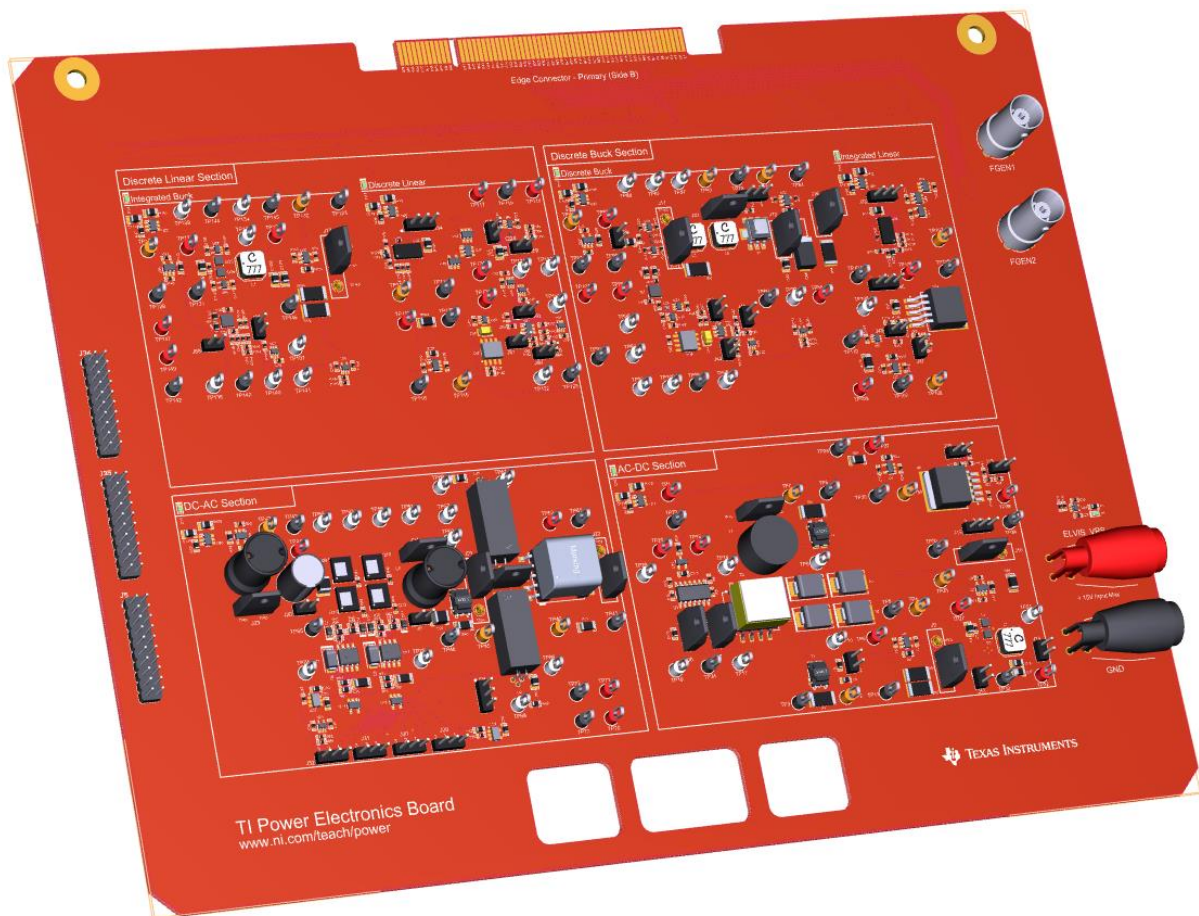
Check Your Understanding

1-1   A

1-2   B

1-3   A

1-4   B

1-5   A

1-6   B

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 10: High-Frequency Transformer Operation

Lab 10: High-Frequency Transformer Operation

The goal of this lab is to investigate the behavior of a high-frequency power transformer, which is widely used in isolated switching power supplies to step-up and step down the voltage and to achieve galvanic isolation between the source and the load. First, we review the principle of operation and the main equations and waveforms of a transformer. Next, we simulate the transformer to analyze the effects of its parameters on voltage and current waveforms. Finally, we perform lab experiments to observe the voltages and currents of a real high-frequency transformer under square-wave voltage operation.
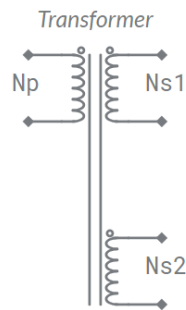
Figure 1-1. Transformer

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a transformer and an AC source with specified parameters, you will calculate the amplitude of its primary and secondary side voltages and currents and the minimum operating frequency needed to avoid saturation, with specified units and accuracy, under different secondary coils configurations.

2. Given a transformer and an AC source with specified parameters, you will simulate its operation under different secondary coils configurations, to analyze the effect of transformer parameters on voltage and current waveforms, verify their consistency with theoretical predictions, and observe the magnetizing current drift caused by primary coil voltage DC component.

3. Given a real transformer and a full-bridge inverter applying a square-wave of given amplitude and frequency to the primary coil voltage, you will observe the transformer voltage and current waveforms and measure their amplitudes, with specified units and accuracy, to verify the transformer behavior in step-up and step-down operation and estimate the transformer magnetizing inductance.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

- ✓ Access Instruments
  https://measurementslive.ni.com/
- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ni-elvis-iii.html
- ✓ View Tutorials
  https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

---

Software: NI Multisim Live

- ✓ Access
  https://www.multisim.com/
- ✓ View Tutorial
  https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

- ✓ Download (Windows OS Only)
  http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

  Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a transformer. First, we analyze the principle of operation and the resulting voltage and current waveforms. Next, we discuss the effect of magnetizing and leakage inductance on the transformer operation. Finally, we analyze the effect of windings resistance.

1-2 Ideal Transformer

A transformer is comprised of a *primary coil* with N_p turns and N *secondary coils* with $N_{s1},…,N_{sN}$ turns, wounded around a core of magnetic material. The transformer converts the AC *primary voltage* $V_p(t)$, applied to the primary coil, into the AC *secondary voltages* $V_{s1}(t)$, …, $V_{sN}(t)$ of secondary coils, according to Equations 1-1:

Equations 1-1
$$V_{s2}(t) = \frac{N_{s1}}{N_p} V_p(t), \qquad … , V_{sN}(t) = \frac{N_{sN}}{N_p} V_p(t)$$

If load resistors R_{o1}, …, R_{oN} are connected to the secondary coils, the secondary currents $I_{s1}(t) = V_{s1}(t)/R_{o1}$, …, $I_{sN}(t) = V_{sN}(t)/R_{oN}$ are proportionally reflected to the primary coil, resulting in the total primary coil current given in Equation 1-2:

Equation 1-2
$$I_p(t) = \frac{N_{s1}}{N_p} I_{s1}(t) + … + \frac{N_{sN}}{N_p} I_{sN}(t)$$

Figure 1-2(a) shows a transformer with two secondary coils. Figures 1-2(b) and 1-2(c) show the primary and secondary voltage and current waveforms of the transformer with $N_p = 10$, $N_{s1} = 5$, $N_{s2} = 2$, $R_{o1} = R_{o2} = 50\Omega$, subjected to a 100kHz/20Vpp sinusoidal and square-wave primary voltage.
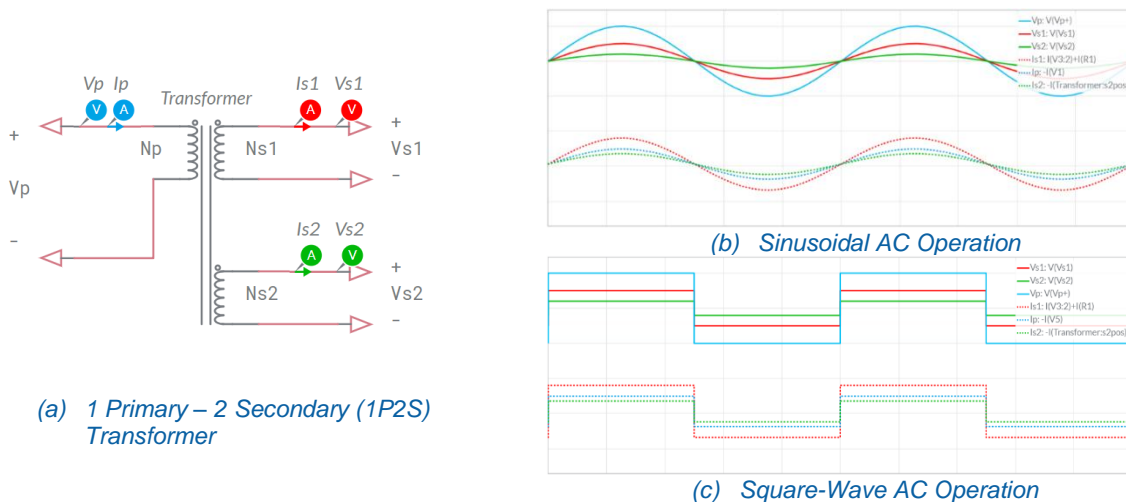

(a) 1 Primary – 2 Secondary (1P2S) Transformer

(b) Sinusoidal AC Operation

(c) Square-Wave AC Operation

Figure 1-2. Ideal Transformer Input and Output Waveforms in AC Operation.

Depending on the turns ratios N_{s1}/N_p, and N_{s2}/N_p, the transformer can convert the primary voltage $V_p(t)$ into higher or lower secondary voltages $V_{s1}(t)$ and $V_{s2}(t)$. Similarly, the secondary currents $I_{s1}(t)$ and $I_{s2}(t)$ are reflected into higher or lower primary coil currents. Based on Equations 1-1 and 1-2, an ideal transformer performs the conversion of voltages and currents without power loss:

Equation 1-3
$$V_p(t)I_p(t) = V_p(t)\frac{N_{s1}}{N_p}I_{s1}(t) + V_p(t)\frac{N_{s2}}{N_p}I_{s2}(t) = V_{s1}(t)I_{s1}(t) + V_{s2}(t)I_{s2}(t)$$

1-3 Real Transformer

Figure 1-3(a) shows the simplified circuit model of a real transformer, where R_p, R_{s1} and R_{s2} are the coil resistances, L_m is the magnetizing inductance and L_p is the primary leakage inductance. The parameters R_p, R_{s1}, R_{s2}, L_m and L_p model the transformer power losses, magnetic core flux and the leakage flux, respectively. In a good transformer, L_m is big and L_p is small. The magnetizing inductance L_m majorly influences the primary coil current waveform, as shown in Figure 1-3(b) for a of transformer with $N_p =10$, $N_{s1} = 5$, $N_{s2} = 2$, $R_p = 50\text{m}\Omega$, $R_{s1} = 30\text{m}\Omega$, $R_{s2} = 35\text{m}\Omega$, $L_m = 100\mu\text{H}$, $L_p = 0.5\mu\text{H}$, subjected to a 100kHz/20Vpp square-wave primary voltage. The effect of the magnetizing inductance is visible as a triangular component on the primary coil current waveform of Figure 1-3(b). The current of the magnetizing inductance can be better observed in no load operation, as shown in Figure 1-3(c).

(a)   1 Primary – 2 Secondary (1P2S) Transformer

(b)   Square-Wave Operation with Load
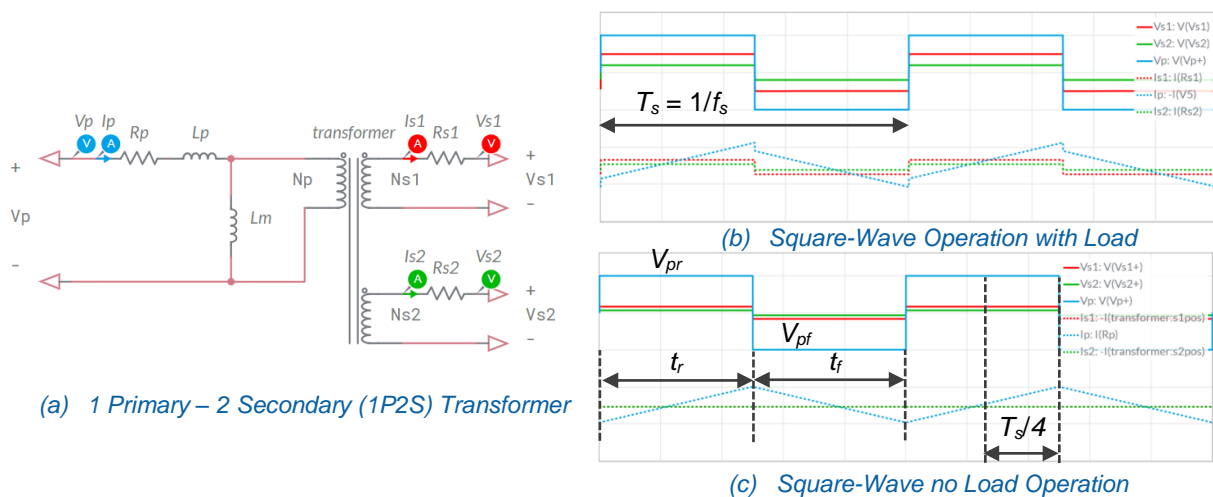
(c)   Square-Wave no Load Operation

Figure 1-3. Real Transformer Input and Output Waveforms in Square-Wave Operation.

The magnetizing inductance L_m depends on primary coil turns number and on magnetic core cross-section A_c, path length ℓ_m and permeability μ, as shown in Equation 1-4:

Equation 1-4
$$L_m = \frac{N_p^2 \mu A_c}{1_m}$$

From Figure 1-3(c), the peak value $I_{Lm,pk}$ of the magnetizing current is given by Equation 1-5:

$$I_{Lm,pk} = \frac{1}{L_m} \int_0^{T_s/4} V_p(t)dt = \frac{V_{Lm}}{4f_s L_m} \; ; \qquad V_{Lm} = \frac{V_p}{1 + R_p \left(\frac{N_{s1}^2}{N_p^2} \frac{1}{R_{s1} + R_{o1}} + \frac{N_{s2}^2}{N_p^2} \frac{1}{R_{s2} + R_{o2}} \right)}$$

The condition $I_{Lm,pk} < I_{sat} = B_{sat}\ell_m/(\mu N_p)$ must be fulfilled to prevent the saturation of the magnetic core, where B_{sat} is the maximum magnetic flux density of the core material. From Equation 1-5, the condition to prevent core saturation determines the maximum value λ_{max} of the Volt-second integral that can be applied to the primary coil:

$$\lambda = \int_0^{T_s/4} V_p(t)dt = \frac{V_{Lm}}{4f_s} < L_m I_{Lm,sat} = \lambda_{max}$$

The DC component of primary coil voltage must be zero, to prevent the magnetizing current to rise above I_{sat}, which can result in the saturation of the magnetic core and overcurrent condition in the primary coil. From Figure 1-3(c), the DC component of primary coil voltage is zero if $V_{pr}t_r + V_{pf}t_f = 0$.

1-4 Transformer Power Losses and Efficiency

The secondary coils resistances R_{s1} and R_{s2} influence the load voltage and power, as shown in Equations 1-6, and cause power losses given by Equations 1-7:

$$V_{Ro1} = \frac{R_{o1}V_{Lm}}{R_{s1} + R_{o1}} \frac{N_{s1}}{N_p} \; ; \quad V_{Ro2} = \frac{R_{o2}V_{Lm}}{R_{s2} + R_{o2}} \frac{N_{s2}}{N_p} \; ; \quad P_{Ro1} = \frac{R_{o1}V_{Lm}^2}{(R_{s1} + R_{o1})^2} \frac{N_{s1}^2}{N_p^2} \; ; \quad P_{Ro2} = \frac{R_{o2}V_{Lm}^2}{(R_{s2} + R_{o2})^2} \frac{N_{s2}^2}{N_p^2}$$

$$P_{Rs1} = \frac{R_{s1}V_{Lm}^2}{(R_{s1} + R_{o1})^2} \frac{N_{s1}^2}{N_p^2} \; ; \quad P_{Rs2} = \frac{R_{s2}V_{Lm}^2}{(R_{s2} + R_{o2})^2} \frac{N_{s2}^2}{N_p^2}$$

The primary coil current has a square component of amplitude I_{sp}, corresponding to the sum of the secondary coils currents reflected to the primary coil, given by Equation 1-8:

$$I_{sp} = V_{Lm} \left(\frac{N_{s1}^2}{N_p^2} \frac{1}{R_{s1} + R_{o1}} + \frac{N_{s1}^2}{N_p^2} \frac{1}{R_{s2} + R_{o2}} \right)$$

The primary coil current also includes the triangular component corresponding to the magnetizing inductance current. The resulting values of the rms primary coil current and of power loss determined by the primary coil resistance R_p are given by Equations 1-9:

$$\text{Equation 1-9} \qquad I_{p,rms} = \sqrt{I_{sp}^2 + \frac{I_{sp}V_{Lm}}{2f_s L_m} + \frac{V_{Lm}^2}{12f_s^2 L_m^2}}; \qquad P_{Rp} = R_p I_{p,rms}^2$$

The magnetic core is affected by hysteresis and eddy current losses, given by Equation 1-10:

$$\text{Equation 1-10} \qquad P_{core} = A_c l_m K_{fe} \left(\frac{V_p}{4f_s A_c N_p} \right)^{\beta}$$

where and K_{fe} and β are characteristic parameters depending on frequency and on magnetic core material. The resulting efficiency of the transformer is given by Equation 1-11:

$$\text{Equation 1-11} \qquad \eta = \frac{P_{load}}{P_{load} + P_{loss}}; \quad P_{load} = P_{Ro1} + P_{Ro2}; \quad P_{loss} = P_{Rs1} + P_{Rs2} + P_{Rp} + P_{core}$$

1-5 Single, Parallel and Series Connections of Secondary Coils

Connecting a single secondary coil to a load resistor R_o, while the other one is open, results in Equations 1-12:

$$\text{Equation 1-12} \quad V_{Lm} = \frac{V_p}{1 + \dfrac{N_{sx}^2}{N_p^2}\dfrac{R_p}{R_{sx} + R_o}}, \quad I_{sp} = \frac{V_{Lm}}{N_p^2}\frac{N_{sx}^2}{R_{sx} + R_o}, \quad P_{Rsx} = \frac{R_{sx}V_{Lm}^2}{(R_{sx}+R_o)^2}\frac{N_{sx}^2}{N_p^2}, \quad P_{Ro} = \frac{R_o V_{Lm}^2}{(R_{sx}+R_o)^2}\frac{N_{sx}^2}{N_p^2}$$

where the subscript *sx* can be *s1* or *s2*. The two secondary coils can be connected in parallel only if $N_{s1} = N_{s2}$. This connection is adopted if a higher output current rating is required. The two coils in parallel are equivalent to a single secondary coil with resistance $R_{seq} = R_{s1}R_{s2}/(R_{s1}+R_{s2})$ and turns number $N_{seq} = N_{s1} = N_{s2}$. The two secondary coils can be connected in series. This connection is adopted if a higher output voltage rating is required. The two coils in series are equivalent to a single secondary coil with resistance $R_{seq} = R_{s1}+R_{s2}$ and turns number $N_{seq} = N_{s1}+N_{s2}$. Connecting the parallel or series secondary coils to a load resistor R_o results in the Equations 1-13:

$$\text{Equation 1-12} \quad V_{Lm} = \frac{V_p}{1 + \dfrac{N_{seq}^2}{N_p^2}\dfrac{R_p}{R_{seq} + R_o}}, \quad I_{sp} = \frac{V_{Lm}}{N_p^2}\frac{N_{seq}^2}{R_{seq} + R_o}, \quad P_{Rseq} = \frac{R_{seq}V_{Lm}^2}{(R_{seq}+R_o)^2}\frac{N_{seq}^2}{N_p^2}, \quad P_{Ro} = \frac{R_o V_{Lm}^2}{(R_{seq}+R_o)^2}\frac{N_{seq}^2}{N_p^2}$$

where R_{seq} and N_{seq} are determined according to the selected connection. Given the connection of secondary coils, the primary coil rms current and ohmic loss and transformer efficiency are given by Equations 1-13:

Equation 1-13 $I_{p,rms} = \sqrt{I_{sp}^2 + \dfrac{I_{sp}V_{Lm}}{2f_sL_m} + \dfrac{V_{Lm}^2}{12f_s^2L_m^2}}$; $P_{Rp} = R_pI_{p,rms}^2$; $\eta = \dfrac{P_{Ro}}{P_{Ro} + P_{loss}}$; $P_{loss} = \begin{cases} P_{Rsx} + P_{core} & \text{single coil} \\ P_{Rseq} + P_{core} & \text{ser/par coils} \end{cases}$

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What is the function of a transformer?
   A. to convert a square-wave source voltage into a sinusoidal load voltage
   B. to convert a primary voltage into proportional secondary voltages
   C. to transform a voltage source into a current source

1-2 What are the factors determining the ratio between primary voltage and secondary voltages?
   A. the cross section and length of coils
   B. the cross section and magnetic path length of magnetic core
   C. the primary and secondary coils turn numbers and secondary coils connection

1-3 How is the primary coil current related to the secondary coils currents?
   A. it is the sum of secondary coils currents, each one multiplied by the relevant secondary-to-primary turns ratio
   B. it is the sum of secondary coils currents
   C. it is the inverted sum of secondary coils currents

1-4 What is the effect of transformer magnetizing inductance?
   A. the primary coil current is affected by a triangular ripple component
   B. the secondary coils currents are affected by a triangular ripple component
   C. the secondary coils voltages are affected by a triangular ripple component

1-5 How can the peak amplitude of magnetizing current be reduced?
   A. by increasing the primary coil voltage or the secondary coils turns numbers
   B. by increasing the magnetizing inductance or the operation frequency
   C. by decreasing the magnetizing inductance or the primary coil turns number

1-6 Why do we need to limit the magnetizing current?
   A. to reduce the size of the transformer
   B. to prevent secondary coils overvoltage
   C. to prevent the magnetic core saturation

2 Exercise

The transformer of the DC-AC Inverter Section of the TI Power Electronics Board for NI ELVIS III is characterized by the following nominal parameters:

- $N_{s1}/N_p = N_{s2}/N_p = 0.585$
- $R_p = 50\text{m}\Omega$, $R_{s1} = 30\text{m}\Omega$, $R_{s2} = 35\text{m}\Omega$
- $L_m = 100\mu\text{H}$, $L_p = 0.5\mu\text{H}$, $\lambda_{max} = 105\mu\text{Vs}$
- $P_{core} \approx 0\text{W}$

Two connection options are available for secondary coils #1 and #2:

option (a): the secondary coil #1 is open and the secondary coil #2 is connected to a 100Ω load resistor R_o

option (b): the secondary coils #1 and #2 are connected in series with a 100Ω load resistor R_o

2-1 Assuming the voltage applied to primary coil is a 100kHz-20Vpp square-wave, use the equations provided in the **Theory and Background** section to calculate:

- the peak value of magnetizing current, in milli Ampère with one decimal digit of accuracy:

option (a): $I_{Lm,pk}$ [mA] = _____ **option (b)**: $I_{Lm,pk}$ [mA] = _____

- the value of the Volt-second integral applied to the primary coil, in micro Volt-second with one decimal digit of accuracy:

option (a): λ [μVs] = _____ **option (b)**: λ [μVs] = _____

- the amplitude of the square-wave voltage applied to load resistor R_o, in Volts with two decimal digits of accuracy:

option (a): V_{Ro} [V] = _____ **option (b)**: V_{Ro} [V] = _____

- the amplitude of the square-wave primary coil current, in milli Ampère with one decimal of accuracy:

option (a): I_{sp} [mA] = _____ **option (b)**: I_{sp} [mA] = _____

- the transformer efficiency, with three decimal digits of accuracy:

option (a): η = _____ **option (b)**: η = _____

2-2 Assuming the voltage applied to primary coil is a 20Vpp square-wave, use the equations provided in the **Theory and Background** section to calculate the minimum operating frequency allowing to prevent the core saturation, in kilo Hertz with three decimal digits of accuracy:

option (a): $f_{s,min}$ [kHz] = _____
option (b): $f_{s,max}$ [kHz] = _____

3 Simulate

The goal of the simulations you will perform in this section is to analyze the operation of a high-frequency transformer under square-wave voltage operation. You will observe the AC voltage and current waveforms under different operating conditions, to verify the impact of PWM switching frequency and the consistency of the theoretical model.

3-1 Instructions

1. Open *Lab10 – High-Frequency Transformer Operation* from this file path:
   https://www.multisim.com/content/926CMvd7zwR336GVmurMDh/lab-10-high-frequency-transformer-operation/
   The circuit schematic for the analysis of the transformer under high-frequency square-wave primary voltage operation is shown in Figure 3-1. The primary voltage is generated by a full-bridge DC-AC inverter. The switch *Str* allows to configure the connection of secondary coils to load resistor R_o, corresponding to options (a) and (b) of the **Exercise** Section. Voltage-Controlled sources *P_probe* and *S_ probe* allow primary and secondary coils differential voltage measurements.
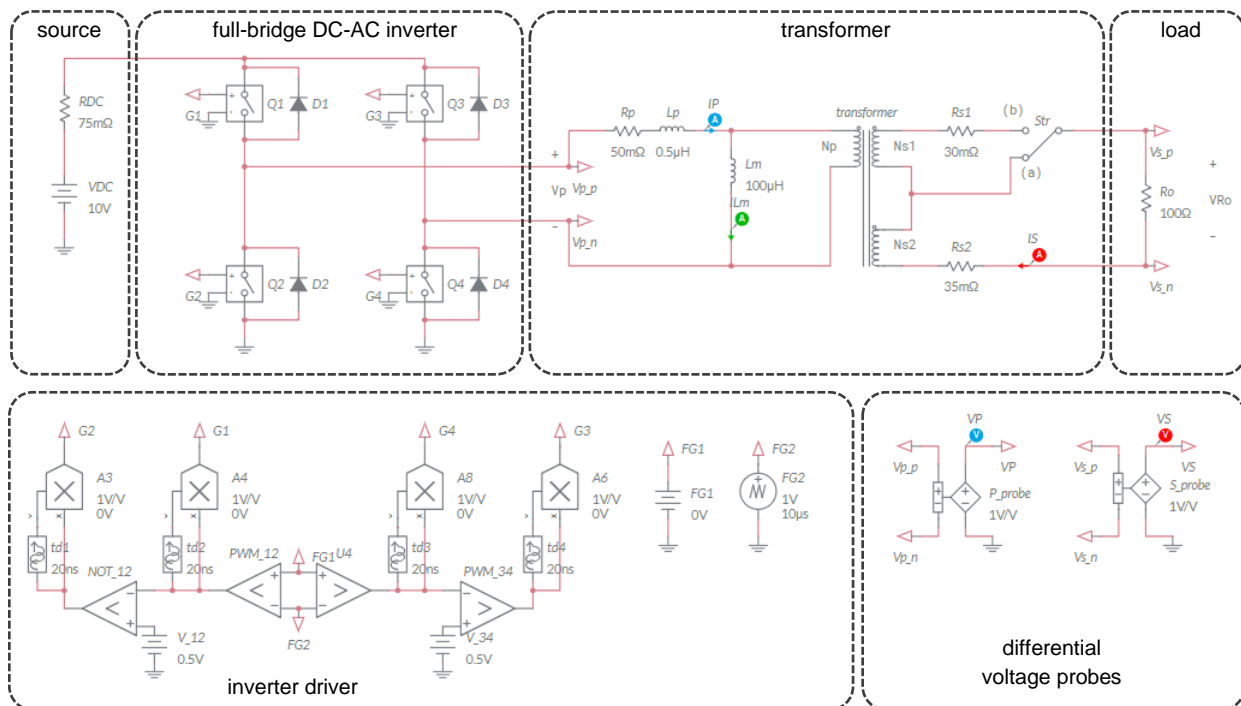

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of the High-Frequency Transformer Operation.

[**Note:** the DC voltage generator FG1 and the triangular voltage generator FG2 determine the switching frequency f_s and the rise and fall times t_r and t_f of the square-wave voltage applied to the primary coil. The amplitude of the square-wave voltage applied to the primary coil is equal to the DC voltage V_{DC} of the source generator. The triangular voltage generator FG2 is set with peak-peak amplitude $V_{rpp} = 1$Vpp, whereas the DC voltage generator FG1 is set with DC voltage $V_d = 0$. This setup provides $t_r = t_f = T_s/2$, so that the DC voltage applied to the primary coil $V_{DC}(t_r - t_f)/T_s$ is zero. If V_d is not zero, the resulting DC voltage applied to the primary coil is $4V_{DC}V_d/V_{rpp}$. This allows to observe the drift of magnetizing current].

3-2 Simulation 1 – Transformer Operation with Zero DC Component in Primary Coil Voltage.

1. Set the switch Str in position (a).
2. Set the circuit parameters as follows:
   - $FG1$: $DC\_mag = 0.0$V, $AC\_mag = 0.0$V;
   - $FG2$: $VA = 1.0$V, $Per = 10$µs, $TF = 5$µs, Offset = -0.5V;
3. Double click on probes VP, IP, VS, IS, and ILm and check the *Show plot* option box.
4. Set *Interactive* simulation and *Split* visualization options.
5. Run the simulation and wait until it stops.
6. Using the *Grapher* cursors in *Y Axis* mode:
   - measure the peak-peak value of the magnetizing current $I_{Lm,pkpk}$, divide by 2 to get the peak value $I_{Lm,pk}$, in milli Ampère with one decimal digit of accuracy, and report the result in Table 3-1-1;
   - measure the difference $I_{SP} = I_{P,pk} - I_{Lm,pk}$ between the peak value $I_{P,pk}$ of the primary coil current and the peak value $I_{Lm,pk}$ of the magnetizing current, in milli Ampère with one decimal digit of accuracy, and report the result in Table 3-1-1;
   - measure the amplitude of load voltage V_{Ro}, in Volt with two decimal digits of accuracy, and report the result in Table 3-1-1.
7. Set the switch Str in position (b) and repeat steps 5-6.
8. Import in Table 3-1-1 the values of $I_{Lm,pk}$, I_{SP} and V_{Ro} calculated in the *Exercise* Section for options (a) and (b).

Table 3-1-1 Square-Wave High-Frequency Transformer Operation.

	$I_{Lm,pk}$ [mA] simulated	$I_{Lm,pk}$ [mA] calculated	I_{SP} [mA] simulated	I_{SP} [mA] calculated	V_{Ro} [mA] simulated	V_{Ro} [mA] calculated
option (a)	248.0	250.0	34.0	34.2	5.81	5.85
option (b)	247.9	249.8	136.4	136.6	11.68	11.61

[**Note:** the simulation time is set to 100µs and the circuit does not reach its steady-state operation within this time. Therefore, the DC component of the current is not exactly zero. If you extend the simulation time to 500µs, or more, you will get zero DC component in the magnetizing current. Decreasing the simulation time step also improves the simulation accuracy].

3-2-1 Is the simulated waveform of magnetizing current fitting the calculation?

    A.   yes
    B.   no
    Please provide your comments: _____

_____

3-2-2 In what condition does the transformer perform step-up voltage conversion?

    A.   option (a)
    B.   option (b)
    Please provide your comments: _____

_____

3-2-3 In what condition is the secondary coil current reflected to primary coil bigger?

    A.   option (a)
    B.   option (b)
    Please provide your comments: _____

_____

3-3   Simulation 2 – Transformer Operation with non-Zero DC Component in Primary Coil Voltage.
1. Set the switch S_{tr} in position (a).
2. Set the circuit parameters as follows:
    - *FG1*: *DC_mag* =0.01V, *AC_mag* = 0.0V;
    - *FG2*: *VA* = 1.0V, *Per* = 10µs, *TF* = 5µs, Offset = -0.5V;
3. Double click on probes *VP*, *IP*, *VS*, *IS,* and *ILm* and check the *Show plot* option box.
4. Set *Interactive* simulation and *Grapher* visualization options.
5. Set the simulation *End time* to 200µs.

6. Run the simulation and wait until it stops.
7. Set the *Time Axis* minimum to 1μs and maximum to 200 μs.

3-3-1 What is the trend of the magnetizing current?

A.   it is triangular with zero DC component
B.   it is triangular with increasing DC component
C.   it is triangular with decreasing DC component
D.   other: _____

Please provide your comments: _____

_____

3-3-2 What is the trend of secondary coil voltage?

A.   it is a square wave with constant small DC component
B.   it is a square wave with increasing DC component
C.   it is a square wave with decreasing DC component
D.   other: _____

Please provide your comments: _____

_____

Troubleshooting tips:
If the simulation does not converge and you get some error message, reload *Lab10 – High-Frequency Transformer Operation* from this file path
https://www.multisim.com/content/926CMvd7zwR336GVmurMDh/lab-10-high-frequency-transformer-operation/
and restart the simulation following the instructions.

4 Implement

The experiments you perform in this section allow you to observe the voltage and current waveforms of a real transformer in high-frequency square-wave primary voltage operation, under different secondary coils configuration. The **DC-AC Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments.
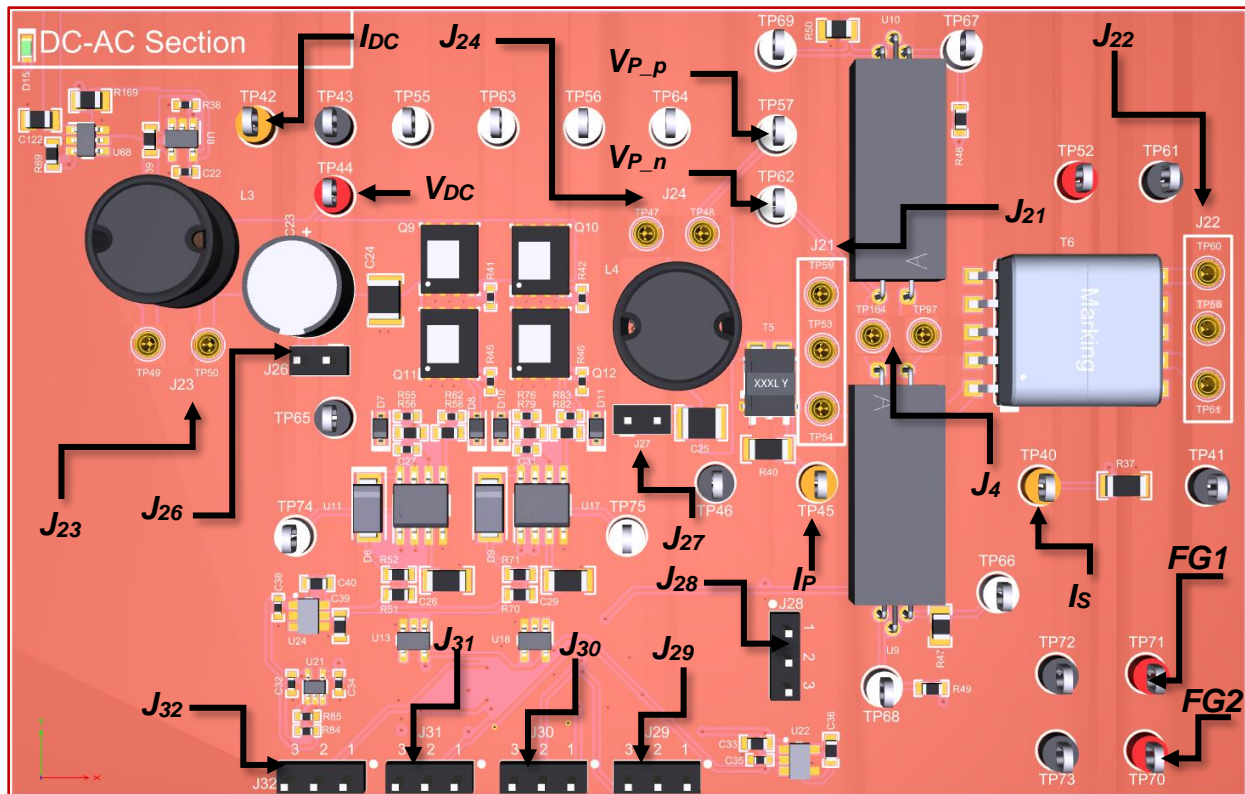

Figure 4-1. TI Power Electronics Board for NI ELVIS III – DC-AC Section Used for the Analysis of High-Frequency Transformer Operation.

The primary square-wave voltage is generated by a full-bridge DC-AC inverter, using four TI's CSD16322Q5C MOSFETs, two TI's TLV7011DPWR comparators and two TI's UCC27712DR MOSFET drivers. The full-bridge AC output is connected to the transformer primary coil by means of the jumper J21. The transformer is a Wurth 7491196112, with one primary and three secondary coils. Two secondary coils only are used in the experiments. The transformer has the following parameters:

- $N_{s1}/N_p = N_{s2}/N_p = 0.585 \pm 3\%$
- $R_p = 50m\Omega$, $R_{s1} = 30m\Omega$, $R_{s2} = 35m\Omega$ (max values @20°C)
- $L_m = 100\mu H \pm 25\%$, $L_p = 0.5\mu H$ max, $\lambda_{max} = 106.5\mu Vs$ (typical)

The jumper J22 allows to set the two secondary coils according to options (a) and (b) already analyzed in **Exercise** and **Simulation** Sections. The load is a 100Ω resistor R_o. The reference signal *FG1* and the triangular switching signal *FG2* are available at test points TP71 and TP70, respectively. The board uses two sensing transformers to sense the primary and secondary coils currents, that can be measured by means of two voltage probes at test points TP45 and TP40 respectively. As the voltage-to-current transconductance of the two sensing transformers is 10, multiplying the voltages measured at test points TP45 and TP40 by 10 provides the primary and secondary coils currents I_P and I_S respectively. The datasheets of components are available at these links:

- CSD16322Q5C MOSFET: http://www.ti.com/lit/ds/symlink/csd16322q5c.pdf
- TLV7011DPWR comparator: (http://www.ti.com/lit/ds/symlink/tlv7011.pdf
- UCC27712DR gate driver: http://www.ti.com/lit/ds/symlink/ucc27712.pdf
- 7491196112 transformer: https://katalog.we-online.de/pbs/datasheet/7491196112.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document:
   http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab9 – DC-AC PWM Inverter Operation*.
5. Connect and configure the instruments as indicated in Tables 4-1 and 4-2.
   [**Note:** the primary coil square-wave voltage can be observed on the *Oscilloscope* Math channel, which provides the difference between CH-1 (V_{P_p}) and CH-2 (V_{P_n}), while primary and secondary coils currents I_P and I_S can be observed on CH-3 and CH-4, respectively]
6. Configure the jumpers of the board as indicated in Table 4-3.

Table 4-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP57 (V_{P_p}), connect CH-2 to TP62 (V_{P_n}) connect CH-3 to TP45 (I_P), connect CH-4 to TP40 (I_S)
Function Generator	connect CH-1 to FGEN1 BNC connector (→TP71 = *FG1*) connect CH-2 to FGEN2 BNC connector (→TP70 = *FG2*)

Table 4-2 Instruments Configuration and setup

Power Supply	*Channel "+"*: Static, 10.00V, *Channel "-"*: Inactive			
Oscilloscope	*Trigger*: Analog Edge, CH-1, set to 50%	*Horizontal*: 2µs/div	*Acquisition*: average	*Measurements*: show
	Channel 1: ON • DC coupling • 10V/div • offset 35V	*Channel 2*: ON • DC coupling • 10V/div • offset 20V	*Channel 3*: ON • DC coupling • 20mV/div • offset 0V	*Channel 4*: ON • DC coupling • 20mV/div • offset 0V	*Math*: ON • CH1-CH2 • 10V/div • offset -20V
Function Generator	*Channel 1*: Sine, Frequency 1Hz, Amplitude 0.0Vpp, DC offset 0.0V *Channel 2*: Triangle, Frequency 100kHz, Amplitude 1Vpp, DC offset 0.0V			

Table 4-3 Jumpers Setup

J21	J22	J23	J24	J26	J27
short TP53-TP54	open	shorted	shorted	shorted	open
J4	**J28**	**J29**	**J30**	**J31**	**J32**
shorted	short 2-3	short 2-3	short 1-2	short 2-3	short 2-3

4-2 Experiment 1 – Transformer in no-load Operation.

1. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
2. Stop the *Oscilloscope*, *Power Supply* and *Function Generator*.
3. Using the *Oscilloscope* Cursors:
   a. measure on CH-3 the peak-peak value of the primary coil current $I_{Lm,pkpk}$ and multiply by 5 to to get the peak value $I_{Lm,pk}$, in milli Ampère with one decimal digit of accuracy: $I_{Lm,pk}$ [mA] = _____ (258.0mA); [**Note:** the multiplying factor 5 results from the multiplication by 10, which is the transcondutance of the current sensing transformer, and the division by 2 to get the positive peak of the triangular waveform].

b. measure on Math channel the amplitude of primary coil voltage V_P, in Volt with one decimal digit of accuracy: V_P [V] = _____

4. Using **Theory and Background** Equations, estimate the magnetizing inductance of the transformer, in micro Henry with one decimal digit of accuracy: L_m [μH] = _____

4-2-1 Is the value of magnetizing inductance estimated from measurements close to its nominal value?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-2-2 Does the waveform on CH-4 shown a square-wave component?

    A.   yes

    B.   no

    Please provide your comments: _____

    _____

4-3 Experiment 2 – Transformer under Loaded Step-Down Mode Operation.

1. Set jumper J22 to SHORT TP51-TP60, connecting secondary coil #2 to the 100Ω load resistor R_o.
2. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
3. Stop the *Oscilloscope*, *Power Supply* and *Function Generator*.
4. Using the *Oscilloscope* Cursors:
   a. measure on CH-3 the peak-peak value of the primary coil current $I_{P,pkpk}$ and multiply by 5 to get the peak value $I_{P,pk}$, in milli Ampère with one decimal digit of accuracy: $I_{P,pk}$ [mA] = _____
   b. measure on CH-4 the amplitude of the secondary coil square-wave current I_S, multiply by 10 to include the sensor transconductance, and provide the result in milli Ampère with one decimal digit of accuracy: I_S [mA] = _____
   c. measure on Math channel the amplitude of primary coil voltage V_P, in Volt with one decimal digit of accuracy: V_P [V] = _____

d. multiply the amplitude of the secondary coil current I_S by N_{s2}/N_p to get the current I_{SP} reflected to primary coil, in milli Ampère with one decimal digit of accuracy: I_{SP} [mA] = _____

e. convert the amplitude of the secondary coil current I_S in Ampère and multiply by the load resistance to obtain the amplitude of load voltage V_{Ro}, in Volt with one decimal digit of accuracy: V_{Ro} [V] = _____

7. Using **Theory and Background** Equations, estimate the peak of magnetizing inductance current, in milli Ampère with one decimal digit of accuracy:
$I_{Lm,pk}$ [mA] = _____

4-3-1 Is the peak value of magnetizing current estimated under loaded step-down conditions similar to the value obtained in no load conditions in *Experiment 1*?
A. yes
B. no
Please provide your comments: _____

_____

4-3-2 Is the amplitude of load voltage consistent with primary coil voltage based on secondary-to-primary turns number ratio N_{s2}/N_p?
A. yes
B. no
Please provide your comments: _____

_____

4-4 Experiment 3 – Transformer under Loaded Step-Up Mode Operation.

1. Set jumper J22 to SHORT TP51-TP58, connecting secondary coils #1 and #2 in series to the 100Ω load resistor R_o.
2. Run *Oscilloscope*, *Function Generator* and *Power Supply*.
3. Stop the *Oscilloscope*, *Power Supply* and *Function Generator*.
4. Using the *Oscilloscope* Cursors:
   a. measure on CH-3 the peak-peak value of the primary coil current $I_{P,pkpk}$ and multiply by 5 to get the peak value $I_{P,pk}$, in milli Ampère with one decimal digit of accuracy: $I_{P,pk}$ [mA] = _____

b. measure on CH-4 the amplitude of the secondary coil square-wave current I_S, multiply by 10 to include the sensor transconductance, and provide the result in milli Ampère with one decimal digit of accuracy: I_S [mA] = _____

c. measure on Math channel the amplitude of primary coil voltage V_P, in Volt with one decimal digit of accuracy: V_P [V] = _____

d. multiply the amplitude of the secondary coil current I_S by $(N_{s1}/N_p+N_{s2}/N_p)$ to get the current I_{SP} reflected to primary coil, in milli Ampère with one decimal digit of accuracy: I_{SP} [mA] = _____

e. convert the amplitude of the secondary coil current I_S in Ampère and multiply by the load resistance to obtain the amplitude of load voltage V_{Ro}, in Volt with one decimal digit of accuracy: V_{Ro} [V] = _____

7. Using **Theory and Background** Equations, estimate the peak of magnetizing inductance current, in milli Ampère with one decimal digit of accuracy: $I_{Lm,pk}$ [mA] = _____

4-4-1 Is the peak value of magnetizing current estimated under loaded conditions similar to the value obtained in no load conditions in *Experiment 1*?
A.   yes
B.   no
Please provide your comments: _____

_____

4-3-2 Is the amplitude of load voltage consistent with primary coil voltage based on secondary-to-primary turns number ratios N_{s1}/N_p and N_{s2}/N_p?
A.   yes
B.   no
Please provide your comments: _____

_____

Troubleshooting tips:
● If the transformer does not work, or its waveforms look much different with respect to simulations, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiments.

5 Analyze

5-1   Compare the values of the peak value of magnetizing current under no-load, step-down and step-up operating conditions and discuss them based on *Theory and Background* equations:

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the operation of a transformer under high-frequency square-wave conditions, and discuss the impact of magnetizing inductance and of step-up and step-down configurations on the resulting voltage and current waveforms.

6-2   Expansion Activities

Investigate the influence of switching frequency on the operation of the transformer, by means of Multisim Live simulations and of the TI Power Electronics Board for NI ELVIS III.

6-2-1. Simulation

Repeat the simulations following the instructions of Sections 3-1, 3-2 and 3-3 by setting the parameters of triangular voltage generator *FG2* as follows:

- *Per* = 5.0µs, *TF* = 2.50µs, for 200kHz operation

6-2-2. Experiment

Repeat the experiments following the instructions of Sections 41, 4-2, 4-3 and 4-4 by setting the frequency of *Function Generator* CH-2 to 200kHz.

6-4   Resources for learning more

- This book provides the fundamentals of transformers in power electronics: R.W.Erickson, D.Maksimovic, *Fundamentals of Power Electronics*, Kluwer Academic Publishers

Answer Key – Check Your Understanding Questions Only

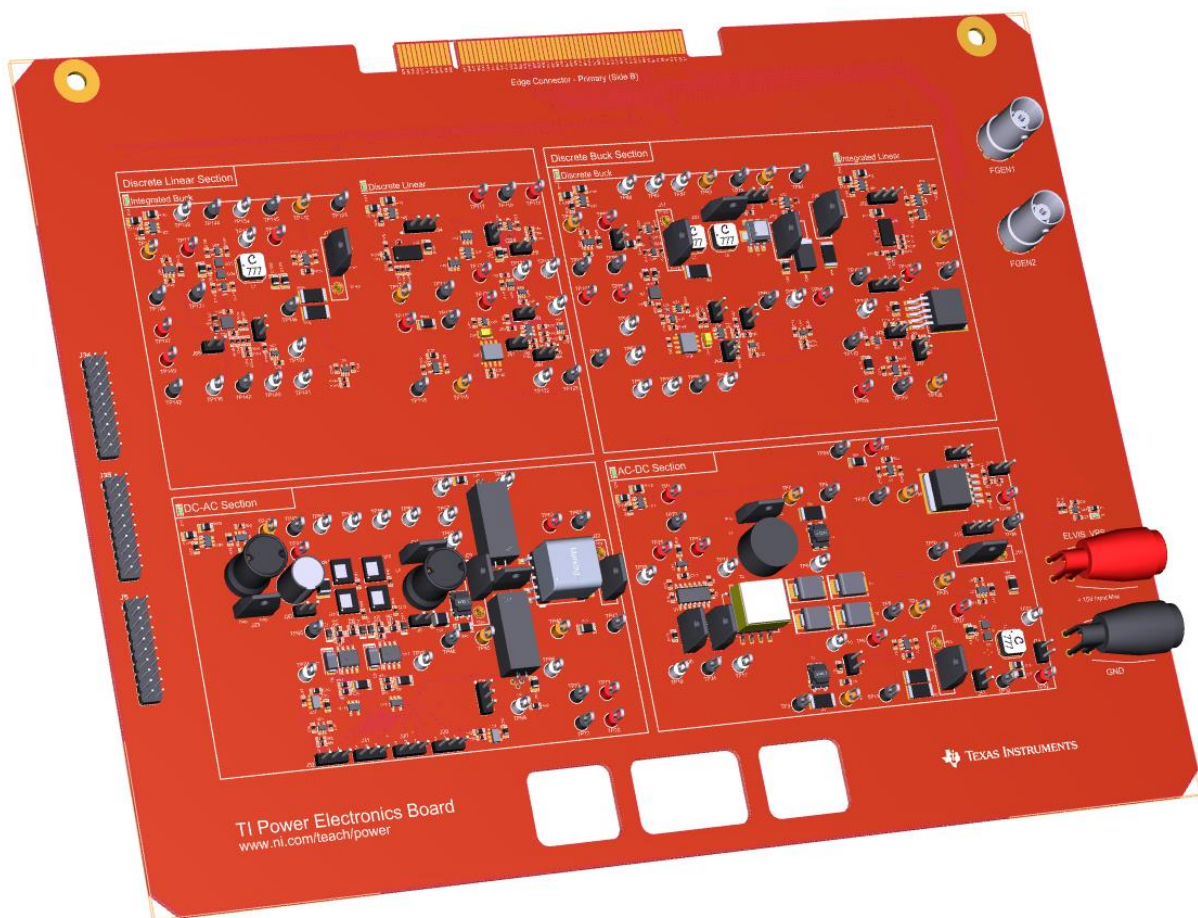### Check Your Understanding

1-1   B

1-2   C

1-3   A

1-4   A

1-5   B

1-6   C

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 11: AC-DC Rectifier Operation

Lab 11: AC-DC Rectifier Operation

The goal of this lab is to investigate the behavior of a diode-bridge AC-DC rectifier, which is used in all power supplies taking energy from AC sources, like grid utility. First, we review the principle of operation of a diode-bridge AC-DC rectifier. Next, we simulate the rectifier to analyze the effects of its parameters on voltage and current waveforms. Finally, we perform lab experiments to observe the voltages and currents of a real AC-DC rectifier under different operating conditions.
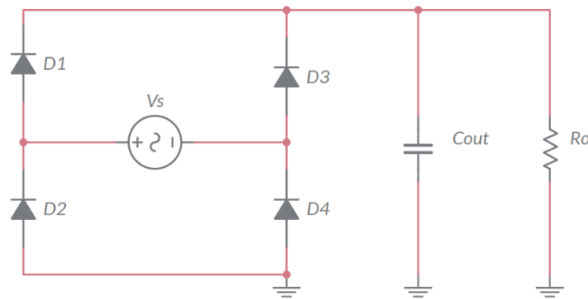

Figure 1-1. Diode-bridge AC-DC Rectifier

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given an AC-DC diode rectifier with specified parameters and an AC source, you will estimate the amplitude of its average DC output voltage and peak-peak AC ripple, with specified units and accuracy, under different output capacitor configurations.

2. Given an AC-DC diode rectifier with specified parameters and an AC source, you will simulate its operation under different output capacitor and AC source inductance, to analyze the effect of system parameters on voltage and current waveforms.

3. Given a real AC-DC diode rectifier with specified parameters and an AC source, you will observe the rectifier voltage and current waveforms and measure the amplitudes of their DC and AC components, with specified units and accuracy, to verify the consistency with simulation results and estimate the system parameters.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

✓ Access Instruments
https://measurementslive.ni.com/
✓ View User Manual
http://www.ni.com/en-us/support/model.ni-elvis-iii.html
✓ View Tutorials
https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

✓ View User Manual
http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

✓ Access
https://www.multisim.com/
✓ View Tutorial
https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

✓ Download (Windows OS Only)
http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of an AC-DC diode-bridge rectifier. First, we analyze the principle of operation and the resulting voltage and current waveforms. Next, we discuss the effect of AC source parameters and of DC output capacitance.

1-2 Ideal Diode-Bridge Rectifier

Figure 1-2(a) shows the typical configuration of an AC-DC diode-bridge rectifier, taking energy from an AC voltage source $V_s(t) = V_s\sin(2\pi f_s t)$ and supplying a DC load resistor R_o.

(a) AC-DC Diode-Bridge Rectifier
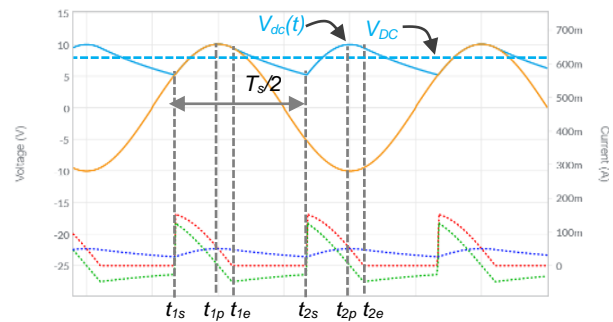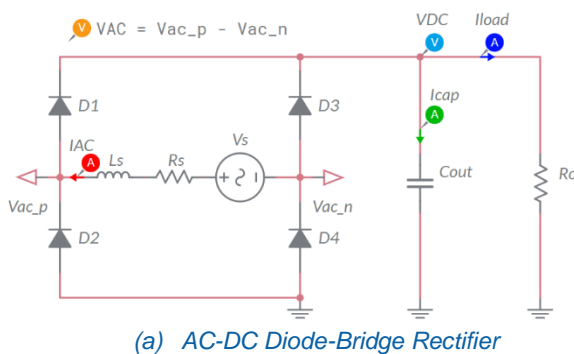
(b) AC-DC rectifier voltage and current waveforms: $R_s=400m\Omega$, $L_s=1nH$, $R_o=200\Omega$, $C_{out}=47nF$, $f_s=50kHz$, $V_s=10V$, $V_F=0V$.

Figure 1-2. AC-DC Rectifier.

In this case, the AC voltage $V_{AC}(t)$ applied between the input nodes V_{ac_p} and V_{ac_n} of the diode-bridge, shown as a yellow trace in Figure 1-2(b), is equal to the source voltage $V_s(t)$. When the voltage $V_s(t)$ is positive, diodes D_1 and D_4 may conduct, thus applying the positive voltage $V_s(t)$ to the output capacitor C_{out}, whereas when the sinusoidal voltage $V_s(t)$ is negative, diodes D_2 and D_3 may conduct, thus inverting the voltage $V_s(t)$ and applying the positive voltage $-V_s(t)$ to the output capacitor C_{out}. In this way, the voltage $V_s(t)$ is *rectified*, namely it is converted into a voltage $V_{dc}(t)$ having a major DC component V_{DC} (dashed cyan line in Figure 1-2(b)) and a minor AC ripple component $\Delta V_{AC}(t) = V_{dc}(t) - V_{DC}$, whose fundamental frequency is twice the frequency f_s of the AC source voltage $V_s(t)$. The diodes D_1 and D_4 conduct during the interval $[t_{1s}, t_{1e}]$, and stop conducting when the sinusoidal voltage $V_s(t)$ is smaller than the voltage $V_{dc}(t)$ of the output capacitor C_{out}, which is also the voltage of the DC load resistor R_o. Similarly, the diodes D_2 and D_3 conduct during the interval $[t_{2s}, t_{2e}]$ and stop conducting when the inverted sinusoidal voltage $-V_s(t)$ becomes smaller than the voltage $V_{dc}(t)$. Over the period $T_s/2$, the

output capacitor C_{out} is charged during the interval $[t_{1s}, t_{1p}]$, t_{1p} being the instant $V_s(t)$ where the voltage reaches the peak, and discharged in the time interval $[t_{1p}, t_{2s}]$. The same happens in the next period $T_s/2$, and so on. The dashed green trace in Figure 1-2(b) shows the capacitor current $I_{cap}(t)$, which is positive during $[t_{1s}, t_{1p}]$ and negative during $[t_{1p}, t_{2s}]$. The dashed red trace shows the current of the AC source voltage, which is positive during $[t_{1s}, t_{1e}]$ and negative during $[t_{1e}, t_{2s}]$. The dashed blue trace shows the current of the DC load resistor R_o, which is always positive, like the voltage $V_{dc}(t)$. The output capacitance C_{out} determines the DC component V_{DC}. If C_{out} is very small, we have $t_{1s} \cong 0$ and $t_{1e} \cong T_s/2$, and V_{DC} is given by Equation 1-1:

Equation 1-1

$$V_{DC} = V_s \frac{2}{\pi}$$

The non-linear circuit equations of the rectifier do not allow easily determining an exact analytical expression of the DC component V_{DC} and of the amplitude ΔV_{ACpp} of the AC ripple component as a function of system parameters. Nevertheless, simplified equations to estimate the expected values of V_{DC} and ΔV_{ACpp} can be derived as follows. The voltage of the output capacitor is equal to $V_{AC}(t)$ in the interval $[t_{1s}, t_{1e}]$. The sinusoidal AC voltage $V_{AC}(t)$ can be well approximated within the half-wave time interval $[0, T_s/2]$ by means of the parabolic function given in Equation 1-2:

Equation 1-2

$$V_{dc}^{(1)}(t) = V_{AC}(t) \cong 8V_s f_s t(1 - 2f_s t)$$

In the interval $[t_{1e}, t_{2s}]$, the voltage of the output capacitor is an exponential function, starting from the value $V_{AC}(t_{1e}) = 8V_s f_s t_{1e}(1 - 2f_s t_{1e})$ and decaying with a time constant $\tau = C_{out}R_o$. This exponential function can be well approximated by means of the linear function given in Equation 1-3:

Equation 1-3

$$V_{dc}^{(2)}(t) \cong V_{dc}^{(1)}(t_{1e})(1 - (t - t_{1e})/\tau)$$

The two functions given in Equations 1-2 and 1-3 are tangent in the instant t_{1e}, which is given by Equation 1-4

Equation 1-4

$$t_{1e} = \frac{1}{4}\left[T_s - 4\tau + \sqrt{T_s^2 + 16\tau^2} \right]$$

The instant t_{2s} can be determined as the intersection of function given by Equation 1-4 with the function given by Equation 1-2 shifted horizontally right side of $T_s/2$. The resulting expression of the instant t_{2s} is given by Equation 1-5:

Equation 1-5

$$t_{2s} = \frac{T_s}{2} + \frac{-B + \sqrt{B^2 - 4A \cdot C}}{2A}$$

$$A = -16V_s f_s^2 \qquad B = 8V_s f_s + \frac{8V_s f_s^2 t_{1e}(T_s - 2t_{1e})}{\tau} \qquad C = -\frac{4V_s f_s^2 t_{1e}(T_s - 2t_{1e})(2t_{1e} - T_s + 2\tau)}{\tau}$$

The approximated values of DC component V_{DC} and amplitude ΔV_{ACpp} of the AC ripple component are given by the simplified Equations 1-6:

Equations 1-6

$$V_{DC} \cong \frac{V_s + V_{dc}^{(2)}(t_{2s})}{2} \qquad \Delta V_{ACpp} \cong V_s - V_{dc}^{(2)}(t_{2s})$$

The real value of V_{DC} will be higher while the real value of ΔV_{ACpp} will be lower than the the result predicted by Equations 1-6.

1-3 Impact of Diodes Voltage Drop

Figure 1-3 shows the effect of the diodes forward voltage drop V_F on voltage and current waveforms of the AC-DC rectifier. It can be observed that the diodes conduct during the interval $[t_{1s}, t_{1e}]$ where $|V_s(t)| > V_{dc}(t) + 2V_F$. The diodes voltage drop causes a reduction of $2V_F$ Volts in the DC component of the output voltage.
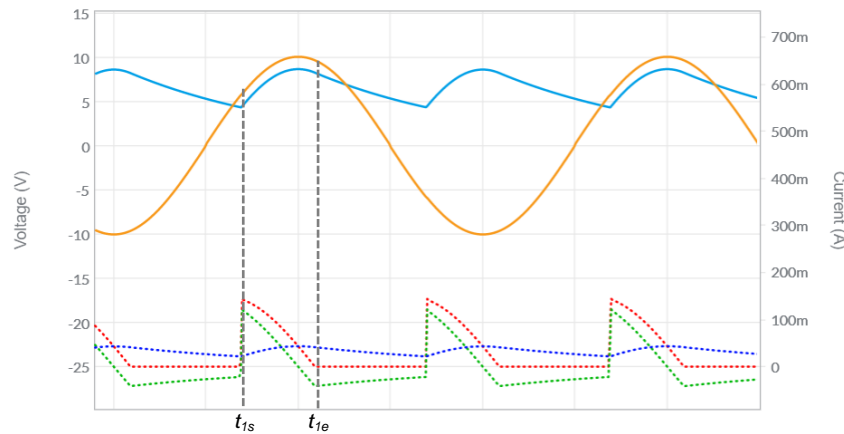

Figure 1-3. Effect of Diodes Voltage Drop on AC-DC Rectifier Waveforms: R_s=400mΩ, L_s=1nH, R_o=200Ω, C_{out}=47nF, f_s=50kHz, V_s=10V, V_F=0.7V.

1-4 Impact of Output Capacitor

Figure 1-4 shows the results obtained by increasing the output capacitance C_{out}. The plots highlight that, as C_{out} increases, the DC component V_{DC} increases, the amplitude ΔV_{ACpp} of the AC ripple component $\Delta V_{AC}(t)$ decreases, the interval $[t_{1s}, t_{1e}]$ shortens, and the peak of the AC voltage source increases. If C_{out} gets very big, the DC component V_{DC} is almost equal to the V_s -2V_F and the amplitude ΔV_{ACpp} of the AC ripple component is almost equal to zero. In real applications, the capacitance C_{out} is limited to a value allowing to have an amplitude ΔV_{ACpp} of the AC ripple component about 5% to 15% of the DC component V_{DC}. A DC-DC post-regulator is normally connected to the output of diode-bridge AC-DC rectifiers, to filter the AC ripple $\Delta V_{AC}(t)$ and regulate the DC output voltage suitable for the DC load (see **Lab12**).
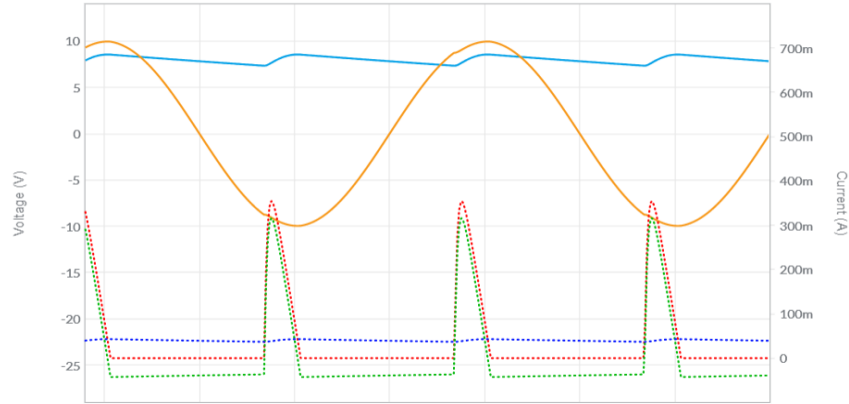
INTERNAL - NI CONFIDENTIAL

Figure 1-4. Effect of Output Capacitor on AC-DC Rectifier Waveforms: R_s=400mΩ, L_s=1nH, R_o=200Ω, C_{out}=47nF+220nF, f_s=50kHz, V_s=10V, V_F=0.7V.

1-5 Impact of Voltage Source Inductance

Figure 1-5 shows the effect of the source inductance L_s on the voltage and current waveforms of the AC-DC rectifier. Comparing Figure 1-5 with Figure 1-3 allows to observe that, during the interval $[t_{1s}, t_{1e}]$, wherein diodes are conducting, the inductance L_s causes a distortion of the AC voltage $V_{AC}(t)$, while smoothing the AC current $I_{AC}(t)$ and the capacitor current $I_{cap}(t)$.

Figure 1-5. Effect of Source Inductance on AC-DC Rectifier Waveforms: R_s=400mΩ, L_s=10µH, R_o=200Ω, C_{out}=47nF, f_s=50kHz, V_s=10V, V_F=0.7V.

The AC voltage $V_{AC}(t)$ during the interval $[t_{1s}, t_{1e}]$ is given by Equation 1-2:

Equation 1-2
$$V_{AC}(t) = V_s(t) - 2V_F - R_s\left(C_{out}\frac{dV_{dc(t)}}{dt} + \frac{V_{dc}(t)}{R_o}\right) - L_s\frac{d}{dt}\left(C_{out}\frac{dV_{dc(t)}}{dt} + \frac{V_{dc}(t)}{R_o}\right)$$

Equation 1-2 highlights that increasing the capacitance C_{out} increases the distortion effect of the source inductance L_s, as shown in Figure 1-6.
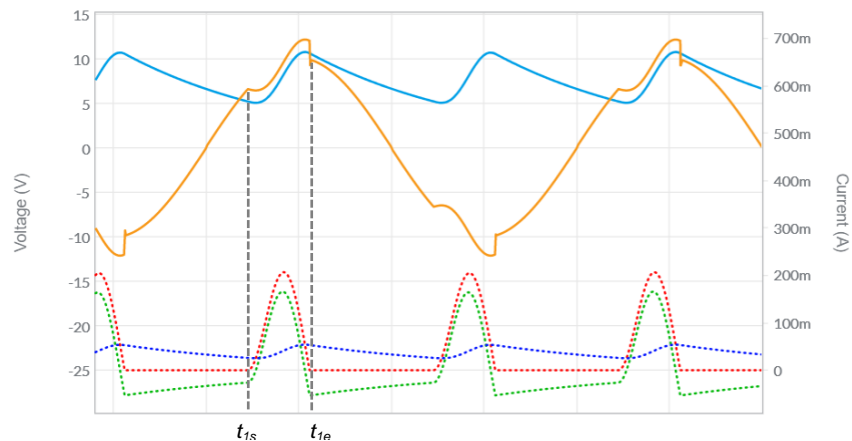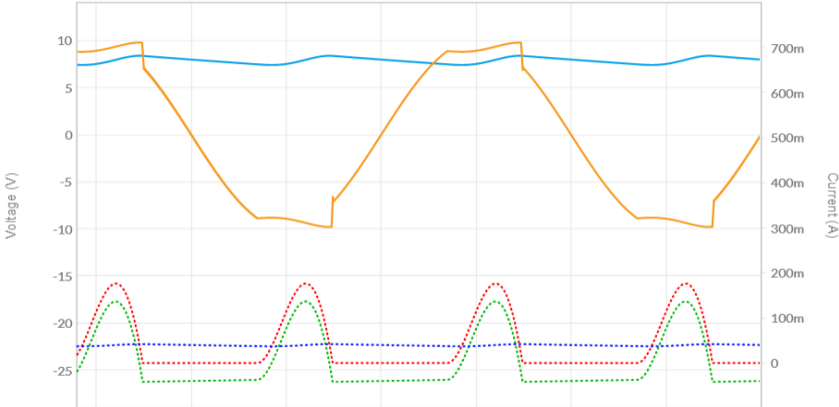

Figure 1-6. Combined Effect of Source Inductance and Output Capacitance on AC-DC Rectifier Waveforms: $R_s=400m\Omega$, $L_s=10\mu H$, $R_o=200\Omega$, $C_{out}=47nF+220nF$, $f_s=50kHz$, $V_s=10V$, $V_F=0.7V$.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What is the function of an AC-DC rectifier?
   A. to convert an input voltage into a proportional output voltage
   B. to convert a sinusoidal AC voltage into a DC voltage
   C. to convert a voltage source into a current source

1-2 What are the factors majorly affecting the DC component and the amplitude of the AC ripple component of the rectifier output voltage?
   A. the output capacitance and load resistance
   B. the phase of the AC source voltage
   C. the frequency of the AC voltage source

1-3 How does the forward voltage drop of diodes impact the rectifier output voltage?
   A. it is not influential
   B. it causes a decrease of the DC component
   C. it causes an increase of the DC component

1-4 What is the effect of AC source inductance on the rectifier operation?
   A. a distortion in the output voltage
   B. an increase of the DC component of the output voltage
   C. a decrease of the amplitude of the AC ripple component of the output voltage

1-5 How does an increase of output capacitance affect the peak current of the AC source?
   A. the peak current decreases
   B. it is not influential
   C. the peak current increases

1-6 How does an increase of the output capacitance affect the DC component and the amplitude of AC ripple of the output voltage?
   A. the DC component and the amplitude of AC ripple decrease
   B. the DC component increases and the amplitude of AC ripple decreases
   C. the DC component decreases and the amplitude of AC ripple increases

2 Exercise

The AC-DC Rectifier Section of the TI Power Electronics Board for NI ELVIS III is characterized by the following nominal parameters:

- $V_F = 0.3V @ 300mA$
- $R_o = 200\Omega$
- $L_s = 3\mu H$
- $R_s = 6\Omega$

Two connection options are available for output capacitor #1 and #2:

- option (a): $C_{out} = 47nF$
- option (b): $C_{out} = 47nF + 220nF$

2-1 Assuming the AC source provides a 50kHz-5Vp sinusoidal voltage, use the equations provided in the **Theory and Background** section to evaluate:

- the DC component of the rectifier output voltage, in Volt with two decimal digits of accuracy:

option (a): V_{DC} [V] = _____   **option (b)**: V_{DC} [mA] = _____

- the amplitude of the AC ripple voltage of the rectifier, in Volt with two decimal digits of accuracy:

option (a): ΔV_{ACpp} [V] = _____   **option (b)**: ΔV_{ACpp} [V] = _____

3 Simulate

The goal of the simulations you will perform in this section is to analyze the operation of an AC-DC rectifier. You will observe the AC voltage and current waveforms under different output capacitor setup, to verify the impact of the capacitance on DC and ripple components on the rectifier output voltage, and the consistency of the theoretical model.

3-1 Instructions

2. Open *Lab11 – AC-DC Rectifier Operation* from this file path:
   https://www.multisim.com/content/BCzmqYVZWKkxG8u23Niho2/lab-11-ac-dc-rectifier-operation/open/
   The circuit schematic for the analysis of the AC-DC rectifier operation is shown in Figure 3-1. The AC voltage is generated by a 50kHz/5V sinusoidal voltage source, with output impedance comprised of 6Ω resistance R_s and 3µH inductance L_s. The switch *SL* allows to add 10µH in series to inductance L_s. The switch *J2* allows to add 220nF in parallel to capacitance C_{out1}, thus enabling options (a) and (b) of the **Exercise** Section. A voltage-controlled source is used to allow AC differential voltage measurement with a single voltage probe.
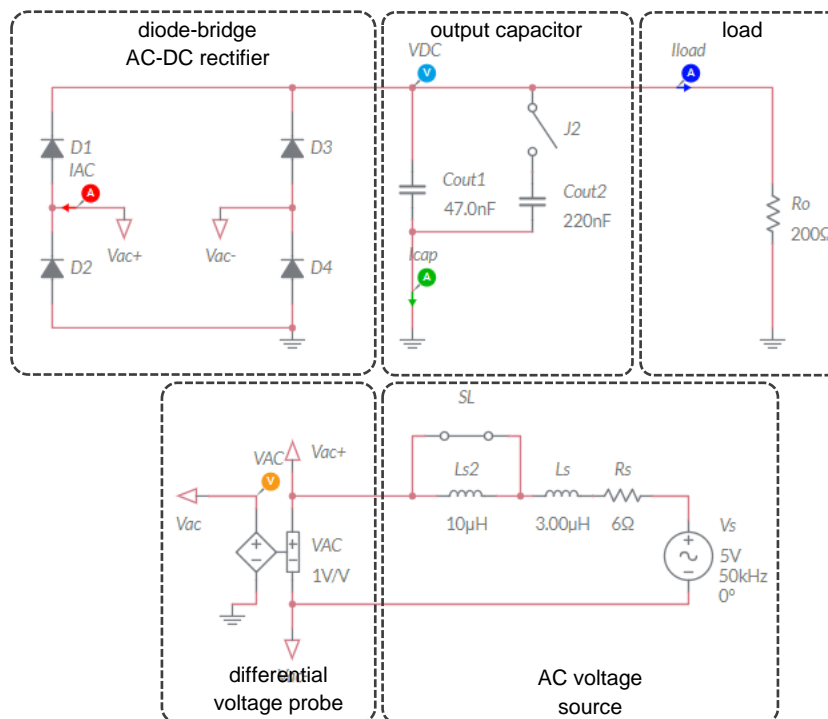

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of the Diode-Bridge AC-DC Rectifier Operation.

3-2 Simulation 1 – AC-DC Rectifier Operation with low source inductance.

1. Set the switch *J2* open and the switch *SL* closed.
2. Set V_s AC voltage source parameters as follows:
   - VA = 5.0V, *Freq*= 50k, VO = 0, *Phase* = 0, TD = 0, DF = 0;
3. Set *Interactive* simulation and *Split* visualization options.
4. Double click on probes *VAC, IAC, VDC, Icap,* and *Iload*, check the *Show plot* option box, and check the *Periodic* option box for *Interactive simulation*.
5. Run the simulation and wait until it stops.
6. In the voltage probe *VDC* measurement box, read the average value V_{AV} and peak-peak value V_{PP}, in Volt with two decimal digits, which provide the DC component V_{DC} and the peak-peak amplitude of the AC ripple component ΔV_{ACpp} of the rectifier output voltage respectively, and report the results in Table 3-1-1 (you may also use Y-axis cursors on trace VDC in the *Grapher* to measure the average value V_{AV} and peak-peak value V_{PP}).
7. In the current probe *IAC* measurement box, read the peak-peak value I_{PP}, in milli Ampère with one decimal digit, which provides the peak I_{ACpeak} of the AC source current, and report the results in Table 3-1-1 (you may also use Y-axis cursors on trace IAC in the *Grapher* to measure the peak value I_{ACpeak}).
8. In the current probe *Icap* measurement box, read the average value I_{AV}, in micro Ampère with one decimal digit, which provides the average capacitor current I_{capDC}, and report the results in Table 3-1-1.
9. In the current probe *Iload* measurement box, read the average value I_{AV}, in milli Ampère with one decimal digit, which provides the average load current I_{outDC}, and report the results in Table 3-1-1.
10. In the current probe *IAC* measurement box, read the average value I_{AV}, in milli Ampère with one decimal digit, which provides the average source current I_{ACDC}, and report the results in Table 3-1-1.
11. Set the switch *J2* closed, and repeat steps 5-10.
12. Import in Table 3-1-1 the values of V_{DC}, ΔV_{ACpp} calculated in the *Exercise* Section for options (a) and (b).

Table 3-1-1 AC-DC Rectifier Operation with 3µH AC source inductance.

	V_{DC} [V] sim.	V_{DC} [V] calc.	ΔV_{ACpp} [V] sim.	ΔV_{ACpp} [V] calc.	I_{Acpeak} [mA] sim.	I_{capDC} [µA] sim.	I_{outDC} [mA] sim.	I_{ACDC} [mA] sim.
option (a) C_{out} = 47nF								
option (b) C_{out} = 47nF+220nF								

3-2-1 Are the results of simulations and calculations consistent?

A.   yes
B.   no
Please provide your comments: _____

_____

3-2-2 Under what condition is the peak of AC source current maximum?

A.   option (a)
B.   option (b)
Please provide your comments: _____

_____

3-2-3 Is the DC load current equal to the DC current of the AC source?

A.   yes
B.   no
Please provide your comments: _____

_____

3-2   Simulation 2 – AC-DC Rectifier Operation with high source inductance.

1. Set the switch $J2$ open and the switch SL open.
2. Set V_s AC voltage source parameters as follows:
   - $VA = 5.0$V, $Freq= 50$k, $VO = 0$, $Phase = 0$, $TD = 0$, $DF = 0$;
3. Set *Interactive* simulation and *Split* visualization options.
4. Double click on probes *VAC, IAC, VDC, Icap,* and *Iload*, check the *Show plot* option box, and check the *Periodic* option box for *Interactive simulation*.
5. Run the simulation and wait until it stops.
6. In the voltage probe *VDC* measurement box, read the average value V_{AV} and peak-peak value V_{PP}, in Volt with two decimal digits, which provide the DC component V_{DC} and the peak-peak amplitude of the AC ripple component ΔV_{ACpp} of the rectifier output voltage respectively, and report the results in Table 3-2-1 (you may also use Y-axis cursors on trace VDC in the *Grapher* to measure the average value V_{AV} and peak-peak value V_{PP}).

7. In the current probe *IAC* measurement box, read the peak-peak value I_{PP}, in milli Ampère with one decimal digit, which provides the peak I_{ACpeak} of the AC source current, and report the results in Table 3-2-1 (you may also use Y-axis cursors on trace IAC in the *Grapher* to measure the peak value I_{ACpeak}).
8. In the current probe *Icap* measurement box, read the average value I_{AV}, in micro Ampère with one decimal digit, which provides the average capacitor current I_{capDC}, and report the results in Table 3-2-1.
9. In the current probe *Iload* measurement box, read the average value I_{AV}, in milli Ampère with one decimal digit, which provides the average load current I_{outDC}, and report the results in Table 3-2-1.
10. In the current probe *IAC* measurement box, read the average value I_{AV}, in milli Ampère with one decimal digit, which provides the average source current I_{ACDC}, and report the results in Table 3-2-1.
11. Set the switch *J2* closed, and repeat steps 5-10.
12. Import in Table 3-2-1 the values of V_{DC}, ΔV_{Acpp}, I_{Acpeak}, I_{capDC}, I_{outDC}, I_{ACDC} obtained in the *Simulation 1*.

Table 3-2-1 AC-DC Rectifier Operation with 13µH AC source inductance..

	V_{DC} [V]		ΔV_{Acpp} [V]		I_{Acpeak} [mA]		I_{capDC} [µA]		I_{outDC} [mA]		I_{ACDC} [mA]	
	sim 1	sim 2	sim1	sim2	sim1	sim2	sim1	sim2	sim1	sim2	sim1	sim2
option (a) C_{out} = 47nF												
option (b) C_{out} = 47nF+220nF												

3-2-1 What is the effect of the increase of source inductance on distortion of AC and output voltage waveform?

    A.   the distortion increases
    B.   the distortion decreases
    C.   no effect
    Please provide your comments: _____

_____

3-2-2 What is the effect of the source inductance increase on output voltage DC component?

      A.   the DC voltage increases
      B.   the DC voltage decreases
      C.   other: _____

_____

Please provide your comments: _____

_____

3-2-3 What is the effect of the increase of source inductance on the amplitude of the AC ripple component of output voltage?

      A.   the amplitude of AC ripple voltage increases
      B.   the amplitude of AC ripple voltage decreases
      C.   other: _____

_____

Please provide your comments: _____

_____

Troubleshooting tips:

If the simulation does not converge and you get some error message, reload *Lab11 – AC-DC Rectifier Operation* from this file path
https://www.multisim.com/content/BCzmqYVZWKkxG8u23Niho2/lab-11-ac-dc-rectifier-operation/open/
and restart the simulation following the instructions.

4 Implement

The experiments you perform in this section allow you to observe the voltage and current waveforms of a real AC_DC diode-bridge rectifier operation, under different output capacitance configuration. The **AC-DC Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments.
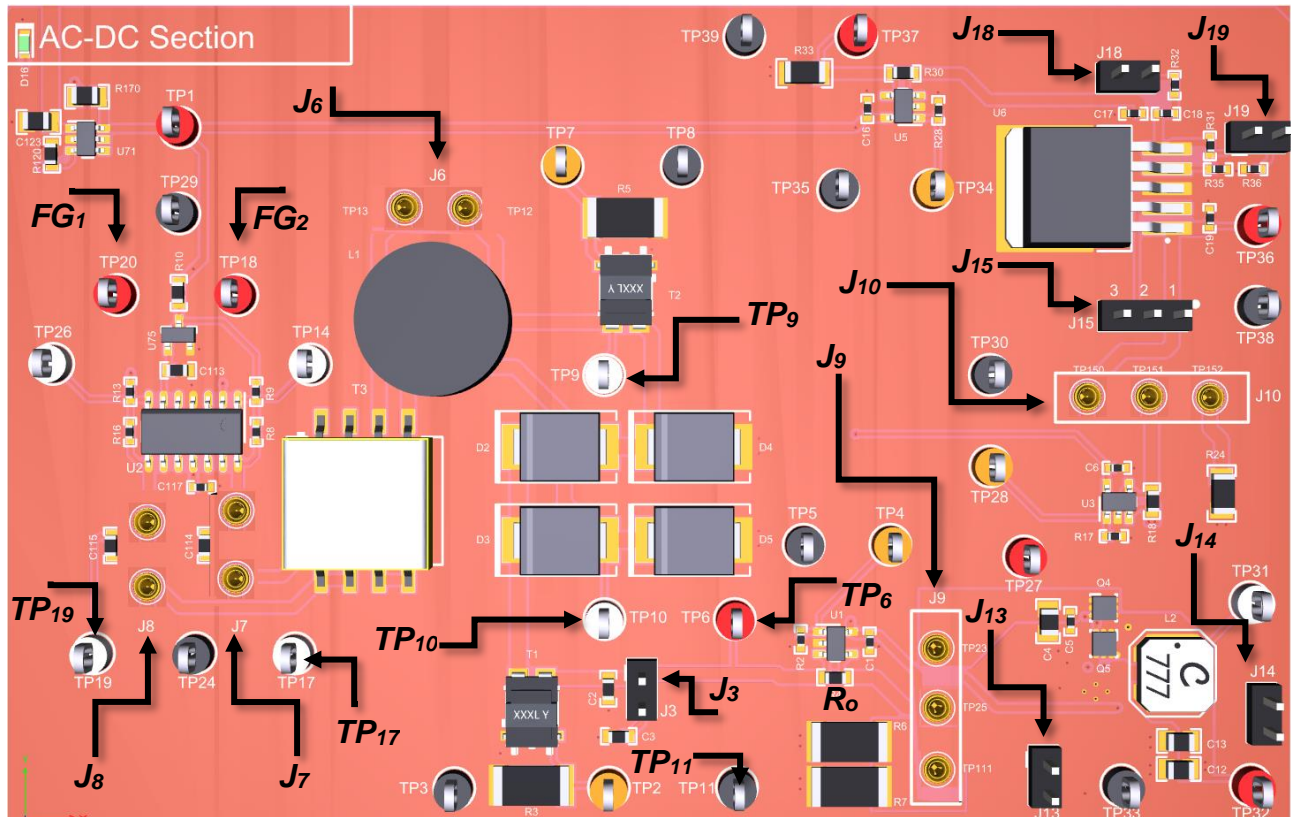

Figure 4-1. TI Power Electronics Board for NI ELVIS III – AC-DC Section Used for the Analysis of Diode-Bridge Rectifier Operation.

The AC source voltage is generated by a circuit comprised of a non-inverting amplifier and an inverting amplifier, using TI's OPA2674I OP-AMP. A TI's LM4040C25I voltage reference provides a common 2.5V bias voltage to the amplifiers. Two synchronized sinusoidal signals (FG_1,FG_2) are injected in the amplifiers to generate two output sinusoids 180° shifted each other. The outputs of the two amplifiers (TP_{17},TP_{19}) are connected in differential mode to the secondary coil of a Wurth 750311308 1:1 transformer, through jumpers J7 and J8. The primary coil of the transformer (TP_9,TP_{10}) is connected to the input of the diode full-bridge, using four B550C-13-FAC Diodes Incorporated 50V/5A Schottky diodes. The output of the diode bridge (TP_6,TP_{11}) can be connected to a 200Ω fixed load resistor R_o or to the input of a 1.2MHz TI's TPS40305 integrated buck converter, whose output can be connected to a 100Ω fixed load resistor

R_{o1}, or to the input of a TI's TPS7A6201-Q1 integrated linear regulator with 100Ω load resistor R_{o2}. The OPAMPs have about 6Ω output resistance. The transformer is characterized by the following parameters:

- Turns ratio: 1:1 ±1%
- Primary coil resistance: R_p = 325mΩ ±10%
- Secondary coil resistance: R_s = 480mΩ ±10%
- Magnetizing inductance: L_m = 100μH±10%
- Primary side leakage inductance: L_p = 3.0μH max.

The jumper J6 allows to connect, or bypass, a 10μH inductor in series to the transformer primary coil. Two Coilcraft CST7030-150LC 150:1 current sensing transformers allow sensing the diode bridge input and output currents at test points TP7 and TP2, respectively, by means of two voltage probes. As the voltage-to-current transconductance of the two sensing transformers is 10, multiplying the voltages measured at test points TP7 and TP2 by 10 provides the diode bridge input and output currents respectively. A TI's INA139NA current shunt monitor allows measuring the DC component of diode bridge output current at test point TP4 by means of a voltage probe. The datasheets of components are available at these links:

- OPA2674I-14DR OPAMP: http://www.ti.com/lit/ds/symlink/opa2674.pdf
- LM4040C25IDBZR voltage reference: http://www.ti.com/lit/ds/symlink/lm4040.pdf
- 750311308 transformer: https://katalog.we-online.com/pbs/datasheet/750311308.pdf
- B550C-13-FAC diode: https://www.diodes.com/assets/Datasheets/ds13012.pdf
- TPS40305 buck regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf
- TPS7A6201-Q1 linear regulator: http://www.ti.com/lit/ds/symlink/tps7a6201-q1.pdf
- CST7030-150LC sensing transformer: https://www.coilcraft.com/pdfs/cst7030.pdf
- INA139NA/3K current monitor: http://www.ti.com/lit/ds/symlink/ina139.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 Instructions

1. Open *Power Supply*, *Function Generator*, *Pattern Generator*, *Digital Multimeter* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab11 – AC-DC Rectifier Operation*.
5. Connect and configure the instruments as indicated in Tables 4-1 and 4-2.
   [**Note:** the AC input voltage of diode bridge can be observed on the *Oscilloscope* Math channel]
6. Configure the jumpers of the board as indicated in Table 4-3.

Table 4-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP9 (V_{AC+}), connect CH-2 to TP10 (V_{AC-}) connect CH-3 to TP7 (I_{AC}), connect CH-4 to TP6 (V_{DC})
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP18 = *FG1*) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP20 = *FG2*)
Pattern Generator	connect TRIG to DIO 0 (red) and GND (black) using a BNC-to-Alligator Cable
Digital Multimeter	connect to TP4 (average I_{load})

Table 4-2 Instruments Configuration and setup

Power Supply	*Channel "+"*: Static, 10.00V, *Channel "-"*: Inactive			
Oscilloscope	*Trigger*: Analog Edge, CH-1, set to 50%	*Horizontal*: 5µs/div	*Acquisition*: average	*Measurements*: show
	CH-1: OFF • DC coupling • 1V/div • offset 0V	*CH-2*: OFF • DC coupling • 1V/div • offset 0V	*CH-3*: ON • DC coupling • 20mV/div • offset 0V	*CH-4*: ON • DC coupling • 1V/div • offset 0V	*Math*: ON • CH1-CH2 • 1V/div • offset 0V
Function Generator	follow instructions provided below			
Pattern Generator	follow instructions provided below			
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: Automatic			

Table 4-3 Jumpers Setup

J6	J7	J8	J9		J3
shorted	shorted	shorted	short TP25-TP111		open
J18	J15	J19	J10	J13	J14
shorted	short 2-3	open	open	open	shorted

7. On *Channel 1* of the *Function Generator*, select *Custom*, use the file selector to select the TDMS waveform *Lab11_FG1.tdms*, set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 100MS/s,set *Generation mode* to *Loop*.

8. On *Channel 2* of the *Function Generator* select *Custom*, use the file selector to select the TDMS waveform *Lab11_FG2.tdms*, set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 100MS/s, set *Generation mode* to *Loop*.

9. On *Logic Analyzer and Pattern Generator*, click on *"+"* in the *Pattern Generator* section, click on *Signal* to add a new signal to the *Pattern Generator*, check the box next to *Logic 0* to add the line and click on the whitespace in the instrument, set *Status* to *On*, set *Mode* to *Clock*, set *Frequency* to 1Hz, set *Duty cycle* to 50%.

10. Run *Oscilloscope*, *Digital Multimeter, Power Supply, Pattern Generator* and *Function Generator*.

11. Measure the DC component of the output voltage V_{DC} on *Oscilloscope* CH-4, in Volt with two decimal digits of accuracy, and report the result in Table 4-4. [**Note:** the measurement of the average value of Channel 4 can performed by means of cursors. The measurement of the RMS value provides an approximated value of the average value]

12. Measure the amplitude of peak-peak output voltage ripple ΔV_{Acpp} on *Oscilloscope* CH-4, in Volt with two decimal digits of accuracy, and report the result in Table 4-4.

13. Measure the average DC load current I_{load} on *Digital Multimeter*, in milli Ampère, with one decimal digit of accuracy: I_{load} [V] = _____ (21.1mA); [**Note:** there can be up to about 15mA DC bias in the measurement. Check the value of the load current with the ratio between the DC output voltage V_{DC} and the load resistance R_o=200Ω]

14. Measure the peak amplitude of diode-bridge AC current I_{AC} on *Oscilloscope* CH-3, in milli Ampère with one decimal digits of accuracy, and report the result in Table 4-4.

15. Stop *Oscilloscope*, *Digital Multimeter, Power Supply*, *Function Generator* and *Pattern Generator*, set jumper J3 to be shorted and repeat steps 10 to 14.

16. Import in Table 4-4 the results of *Simulation 1* relevant to V_{DC}, ΔV_{Acpp} and I_{Acpeak}.

Table 4-4 AC-DC Rectifier Operation with different output capacitance.

	V_{DC} [V]		ΔV_{Acpp} [V]		I_{ACpeak} [mA]	
	sim 1	exp	sim 1	exp	sim 1	exp
C_{out} = 47nF						
C_{out} = 47nF+220nF						

4-2-1 Are the simulation values of output voltage DC component and peak-peak AC ripple consistent with experimental measurements?

A.   yes

B.   no

Please provide your comments: _____

_____

_____

4-2-2 Are the simulation values of peak AC diode bridge current consistent with experimental measurements?

A.   yes

B.   no

Please provide your comments: _____

_____

_____

Troubleshooting tips:

- If the AC-DC rectifier does not work, or its waveforms look much different with respect to simulations, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-1, 4-2 and 4-3, and restart the experiments.

5 Analyze

5-1   Comparing the simulated and experimental values of the DC output voltage average and peak-peak ripple values, identify the parameters of the simulation model to change in order to achieve a better agreement, based on concepts discussed in the *Theory and Background* section:

_____

_____

_____

6 Conclusion

6-1 Summary

Write a summary of what you observed and learned about the operation of an AC-DC diode bridge rectifier, and discuss the impact of the output capacitor on the resulting voltage and current waveforms.

6-2 Expansion Activities

6-2-1. Measure diodes voltage drop

a. Repeat the experiment following the instructions of Section 4-1.
b. Set the *Oscilloscope* cursors in *Track* mode, associate Cursor 1 to Math CH and Cursor 2 to CH-4
c. Align the cursors horizontally in a time instant where Math CH trace is higher than CH-4 trace and read the difference between the two traces measured by the *Oscilloscope*

Divide the measured voltage by two to obtain the forward voltage drop of each diode.

6-2-2. No load operating condition

a. Repeat the experiment following the instructions of Section 4-1 with jumper J9 open, which allows to disconnect the load resistor from the output of the rectifier.
b. Analyze the waveforms of input and output voltages of diode bridge rectifier, to verify that the input voltage is an ideal sine wave without distortion and the output voltage is a constant without AC ripple.

6-4 Resources for learning more

- This book provides the fundamentals of AC-DC diode bridge rectifiers:
  N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley & Sons, Inc.

Answer Key – Check Your Understanding Questions Only
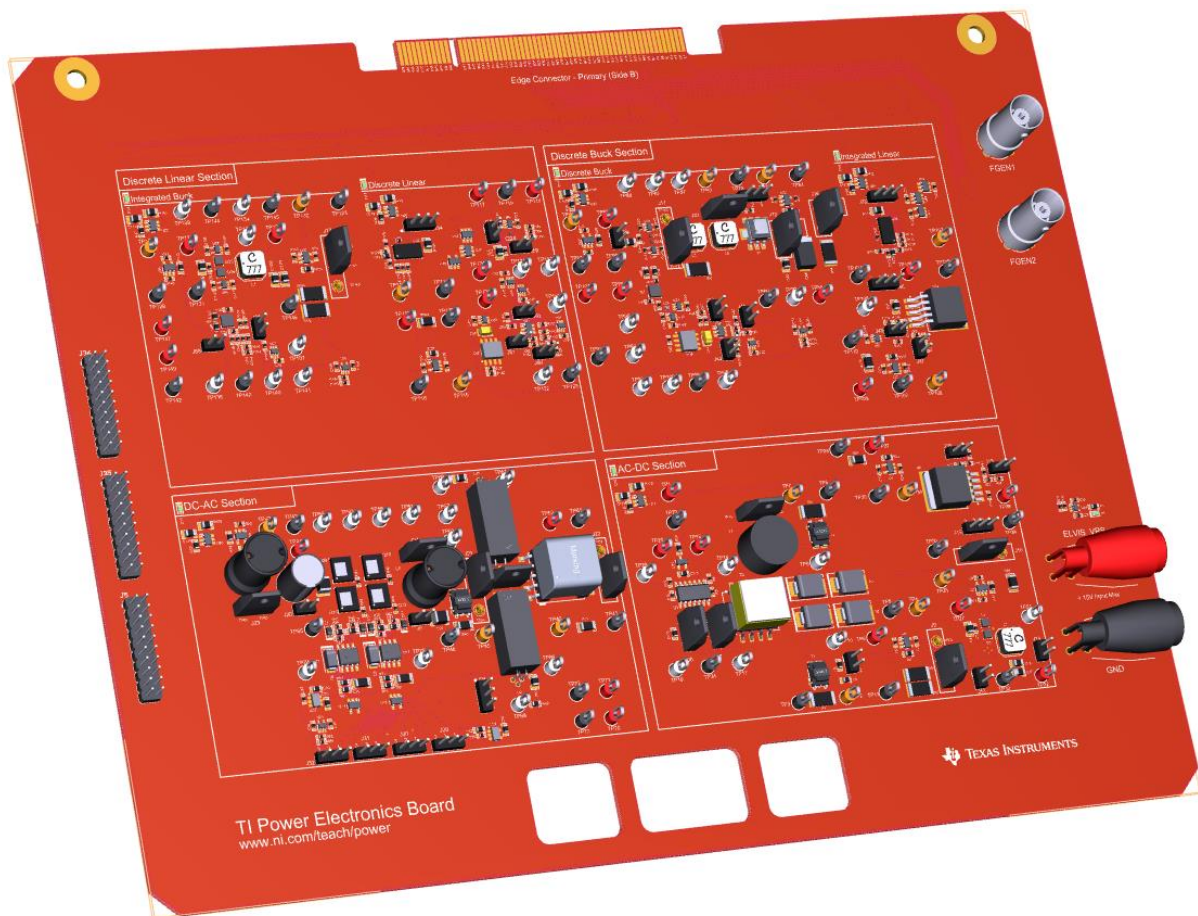
Check Your Understanding

1-1   B

1-2   A

1-3   B

1-4   A

1-5   C

1-6   B

Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III

Lab 12: Post Regulators Operation

Lab 12: Post Regulators Operation

The goal of this lab is to analyze the behavior of power electronic system composed by a diode-bridge AC-DC rectifier, a buck DC-DC regulator and a linear regulator. This system emulates the typical configuration of many real world power supplies, using:
- a rectifier to convert the AC voltage of a power source into a DC voltage;
- a switching regulator to regulate the rectifier DC output voltage and adjust its level to better fit the application requirements;
- a linear regulator to filter the switching ripple of the output voltage of the switching regulator and provide the final voltage regulation required by the load.

In this Lab we analyze the system configuration, we simulate it to analyze the impact of main setup parameters, and we perform lab experiments to observe the main voltages and currents of a real system under different operating conditions.
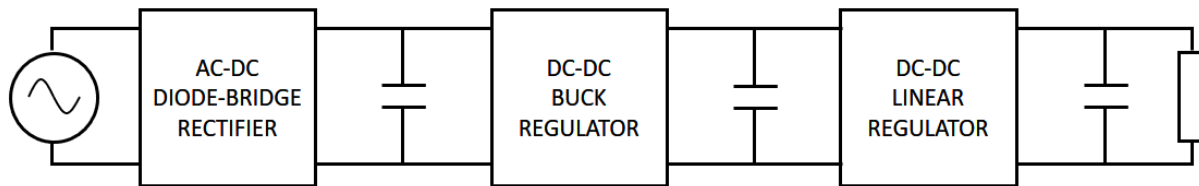

Figure 1-1. Diode-bridge AC-DC Rectifier with Buck DC-DC regulator and Linear post-regulator

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a system composed by an AC-DC diode rectifier, a buck DC-DC regulator and a linear post-regulator, you will calculate the average voltages and currents of each block, with specified units and accuracy, under different setup conditions.
2. Given a system composed by an AC-DC diode rectifier, a buck DC-DC regulator and a linear post-regulator, you will simulate its operation under different setup conditions, to analyze the average voltage and current and the AC noise.
3. Given a real system composed by an AC-DC diode rectifier, a buck DC-DC regulator and a linear post-regulator, you will observe its voltage and current waveforms in different points, and measure the amplitudes of their DC and AC components with specified units and accuracy, to verify the consistency with simulation results and estimate system parameters.

Required Tools and Technology

Platform: NI ELVIS III

Instruments used in this lab:
- Function generator
- Digital multimeter
- Oscilloscope
- Power Supply

Note: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.

- ✓ Access Instruments
  https://measurementslive.ni.com/
- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ni-elvis-iii.html
- ✓ View Tutorials
  https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M

Hardware: TI Power Electronics Board

- ✓ View User Manual
  http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html

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Software: NI Multisim Live

- ✓ Access
  https://www.multisim.com/
- ✓ View Tutorial
  https://www.multisim.com/get-started/

Software: TI Power Electronics Configuration Utility

- ✓ Download (Windows OS Only)
  http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip

  Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by NI Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations and comparisons on simulations and experimental results
- ✓ Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a power conversion system comprised of an AC-DC diode-bridge rectifier, a DC-DC Buck regulator and a linear regulator. We analyze the main voltage and current waveforms in different points of the system and discuss the relationships among them based on the operation principle of each functional block.

1-2 Ideal Diode-Bridge Rectifier

Figure 1-2 shows the typical configuration of an AC-DC diode-bridge rectifier, taking energy from an AC voltage source $V_s(t) = V_s\sin(2\pi f_s t)$ and supplying a DC load resistor R_o through a DC-DC buck regulator and a DC-DC linear post regulator.
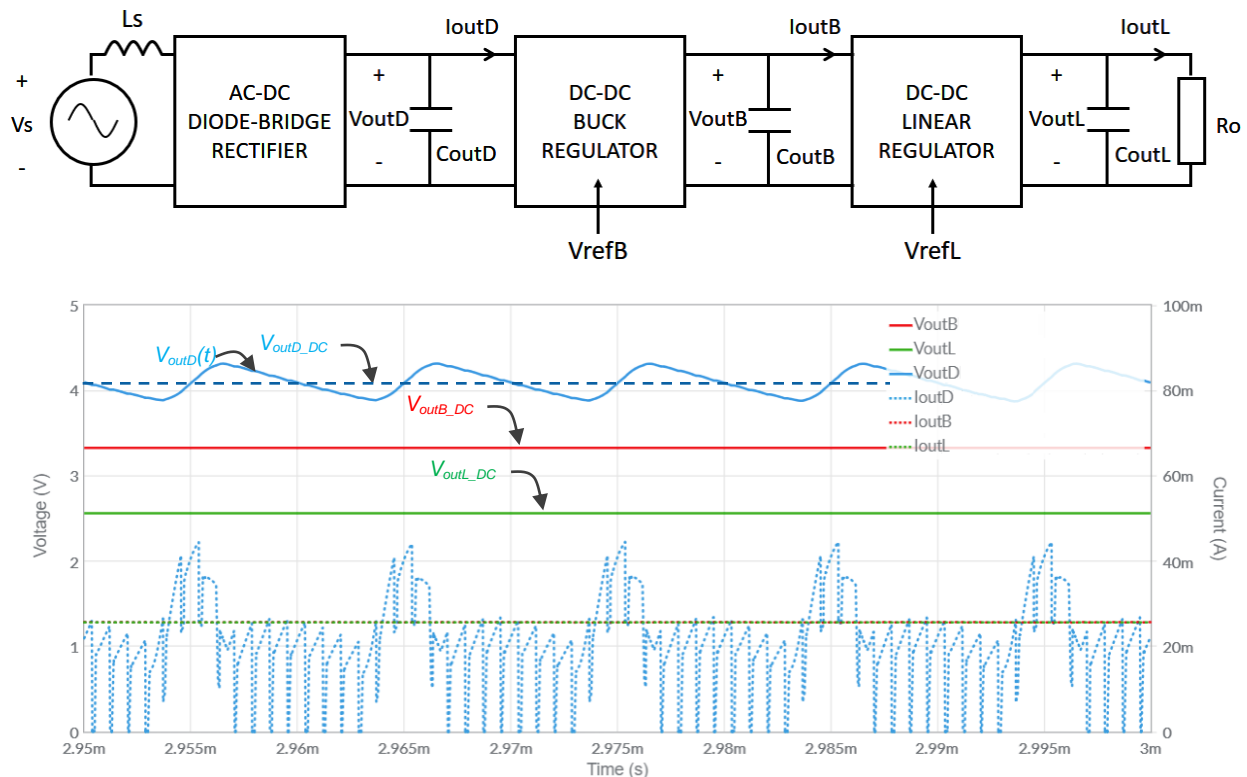
Figure 1-2. Diode-Bridge AC-DC Rectifier with DC-DC Buck Regulator and DC-DC Linear Post-Regulator

The diode bridge rectifier converts the sine source voltage $V_s(t)$ into a non regulated voltage $V_{outD}(t)$, comprised of a DC component V_{outD_DC} and an periodical AC ripple component $\Delta V_{outD\_AC}(t)$ at frequency $2f_s$. The value of V_{outD_DC} and the peak-peak amplitude of $\Delta V_{outD\_AC}(t)$ are determined by the load, the output capacitor C_{outD} and the source inductance L_s (see

LAB11). Typically, the peak-peak amplitude of $\Delta V_{outD\_AC}(t)$ can be about 10% of V_{outD_DC}. The variability of V_{outD_DC} and the large amplitude of $\Delta V_{outD\_AC}(t)$ are not tolarated by DC loads like analog and digital electronic devices. The function of the DC-DC buck regulator is to convert the unregulated DC voltage $V_{outD}(t)$ into a regulated DC voltage $V_{outB}(t)$ and to suppress the large ripple component $\Delta V_{outD\_AC}(t)$. The output voltage $V_{outB}(t)$ of the buck regulator is comprised of a regulated DC component V_{outB_DC}, an AC ripple component $\Delta V_{outB\_AC\_2fs}(t)$ at the frequency $2f_s$ of the rectifier output ripple $\Delta V_{outB\_AC\_fs}(t)$, and an AC ripple component $\Delta V_{outB\_AC\_fs}(t)$ at the switching frequency f_{sw} of the buck regulator itself, as shown in Figure 1-3, where $2f_s = 100$kHz and $f_{sw} = 1.2$MHz.
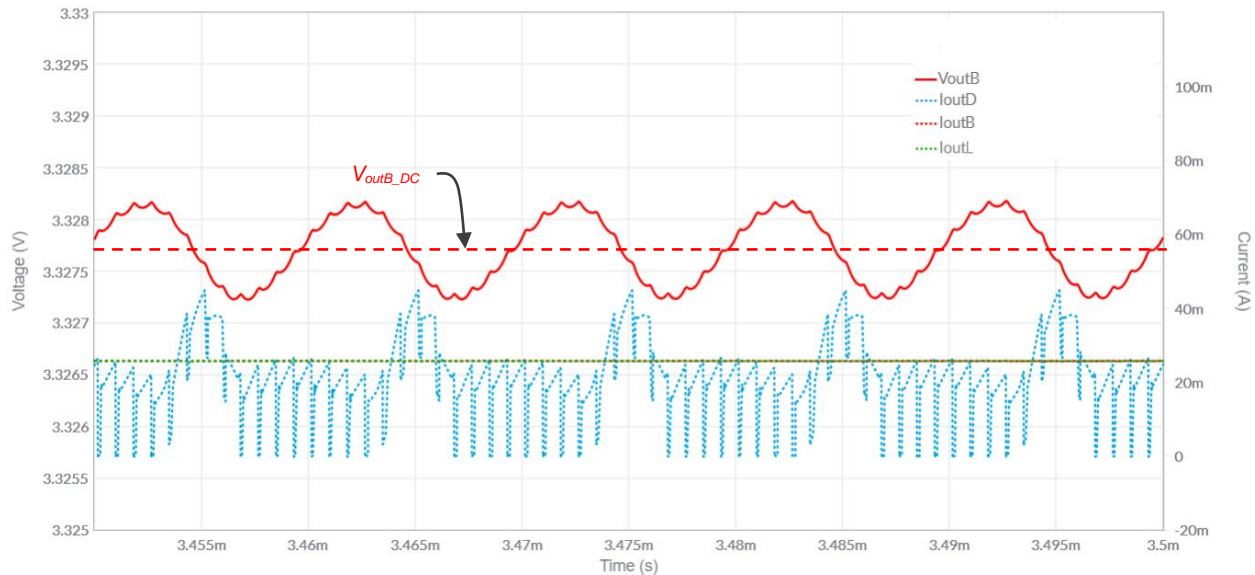

Figure 1-3. Output Voltage of DC-DC Buck Regulator

The value of V_{outB_DC} is regulated by the control circuitry of the buck regulator and is proportional to a reference voltage V_{refB} (see **LAB8**). The peak-peak amplitude of $\Delta V_{outB\_AC}(t)$ is determined by the output capacitance C_{outB} of the buck regulator (see **LAB6**), and it is very small compared to V_{outB_DC} (typically 1%-2%). Certain special devices, like electronic circuits used in medical diagnostic equipments or in automotive and aerospace applications, do not tolerate the switching ripple characterizing the output voltage of switching regulators. In these cases, a linear post-regulator can be used, to achieve the adjustment of the regulated load voltage to lower levels and to suppress the switching ripple noise. The output voltage $V_{outL}(t)$ of the linear regulator is then comprised of a regulated DC component V_{outL_DC} and a negligible AC ripple component $\Delta V_{outL\_AC}(t)$ at the switching frequency f_{sw} of the switching regulator, as shown in Figure 1-4.
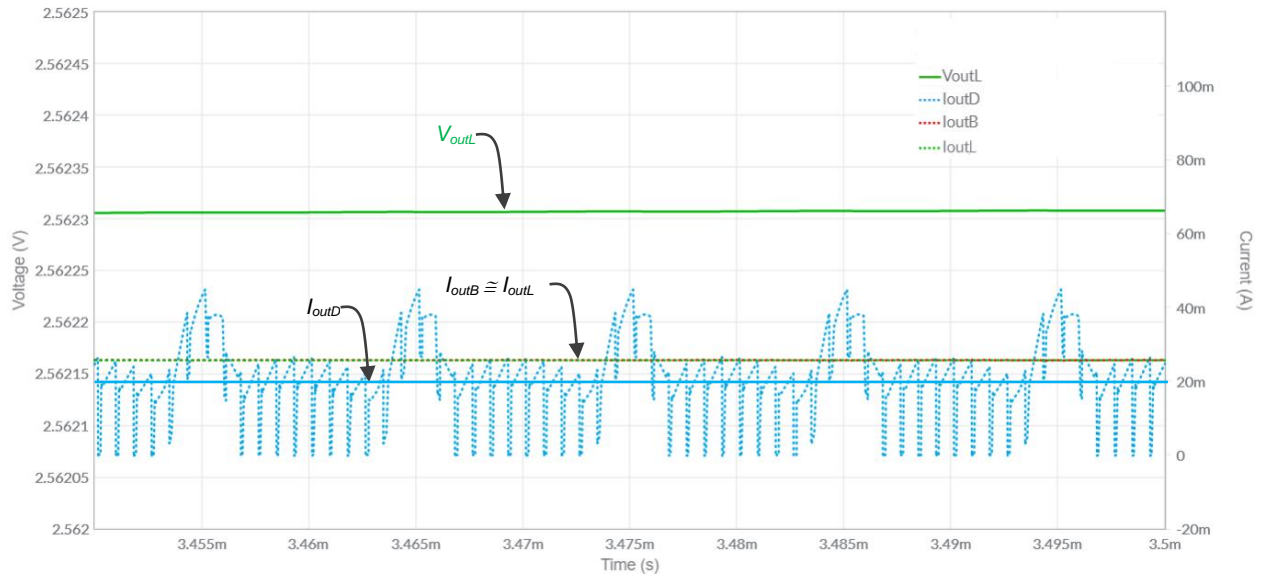
Figure 1-4. Output Voltage of DC-DC Linear Regulator

The value of V_{outL} is proportional to a reference voltage V_{refL}, and is regulated by the control circuitry of the linear regulator (see **LAB4**). The peak-peak amplitude of $\Delta V_{outL\_AC}(t)$ is determined by the output capacitance C_{outL} of the linear regulator or by the control circuitry of the linear regulator, depending on its frequency, and it is very small compared to V_{outL_DC} (typically less than 1%).

Both the DC-DC buck regulator and the DC-DC linear regulator perform a step-down regulation. They can only regulate an average output DC voltage V_{out} at a lower level than the average input DC voltage V_{in}. The main difference between them is that, given the voltage conversion ratio $M=V_{out}/V_{in}$ between the output and the input voltage, the efficiency of DC-DC buck regulator can be much higher that the efficiency of the DC-DC linear regulator (see **Lab1** and **Lab5**). Moreover, the average input current I_{in} of the buck regulator is lower than the average output current I_{out}, according to Equation 1-1:

Equation 1-1
$$I_{in} = I_{out}\frac{V_{out}}{\eta V_{in}} < I_{out}$$

where $\eta=P_{out}/P_{in}$ is the efficiency of the buck regulator. The average input current of the linear regulator, instead, is slightly higher than the output current, according to Equation 1-2:

Equation 1-2
$$I_{in} = I_{out} + I_{gnd} > I_{out}$$

where I_{gnd} is the ground current of the linear regulator, whose value can range from few tens to hundreds of micro Ampères, depending on the regulator technology and current rating.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What is the function of a DC-DC regulator?
  A. to convert a non-regulated DC input voltage into a regulated DC output voltage
  B. to convert a DC voltage source into a DC current source
  C. to convert a DC input voltage into a sinusoidal AC output voltage

1-2 What is the function of a linear regulator?
  A. to convert a DC input voltage into a DC output voltage of higher value
  B. to regulate a DC output voltage suppressing AC input voltage noise
  C. to convert a DC input voltage into an output voltage increasing linearly in the time

1-3 What is the main difference between a buck and a linear regulator?
  A. the buck steps up the voltage while the linear steps down the voltage
  B. the buck can have much higher efficiency than the linear
  C. the buck can have much higher input current than the linear

1-4 What is the main function of a buck regulator when placed on the output of a diode bridge rectifier?
  A. to increase the efficiency
  B. to regulate the voltage and suppress the AC ripple
  C. to limit the output current of the diode bridge rectifier

1-5 What is the main function of a linear regulator when placed on the output of a buck regulator?
  A. to suppress switching noise
  B. to increase the efficiency
  C. to increase the voltage

1-6 Where do we find the maximum average DC current in a system comprised of a diode bridge rectifier, a buck regulator and a linear regulator?
  A. at the output of the diode bridge rectifier
  B. at the output of the buck regulator
  C. at the output of the linear regulator

2 Exercise

The AC-DC diode bridge rectifier of the TI Power Electronics Board for NI ELVIS III generates an output voltage characterized by a 4.1V DC component and a 430mV peak-peak amplitude ripple component at 100kHz. A DC-DC buck regulator is connected to the output of the rectifier, with two output regulation options:

- option B1: $V_{outB\_DC} = 5V$
- option B2: $V_{outB\_DC} = 3.3V$

The output of the buck regulator can be connected to a 100Ω load resistor or to a linear regulator, with two output regulation options:

- option L1: $V_{outL\_DC} = 3.3V$
- option L2: $V_{outL\_DC} = 2.5V$

The output of the linear regulator is connected to a 100Ω load resistor.

2-1 Based on the characteristics of the buck and linear regulator summarized in the **Theory and Background** Section, assuming that the buck regulator has 90% efficiency and that the ground current of the linear regulator is negligible, check the feasible combinations in Table 2-1 and calculate the values of the average DC output currents I_{outD_DC}, I_{outD_DC} and I_{outD_DC} of rectifier, buck regulator and linear regulator, respectively, in milli Ampère with one decimal digit of accuracy.

	feasible	I_{outD_DC} [mA]	I_{outB_DC} [mA]	I_{outL_DC} [mA]
buck output connected to 100Ω resistor with option B1 setup	☐ yes ☐ no			
buck output connected to 100Ω resistor with option B2 setup	☐ yes ☐ no			
buck output connected linear input with option B1-L1 setup	☐ yes ☐ no			
buck output connected linear input with option B1-L2 setup	☐ yes ☐ no			
buck output connected linear input with option B2-L1 setup	☐ yes ☐ no			
buck output connected linear input with option B2-L2 setup	☐ yes ☐ no			

3 Simulate

The goal of the simulations you will perform in this section is to analyze the operation of of a power conversion system comprised of an AC-DC diode-bridge rectifier, a DC-DC Buck regulator and a linear regulator. You will observe the voltage and current waveforms at the output of each block of the system, to verify the impact of the conversion, regulation and filtering capabilities of buck regulator and linear regulator.

3-1 Instructions

1. Open *Lab12 – Post-Regulator Operation* from this file path:
   https://www.multisim.com/content/jmMuKf3CNeGgZt5Jy8BPff/lab12-post-regulators-operation/open/
   The circuit schematic for the analysis of the power conversion system comprised of an AC-DC diode-bridge rectifier, a DC-DC Buck regulator and a linear regulator is shown in Figure 3-1.
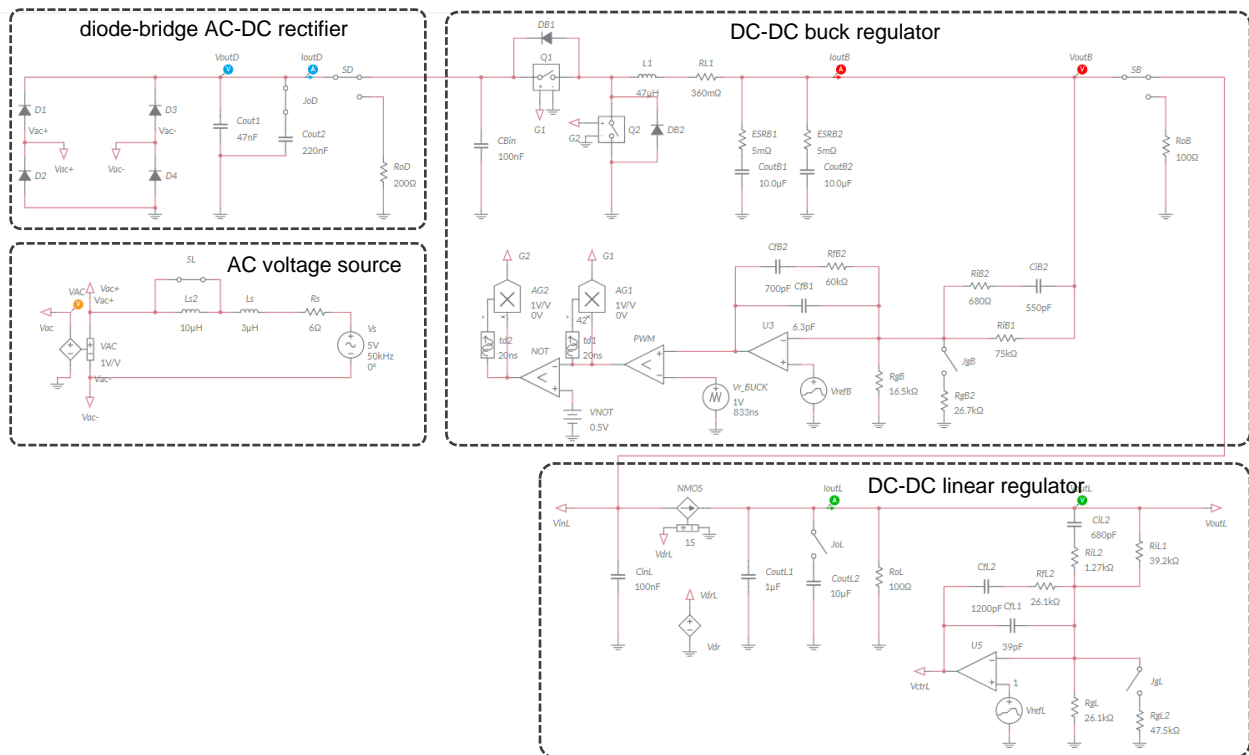

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Post-Regulators Operation.

The AC voltage is generated by a 50kHz/5V sinusoidal voltage source, with output impedance comprised of 6Ω resistance R_s and 3µH inductance L_s. The switch SL allows

to add 10µH in series to inductance L_s. The switch *JoD* allows to add 220nF in parallel to capacitance C_{out1} of the rectifier. A voltage-controlled source allows AC differential voltage measurement with a single voltage probe. The rectifier output can be conected to the 200Ω *RoD* load resistor, or to the input of a DC-DC buck regulator, by means of the switch *SD*. The switch *JgB* allows to set the output voltage of the buck regulator with two options:

- **option B1 (*JgB* closed)**: $V_{outB\_DC} = 5V$
- **option B2 (*JgB* open)**: $V_{outB\_DC} = 3.3V$

The output of the buck regulator can be connected to the 100Ω *RoB* load resistor, or to the input of the linear regulator by means of switch *SB*. The switch *JgL* allows to set the output voltage of the linear regulator with two options:

- **option L1 (*JgL* closed)**: $V_{outL\_DC} = 3.3V$
- **option L2 (*JgL* open)**: $V_{outL\_DC} = 2.5V$

The output of the linear regulator is connected to the 100Ω load *RoL* resistor.

The simulation schematic includes the two voltage generators *VrefB* and *VrefL*, which provide the voltage reference for the buck and the linear regulator, respectively. These generators start from zero and ramp up linearly to reach their nominal values (1.024V for *VrefB* and 0.800V for *VrefL*) in 1.25ms. The *VrefL* generator starts ramping with 1.25ms delay with respect to *VrefB*, thus allowing the buck regulator to reach its nominal output voltage. The total simulation time is set to 3.5ms to allow the regulators to reach a steady-state operation. Figure 3-2 shows an example of the expected output voltage waveforms of buck regulator and linear regulator resulting from this *sequential soft-start* logic.
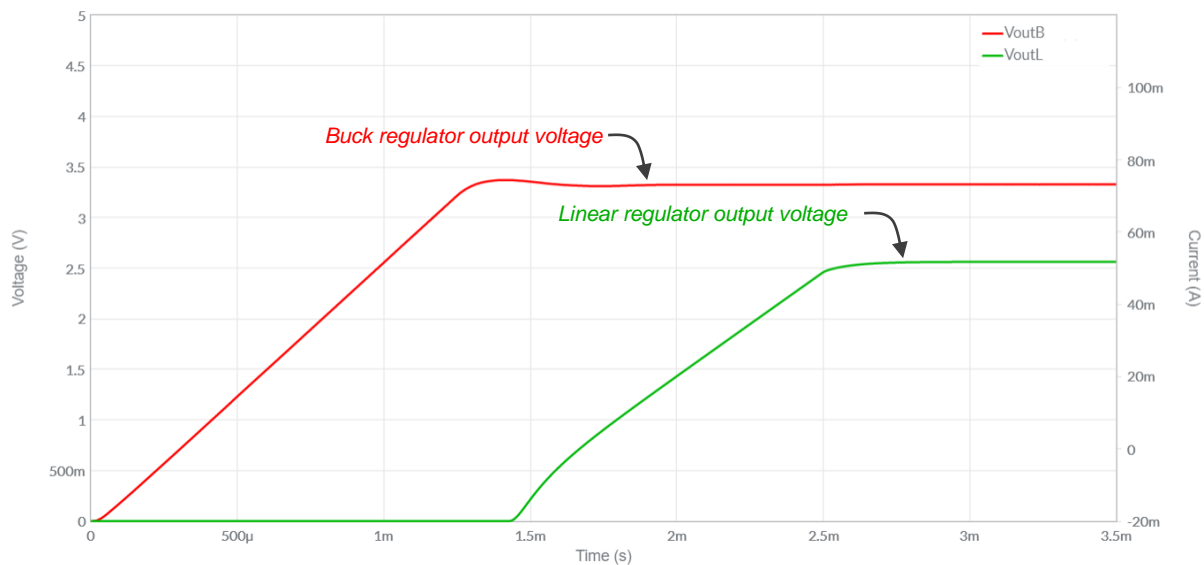

Figure 3-2. Sequential Soft-Start of Buck and Linear Regulators.

3-2   Simulation 1 – Operation with buck regulator connected to 100Ω load resistor.

1. Set switches *JoD* and *SL* to be closed, switches *JoL*, *JgB* and *JgL* to be open, switch *SD* to be closed on buck regulator input, switch *SB* to be closed on load resistor *RoB*.
2. Set *Interactive* simulation and *Split* visualization options.
3. Double click on probes *VoutD*, *IoutD*, *VoutB*, *IoutB*, *VoutL* and *IoutL*, check the *Show plot* option box and the *Instant* and *Periodic* option boxes.
4. Run the simulation. During the simulation you will observe in the *Grapher*, that:
   - the **rectifier output voltage** (***VoutD*** blue continuous trace) has a DC component and a well visible 100kHz ripple;
   - the **buck regulator output volta**ge (***VoutB*** red continuous trace) rises during the simulation and settles after about 1.5ms of simulation time, with no visible AC ripple at 100kHz;
   - the **linear regulator output voltage** (***VoutL*** green continuous trace) is zero;
   - the **rectifier output current** (***IoutD*** blue dashed trace) has a 1.2MHz AC ripple component plus a 100kHz bumping AC ripple (as shown in Figure 1-2);
   - the **buck regulator output current** (***IoutB*** red dashed trace) rises linearly in the time and settles after about 1.5ms of simulation time, with no visible 100kHz AC ripple;
   - the **linear regulator output current** (***IoutL*** green dashed trace) is zero.
5. Read the average measurement V_{AV} of voltage probes *VoutB* and *VoutL,* in Volt with three decimal digits of accuracy, and the average measurement I_{AV} of current probes *IoutB* and *IoutL*, in milli Ampère with one decimal digit of accuracy, and report the results in Table 3-2-1.
6. Use the cursors in *Track* mode on voltage probe *VoutD* to measure the average value and the amplitude of peak-peak 100kHz AC ripple of the rectifier output voltage, in Volts with three decimal digits of accuracy, and report the results in Table 3-2-1 (you may also adjust Y-axis range to better visualize the waveform).
7. Zoom-in the Y-axis around the *VoutB* trace until you see the 100kHz AC ripple, use the cursors in *Track* mode on voltage probe *VoutB* to measure the amplitude of peak-peak 100kHz AC ripple of the buck regulator output voltage, in milli Volts with three decimal digits of accuracy, and report the results in Table 3-2-1.

Table 3-2-1 Operation with buck regulator connected to 100Ω load resistor.

V_{outD_AV} [V]	V_{outB_AV} [V]	V_{outL_AV} [V]	I_{outB_AV} [mA]	I_{outL_AV} [mA]	ΔV_{outD_AC} [V]	ΔV_{outB_AC} [mV]

3-2-1 Is the average output voltage of buck regulator lower than the average output voltage of diode-bridge rectifier?

A.   yes

B.   no

Please provide your comments: _____

_____

3-2-2 Is the peak-peak amplitude of the 100kHz AC output voltage ripple of buck regulator lower than the peak-peak amplitude of the 100kHz AC output voltage ripple of diode-bridge rectifier?

A.   yes

B.   no

Please provide your comments: _____

_____

3-3   Simulation 2 – Operation with buck regulator connected to linear regulator.
   1.   Set switch *SB* to be closed on linear regulator input.
   2.   Run the simulation. During the simulation you will observe in the *Grapher*, that:
        -   the **rectifier output voltage** (*VoutD* blue continuous trace) has a DC component and a well visible 100kHz ripple;
        -   the **buck regulator output volta**ge (*VoutB* red continuous trace) rises during the simulation and settles after about 1.5ms of simulation time, with no visible AC ripple at 100kHz;
        -   the **linear regulator output voltage** (*VoutL* green continuous trace) starts rising after about 1.25ms and settles after further 1.5ms of simulation time, with no visible AC ripple at 100kHz;
        -   the **rectifier output current** (*IoutD* blue dashed trace) has a 1.2MHz AC ripple component plus a 100kHz bumping AC ripple (as shown in Figure 1-2);
        -   the **buck regulator output current** (*IoutB* red dashed trace) rises linearly in the time and settles after about 1.5ms of simulation time, with no visible 100kHz AC ripple;
        -   the **linear regulator output current** (*IoutL* green dashed trace) starts rising after about 1.25ms and settles after further 1.5ms of simulation time, with no visible AC ripple at 100kHz;

3. Read the average measurement V_{AV} of voltage probes *VoutB* and *VoutL,* in Volt with three decimal digits of accuracy, and the average measurement I_{AV} of current probes *IoutB* and *IoutL*, in milli Ampère with one decimal digit of accuracy, and report the results in Table 3-3-1.
4. Use the cursors in *Track* mode on voltage probe *VoutD* to measure the average value and the amplitude of peak-peak 100kHz AC ripple of the rectifier output voltage, in Volts with three decimal digits of accuracy, and report the results in Table 3-3-1 (you may also adjust Y-axis range to better visualize the waveform).
5. Zoom-in the Y-axis around the *VoutB* trace until you see the 100kHz AC ripple, use the cursors in *Track* mode on voltage probe *VoutB* to measure the amplitude of peak-peak 100kHz AC ripple of the buck regulator output voltage, in milli Volts with three decimal digits of accuracy, and report the results in Table 3-3-1.
6. Zoom-out the Y-axis until you see the *VoutL* trace, then zoom-in the Y-axis around the *VoutL* trace until you see the 100kHz AC ripple, use the cursors in *Track* mode on voltage probe *VoutL* to measure the amplitude of peak-peak 100kHz AC ripple of the buck regulator output voltage, in milli Volts with three decimal digits of accuracy, and report the results in Table 3-3-1. [**Note**: *VoutL* trace looks rising as the simulation has not reached the real steady-state yet].

Table 3-3-1 Operation with buck regulator connected to 100Ω load resistor.

V_{outD_AV} [V]	V_{outB_AV} [V]	V_{outL_AV} [V]	I_{outB_AV} [mA]	I_{outL_AV} [mA]	ΔV_{outD_AC} [V]	ΔV_{outB_AC} [mV]	ΔV_{outL_AC} [mV]

3-3-1 Is the average output voltage of buck regulator lower than the average output voltage of diode-bridge rectifier?
A.   yes
B.   no
Please provide your comments: _____

_____

3-3-2 Is the peak-peak amplitude of the 100kHz AC output voltage ripple of buck regulator lower than the peak-peak amplitude of the 100kHz AC output voltage ripple of diode-bridge rectifier?
A.   yes
B.   no
Please provide your comments: _____

_____

3-3-3 Is the average output voltage of linear regulator lower than the average output voltage of buck regulator?

    A.   yes

    B.   no

Please provide your comments: _____

_____

3-3-4 Is the peak-peak amplitude of the 100kHz AC output voltage ripple of buck regulator lower than the peak-peak amplitude of the 100kHz AC output voltage ripple of diode-bridge rectifier?

    A.   yes

    B.   no

Please provide your comments: _____

_____

3-3-5 Is the average output current of linear regulator lower or higher than the average output current of buck regulator?

    A.   lower

    B.   higher

    C.   other:_____

Please provide your comments: _____

_____

Troubleshooting tips:
1. If the simulation does not converge and you get some error message, reload *Lab12 – Post-Regulator Operation* from this file path:
https://www.multisim.com/content/jmMuKf3CNeGgZt5Jy8BPff/lab12-post-regulators-operation/open/
and restart the simulation following the instructions.

4 Implement

The experiments you perform in this section allow you to observe the voltage and current waveforms of a system comprised of an AC-DC diode-bridge rectifier, a DC-DC Buck regulator and a linear regulator, under different configuration setup. The **AC-DC Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 will be used to perform the experiments.
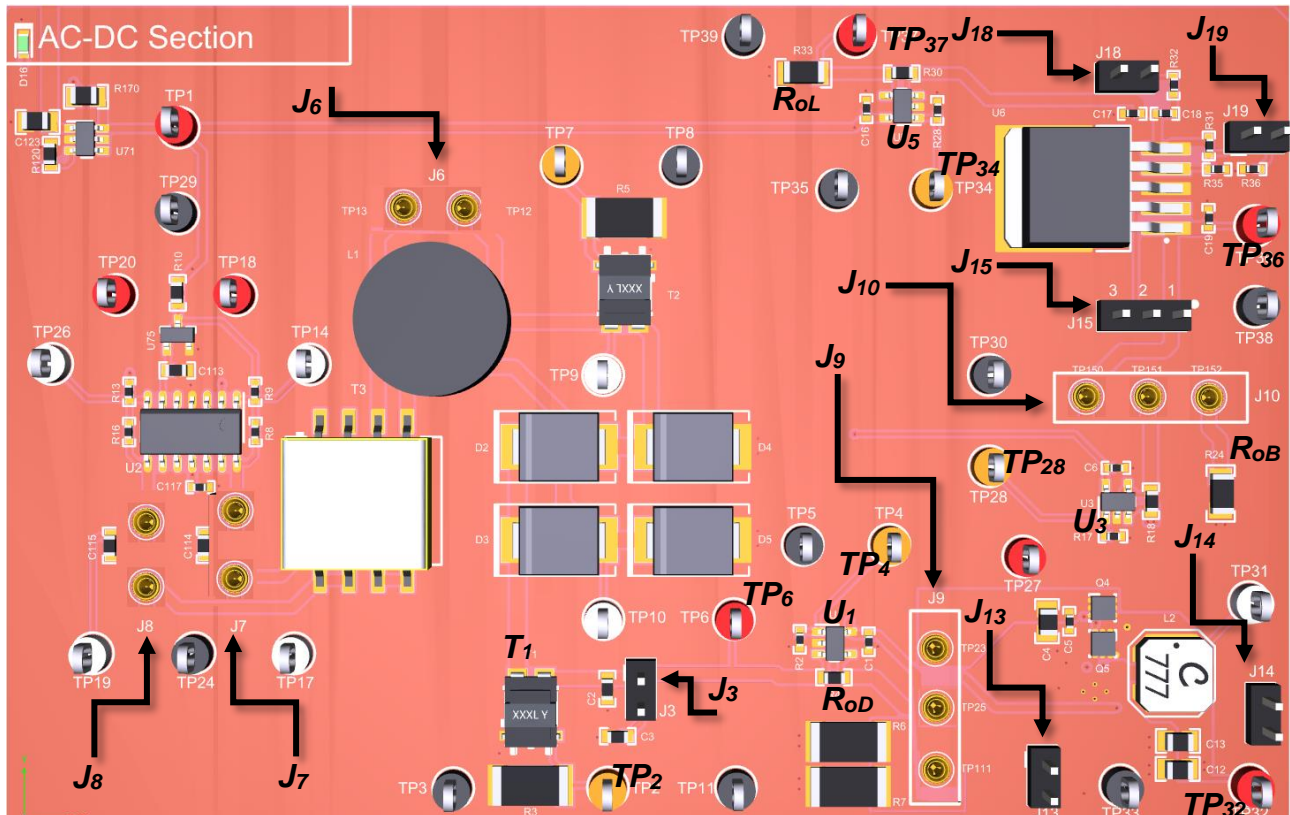

Figure 4-1. TI Power Electronics Board for NI ELVIS III – AC-DC Section Used for the Analysis of Post Regulators Operation.

The output of the diode bridge can be connected to the 200Ω fixed load resistor R_{oD} (parallel of R6 and R7) or to the input of a 1.2MHz TI's TPS40305 integrated buck converter. The buck regulator output can be connected to the 100Ω fixed load resistor R_{oB} (R24), or to the input of a TI's TPS7A6201-Q1 integrated linear regulator whose output is connected to the 100Ω load resistor R_{oL} (R33). The DC output currents of diode bridge rectifier, buck regulator and linear regulator are sensed by means of TI's INA139 current monitor chips $U1$, $U3$ and $U5$, respectively, allowing the current measuement by means of a multimeter or a voltage probe. The transformer $T1$ senses the diode bridge AC output current, with sensing gain 0.1. The waveforms of interest in the experiment are available at following test points:

- diode bridge rectifier output voltage V_{outD}: TP_6;
- buck regulator output voltage V_{outB}: TP_{32};
- linear regulator output voltage V_{outL}: TP_{37};
- diode bridge rectifier DC output current I_{outD_DC}: TP_4;
- diode bridge rectifier AC output current I_{outD_AC}: TP_2;
- buck regulator DC output current I_{outB_DC}: TP_{28};
- linear regulator DC output current I_{outL_DC}: TP_{34}.

The datasheets of TI's components are available at these links:
- TPS40305 buck regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf
- TPS7A6201-Q1 linear regulator: http://www.ti.com/lit/ds/symlink/tps7a6201-q1.pdf
- INA139NA/3K current monitor: http://www.ti.com/lit/ds/symlink/ina139.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 Instructions

1. Open *Power Supply*, *Function Generator*, *Pattern Generator*, *Digital Multimeter* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Buck Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab12 – Post-Regulators Operation*.
5. Connect and configure instruments as indicated in Tables 4-1 and 4-2.

Table 4-1 Instruments Connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP6 (V_{outD}), connect CH-2 to TP32 (V_{outB}) connect CH-3 to TP37 (V_{outL}), connect CH-4 to TP2 (I_{outD_AC})
Function Generator	connect CH-1 to FGEN1 BNC connector ($\rightarrow$TP18 = *FG1*) connect CH-2 to FGEN2 BNC connector ($\rightarrow$TP20 = *FG2*)
Pattern Generator	connect TRIG to DIO 0 (red) and GND (black) using a BNC-to-Alligator Cable
Digital Multimeter	connect to TP4 (I_{outD_DC}), TP28 (I_{outB_DC}) or TP34 (I_{outL_DC}) as per instructions

Table 4-2 Instruments Configuration and setup

Power Supply	*Channel "+"*: Static, 10.00V, *Channel "-"*: Inactive			
Oscilloscope	*Trigger*: Analog Edge, CH-1, set to 50%	*Horizontal*: 5µs/div	*Acquisition*: average	*Measurements*: show
	CH-1: OFF • DC coupling • 1V/div • offset 0V	*CH-2*: OFF • DC coupling • 1V/div • offset 0V	*CH-3*: ON • DC coupling • 1V/div • offset 0V	*CH-4*: ON • DC coupling • 20mV/div offset 0V
Function Generator	*follow instructions provided below*			
Pattern Generator	*follow instructions provided below*			
Digital Multimeter	*Measurement mode*: DC voltage; *Range*: 50mV			

4-2 Experiment 1 – Operation with buck regulator connected to 100Ω load resistor.

1. Configure the jumpers of the board as indicated in Table 4-2-1.

Table 4-2-1 Jumpers Setup

J6	J7	J8	J9	J3	
shorted	shorted	shorted	short TP25-TP23	shorted	
J18	J15	J19	J10	J13	J14
open	short 2-3	open	short TP151-TP152	open	open

2. On *Channel 1* of the *Function Generator*, select *Custom*, use the file selector to select the TDMS waveform *Lab12_FG1.tdms*, set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 100MS/s,set *Generation mode* to *Loop*.

3. On *Channel 2* of the *Function Generator* select *Custom*, use the file selector to select the TDMS waveform *Lab12_FG2.tdms*, set *Trigger source* to *TRIG*, set *Gain* to 1, set *Update rate* to 100MS/s, set *Generation mode* to *Loop*.

4. On *Logic Analyzer and Pattern Generator*, click on *"+"* in the *Pattern Generator* section, click on *Signal* to add a new signal to the *Pattern Generator*, check the box next to *Logic 0* to add the line and click on the whitespace in the instrument, set *Status* to *On*, set *Mode* to *Clock*, set *Frequency* to 1Hz, set *Duty cycle* to 50%.

5. Run *Oscilloscope*, *Digital Multimeter, Power Supply, Pattern Generator* and *Function Generator*.

6. Measure the DC component of the diode bridge output voltage V_{outD_DC} on *Oscilloscope* CH-1, in Volt with three decimal digits of accuracy, and report the result in Table 4-2-2. [**Note:** the measurement of the average value can performed by means of cursors. The RMS measurement provides an approximation of the average value]

7. Measure the amplitude of peak-peak output voltage ripple ΔV_{outD_AC} on *Oscilloscope* CH-1, in Volt with three decimal digits of accuracy, and report the result in Table 4-2-2.

8. Measure the DC component of the buck regulator output voltage V_{outB_DC} on *Oscilloscope* CH-2, in Volt with three decimal digits of accuracy, and report the result in Table 4-2-2. [**Note:** The RMS measurement provides a good approximation of the average value]

9. On *Oscilloscope* CH-2, set the vertical axis to 10mV/div, set the vertical offset to a negative value $-V_{outB\_DC}$, use cursors to measure (if visible) the peak-peak amplitude of the 100kHz AC ripple on output voltage of buck regulator, in milli Volt with three decimal digits of accuracy, and report the result in Table 4-2-2. [**Note:** If you are not able to observe any 100kHz AC ripple report 0.000 in Table 4-2-2]

10. Connect the *Digital Multimeter* to TP4-TP5 to measure the average DC output current of diode bridge I_{outD_DC}, in milli Ampère, with one decimal digit of accuracy, and report the result in Table 4-2-2.

11. Connect the *Digital Multimeter* to TP28-TP30 to measure the average DC output current of buck regulator I_{outB_DC}, in milli Ampère, with one decimal digit of accuracy, and report the result in Table 4-2-2.

12. Stop *Oscilloscope*, *Digital Multimeter, Power Supply, Function Generator* and *Pattern Generator*.

Table 4-2-2 Operation with buck regulator connected to 100Ω load resistor.

V_{outD_DC} [V]	V_{outB_DC} [V]	I_{outD_DC} [mA]	I_{outB_DC} [mA]	ΔV_{outD_AC} [V]	ΔV_{outB_AC} [mV]

4-2-1 Does the DC output voltage of buck regulator correspond to the expected value?
   A.   yes
   B.   no
   Please provide your comments: _____

_____

4-2-2 Is the peak-peak amplitude of the 100kHz AC ripple of the buck regulator output voltage lower than the peak-peak amplitude of the 100kHz AC ripple of the diode bridge output voltage?

A.   yes

B.   no

Please provide your comments: _____

_____

_____

4-3 Experiment 2 – Operation with buck regulator connected to linear regulator.

1. Configure the jumpers of the board as indicated in Table 4-3-1.

Table 4-3-1 Jumpers Setup

J6	J7	J8	J9	J3	
shorted	shorted	shorted	short TP25-TP23	shorted	
J18	J15	J19	J10	J13	J14
open	short 1-2	open	short TP150-TP151	shorted	open

2. Run *Oscilloscope*, *Digital Multimeter, Power Supply, Pattern Generator* and *Function Generator*.

3. Measure the DC component of the diode bridge output voltage V_{outD_DC} on *Oscilloscope* CH-1, in Volt with three decimal digits of accuracy, and report the result in Table 4-3-2. [**Note:** the measurement of the average value can performed by means of cursors. The RMS measurement provides an approximation of the average value]

4. Measure the amplitude of peak-peak output voltage ripple ΔV_{outD_AC} on *Oscilloscope* CH-1, in Volt with three decimal digits of accuracy, and report the result in Table 4-3-2.

5. Measure the DC component of the buck regulator output voltage V_{outB_DC} on *Oscilloscope* CH-2, in Volt with three decimal digits of accuracy, and report the result in Table 4-3-2. [**Note:** The RMS measurement provides a good approximation of the average value]

6. On *Oscilloscope* CH-2, set the vertical axis to 10mV/div, set the vertical offset to a negative value -V_{outB_DC}, use cursors to measure (if visible) the peak-peak amplitude of the 100kHz AC ripple on output voltage of buck regulator, in milli Volt with three decimal digits of accuracy, and report the result in Table 4-3-2. [**Note:** If you are not able to observe any 100kHz AC ripple report 0.000 in Table 4-3-2]

7. Measure the DC component of the linear regulator output voltage V_{outL_DC} on *Oscilloscope* CH-3, in Volt with three decimal digits of accuracy, and report the result in Table 4-3-2. [**Note:** The RMS measurement provides a good approximation of the average value]
8. On *Oscilloscope* CH-3, set the vertical axis to 10mV/div, set the vertical offset to a negative value $-V_{outL\_DC}$, use cursors to measure (if visible) the peak-peak amplitude of the 100kHz AC ripple on output voltage of linear regulator, in milli Volt with three decimal digits of accuracy, and report the result in Table 4-3-2. [**Note:** If you are not able to observe any 100kHz AC ripple report 0.000 in Table 4-3-2]
9. Connect the *Digital Multimeter* to TP4-TP5 to measure the average DC output current of diode bridge I_{outD_DC}, in milli Ampère, with one decimal digit of accuracy, and report the result in Table 4-2-2.
10. Connect the *Digital Multimeter* to TP28-TP30 to measure the average DC output current of buck regulator I_{outB_DC}, in milli Ampère, with one decimal digit of accuracy, and report the result in Table 4-2-2.
11. Connect the *Digital Multimeter* to TP34-TP35 to measure the average DC output current of linear regulator I_{outL_DC}, in milli Ampère, with one decimal digit of accuracy, and report the result in Table 4-3-2.
12. Set the jumper J13 to be open, set Channel 2 and Channel 3 with zero offset and 1V/div resolution, and repeat the steps 3-11.
13. Stop *Oscilloscope*, *Digital Multimeter, Power Supply, Function Generator* and *Pattern Generator*.

Table 4-3-2 Operation with buck regulator connected to linear regulator.

J13	V_{outD_DC} [V]	V_{outB_DC} [V]	V_{outL_DC} [V]	I_{outD_DC} [mA]	I_{outB_DC} [mA]	I_{outL_DC} [mA]	ΔV_{outD_AC} [V]	ΔV_{outB_AC} [mV]	ΔV_{outL_AC} [mV]
shorted									
open									

4-3-1 Does the DC output voltage of buck regulator correspond to the expected value?
    A.   yes
    B.   no
    C.   other:_____

Please provide your comments: _____

_____

_____

4-2-2 Is the peak-peak amplitude of the 100kHz AC ripple of the buck regulator and linear regulator output voltages lower than the peak-peak amplitude of the 100kHz AC ripple of the diode bridge output voltage?

A.   yes

B.   no

Please provide your comments: _____

_____

_____

Troubleshooting tips:

- If the system does not work, or its waveforms look much different with respect to simulations, verify the correct setup and connections of jumpers and instruments, following the directions provided in Tables 4-2-1, 4-2-2, 4-2-3, 4-3-1, 4-3-2, 4-3-3 and restart the experiments.

5 Analyze

5-1   Comparing the simulated and experimental values of the DC output voltage average and peak-peak ripple values, identify the parameters of the simulation model to change in order to achieve a better agreement, based on concepts discussed in the *Theory and Background* section:

_____

_____

_____

6 Conclusion

6-1   Summary

Write a summary of what you observed and learned about the operation of system a comprised of an AC-DC diode-bridge rectifier, a DC-DC buck regulator and a linear regulator, and discuss the impact of the buck and linear regulators on the DC and AC components of their own output voltages, given the input voltage DC and AC components.

6-2 Expansion Activities

6-2-1. Impact of diode bridge rectifier output voltage

Set the jumper J3 to be open and repeat the experiments 1 and 2, to observe the effects of a smaller output capacitor.

6-2-2. Understanding diode bridge rectifier

Execute Lab11 to learn more on diode bridge rectifier.

6-2-3. Understanding buck regulator

Execute Labs 5-8 to learn more on buck regulator.

6-2-4. Understanding linear regulator

Execute Labs 1-4 to learn more on linear regulator

6-2-5. Understanding AC sources

Execute Lab 9 to learn more on how to generate an AC sine voltage by means of a DC-AC inverter.

6-3 Resources for learning more

- This book provides the fundamentals of AC-DC diode bridge rectifiers:
  N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley & Sons, Inc.
- This book provides the fundamentals of switching regulators:
  S. Maniktala, *Switching Power Supplies A - Z*, Newness
- This document provides the fundamentals of linear regulators:
  Linear Regulators: Theory of Operation and Compensation, http://www.ti.com/lit/an/snva020b/snva020b.pdf

Answer Key – Check Your Understanding Questions Only

Check Your Understanding

1-1   A

1-2   B

1-3   B

1-4   B

1-5   A

1-6   B