Power Tips: Designing a CCM flyback converter
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A continuous-conduction-mode (CCM) flyback converter is often used in medium power, isolated applications. CCM operation is characterized by lower peak switching currents, less input and output capacitance, reduced EMI and a narrower operational duty-cycle range than discontinuous-conduction-mode (DCM) operation. These virtues, along with being low cost, mean they have been widely adopted in commercial and industrial applications. This article will provide the power stage design equations for a 53 Vdc to 12 V at 5 A CCM flyback previously discussed in Power Tips #76: Flyback converter design considerations.

Figure 1 shows a detailed 60-W flyback schematic, operating at 250 kHz. The duty-cycle is selected to be 50 percent maximum at the minimum input voltage of 51 V and maximum load. Although operation beyond 50 percent is acceptable, it is not necessary in this design. The duty-cycle will decrease only a few percent while in CCM operation because of the relatively low high-line input voltage of 57 V. However, if the load is greatly reduced and the converter enters DCM operation, duty-cycle will significantly decrease.

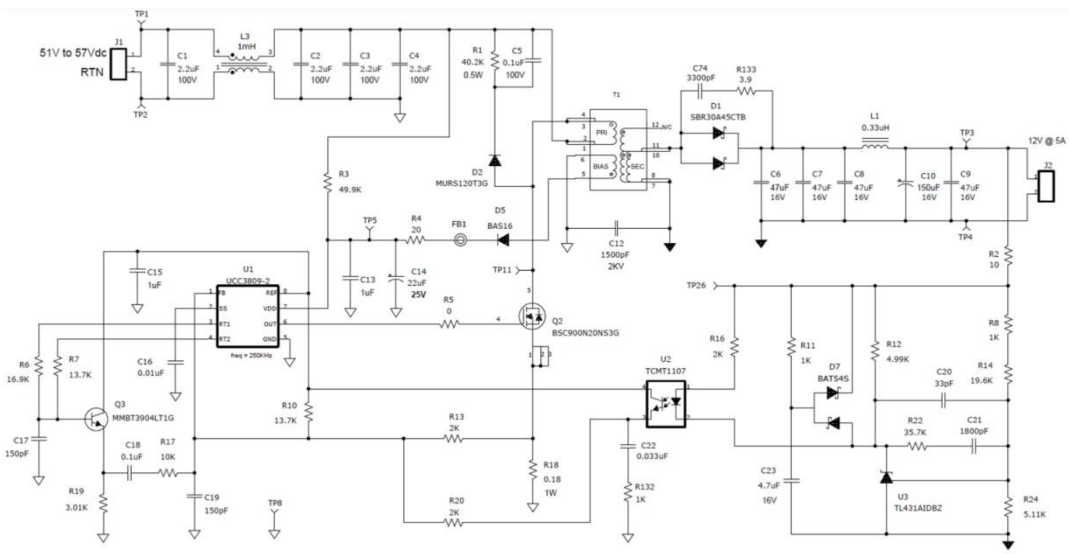

Figure 1: **60-W CCM flyback converter schematic.**

Design specifics

To prevent core saturation, the volt-second product for the windings on/off times must balance. This equates to:

$$Vinmin * dmax = (Vout + Vd) * (1 - dmax) * Nps, \text{ where } Nps = \frac{Npri}{Nsec} \qquad (1)$$

Set dmax to 0.5 and calculate the turn-ratios for Nps12 (Npri : N12V) and Nps14 (Npri : N14V):

$$Nps12 = \frac{Vinmin}{(Vout+Vd)} * \frac{dmax}{(1-dmax)} = \frac{51\text{V}}{(12\text{V}+0.5\text{V})} * \frac{0.5}{(1-0.5)} \sim 4 \text{ (4:1 step-down)} \quad (2)$$

$$Nps14 = \frac{Vinmin}{(Vout+Vd)} * \frac{dmax}{(1-dmax)} = \frac{51\text{V}}{(14\text{V}+0.5\text{V})} * \frac{0.5}{(1-0.5)} \sim 3.5 \text{ (3.5:1 step-down)} \quad (3)$$

Operating duty-cycle and FET voltage can be calculated now that the transformer turns ratio is set.

$$d = \frac{Nps12*(Vout+Vd)}{Vin+Nps12(Vout+Vd)} = \frac{4*(12\text{V}+0.5\text{V})}{57\text{V}+4*(12\text{V}+0.5\text{V})} \sim 0.47 \text{ (dmin at } V_{IN} = 57\text{V)} \quad (4)$$

$$Vdsmax = Vinmax + Nps12 * (Vout + Vd) = 57\text{V} + 4 * (12\text{V} + 0.5\text{V}) = 107\text{V} \quad (5)$$

Vdsmax represents the “flat top” voltage on FET Q2 drain without ringing. Ringing is typically related to the transformer leakage inductance, parasitic capacitances (T1, Q1, D1), and switching speed. Derate the FET voltage an additional 25-50 percent, selecting a 200-V FET. The transformer must have excellent coupling between windings and a maximum leakage inductance of one percent or less, if possible, to minimize ringing.

When Q2 is on, diode D1 has a reverse voltage stress equal to:

$$VD1piv = Vout + \frac{Vinmax}{Nps12} = 12\text{V} + \left(\frac{57\text{V}}{4}\right) \sim 26\text{V} \quad (6)$$

Ringing is common when the secondary winding swings negative due to leakage inductance, diode capacitance and reverse recovery characteristics. Using ultrafast (<35 nS), Schottky and SiC diodes can help minimize reverse-recovery effects and minimize diode snubber losses. D1 conducts during the FET off-time with a flat-top current of:

$$ID1 = \frac{Ioutmax}{(1-dmax)} = \frac{5\text{A}}{(1-0.5)} = 10\text{A} \quad (7)$$

I selected a 30 A/45 V rated D²PAK package to reduce the forward voltage drop to 0.33 V at 10 A. Power dissipation is equal to:

$$PD1 = Ioutmax * Vd = 5\text{A} * 0.33\text{V} \sim 1.7\text{W} \quad (8)$$

A heatsink or airflow for proper thermal management is recommended. You can calculate the primary inductance from:

$$Lmin = \frac{Vinmin^2 * dmax^2 * \eta}{2 * fsw * Poutmin} = \frac{51\text{V}^2 * 0.5^2 * 0.91}{2 * 250\text{KHz} * 15\text{W}} \sim 80\text{uH} \quad (9)$$

where η is the estimated efficiency, and P_{OUTMIN} is where the converter enters discontinuous-mode operation (DCM), which is typically 20-30 percent of P_{OUTMAX}.

Peak primary current occurs at V_{INMIN} and is equal to:

$$Ipri_{pk} = \frac{Ioutmax}{(1-dmax)*Nps12} + \frac{Vinmin*dmax}{2*Lpri*fsw} = \frac{5\text{A}}{(1-0.5)*4} + \frac{51\text{V}*0.5}{2*80\text{uH}*250\text{KHz}} \sim 3.14\text{A} \quad (10)$$

This is necessary to determine the maximum current sense resistor (R18) value to prevent tripping of the controller's primary over-current (OC) protection. For the UCC3809, the voltage across R18 cannot exceed 0.9 V to guarantee full output power. For this example I choose a 0.18 Ohm value. A smaller resistance is acceptable as it reduces power loss. But too small a resistance increases noise sensitivity and makes the OC threshold high, risking transformer saturation or even worse, stress-related circuit failure during an OC fault. The power dissipated in the current sense resistor is:

$$PRs = \left[\frac{Ioutmax*\sqrt{dmax}}{(1-dmax)*Nps12}\right]^2 * Rs = \left[\frac{5\text{A}*\sqrt{0.5}}{(1-0.5)*4}\right]^2 * 0.18\Omega \sim 0.56\text{W} \tag{11}$$

With $Ipri_{pk}$ calculated, FET conduction and turn-off switching losses are estimated from:

$$Pcond = \left[\frac{Ioutmax*\sqrt{d}}{(1-d)*Nps12}\right]^2 * Rs = \left[\frac{5\text{A}*\sqrt{0.47}}{(1-0.47)*4}\right]^2 * 0.12\Omega \sim 0.3\text{W} \quad (\text{Vin=57V}) \tag{12}$$

$$Psw = \frac{1}{4} * tsw * fsw * Vds * Ipri_{pk} = \frac{1}{4} * 25\text{nS} * 250\text{KHz} * 160\text{V} * 3.03\text{A} \sim 0.76\text{W} \tag{13}$$

Loss calculations associated with Coss are somewhat nebulous, as this capacitance is quite non-linear, decreasing with higher Vds, and for this design is estimated to be 0.2 W.

Capacitor requirements generally consist of calculating the maximum RMS current, the minimum capacitance necessary to obtain the desired ripple voltage and holdup for transients. Output capacitance and I_{OUTRMS} are calculated as:

$$Coutmin = \frac{Ioutmax*\text{dmax}}{fsw*Vripout} = \frac{5\text{A}*0.5}{250\text{KHz}*0.12\text{V}} = 83\text{uF} \tag{14}$$

$$Ioutrms = \text{Ioutmax} * \sqrt{\frac{dmax}{1-dmax}} = 5\text{A} * \sqrt{\frac{0.5}{1-0.5}} = 5\text{A} \tag{15}$$

Ceramic capacitors alone are suitable, but seven would be required to realize 83 µF after DC-biasing effects. Therefore, I only chose enough to handle the RMS current and followed with an LC filter to reduce output ripple voltage, as well as improve load transients. If large load transients exist, additional output capacitance may be required to reduce voltage droop.

The input capacitance is equal to:

$$Cinmin = \frac{Ipri_{pk}*\text{dmax}}{2*fsw*Vinrip} = \frac{3.14\text{A}*0.5}{2*250\text{KHz}*1.5\text{V}} = 2\text{uF} \tag{16}$$

where V_{INRIP} is the allowable input ripple voltage and is set to three percent of V_{IN} or ~1.5 V.

Again, you must consider the capacitance-robbing DC-bias effect. The RMS current is approximately:

$$Iinrms = \frac{Ioutmax}{Nps} * \sqrt{\frac{dmax}{1-dmax}} = \frac{5\text{A}}{4} * \sqrt{\frac{0.5}{1-0.5}} = 1.25\text{A} \tag{17}$$

Figure 2 shows the prototype converter's efficiency while **Figure 3** shows the flyback evaluation board.

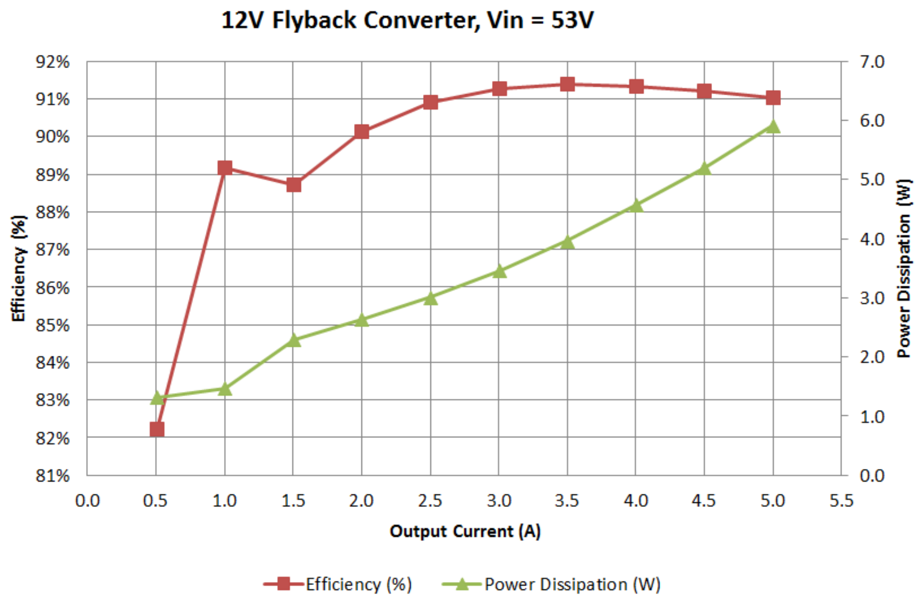

Figure 2: Converter efficiency and losses dictate package selection and thermal requirements.

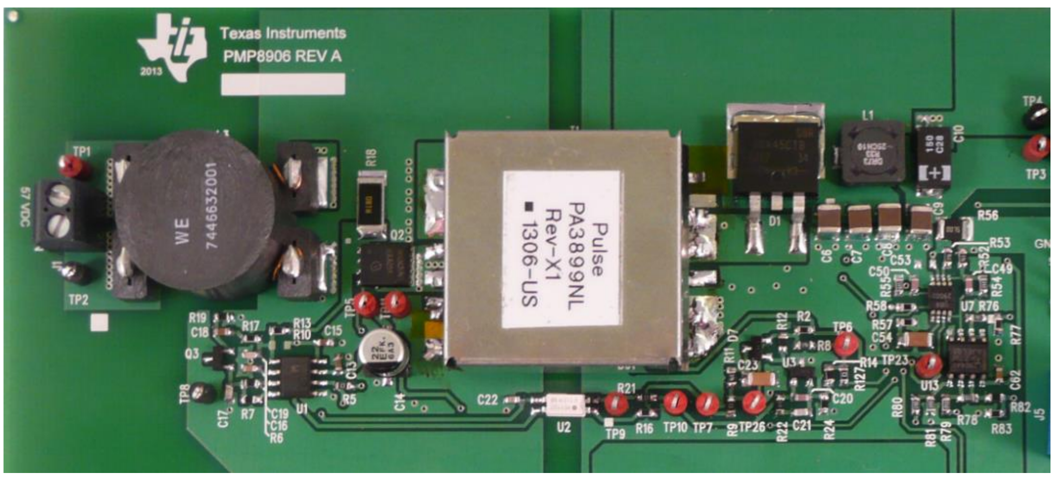

Figure 3: 60W flyback evaluation hardware measures 100mm x 35mm.

Aid in selecting the proper compensation component values can be investigated here: [Compensating isolated power supplies]

This design example covers basic component calculations of a functional CCM flyback design. However, initial estimates often make it necessary to iterate the calculations in order to fine tune it. Still, more detail work is often necessary in areas such as transformer design and control-loop stabilization in order to obtain a well-working, optimized flyback.

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