UCC28782 High Frequency Active Clamp Flyback Controller

1 Features

- Adaptive control for fast zero voltage switching (ZVS) tracking and dead time optimization
- Dynamic bias power management for digital isolator and GaN driver
- Integrated switching bias regulator for wide output voltage range with one auxiliary winding
- Low-side PWM driver with dedicated ground return for high-frequency switching
- Low-EMI frequency dithering without transient response and audible noise tradeoff
- Programmable adaptive burst mode with internal compensation and audible noise mitigation
- Programmable standby mode and active X-capacitor discharge for low standby power
- Auto-balancing clamping capacitor voltage and CCM avoidance control for low snubber loss
- Brownout detection without direct line sensing
- Multi-function FLT pin for line over-voltage, NTC thermistor interface, or external enable function
- Over-temperature, over-voltage, output short-circuit, over-current, over-power, and pin-fault protections
- Auto-recovery and group latch fault options with fast latch reset capability

2 Applications

- High-density AC-to-DC adapters for laptop, tablet, TV, set-top box, and printer
- USB power delivery, and fast phone chargers
- AC-to-DC or DC-to-DC auxiliary power supply
- Audio soundbars, and smart speakers
- Battery chargers for power tools and E-bikes
- USB wall outlets
- LED lighting

3 Description

UCC28782 enables high-density active-clamp flyback (ACF) converters that comply with stringent global efficiency standards. ZVS is achieved over a wide operating range with advanced auto-tuning and dead-time control. The adaptive multimode control maintains high efficiency while mitigating audible noise and reducing output ripple in burst mode. User programmable control modes allow performance to be optimized for different switching frequency ranges and power levels.

UCC28782 reduces the passive component size and external component count by variable switching frequency capability up to 1.5 MHz, integrated switching regulator for simple controller biasing, internal loop compensation for stabilizing burst mode, and unique frequency dithering for spreading the EMI spectrum. The internal low-side driver enhances high frequency switching, and the built-in power management functions reduce the driver loss.

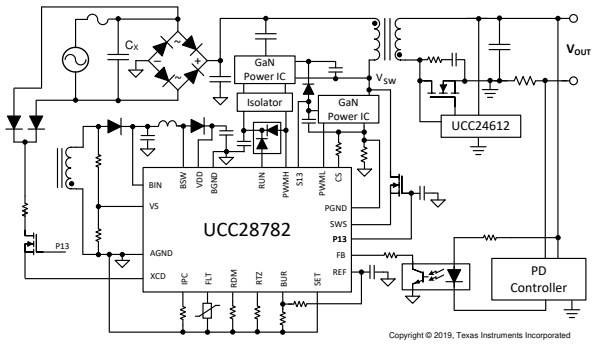
UCC28782 works with VDS-sensing synchronous rectifier (SR) controllers, such as UCC24612, to achieve higher efficiency. The robust switching control mitigates the excessive SR voltage stress caused by the over-charged clamping capacitor voltage or CCM, so the power loss of SR snubber can be reduced.

Device Information(1)

ORDERABLE PART NUMBER	PACKAGE	BODY SIZE	PROTECTION OPTIONS
UCC28782	WQFN-24	4.00 mm × 4.00 mm	All system faults in auto-recovery
UCC28782L	WQFN-24	4.00 mm × 4.00 mm	OTP, OVP, SCP, OCP, and OPP are latch-off faults

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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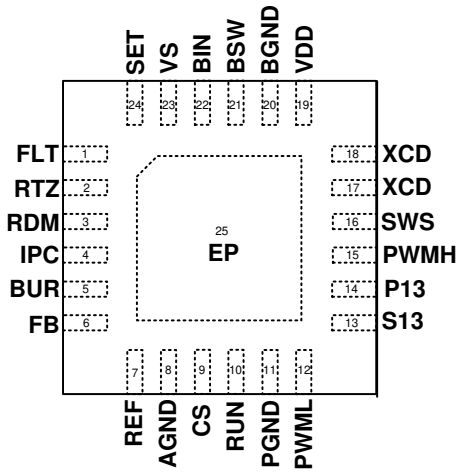
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2020	*	Product Preview release.

5 Pin Configuration and Functions

RTW Package
24-Pin WQFN
Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	PIN#		
FLT	1	I	The controller enters into fault state if the FLT-pin voltage is pulled above 4.5 V or below 0.5 V. A 50-µA current source directly interfaces with an external NTC (negative temperature coefficient) thermistor to AGND pin for remote temperature sensing. 47-µs fault delay allows a filter capacitor to be placed on the FLT pin without false triggering the 0.5-V OTP fault when the controller enters into a run state from a wait state. Pulling this pin low shuts down PWM action and initiates a fault response. Alternatively, a high-resistance voltage divider can be used to sense the bulk input capacitor voltage for line OVP detection, and a 700-µs fault delay helps to prevent false triggering the 4.5-V line OVP by the short-duration bulk capacitor voltage overshoot during line surge and ESD strike events. When FLT pin voltage is used for line OVP detection, the external OTP can be implemented on CS pin.
RTZ	2	I	A resistor between this pin and AGND pin programs an adaptive delay for transiting to zero voltage from the turn-off edge of the high-side clamp switch to the turn-on edge of the low-side switch.
RDM	3	I	A resistor between this pin and AGND pin programs a synthesized demagnetization time used to control the on-time of the high-side switch to achieve zero voltage switching on the low-side switch. The controller applies a voltage on this pin that varies with the output voltage derived from the VS pin signal.
IPC	4	I	A 50-µA current source directly interfaces with a resistor (R_{IPC}) to AGND pin to program the peak current level at very light load, so burst frequency can be further reduced for low tiny power and standby power. If the IPC pin is connected to AGND without R_{IPC}, the peak current level in very light load is set to a minimum level for the output ripple or audible noise sensitive designs. R_{IPC} can also be connected between this pin and the CS pin or IPC pin can be directly connected to CS pin, so the 50-µA IPC current can create an output voltage dependent offset voltage on the CS pin for reducing output ripple in adaptive burst mode and improving light-load efficiency at lower output voltage level of a wide output voltage range design.
BUR	5	I	This pin is used to program the burst threshold of the converter at light load. A resistive divider between REF pin and AGND pin is used to set a voltage at this pin to determine the peak current level when the converter enters the adaptive burst mode (ABM). In addition, the Thevenin resistance on BUR pin (equivalent resistance of the divider resistors in parallel) is used to set an offset voltage for smooth mode transition. A 2.7-µA pull up current increases the peak current level when the converter enters the low power mode (LPM) from ABM. A 5-µA pull down current reduces the peak current level when the converter enters into heavy load mode (adaptive amplitude modulation, AAM) from ABM.
FB	6	I	The feedback current signal to close the converter regulation loop is coupled to this pin. This pin presents a 4-V output that is designed to have 0-µA to 75-µA current pulled out of the pin corresponding to the converter operating from full-power to zero-power conditions. A 220-pF filter capacitor between FB pin and REF pin is recommended to desensitize the feedback signal from noise interference.
REF	7	O	5V reference output that requires a 0.22-µF ceramic bypass capacitor to AGND pin. This reference is used to power internal circuits and can supply a limited external load current.
AGND	8	G	Analog ground. Return all analog control signals to this ground.
CS	9	I	This is the current sense input pin. This pin couples to a current-sense resistor through a line-compensation resistor to control the peak primary current in each switching cycle. A current source from this pin is proportional to the converter's input voltage, creates an offset voltage across the line-compensation resistor to program an OPP level at high line. The CS pin also provides an alternative OTP function, when FLT pin is used for line OVP. A small-signal diode in series with a NTC resistor is connected between PWMH pin and CS pin to form the OTP detection. When PWMH is high, the NTC resistor and the line-compensation resistor become a resistor divider from 5 V and creates a temperature dependent voltage on CS pin. When CS pin voltage is higher than 1.2 V in PWMH on state for 2 consecutive cycles, the OTP fault on CS pin is triggered.
RUN	10	O	This output pin is high when the controller is in a run state. This output is low during start-up, wait, and fault states. A 2.2-µs timer delays the initiation of PWML switching after this pin has gone high and S13-pin voltage is above the 10-V power good threshold. The pull up driving capability of both RUN and PWMH pins allow the bias power management to a digital isolator and GaN power IC through a common-cathode small-signal diode, so the power consumption can be reduced in wait state.
PGND	11	G	Low-side ground return of the PWML driver. The internal level shifter allows the common return impedance to be eliminated, and its impact to higher frequency operation. For GaN-based gate-injection transistor (GIT), this pin can be directly connected to the separate source pin of a GIT GaN, which enhances the turn-off speed and decouples the additional voltage spike on the current-sense resistor and layout parasitic to the gate-to-source voltage. For GaN power IC with integrated driver, this pin can also be connected to its local ground, so an external filter between the controller PWML output and GaN PWM input can be eliminated.
PWML	12	O	Low-side switch gate driver output. The high-current capability (-0.5A/+2A) of PWML enables to drive a Silicon power MOSFET with higher capacitive loading, a GIT GaN with continuous on-state current, or a GaN power IC with logic input. The maximum voltage level of PWML is clamped to the P13 pin voltage.

(1) I = Input, O = Output, P = Power, G = Ground

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	PIN#		
S13	13	O	S13 is coupled to P13 through an internal 2-Ω switch controlled by the RUN pin. When RUN is high, the S13 decoupling capacitor is charged up to 13 V by an internal soft-start current limiter. The S13 pin voltage needs to increase above 10 V to initiate PWML switching. When RUN is low, S13 is discharged by the S13 pin loading, such as GaN power IC. The power-on delay of the GaN power IC on S13 must be less than 2 µs to be responsive to PWML. If not, VDD or P13 is more suitable, but the wait-state power consumption will be compromised. A 22-nF ceramic capacitor between S13 and AGND pins is recommended.
P13	14	O	P13 is a regulated 13-V output voltage derived from V_{VDD}. During V_{VDD} startup, P13 pin is connected with VDD pin internally, so the external high-voltage depletion MOSFET, such as BSS126, can provide the controlled startup current to charge a VDD capacitor. After the initial startup, P13 recovers back to 13-V regulation. A 1-µF ceramic bypass capacitor is required from P13 to AGND.
PWMH	15	O	PWM output signal used to control the gate of the high-side clamp switch through an external high-voltage gate driver. The weak driving capability is designed to bias the isolator through a small-signal diode or can also transmit the signal to high-side driving circuitry through a pulse transformer. The maximum voltage level of PWMH is clamped to 5-V REF level.
SWS	16	I	This sensing input is used to monitor the switch-node voltage as it nears zero volts in normal operation for ZVS auto-tuning. The source of a high-voltage depletion mode MOSFET, such as BSS126, is coupled to this pin through a current limit resistor, so only useful switching characteristic below around 15 V is monitored. During start-up, this pin is connected to the VDD pin internally to allow BSS126 to provide start-up current. The 499-Ω current limit resistor and a back-to-back TVS across BSS126 gate and source should be added to protect the gate-to-source voltage from the potential abnormal voltage stress. The clamping voltage of TVS should be less than BSS126 voltage rating but stay off below 17.5 V. Moreover, the 499-Ω resistor and a 22-pF ceramic capacitor between this pin and bulk input capacitor ground form a small sensing delay to help the internal detection circuit to identify the ZVS characteristic correctly.
XCD	17, 18	I	X-cap discharge input pins with 2-mA maximum discharge current capability. Line zero-crossing (LZC) on XCD pins is used to detect AC line presence. When LZC is missing over 84-ms timeout period, the discharge current is enabled for a maximum period of 300 ms followed by a 700-ms no current blanking time. When AC line recovers and LZC is detected again, UCC28782L can reset the latch fault state immediately and will attempt to restart without waiting for fully discharging of bulk input capacitor. For UCC28782, if the controller is in 1.5-s auto-recovery fault state, LZC can reset the timer and speed up the restart attempt. The two redundant XCD pins help to provide the X-cap discharge function even when one pin is in fail-open condition. To form the discharge path, the anode of two high-voltage diode rectifiers is connected to each X-cap terminal, the two diode cathodes are connected together to a 27-kΩ current limit resistor, and BSS126 drain-to-source couples the resistor to XCD pins. If x-cap discharge function is not needed, XCD pins are connected to AGND pin to disable the function.
VDD	19	P	Controller bias power input. VDD pin is also the integrated boost converter output. A hold-up capacitor to BGND pin is required. For fixed-output applications where the boost converter is optional, VDD pin can directly connect to the rectified primary-side auxiliary winding voltage, so the boost-converter components can be eliminated.
BGND	20	G	Boost converter return pin connected to the source terminal of internal 30-V 0.9-Ω boost switch. The separate ground return simplifies PCB layout design to minimize the high di/dt switching loop along with the boost diode and VDD capacitor, so the noise-coupling effect to other sensitive nodes can be mitigated.
BSW	21	I	Boost converter switch node, connected to the drain terminal of internal 30-V 0.9-Ω boost switch. For wide output voltage application, boost inductor and boost diode anode are connected to this pin. For fixed output voltage design, BIN and BSW pins should be connected to BGND pin, so the boost-converter control is disabled in order to lower the controller run current. A 22-µH chip inductor with higher than 0.4-A saturation current capability is recommended for boost inductor selection. If the maximum VDD-pin voltage is less than 30V, a 30-V rated Schottky diode not smaller than SOD-323 package is recommended as boost diode, so the BSW voltage stress from the diode reverse recovery effect can be avoided when the converter operates in short-duration CCM.
BIN	22	I	Boost converter input pin. For wide output voltage application, when the boost converter is needed to improve the converter efficiency, BIN pin is connected to the rectified auxiliary winding voltage. A 33 µF energy storage capacitor in parallel with 10 µF ceramic capacitor is recommended. The 33-µF cap can be placed close to the auxiliary rectification diode and the auxiliary winding ground terminal to minimize the rectification switching loop. The 10-µF cap can be placed close to the boost inductor and BGND pin to minimize the boost input switching loop. If the boost converter is not needed, BIN and BSW should be connected to BGND pin.
VS	23	I	This voltage sensing input pin is coupled to the auxiliary winding of the converter's transformer via a resistor divider. The pin and the associated external resistors are used to monitor the output and input voltages of the converter at different moments in each switching cycle.
SET	24	I	This pin is used to configure the controller to be optimized for Gallium Nitride (GaN) power FETs or Silicon (Si) power FETs on the primary side. Depending on the setting, it will optimize parameters of the ZVS control loop, dead-time adjustment, and protection features. When pulled high to REF pin, it is optimized for Si FETs. When pulled low to AGND, it is optimized for GaN FETs.
EP	25	G	Thermal pad connected only to AGND.

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