Problem with Texas Instruments Ucc25600 resonant mode controller at around 150 to 350KHz operation

Re: TI document SLUS846C UCC25600 June 2015

Our application for the variable frequency controller is a circuit converting 360V to 12V at 17A. the frequency range is 150Khz at max load to 350KHz at very light load and burst mode when off load. The converter is required to have a significant holdup period of 250ms in case of loss of input, and the frequency goes down to about 60KHz minimum during the hold up.

The first problem is that for the IC to function correctly as described on the datasheet the soft start would be expected to start the switch drive at 350KHz where the converter through power is low and gradually reduce the switching frequency to avoid a current surge. At switch on the output voltage will be below the regulation point (zero) and the control loop (as described in typical application on datasheet) will demand maximum power. Fig 1 shows the characterisation of a sample of the IC, it can be seen that the soft start function does not start at 350KHz, it starts at around 150KHz. This means that the soft start simply does not work for our application. The resonant circuit is not much different in our application to the example application on the datasheet where the resonant frequency was specified as 130KHz. With 130KHz resonant frequency you would not want the switching to start at 150KHz.

Fig 1

A second problem with the controller is when the RT control is set for minimum through power (maximum frequency and burst mode) there is a different problem with the soft start function.

Fig 2 shows the IC operating through a soft start ramp with the RT control set for minimum through power. Trace 1 (blue) shows the switch drive output, trace 3 (purple) shows the soft start ramp.

It does not make any difference exactly what the RT current is, it can be set for just above 350KHz, or significantly above 350KHz, the IC behaves as Fig 2.

The datasheet explains that the IC is intended to go into burst mode to allow voltage regulation off load where the output voltage may exceed the intended set point at 350KHz switching. It can be seen in Fig 2 that although the RT control is demanding burst mode, for the lower part of the soft start ramp the burst mode is disabled and the output continually switches (at about 350KHz).

This means that if the voltage exceeds to set point during the early part of the soft start ramp, the control lop will not enter burst mode to keep the voltage on regulation.

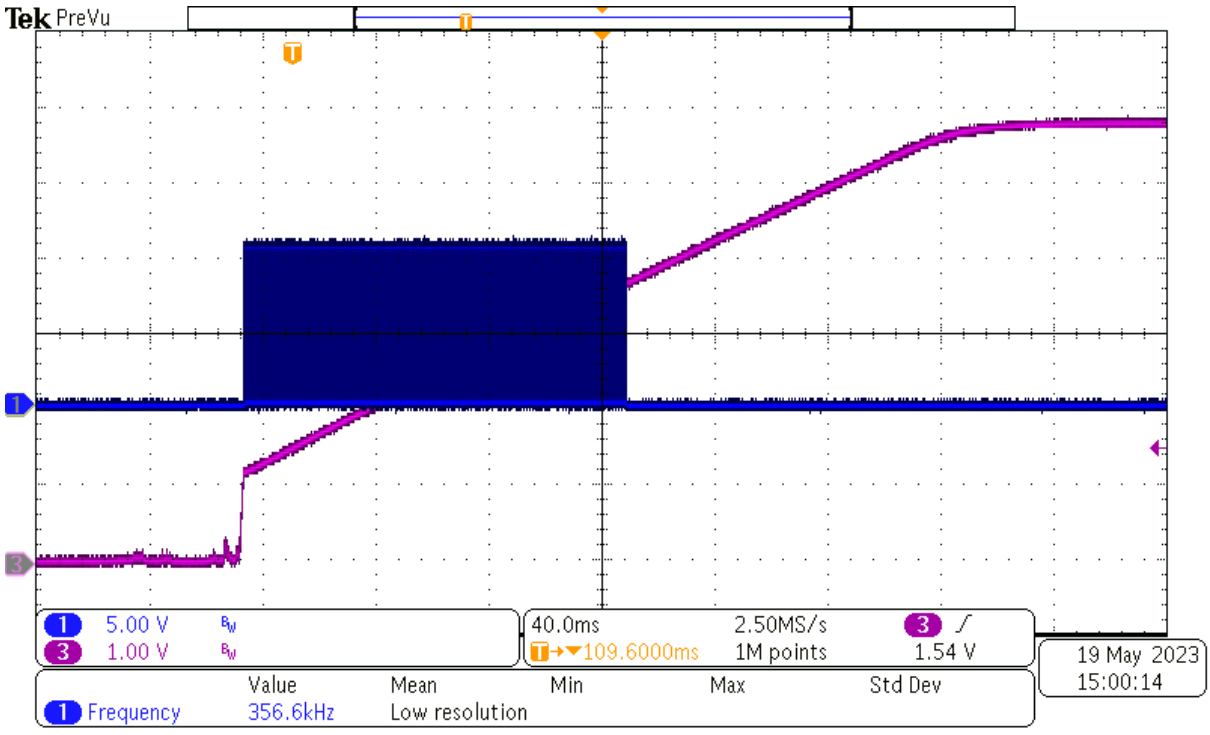


Fig 2

Fig 3 shows the effect of the second problem in a PSU. The blue trace is the control loop error function, the Yellow trace is the output voltage, the purple trace is the soft start voltage.

At switch on the start-up ramp is controlled by a circuit external to the ucc25600 because of the controller would start at a frequency which would cause a current limit condition. It can be seen that the output voltage overshoots the 12V set point and stays there for approximately 250ms because the controller has disabled the burst mode during the early SS period, and there is no load on the 12V. The error function is demanding burst mode, but this has no effect. When the SS voltage

reaches approx 3.5V after approx. 250 ms of 12V being present the controller IC changes mode to allow burst mode and the voltage then regulates at 12V. It can be seen from the change in error function voltage after the SS ramp goes through the ~3.5V threshold that there is plenty of control capability, but the controller will not allow burst mode below a SS voltage of ~3.5V.

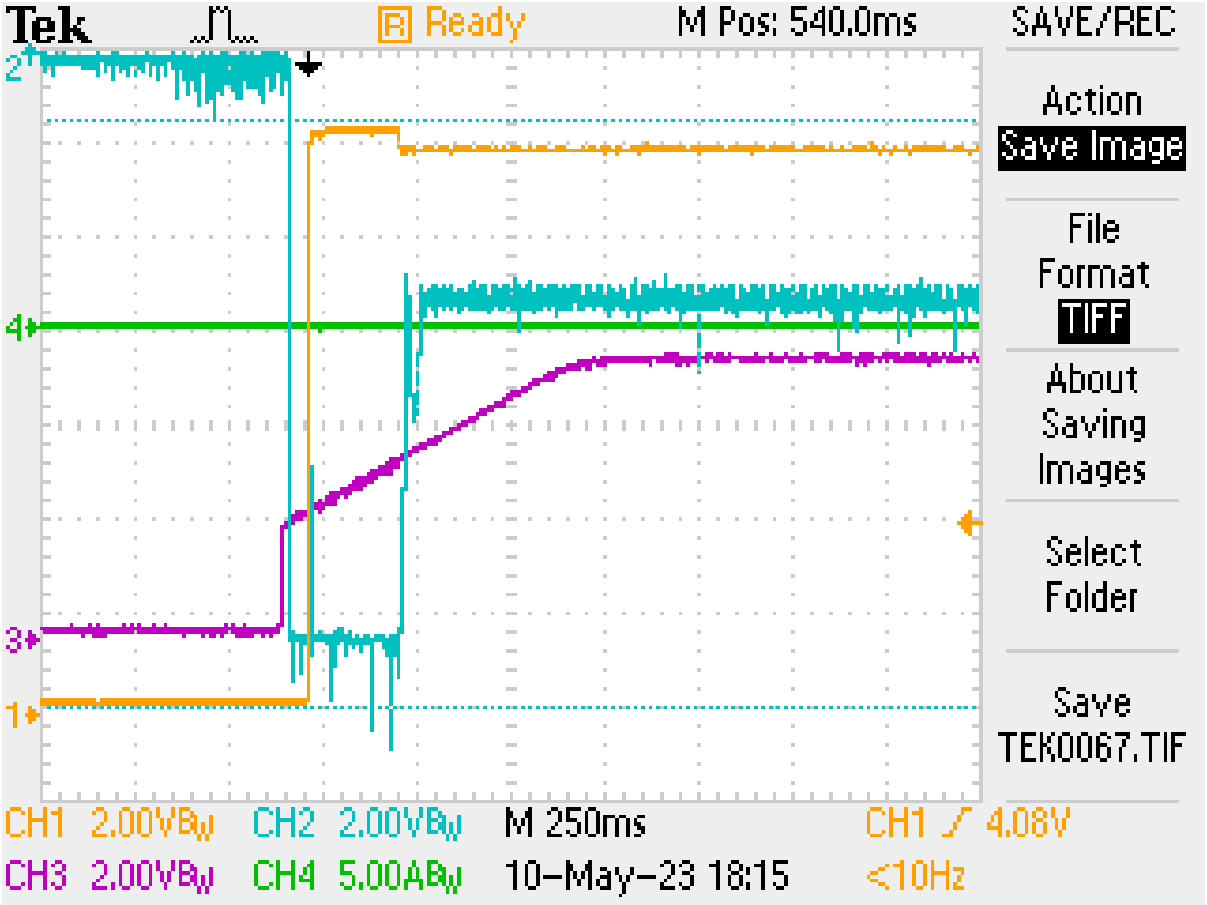
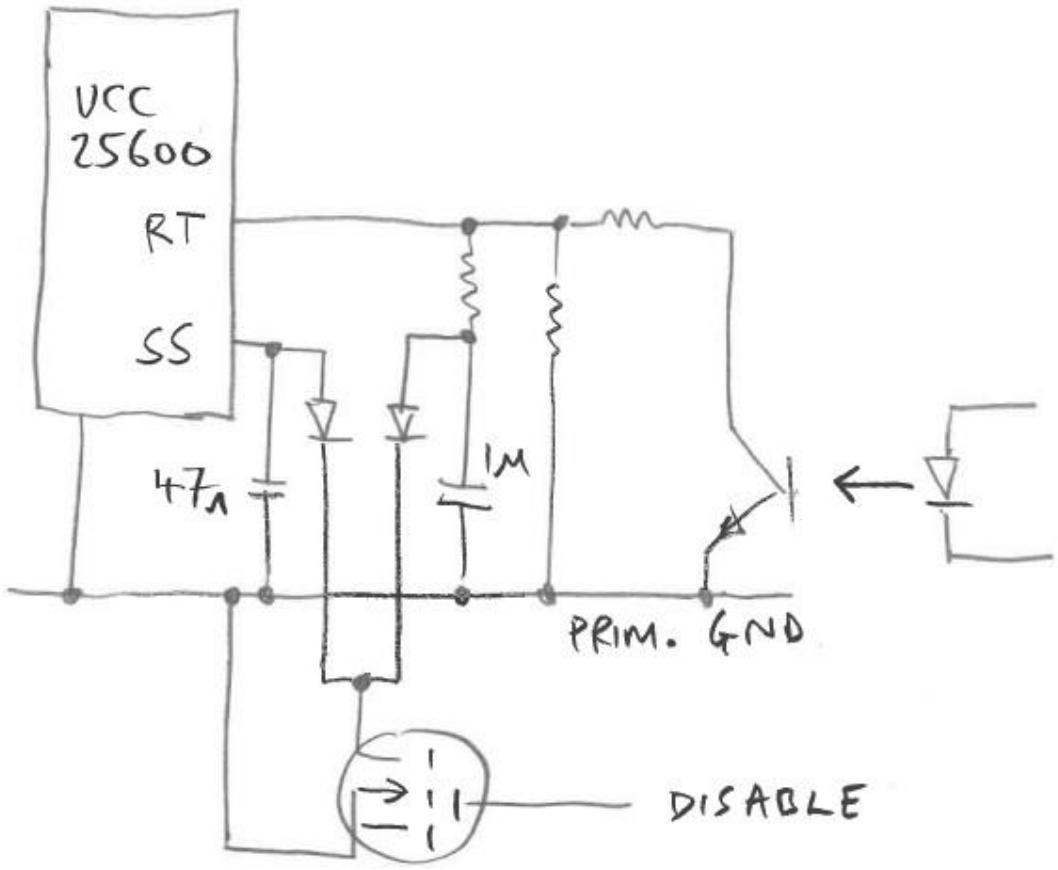


Fig 3

The datasheet does have an equation to represent the IC transfer function eq. (2) page 11, but this does not show the behaviour that we see.

Fig 4 shows a circuit we have used that allows the PSU to start with a normal soft start ramp. When the IC is disabled (which is the pre-start condition) the SS capacitor is discharged and also an additional current is passed down the RT control pin from a slow control circuit which has a time constant longer than the SS time constant. At start up the SS pin is released an this completes the UCC256 ramp while the RT pin is held at 350KHz. The SS pin completes the SS ramp before the output voltages reaches regulation point so there is no overshoot. The slow control on the RT pin provides the actual slow start ramp after the UCC 256 ramp has completed.



A circuit we have used to overcome the limitation of the IC

Fig 4