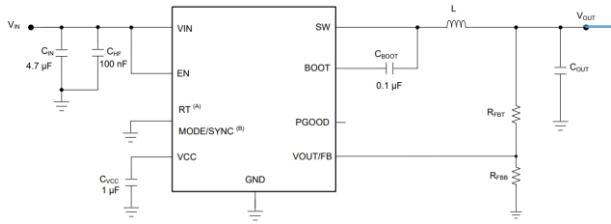
Part of the Power tree using cascaded TPS62441 with LMR43620MSC3RPERQ1

.

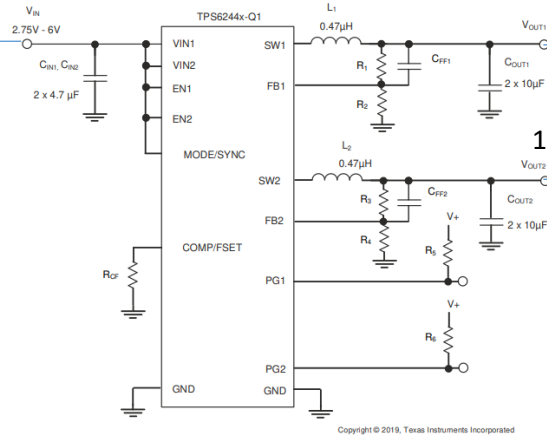
3.3V



LMR43620MSC3RPERQ1

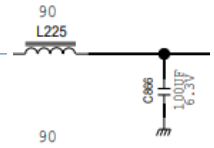
VIN = [5-17V]

OUT = 3.3V



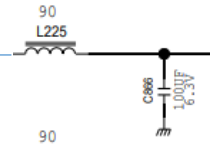
1.0V 0.25A typ.

1.3V 0.5A typ.



To load

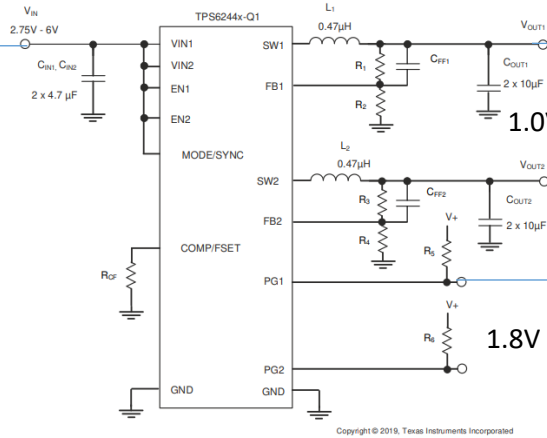
4x LC branch with 100µF (400µF)



To load

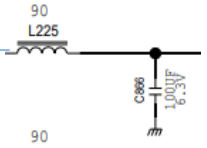
15x LC branch with 100µF (1500µF)

TPS62441



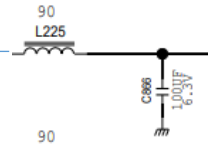
1.0V 0.05A typ.

1.8V 0.11A typ.



To load

2x LC branch with 100µF (200µF)



To load

7x LC branch with 100µF (700µF)

TPS62441

The TPS62441 will operate in two modes:

- Internal clock at 1.8MHz : 100K setting, MODE SYNC grounded (the device operates in PWM or PFM mode)

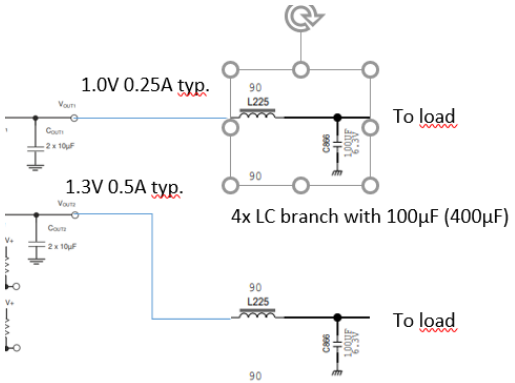
100 kΩ .. 45 kΩ	for best transient response (larger output capacitance) (comp setting 2) SSC disabled	1.8MHz (100 kΩ) ..4 MHz (45 kΩ) according to Equation 3	30 µF	18 µF	15 µF

- External CLOCK 2.5Mhz on MODE SYNC

Question 1 : stability of TPS62441 with output capacitor larger than 200µF.

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1, up to the maximum of 200-µF effective capacitance in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

Does the TPS62441 will be steady with multiple LC branches as below?



Question 2 : inrush current of TPS62441 with output capacitor larger than 200µF

The inrush current will be limited by the fixed soft start 1.1ms

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; the device is not in current limit	0.7	1.1	1.5	ms

With large output capacitors (up to 1500µF), this soft start is not enough. The high side current limit will be triggering and the time to reach final output voltage value will be increased. Does the TPS61441 can operate in such condition? Is there an internal max Ton delay protection witch can be triggering? (time out if the output voltage take too much time to reach the final value)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMH}	High-side FET switch current limit	DC value, for the TPS62441; V_{IN} = 3 V to 6 V	2.1	2.6	3.1	A

Question 3 : inrush current of TPS62441 sequencing

The EN1 and EN2 will be set high with a delay (power good sequencing).

Is there an individual soft start for each channel?

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; the device is not in current limit	0.7	1.1	1.5	ms