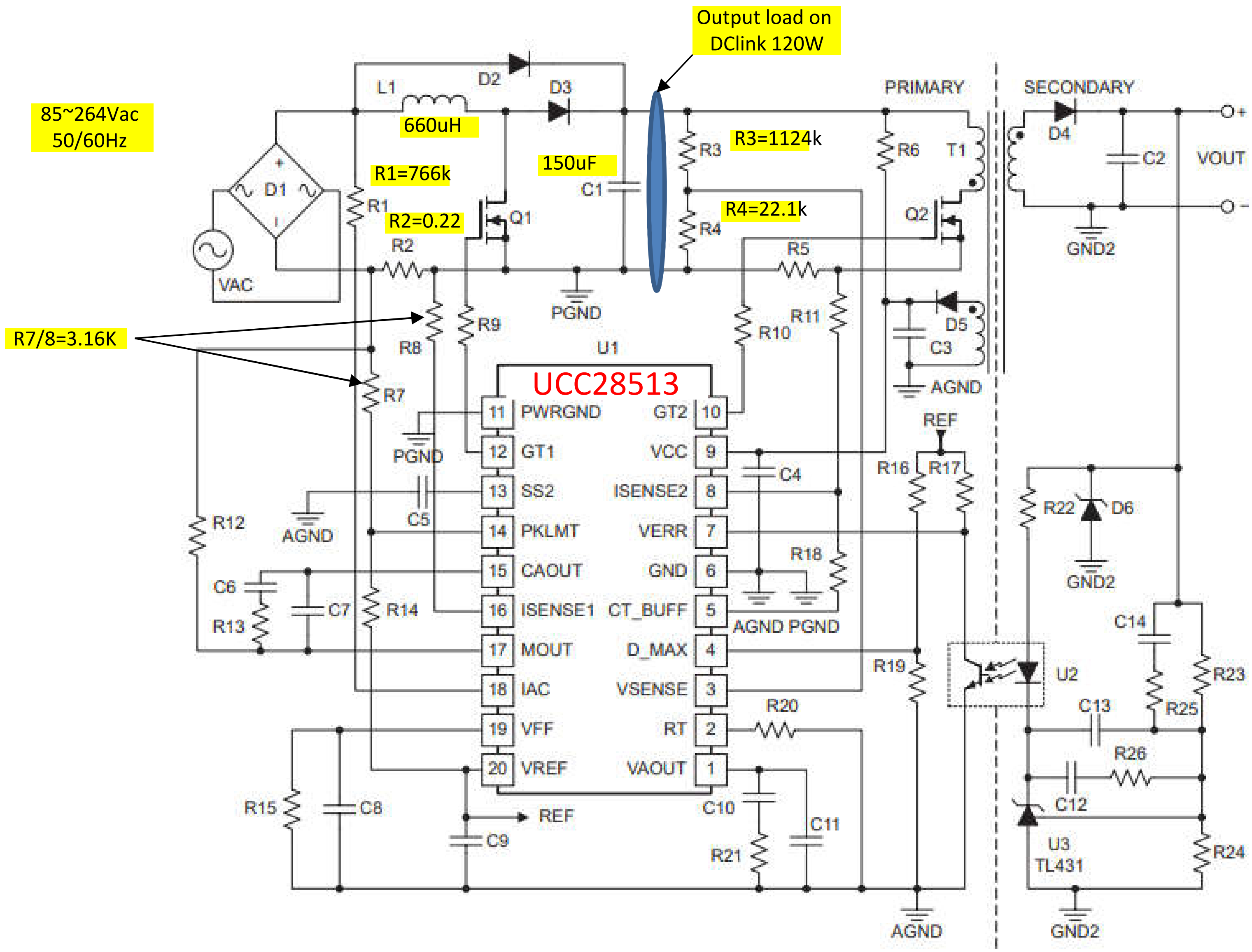
UCC28513 questions, Alex W., 11/17/2022

- The boost stage design is based on UCC28513. The PFC stage works well up to 200-220Vac input. Above this voltage range there are significant distortions at the points where sinusoidal input voltage reaches to its positive and negative peaks
- Output voltage is 385Vac
- Input voltage range is 85-264Vac; 50/60Hz
- The load on DC link output is 120W max
- Boost stage switching frequency is 277kHz
- Verified that the Vcc aux supply and Vref are stable
- Observed that the AC ripple on DC link goes up at around 200Vac but not sure it this is the reason or the result
- Observed that the duty cycle is about 70% at the peak sine wave at 85Vac but drops down to ~15% at the peaks of 220Vac at which point I start get distortions on the input current.
- The provided test results are at ~30W output power. It was observed that changing the load did not affect the behavior at around 220Vac.

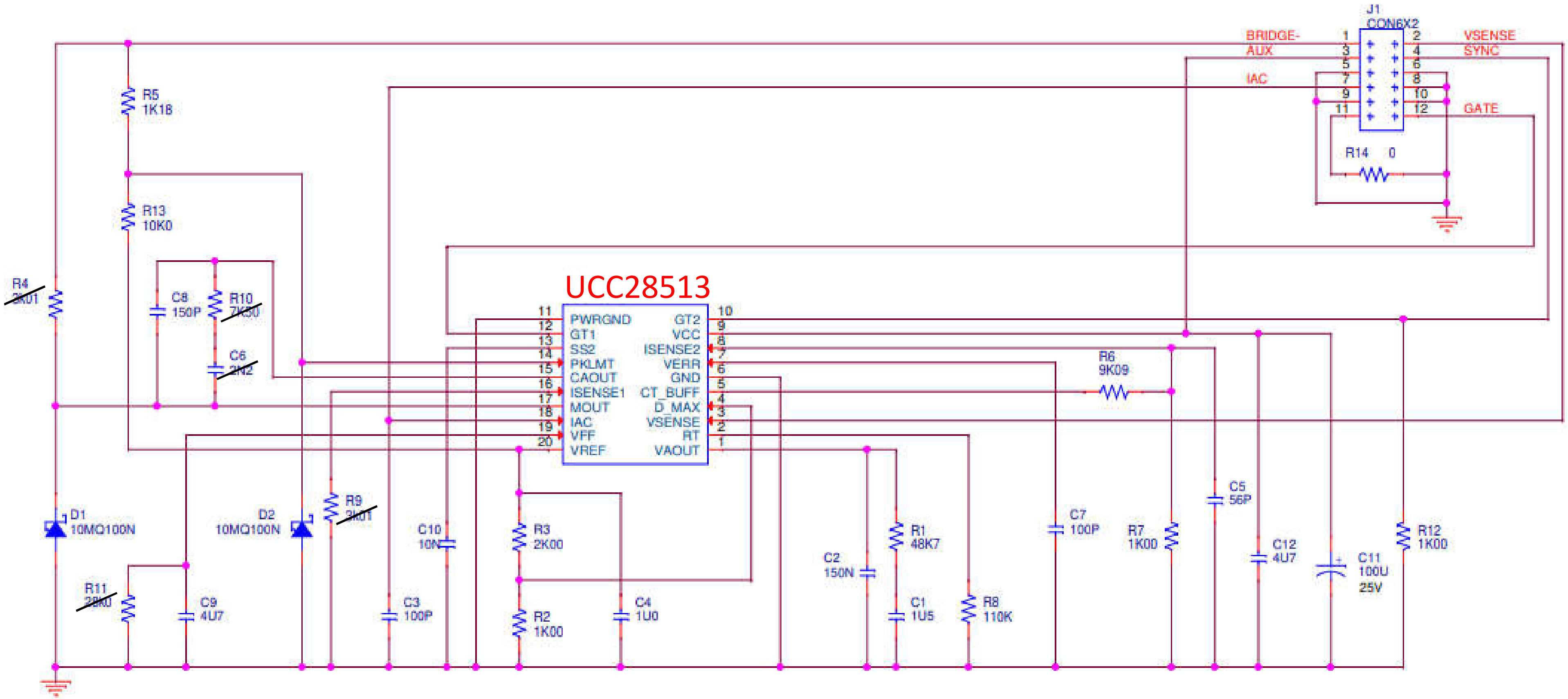
<u>Questions:</u>

1. Based on the design values, what could potentially cause the distortions at the peak of sine waves at and above ~ 200Vac?
2. Fig. 36 on data sheet talks about max capacitance vs min duty cycle. What capacitor is referred in Fig 36?

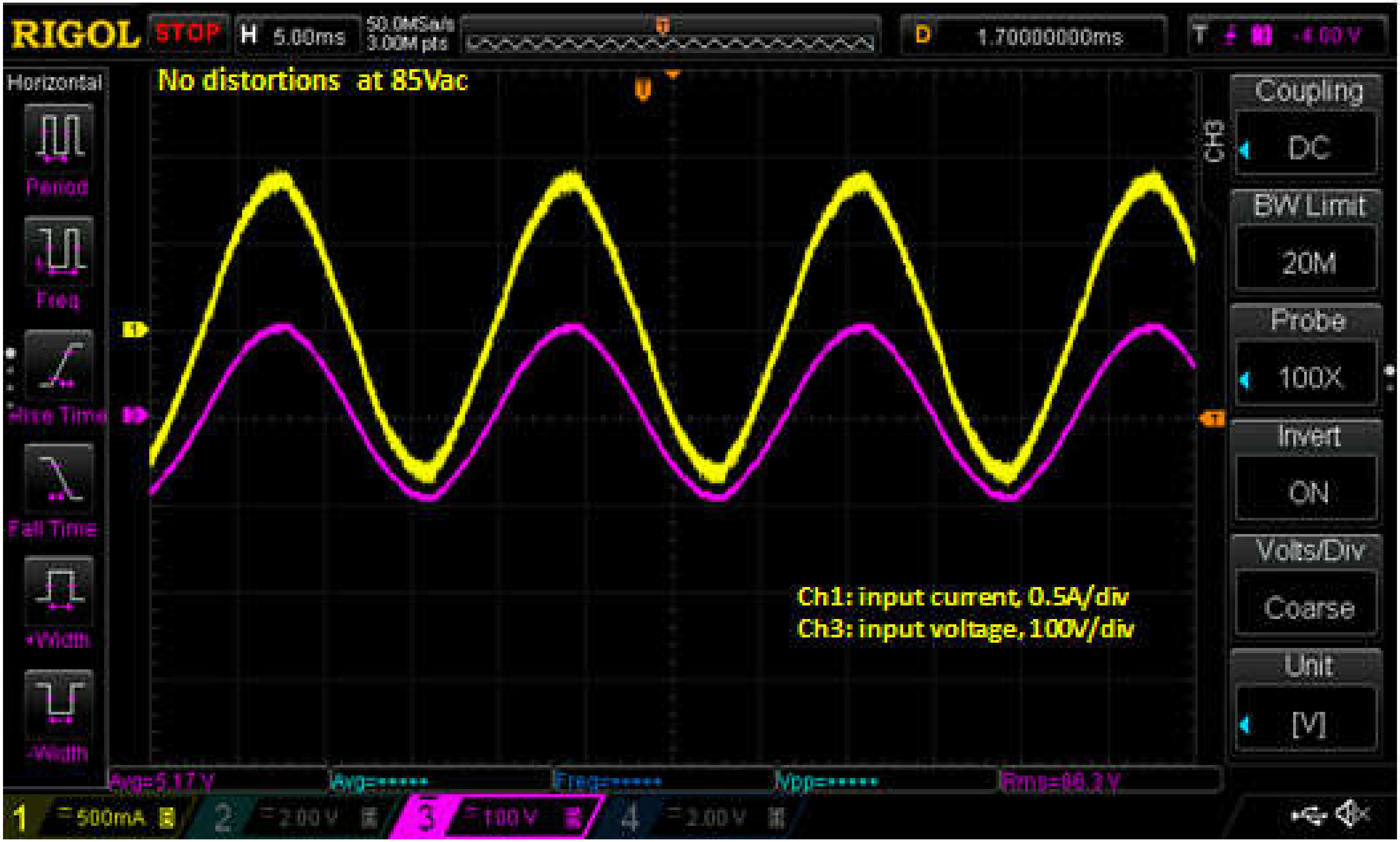


Output load on DClink 120W
85~264Vac 50/60Hz
660uH
R1=766k
R2=0.22
150uF
R3=1124k
R4=22.1k
R7/8=3.16K
UCC28513
L1
D1
D2
D3
D4
D5
D6
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
Q1
Q2
T1
U1
U2
U3
TL431
VAC
PGND
AGND
GND2
PRIMARY
SECONDARY
VOUT
REF
AGND PGND
11 PWRGND
12 GT1
13 SS2
14 PKLMT
15 CAOUT
16 ISENSE1
17 MOUT
18 IAC
19 VFF
20 VREF
GT2 10
VCC 9
ISENSE2 8
VERR 7
GND 6
CT_BUFF 5
D_MAX 4
VSENSE 3
RT 2
VAOUT 1

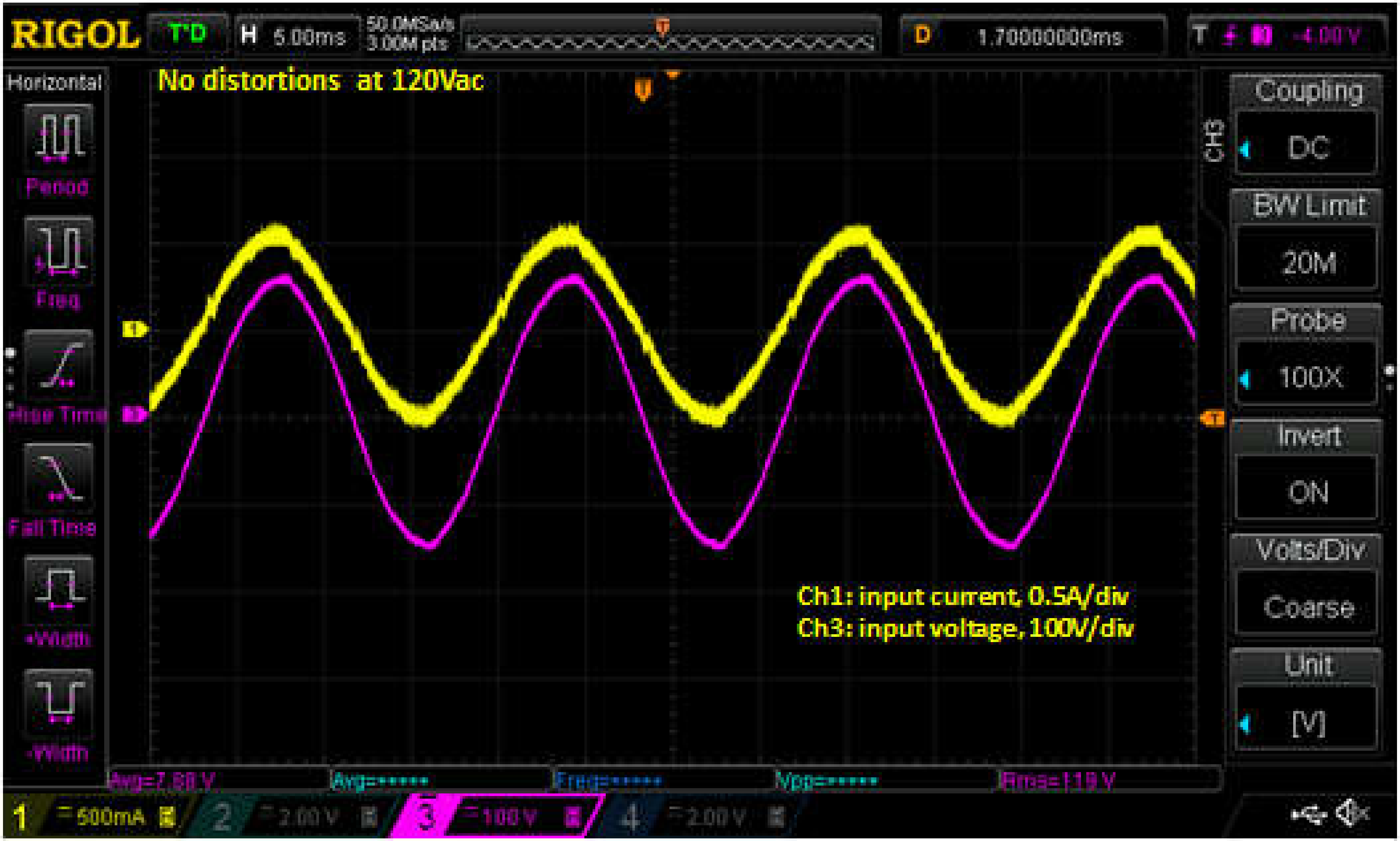
RefDes on data sheet	RefDes in design	values
R1	R47+R50	766K
R2	R43	0.22
R8/R12	R4/R9	3.16K
R3	R44+R49	1124K
R4	R60	22.1k
C1	C32	150uF
L1	L2	660uH
R13	R10	15.8K
C6	C6	680pF
C7	C8	150pF
R15	R11	30.1K
C8	C9	4.7uF
C10	C1	1.5uF
C11	C2	150nF
R21	R1	48.7K
R14	R13	10K
R7	R5	1.18K
C9	C4	1uF



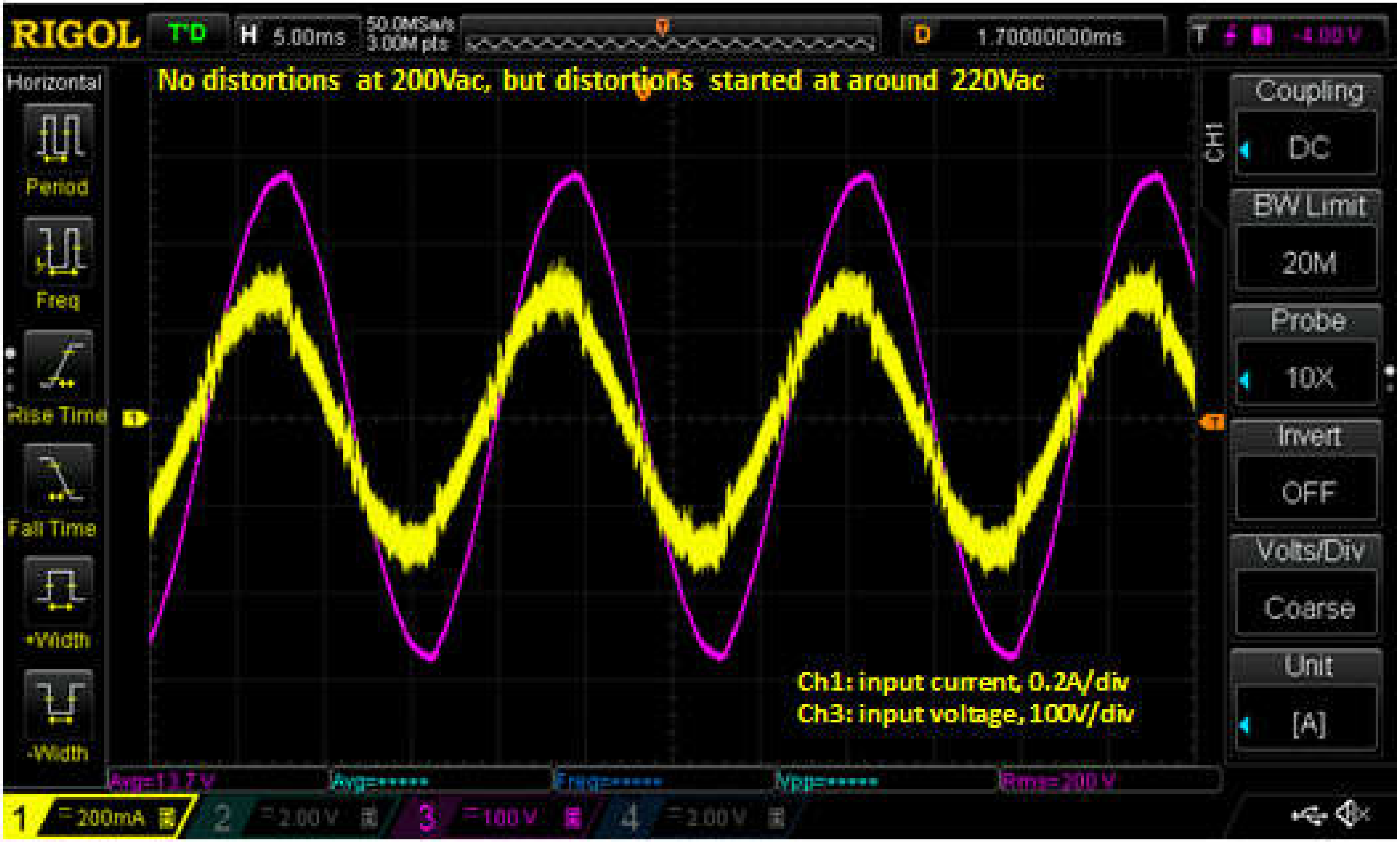
RefDes on data sheet	RefDes in design	values
R8/R12	R4/R9	3.16K
R13	R10	15.8K
C6	C6	680pF
R15	R11	30.1K

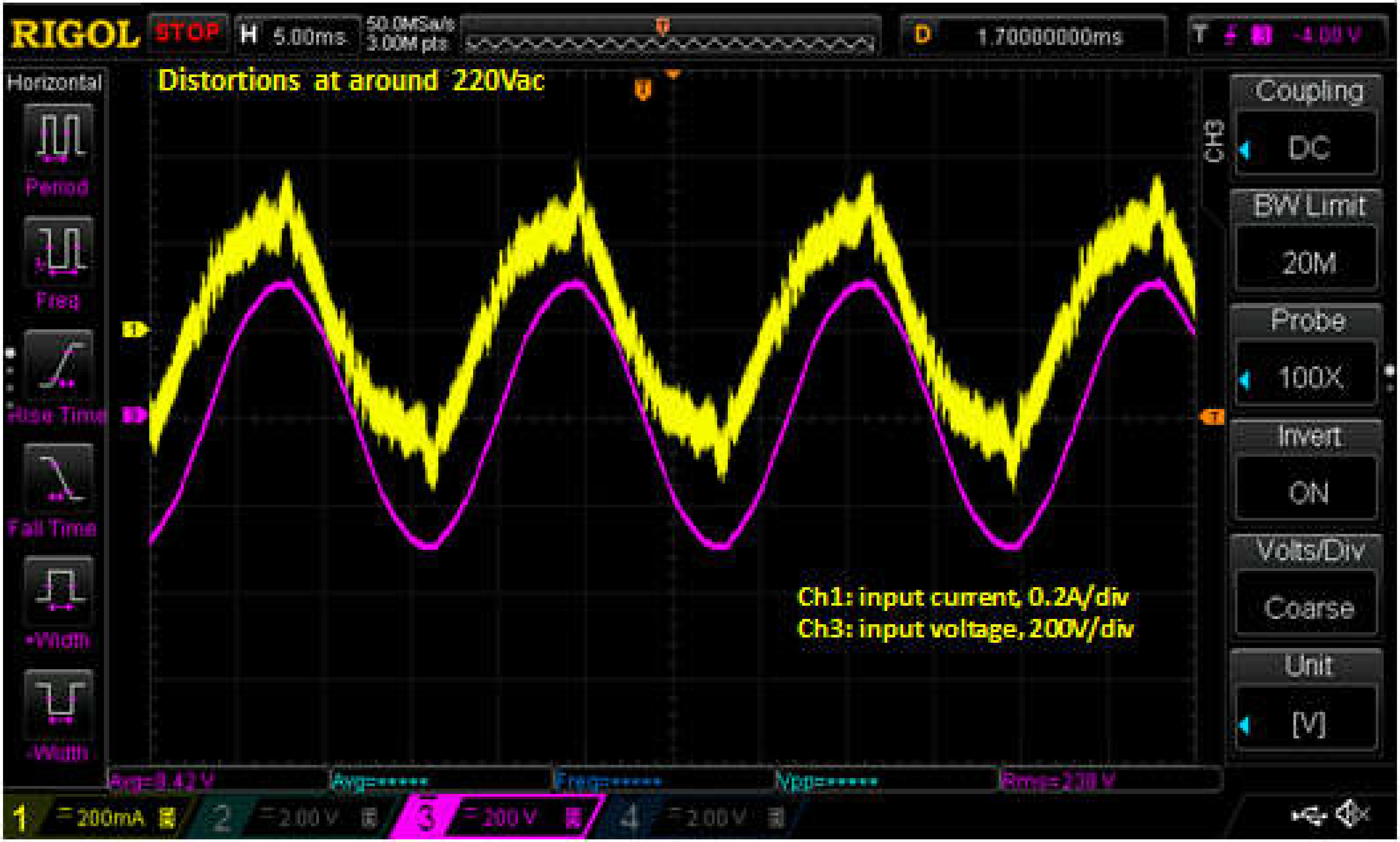


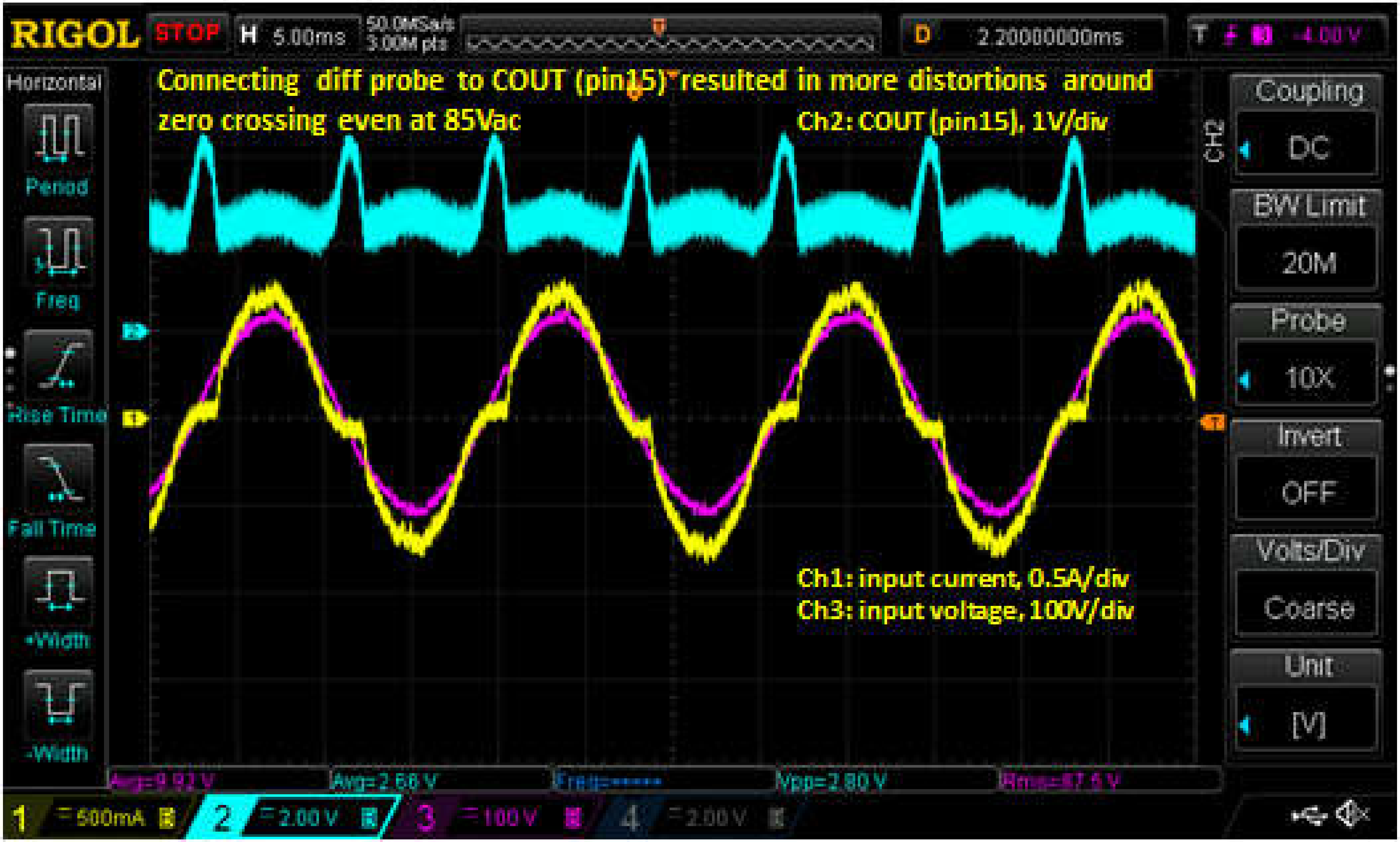
RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
No distortions at 85Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH3
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
500mA
100 V

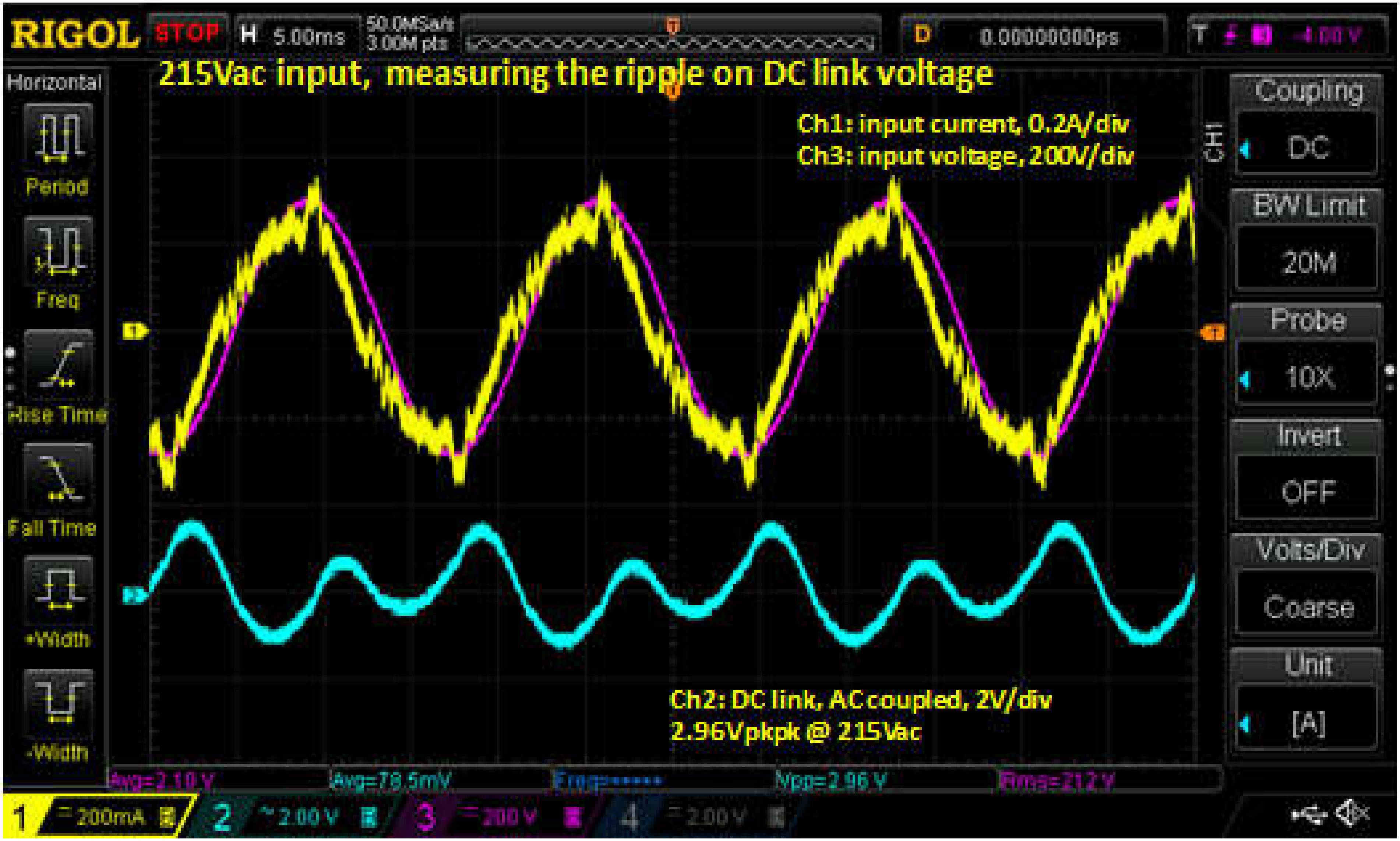

RIGOL
T'D
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
T -4.00 V
Horizontal
No distortions at 120Vac
Period
Freq
Rise Time
Fall Time
+Width
-Width
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
CH3
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
Avg=7.88 V
Avg=******
Freq=******
Vpp=******
Rms=119 V
1 500mA
2 2.00 V
3 100 V
4 2.00 V

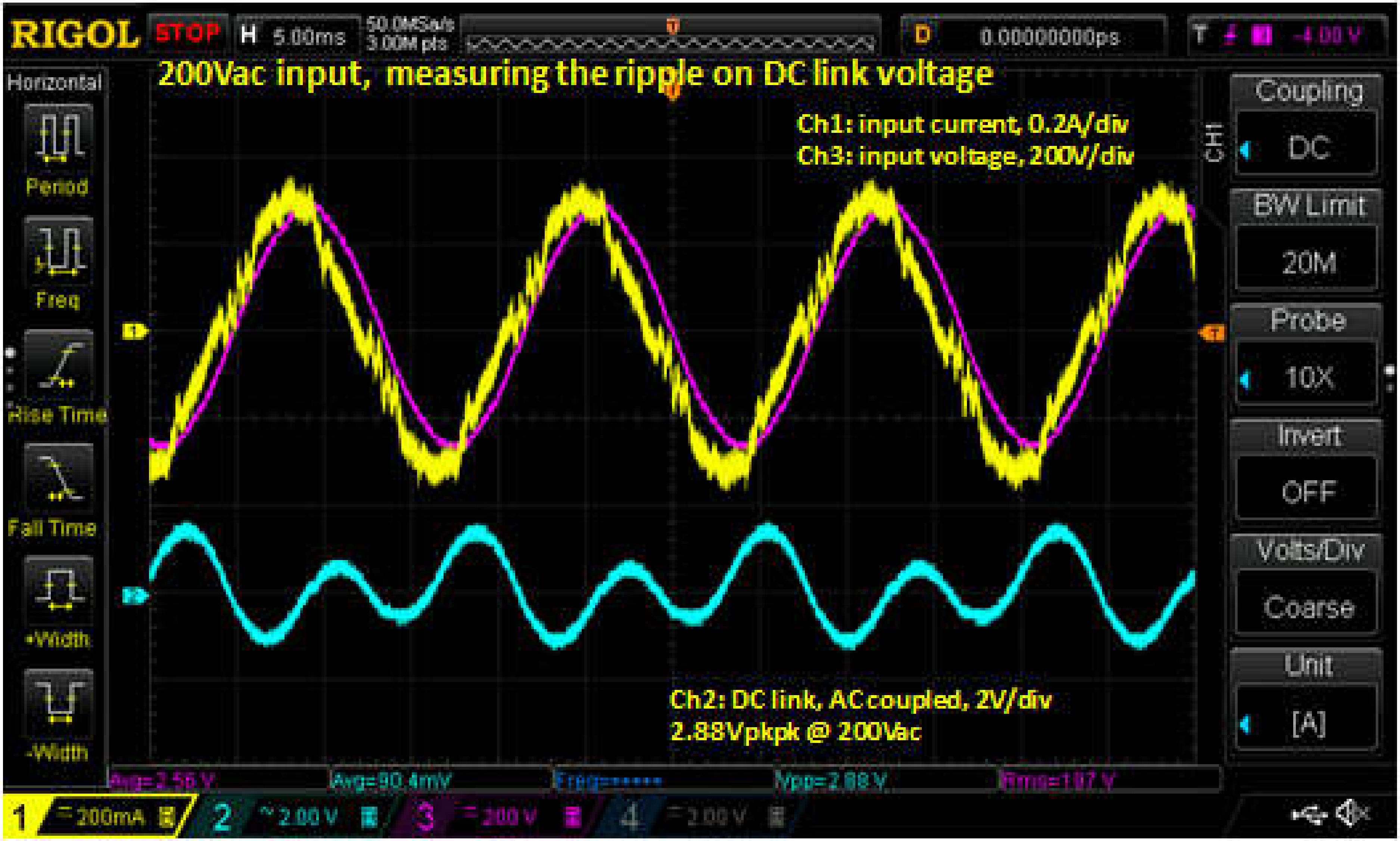
No distortions at 200Vac input, displacement between current and voltage is probably caused by the input capacitors on EMI filter




RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
Distortions at around 220Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
CH3
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
200mA
2.00 V
200 V
2.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 2.20000000ms
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
Connecting diff probe to COUT (pin15) resulted in more distortions around
zero crossing even at 85Vac
Ch2: COUT (pin15), 1V/div
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH2
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Avg=2.66 V
Vpp=2.80 V
1 500mA
2 2.00 V
3 100 V
4 2.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.00000000ps
215Vac input, measuring the ripple on DC link voltage
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Ch2: DC link, AC coupled, 2V/div
2.96Vpkpk @ 215Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Avg=2.10 V
Avg=78.5mV
Vpp=2.96 V
Rms=212 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V

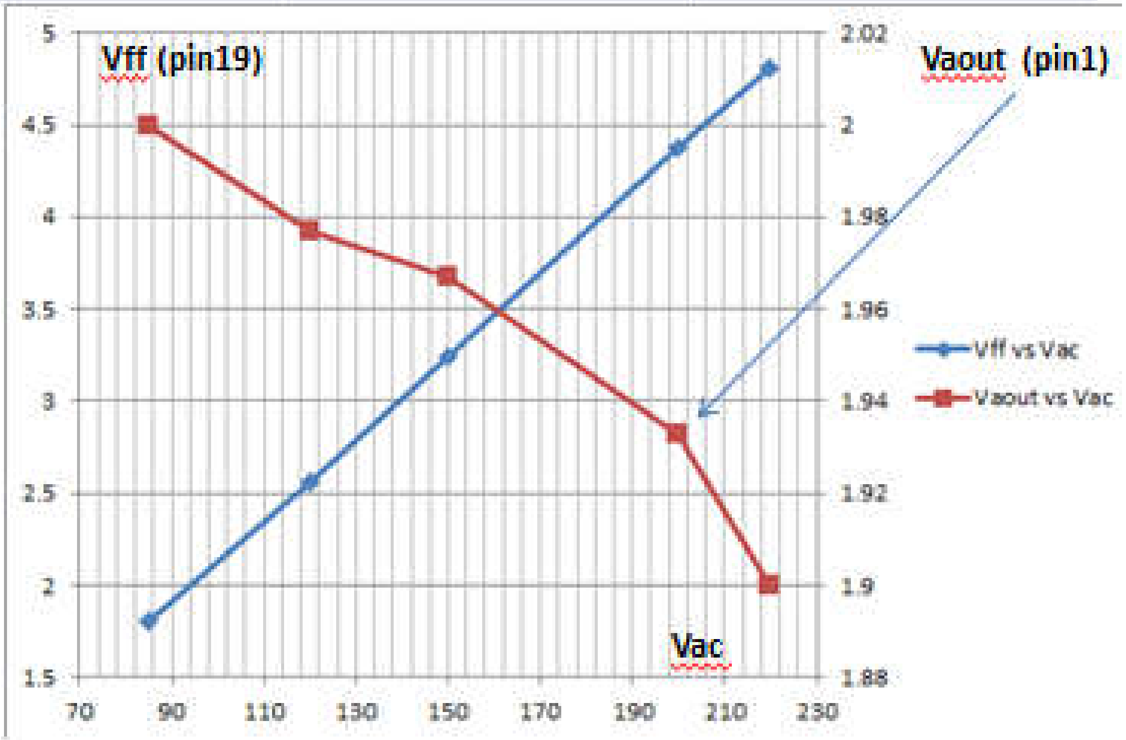

RIGOL STOP H 5.00ms 50.0MSa/s 3.00M pts
D 0.00000000ps
-4.00 V
200Vac input, measuring the ripple on DC link voltage
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Ch2: DC link, AC coupled, 2V/div
2.88Vpkpk @ 200Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Avg=2.56 V
Avg=90.4mV
Vpp=2.88 V
Rms=187 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V

Input voltage (Vrms)	Vff on pin19 w/ DiffProbe (Vdc)	Vaout on pin1 w/ DVM (Vdc)
85	1.80	2.000
120	2.56	1.977
150	3.24	1.967
200	4.38	1.933
220	4.81	1.900

$0 \le i_{IAC}(t) \le 500\ \mu A,$

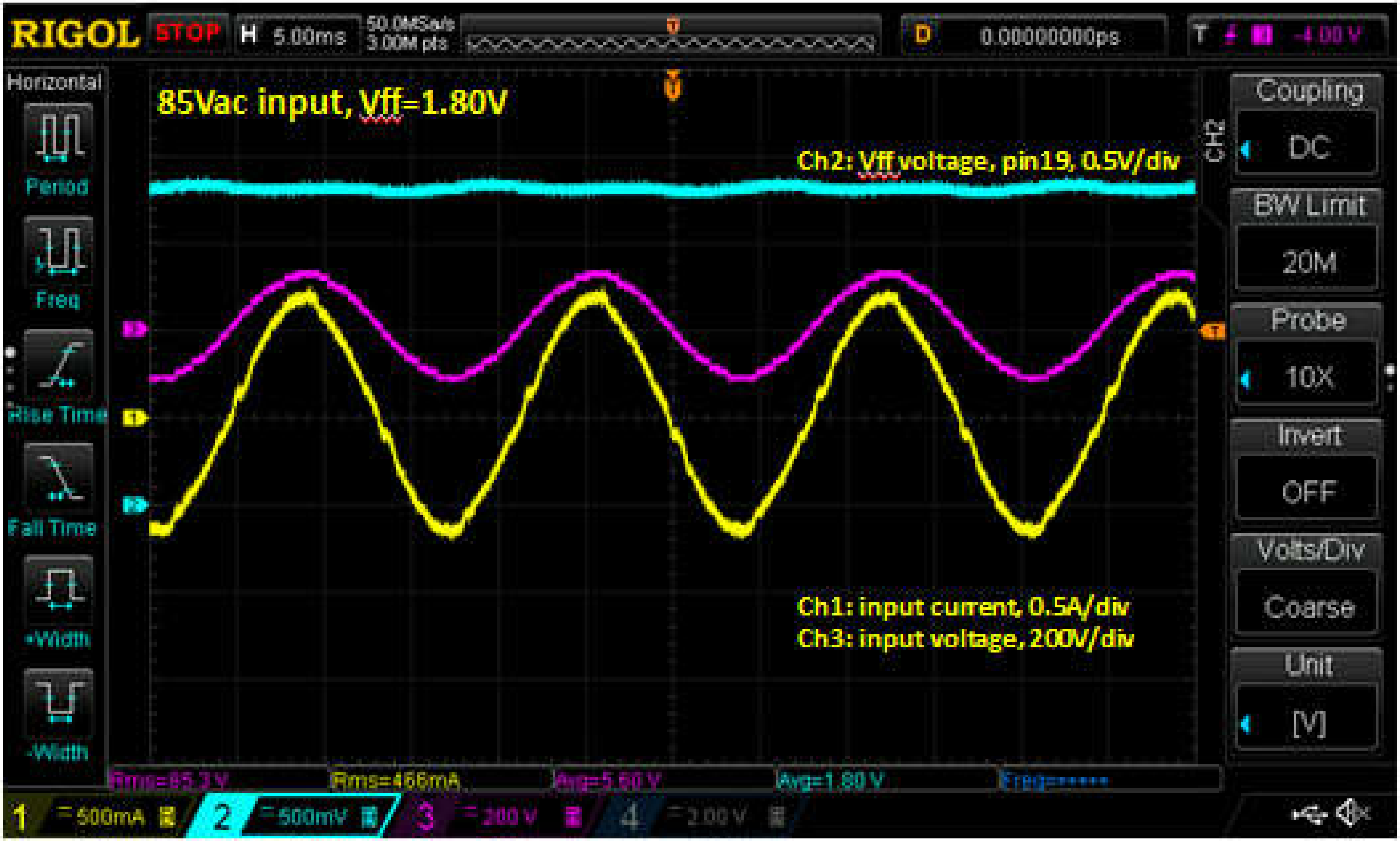
$0 \le V_{VAOUT}(t) \le 5\ V,$

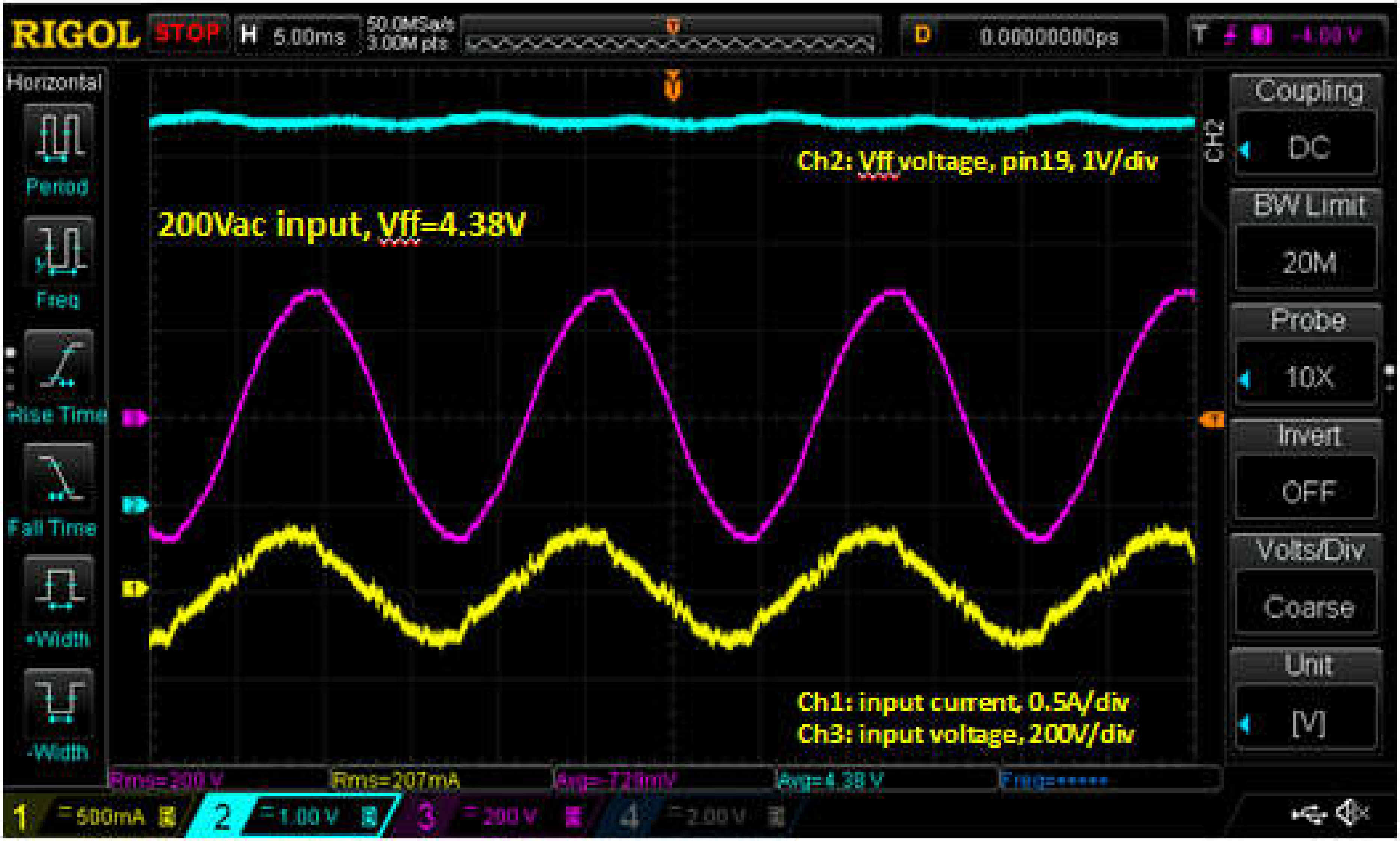
$1.4\ V \le V_{VFF} \le V_{VREF} - 1.4\ V$



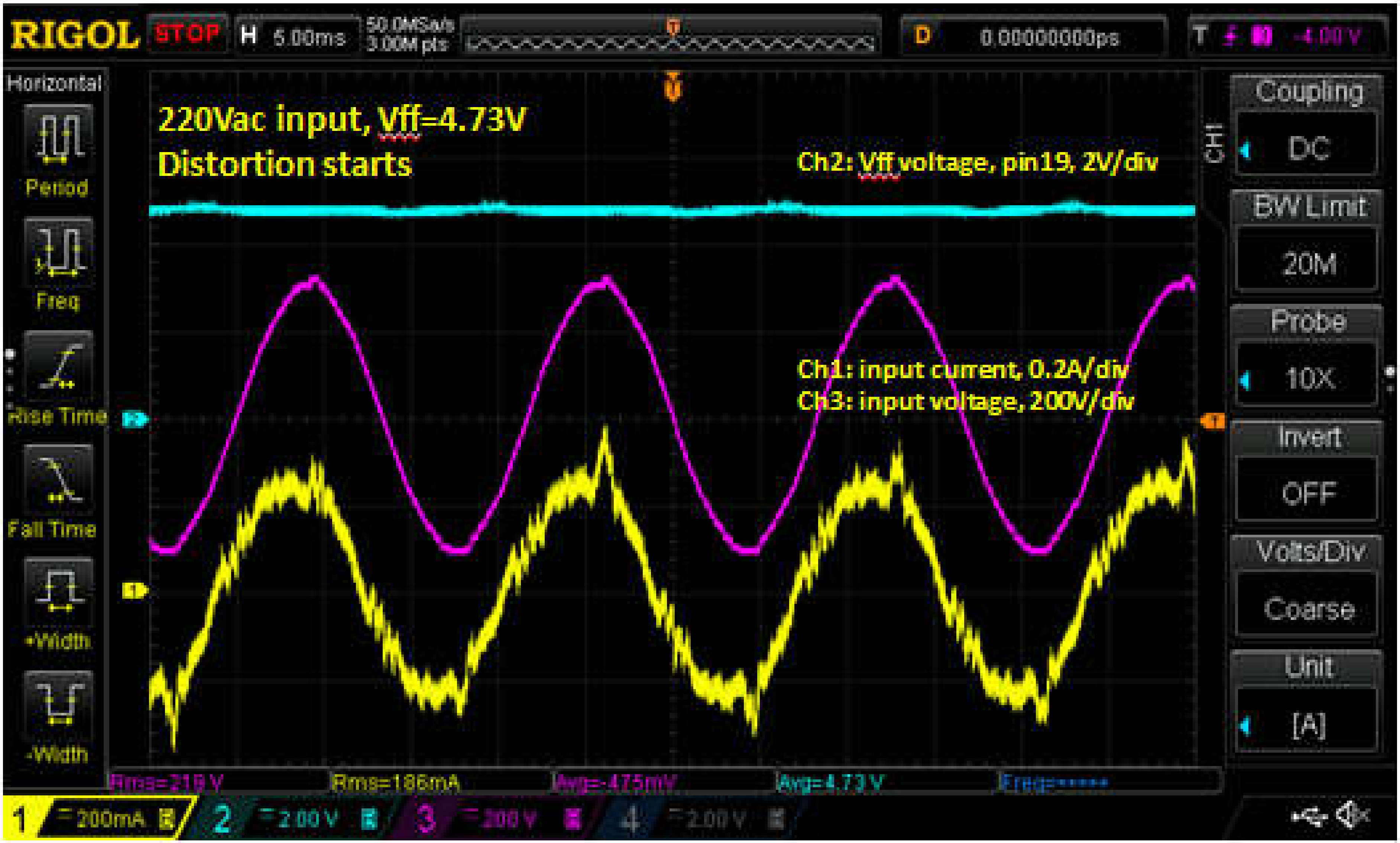
- Vff increases proportionally and Vaout drops inversely as Vac increases.
- Vaout seems to start low at 2V and not varying within its full range of 0-5V

65


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.00000000ps
85Vac input, Vff=1.80V
Ch2: Vff voltage, pin19, 0.5V/div
Ch1: input current, 0.5A/div
Ch3: input voltage, 200V/div
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH2
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Rms=85.3 V
Rms=466mA
Avg=1.80 V
1
500mA
2
500mV
3
200 V
4
2.00 V

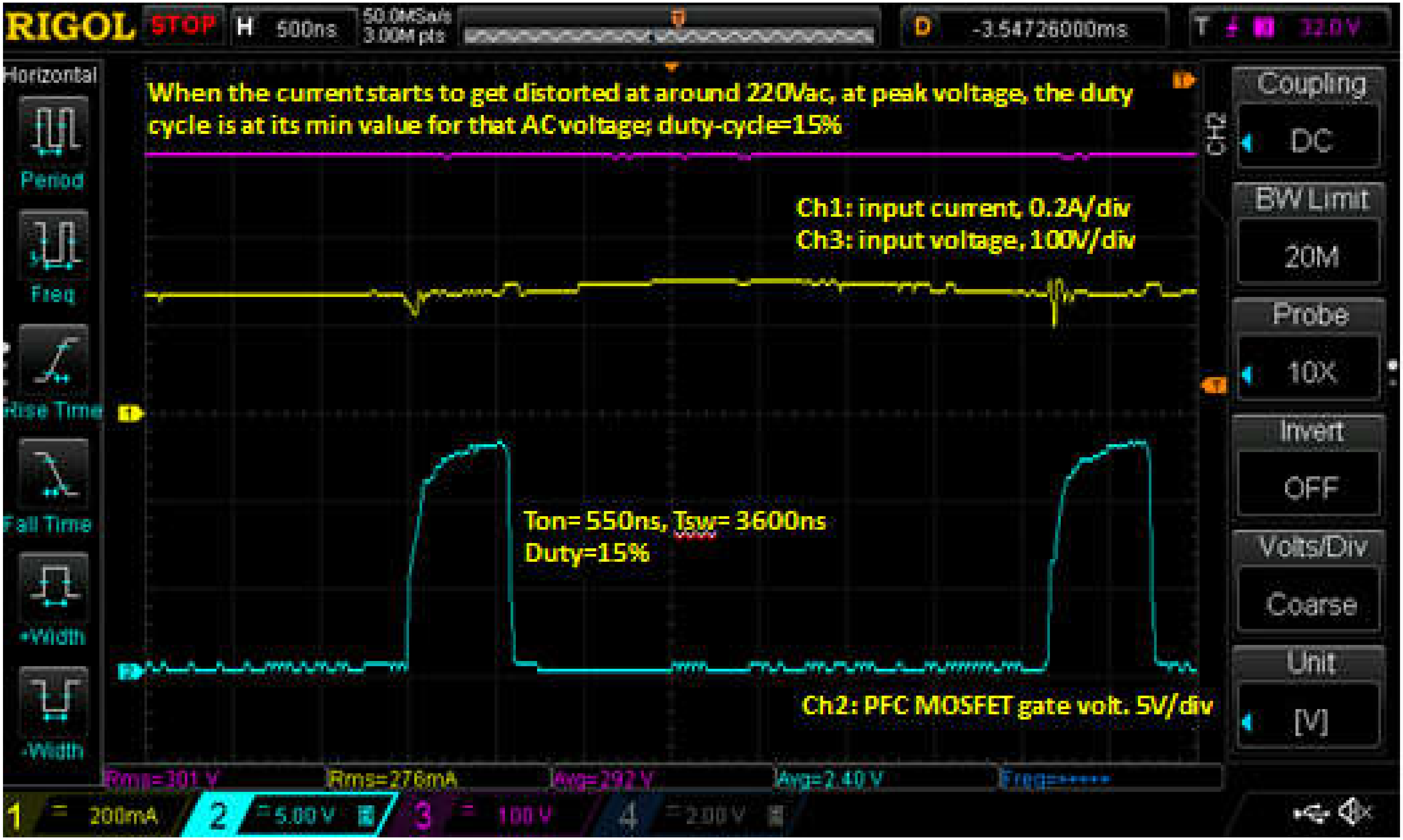


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.00000000ps
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
Ch2: Vff voltage, pin19, 1V/div
200Vac input, Vff=4.38V
Ch1: input current, 0.5A/div
Ch3: input voltage, 200V/div
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Rms=207mA
Avg=4.38 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.00000000ps
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
220Vac input, Vff=4.73V
Distortion starts
Ch2: Vff voltage, pin19, 2V/div
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Rms=218 V
Rms=186mA
Avg=-475mV
Avg=4.73 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V

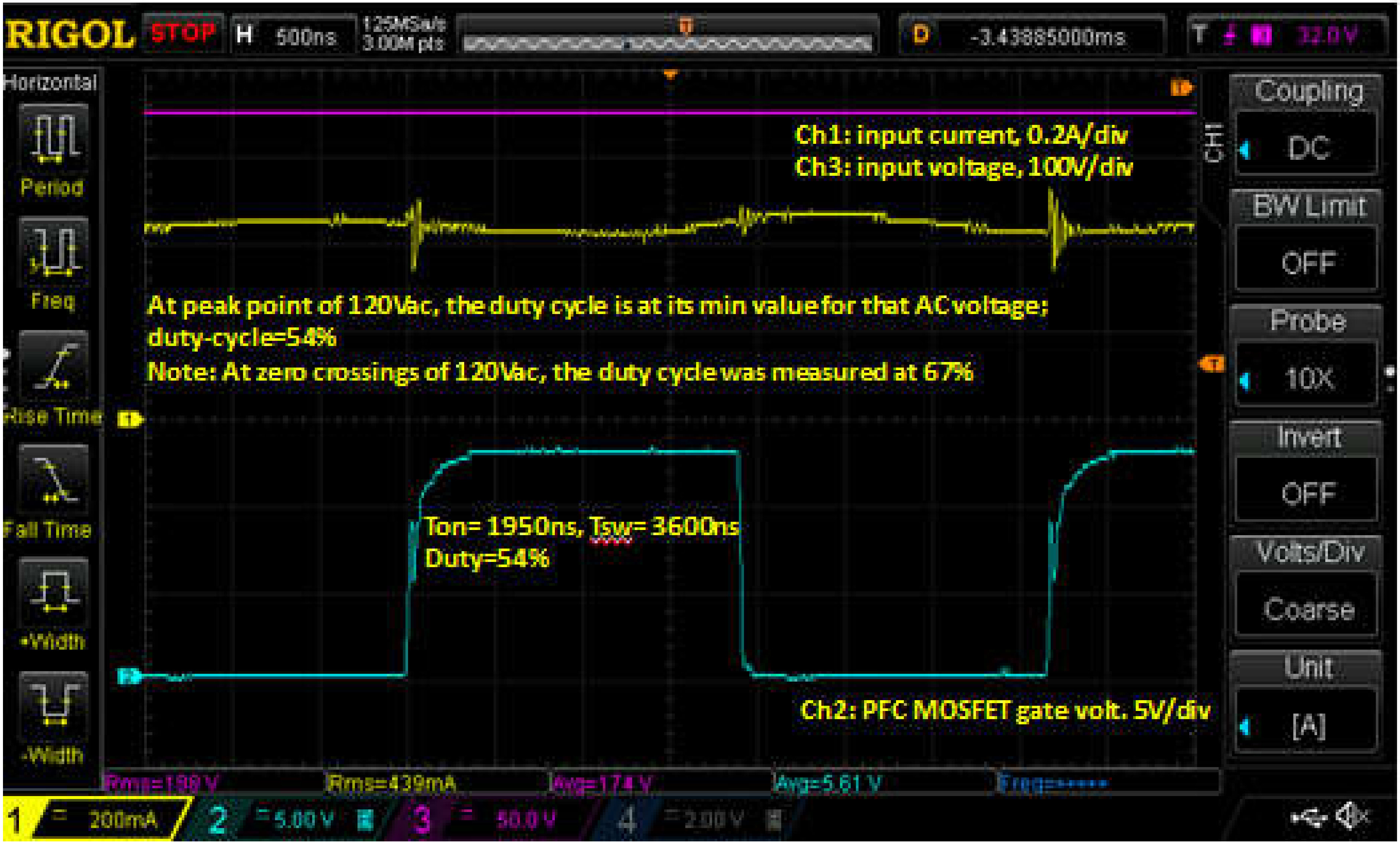
UCC28513 questions to TI, Alex W., 11/17/2022

At the peak of sinewaves when distortion starts, the duty cycle of boost MOSFET is about 15%



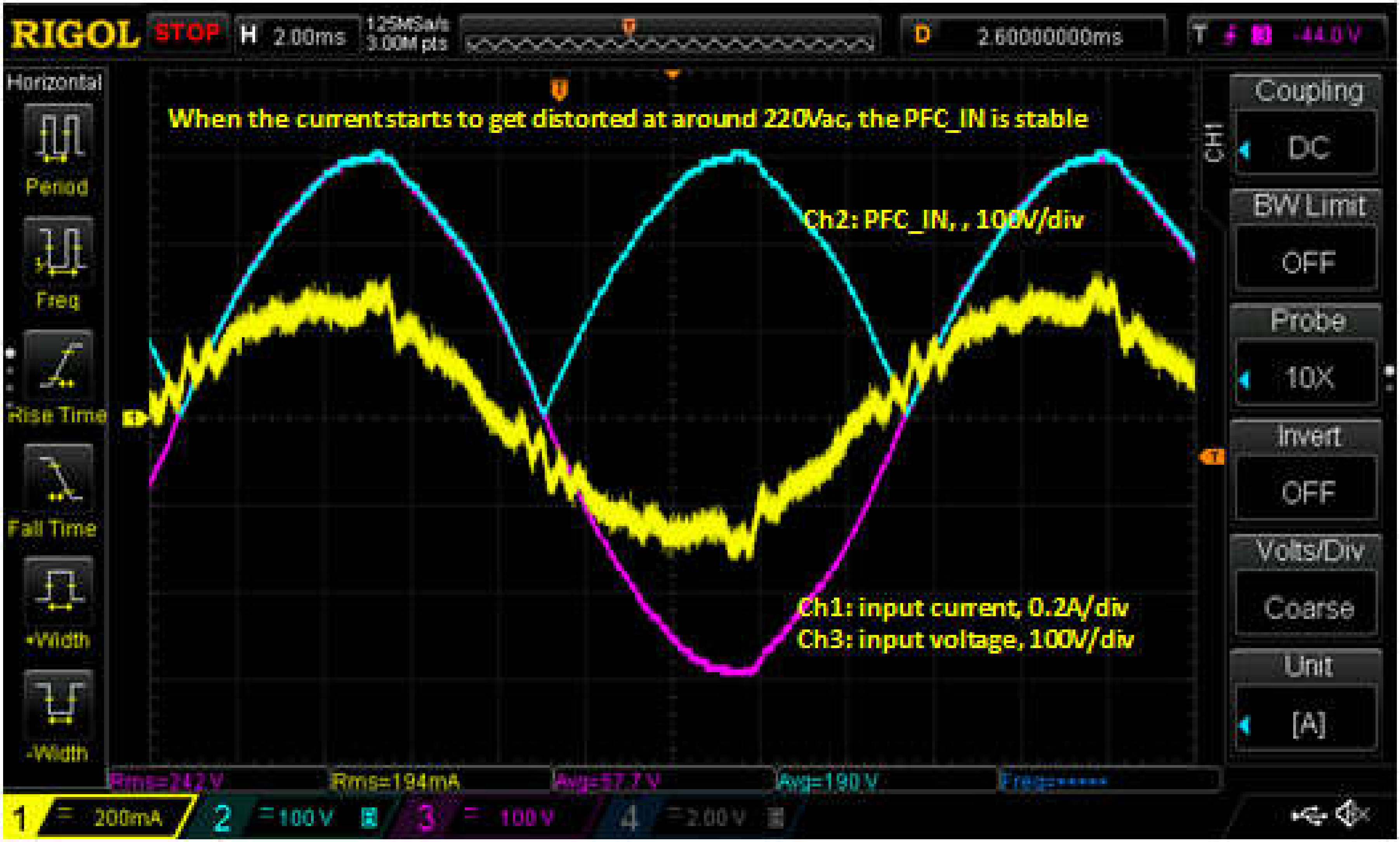
UCC28513 questions to TI, Alex W., 11/17/2022

At the peak of sinewaves at 120Vac, the duty cycle of boost MOSFET is about 54%



UCC28513 questions to TI, Alex W., 11/17/2022

At 220Vac when distortions starts, the rectified input voltage (used for Vff) is shown below



Referring to Fig 36 in the data sheet of UCC28513DW, what specific capacitor controls the min duty cycle?

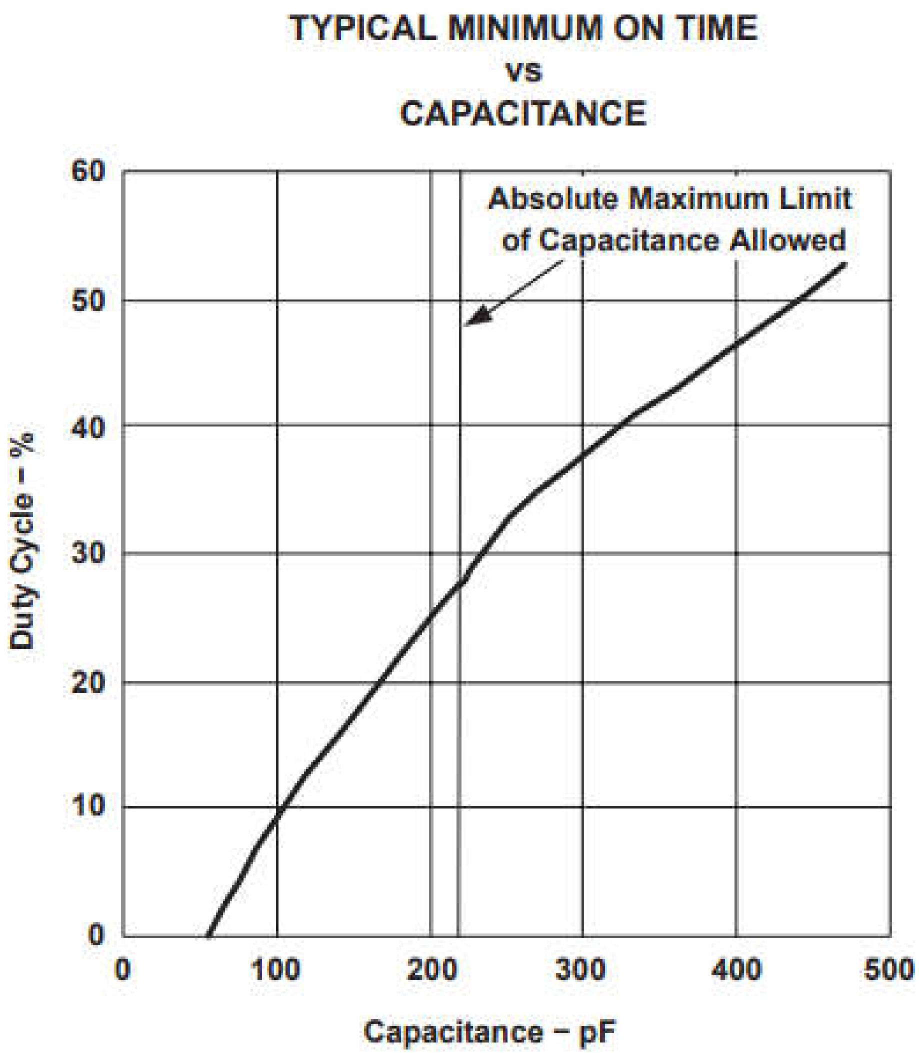
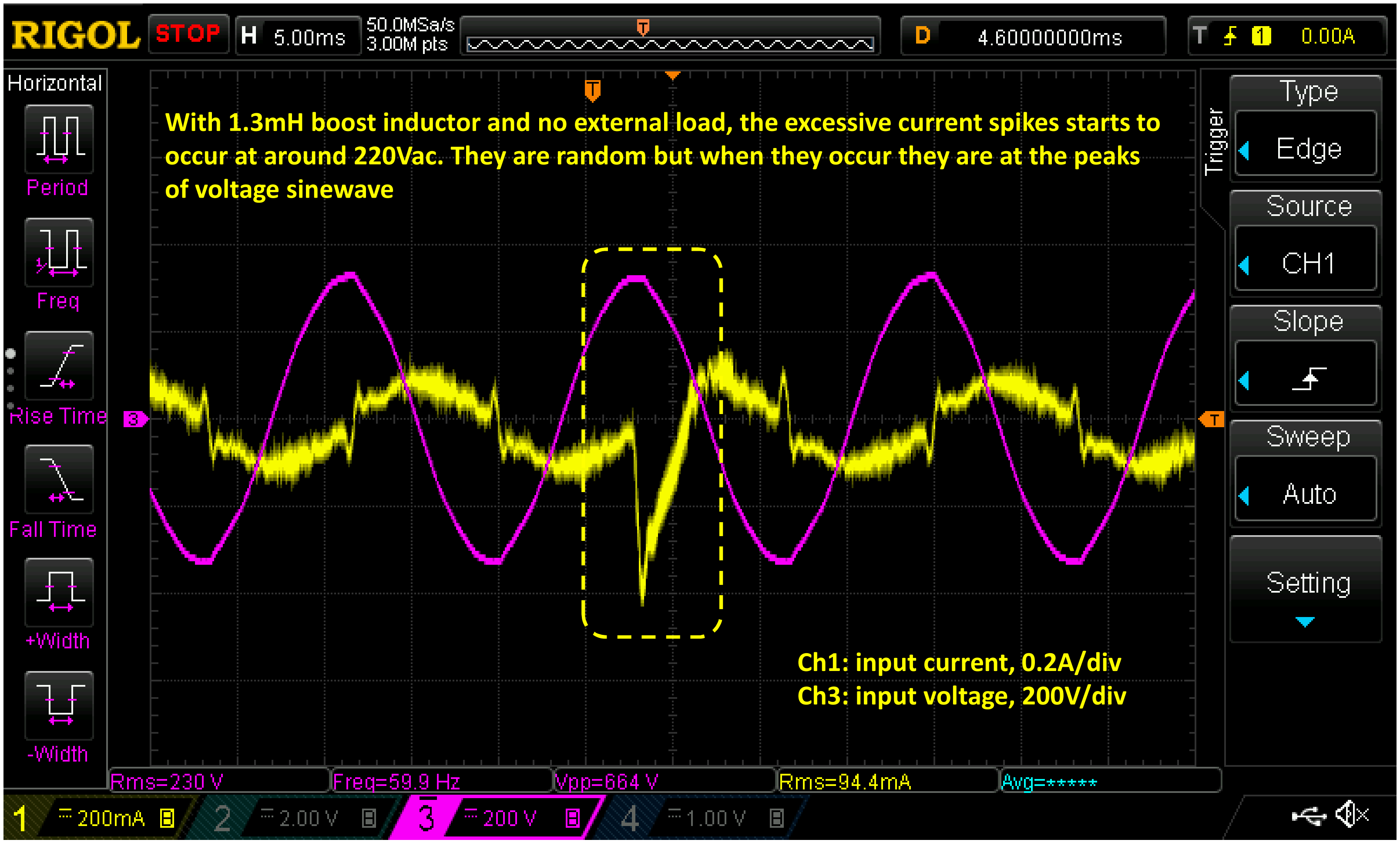


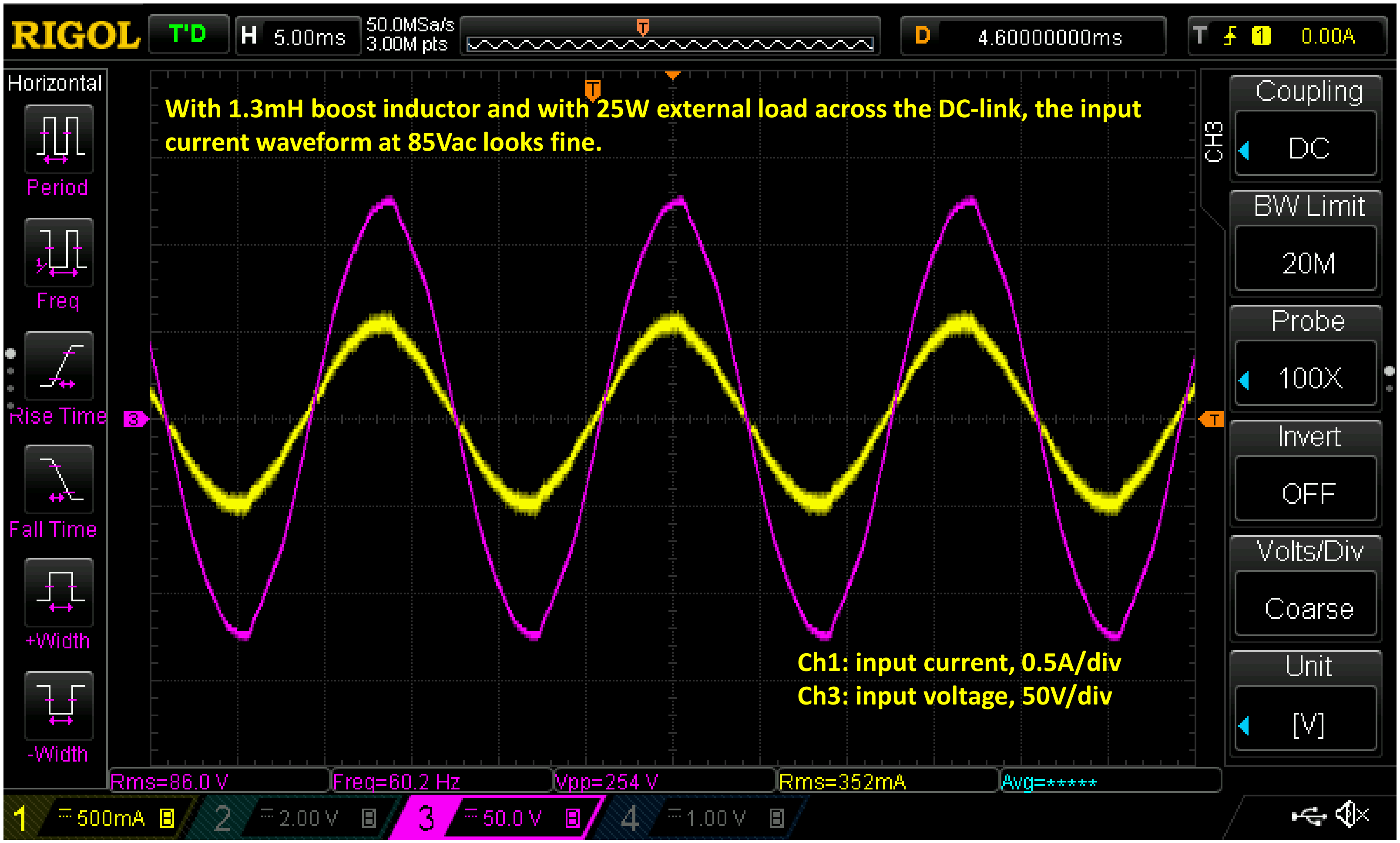
Figure 36

Note: The capacitor on Isense2 affects the min duty cycle on GATE2 output, PFC is on GATE1 output

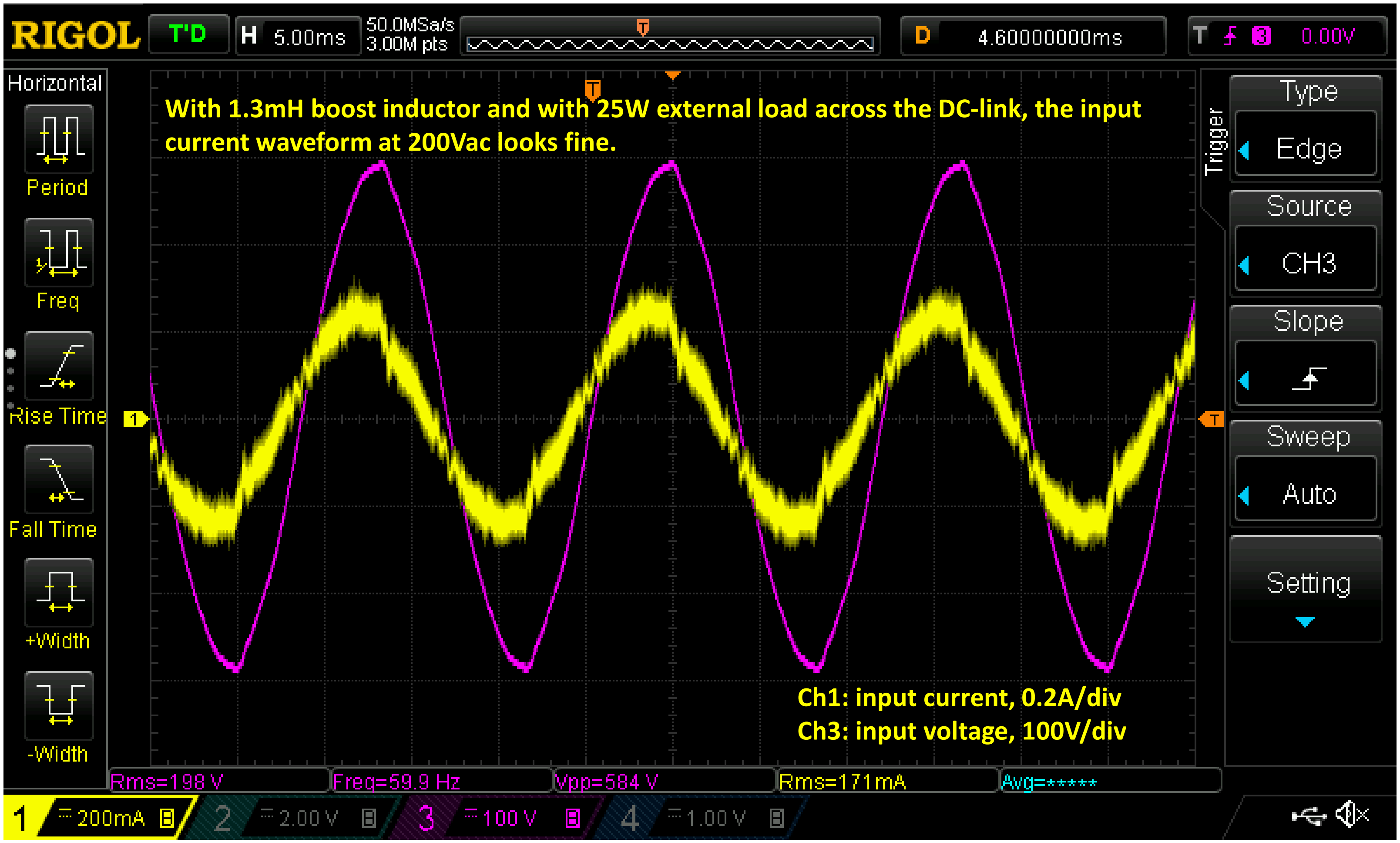
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



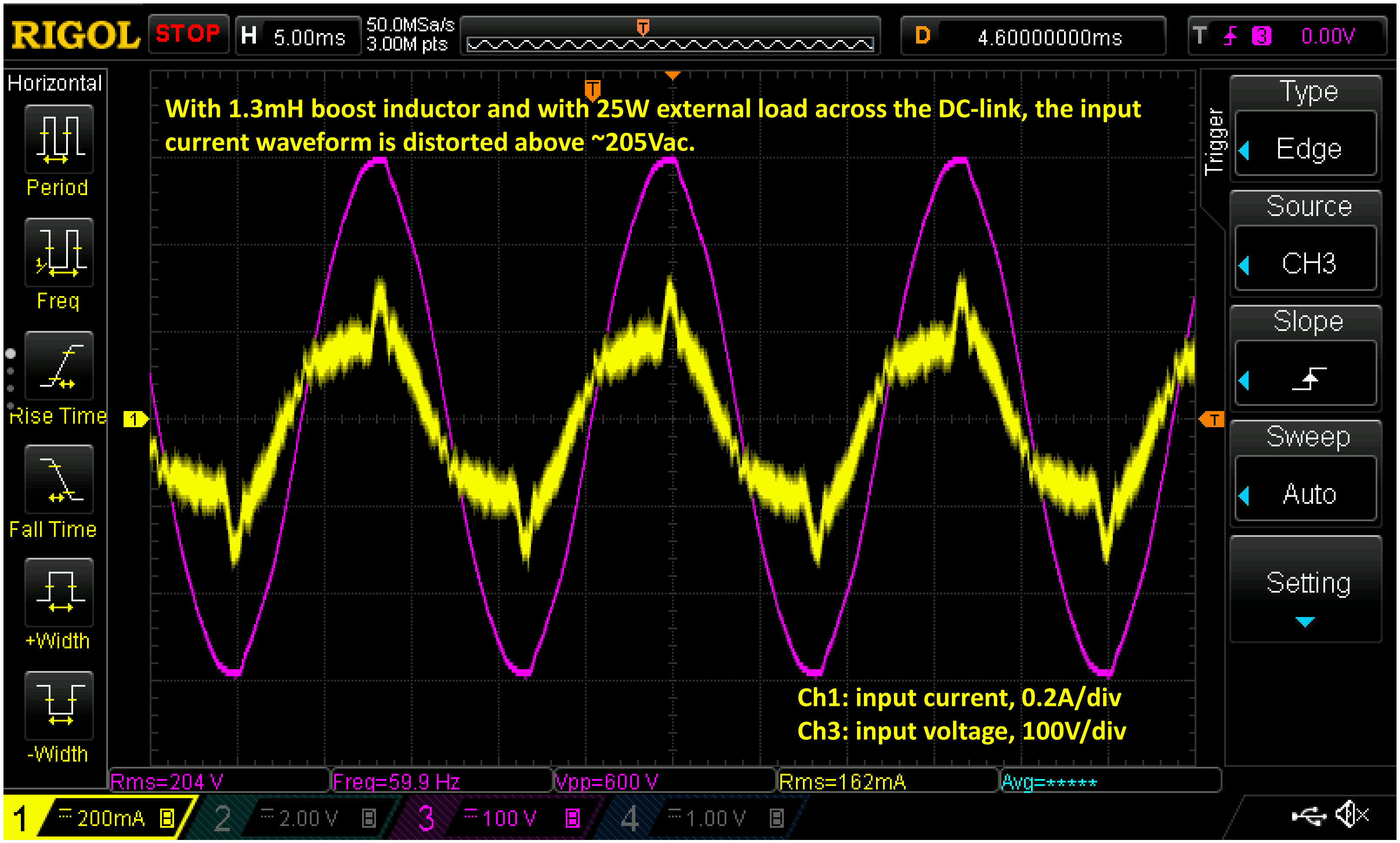
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



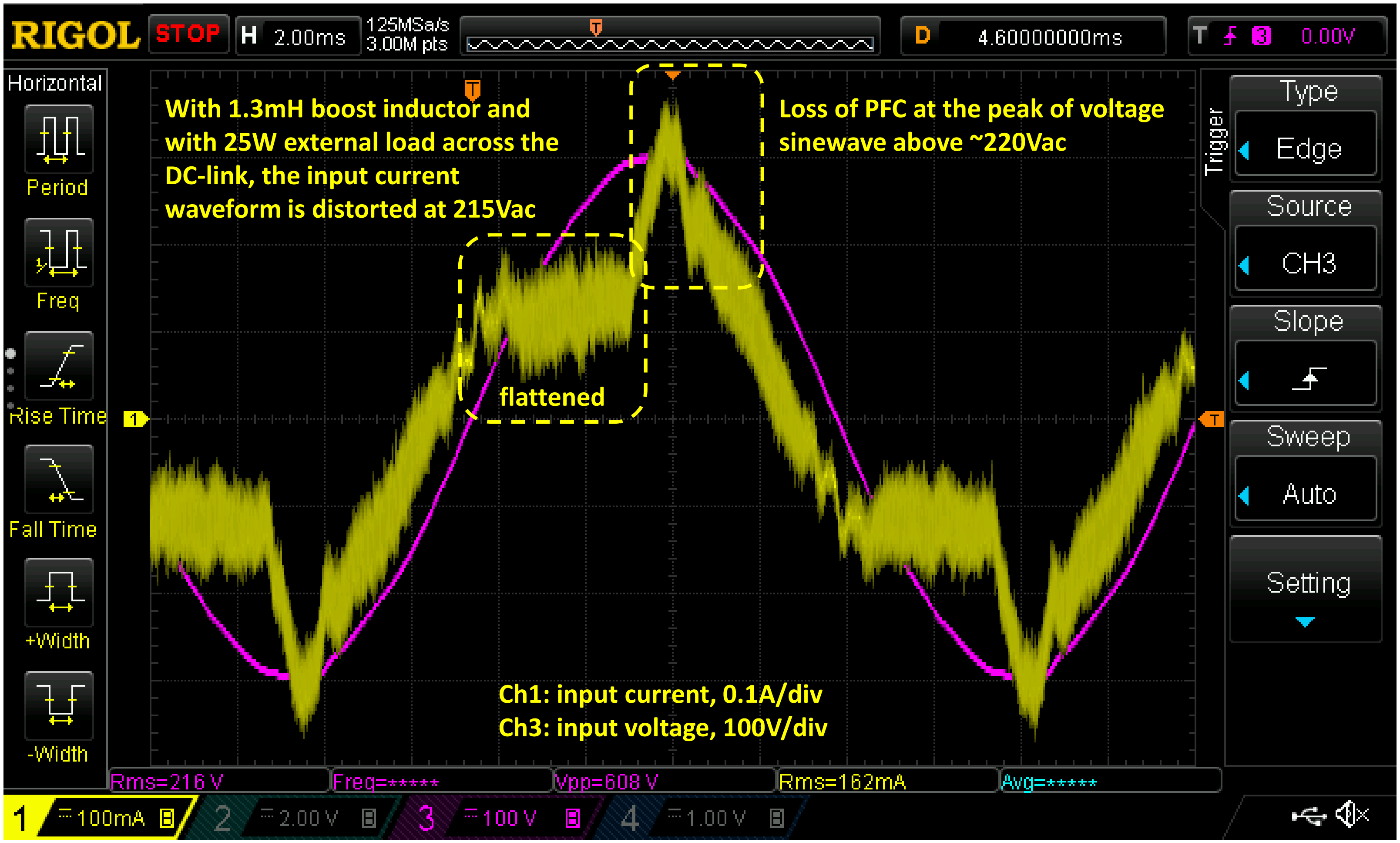
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



Boost inductor is changed from 660uH to 2x660uH= 1.32mH



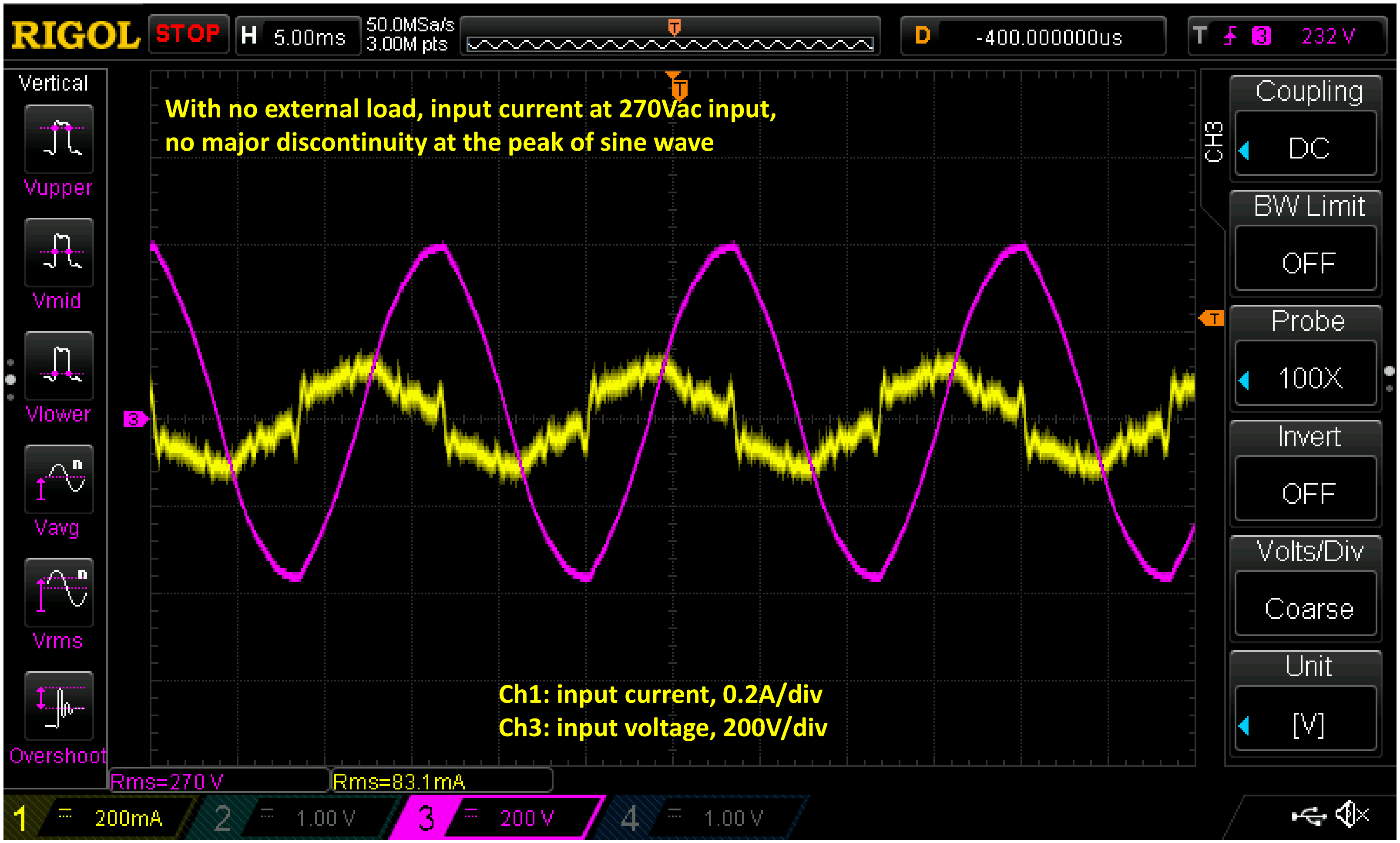
Boost inductor is changed from 660uH to 2x660uH= 1.32mH

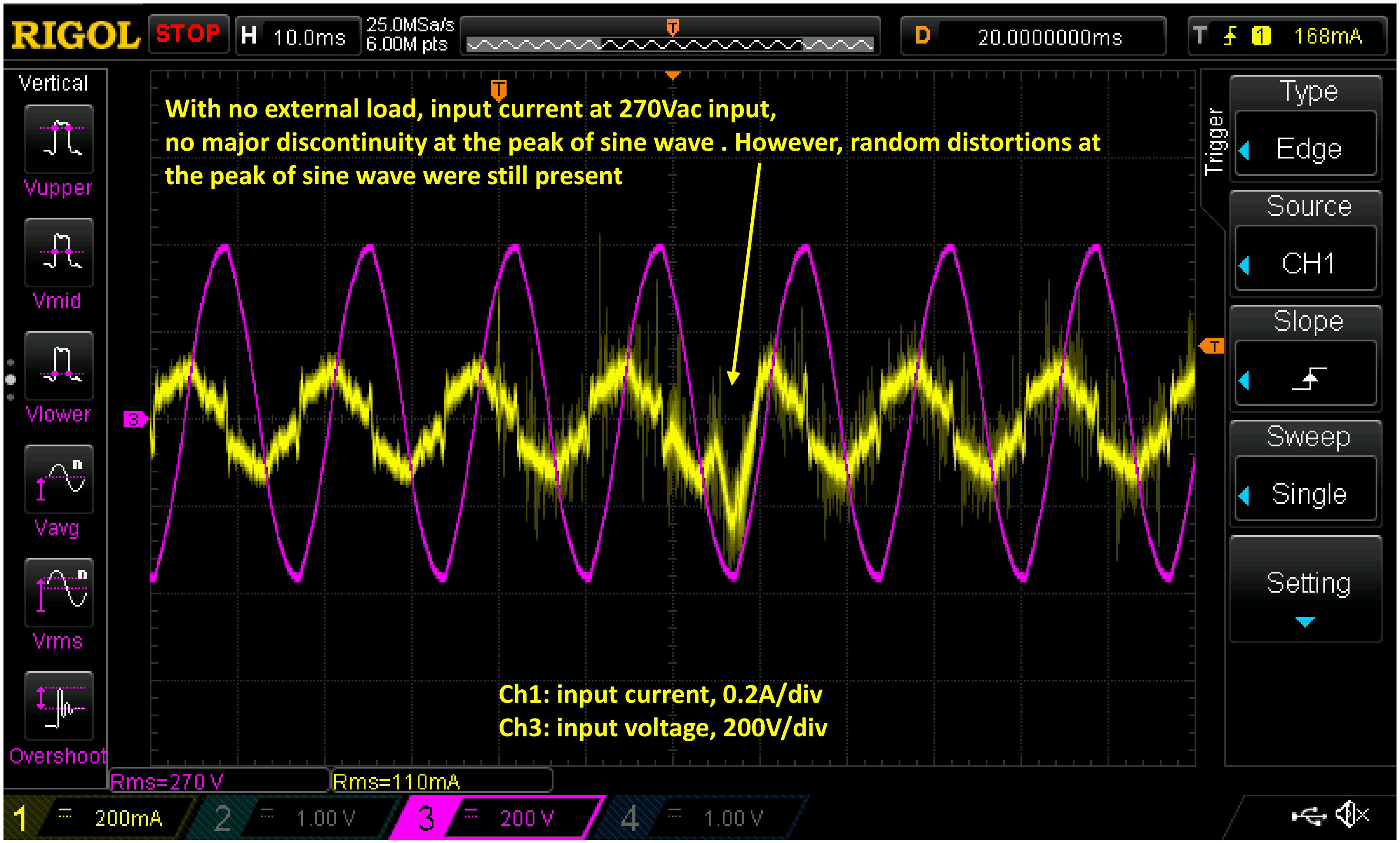


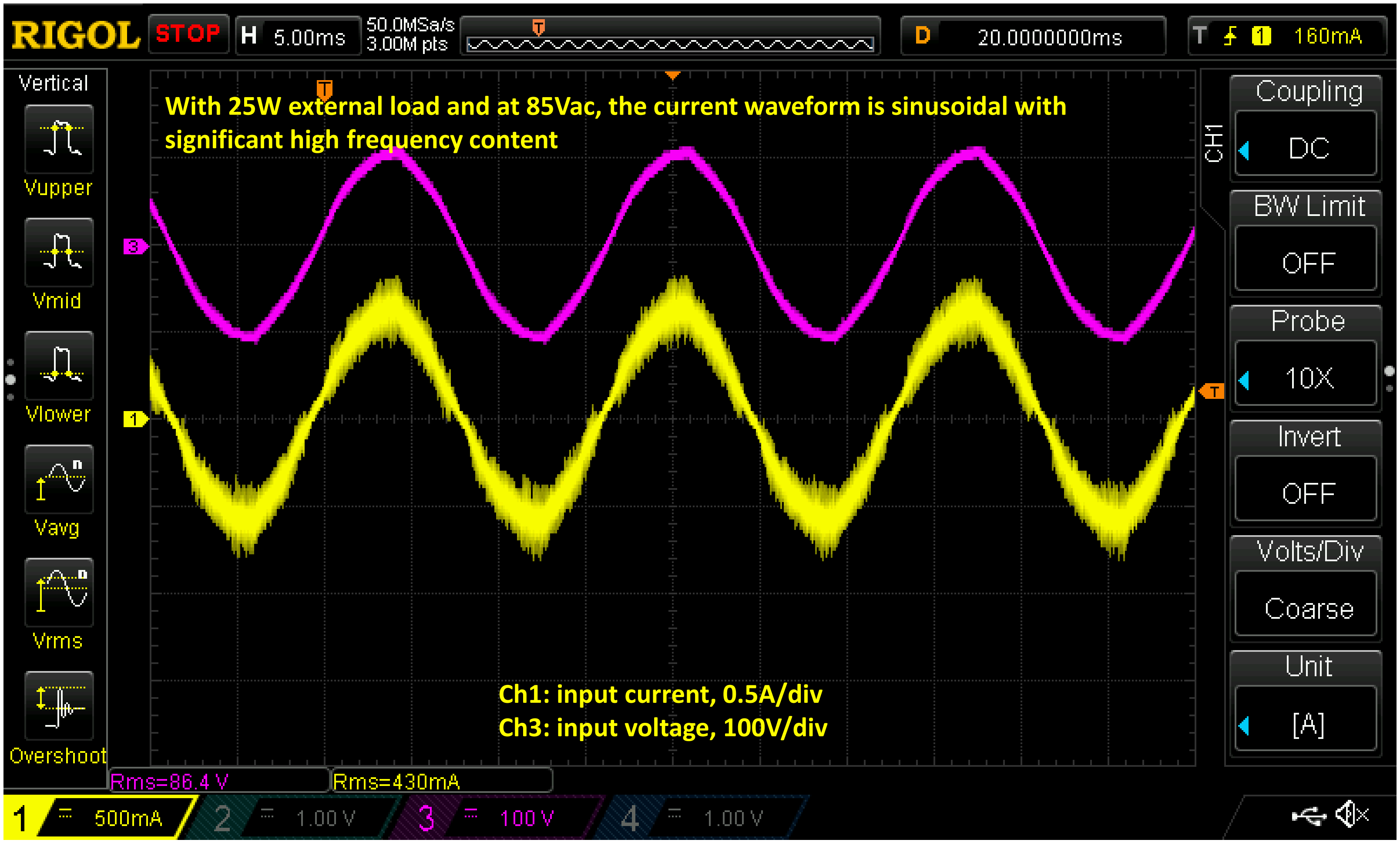
RefDes on data sheet	RefDes in design	values	Values on 12/11/2022
R1	R47+R50	766K	
R2	R43	0.22	**0.44**
R8/R12	R4/R9	3.16K	**2.74K**
R3	R44+R49	1124K	
R4	R60	22.1k	
C1	C32	150uF	
L1	L2	660uH	
R13	R10	15.8K	**55K (56K//3.3Meg)**
C6	C6	680pF	**233pF (200p//33p)**
C7	C8	150pF	**33pF**
R15	R11	30.1K	
C8	C9	4.7uF	
C10	C1	1.5uF	
C11	C2	150nF	
R21	R1	48.7K	
R14	R13	10K	
R7	R5	1.18K	**1.50K (3.3K//2.74K)**
C9	C4	1uF	

Changes made on 12/11 are highlighted

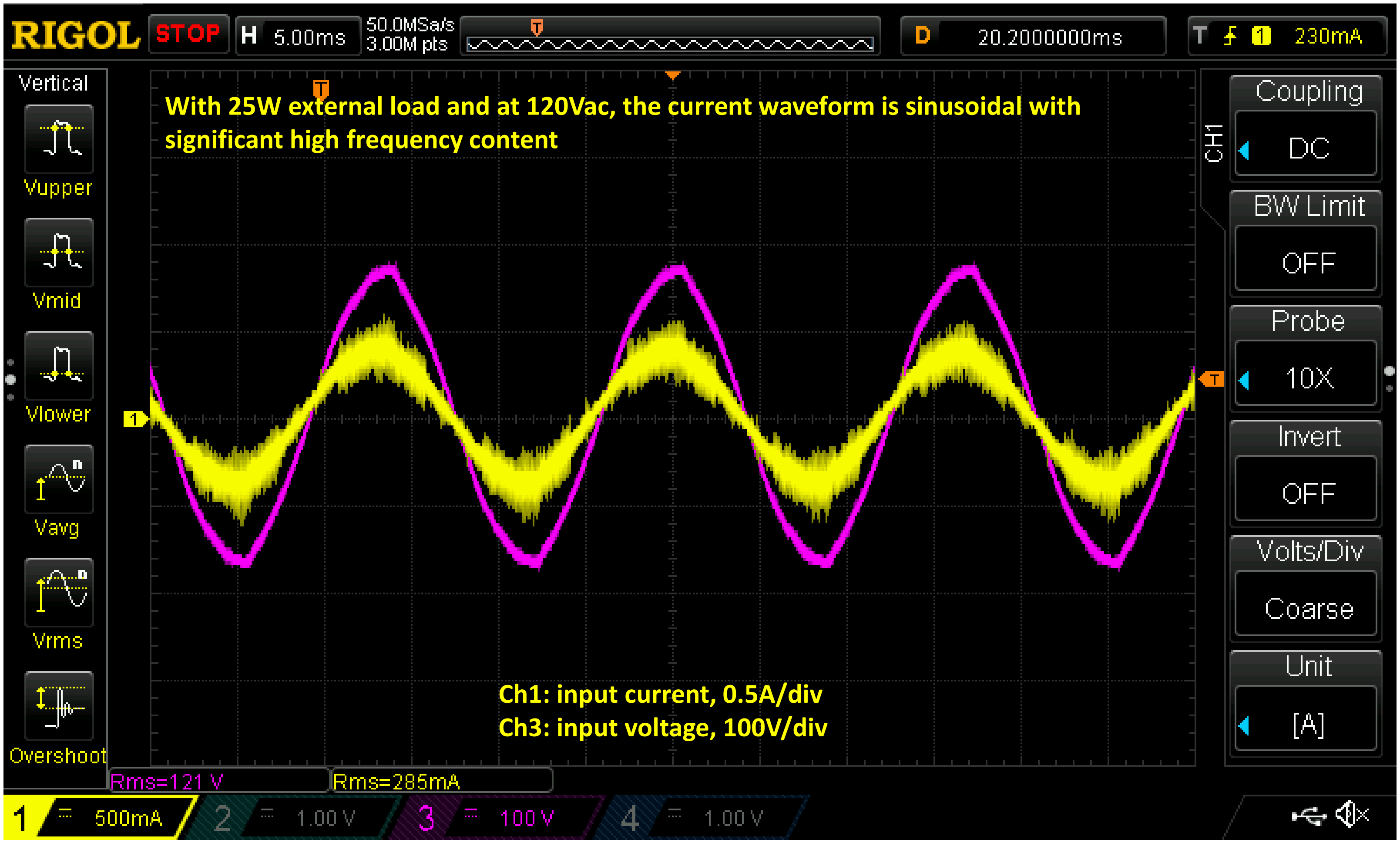
Also tried 15.8k

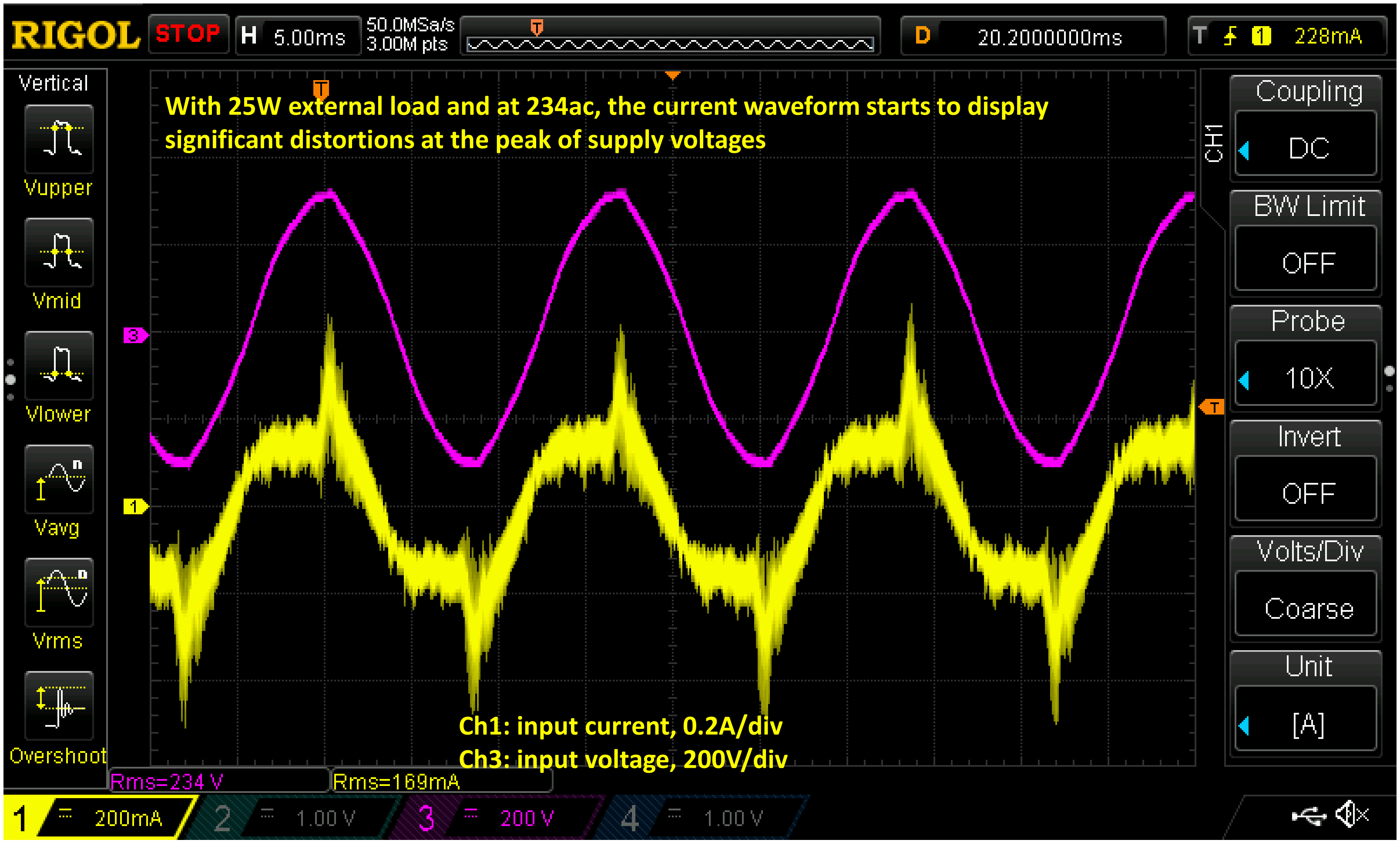

RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D -400.000000us
T 3 232 V
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With no external load, input current at 270Vac input,
no major discontinuity at the peak of sine wave
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
CH3
Coupling
DC
BW Limit
OFF
Probe
100X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Rms=270 V
Rms=83.1mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V


RIGOL
STOP
H 10.0ms
25.0MSa/s
6.00M pts
D 20.0000000ms
T 1 168mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
Trigger
Type
Edge
Source
CH1
Slope
Sweep
Single
Setting
With no external load, input current at 270Vac input,
no major discontinuity at the peak of sine wave . However, random distortions at
the peak of sine wave were still present
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Rms=270 V
Rms=110mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V



RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 20.0000000ms
T 1 160mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 85Vac, the current waveform is sinusoidal with significant high frequency content
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Rms=86.4 V
Rms=430mA
1 500mA
2 1.00 V
3 100 V
4 1.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 20.2000000ms
T 230mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 120Vac, the current waveform is sinusoidal with significant high frequency content
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Rms=121 V
Rms=285mA
1 500mA
2 1.00 V
3 100 V
4 1.00 V


RIGOL STOP H 5.00ms 50.0MSa/s 3.00M pts
D 20.2000000ms
T 1 228mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 234ac, the current waveform starts to display significant distortions at the peak of supply voltages
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Rms=234 V
Rms=169mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]

Measuring inductor current vs gate voltages, 12/18

There are only two current probes at the moment:

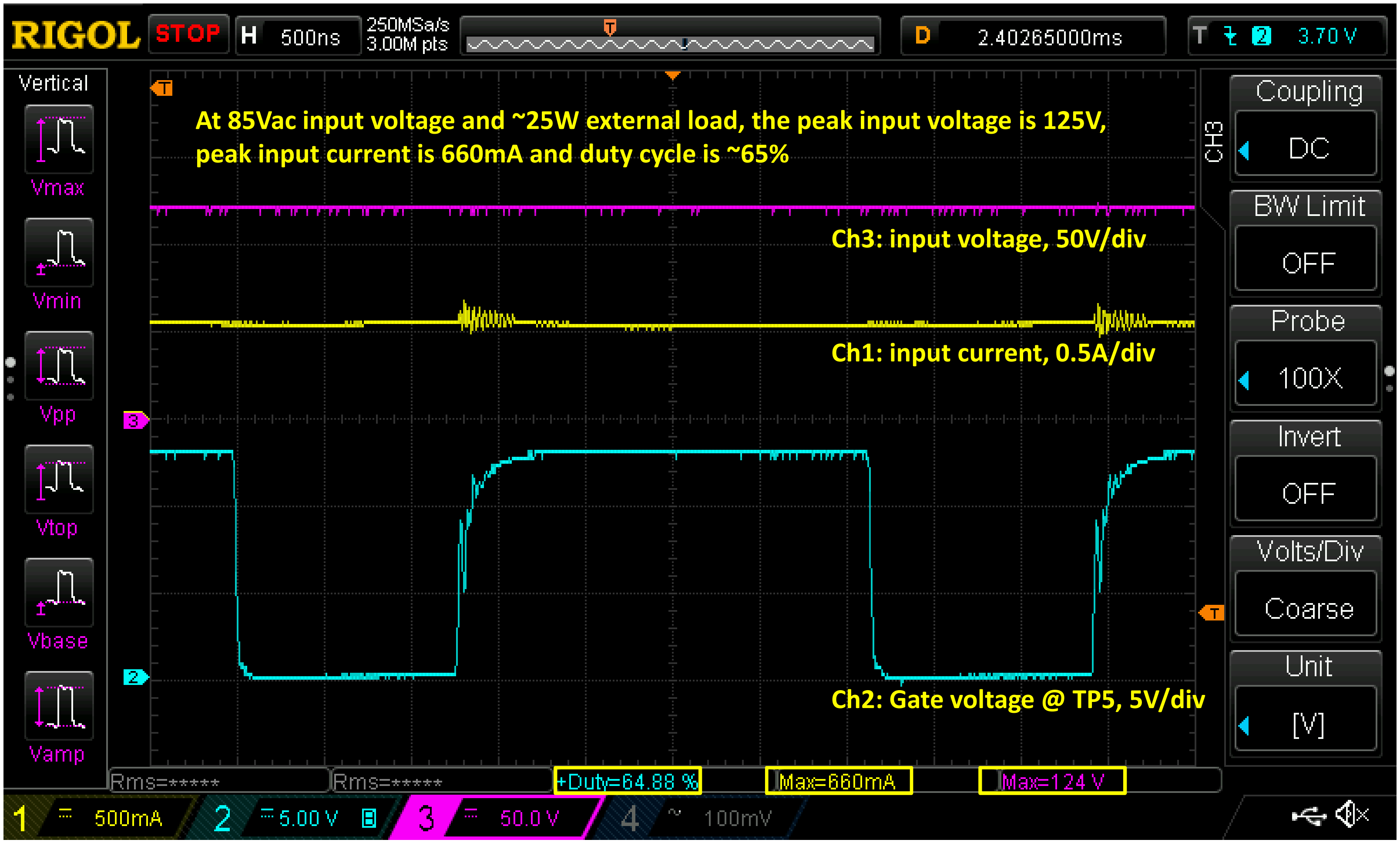
Ch1: Fluke 80i-110S has limited bandwidth and is used to measure 60Hz input current only.

Ch4: Rogowski probe, CWTUM-015-B, is used to measure the high frequency switching ripple only.

In addition, a 100mΩ and 20mΩ sense resistor was connected in series with inductor and the voltage across the resistor was measured with a differential probe. However, doing so resulted in further instability and distortion and therefore abandoned.

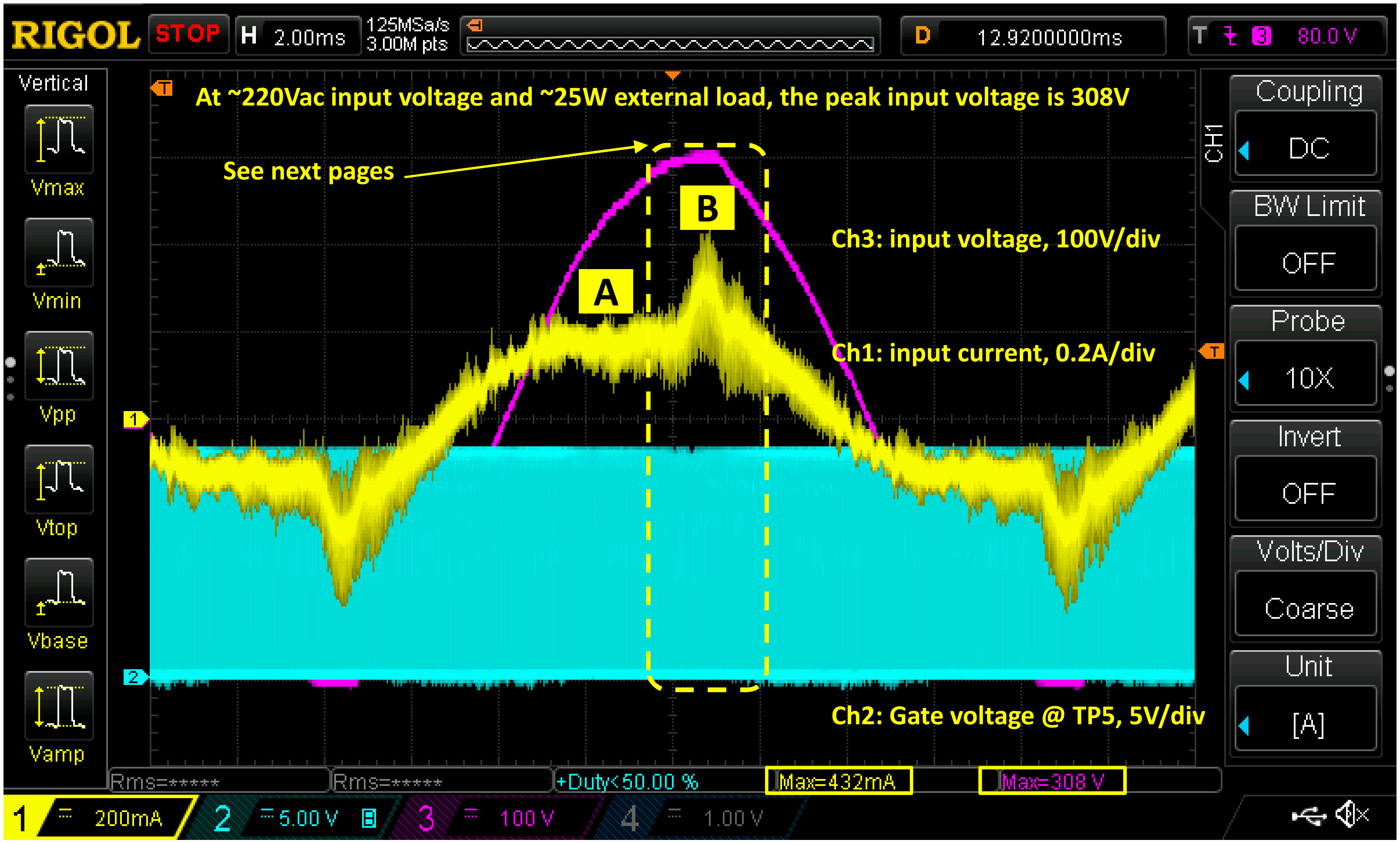
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



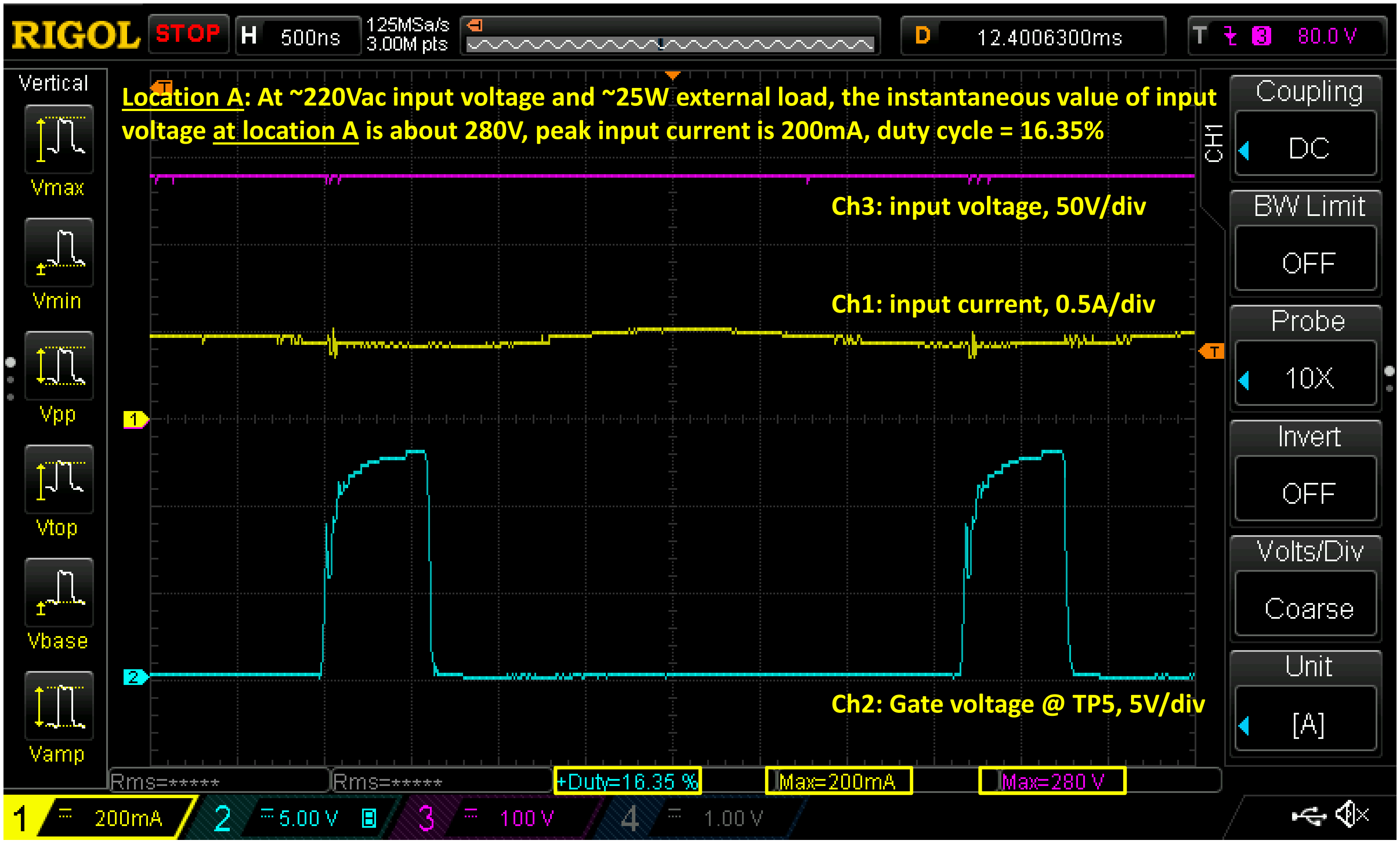
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



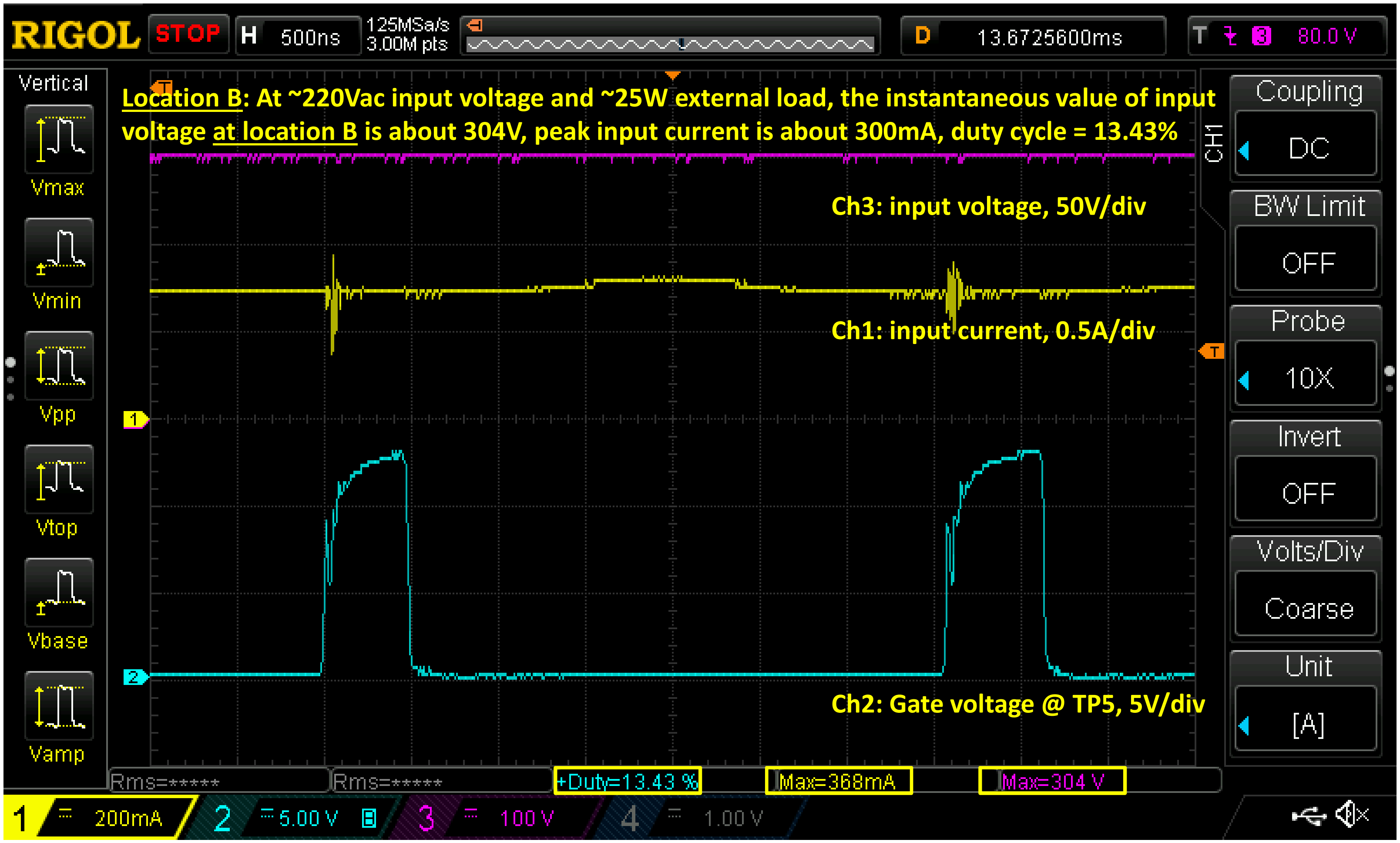
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current

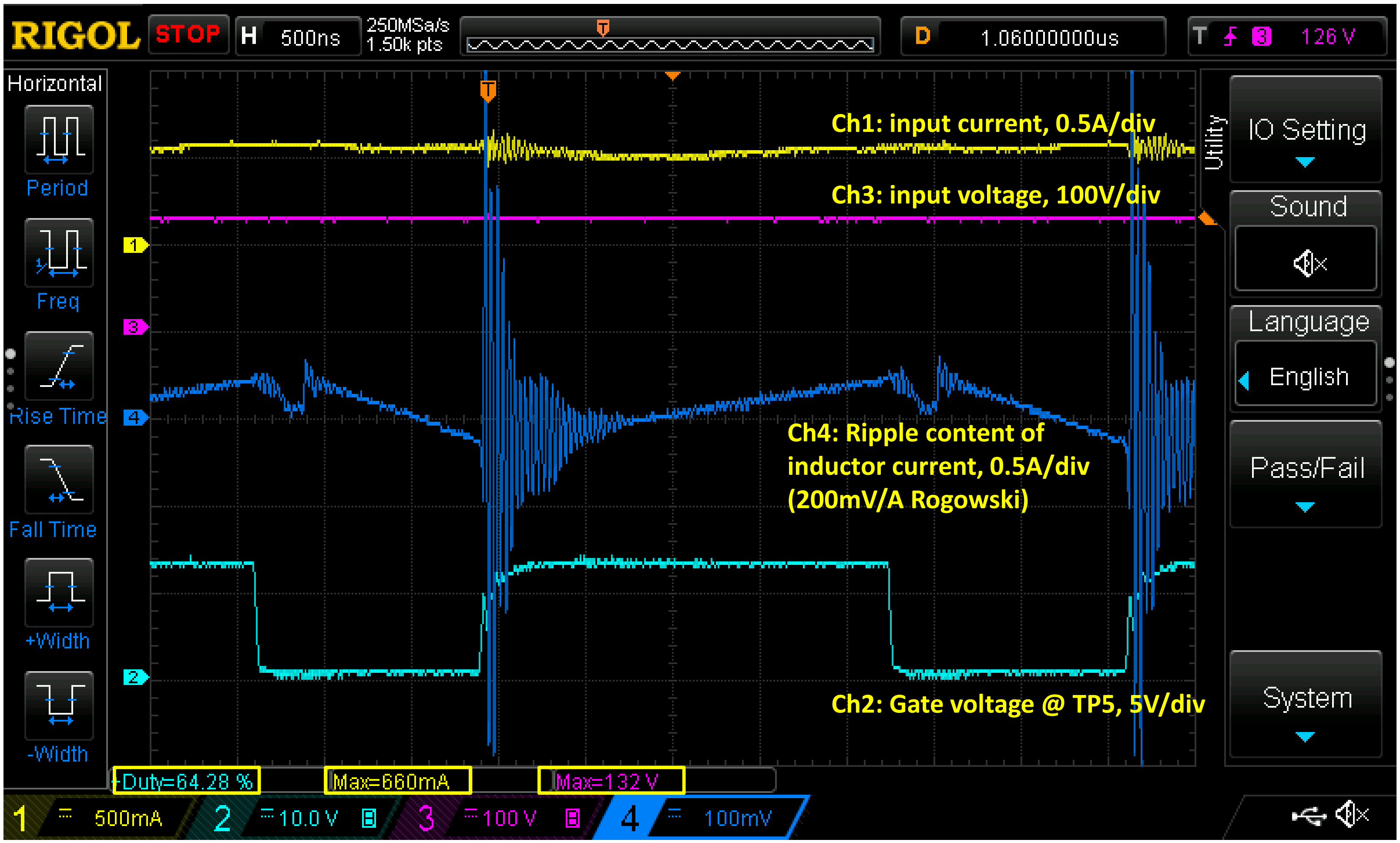


Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current

Ch4: Current probe is Rogowski CWTUM-015-B, which can measure high frequency only.

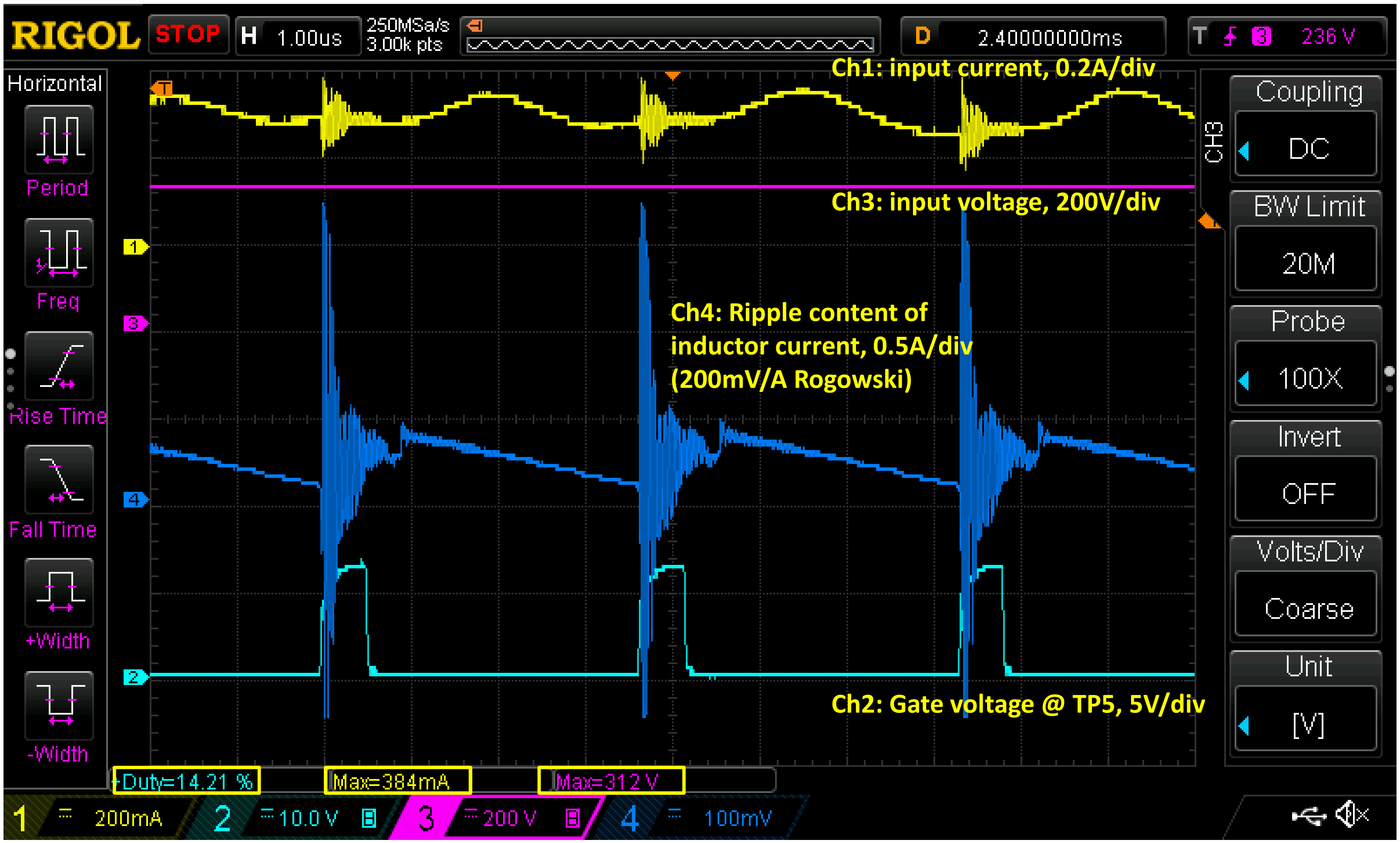
At the peak of 85Vac input voltage and ~25W external load, the instantaneous value of input voltage is 132V, peak input current is 660mA, duty cycle = 64.28%



Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current
Ch4: Current probe is Rogowski CWTUM-015-B, which can measure high frequency only.

At the peak of 220Vac input voltage and ~25W external load, the instantaneous value of input voltage is 312V, peak input current is ~300mA (location B), duty cycle is about 14.2%

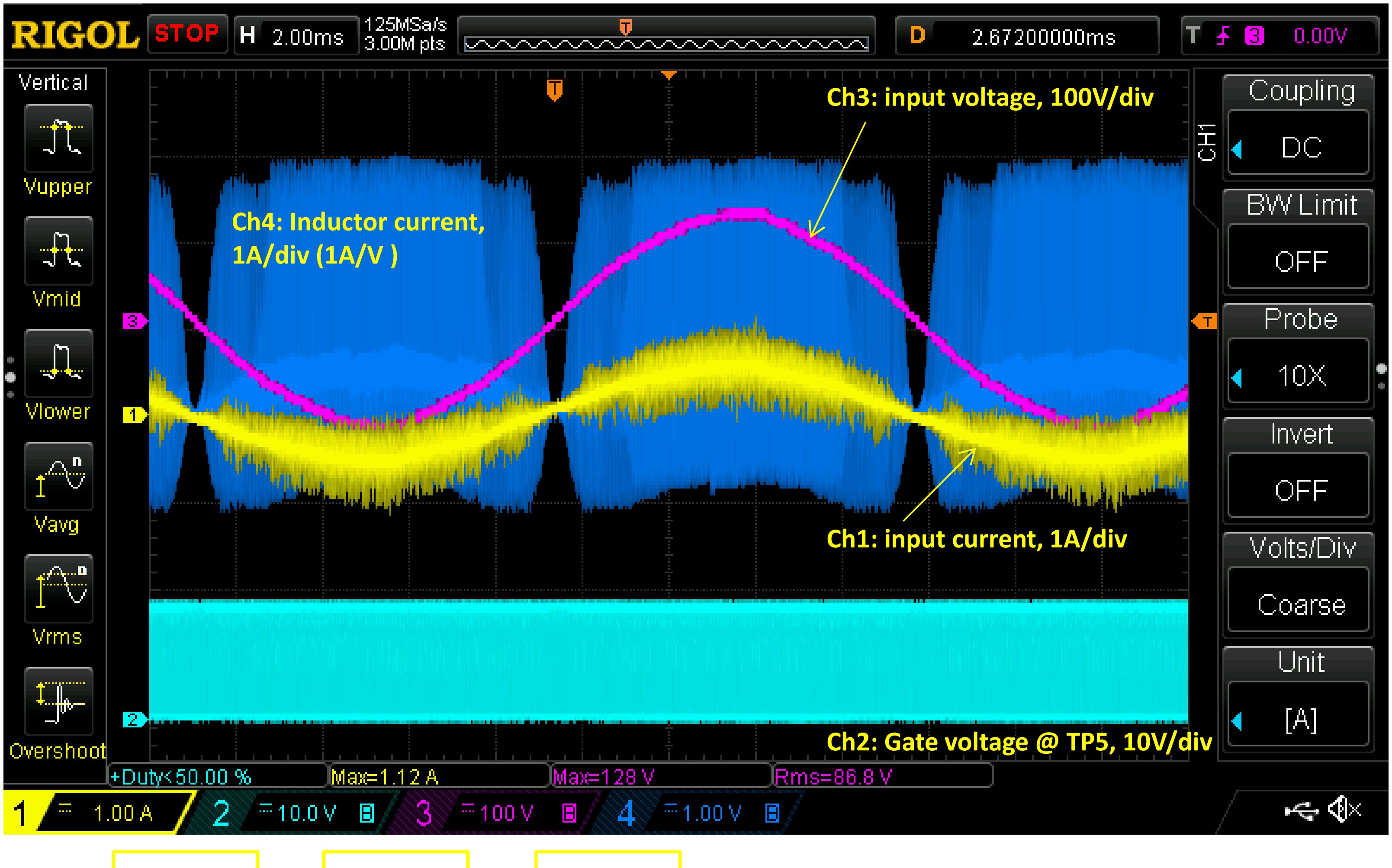


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

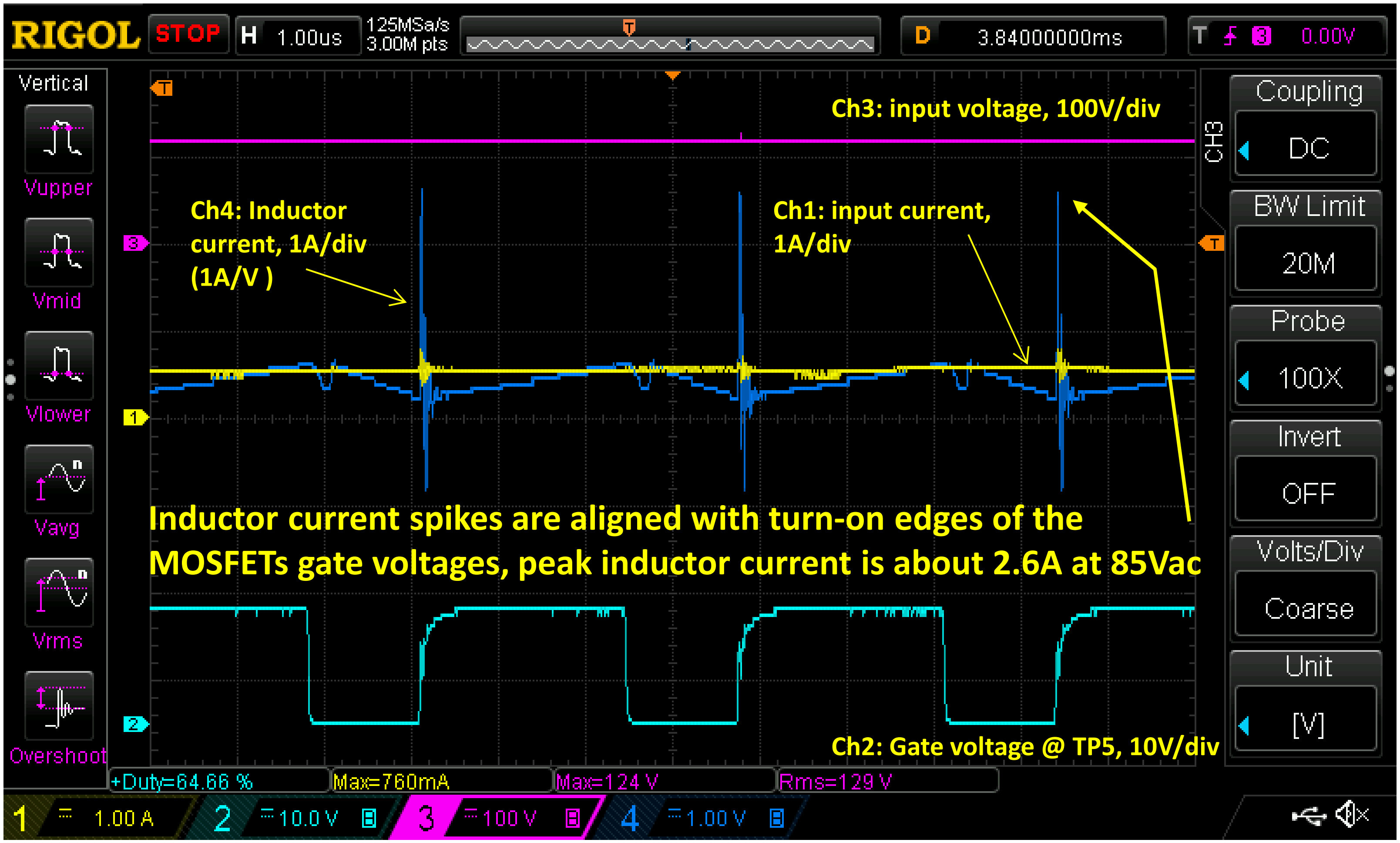
At 85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

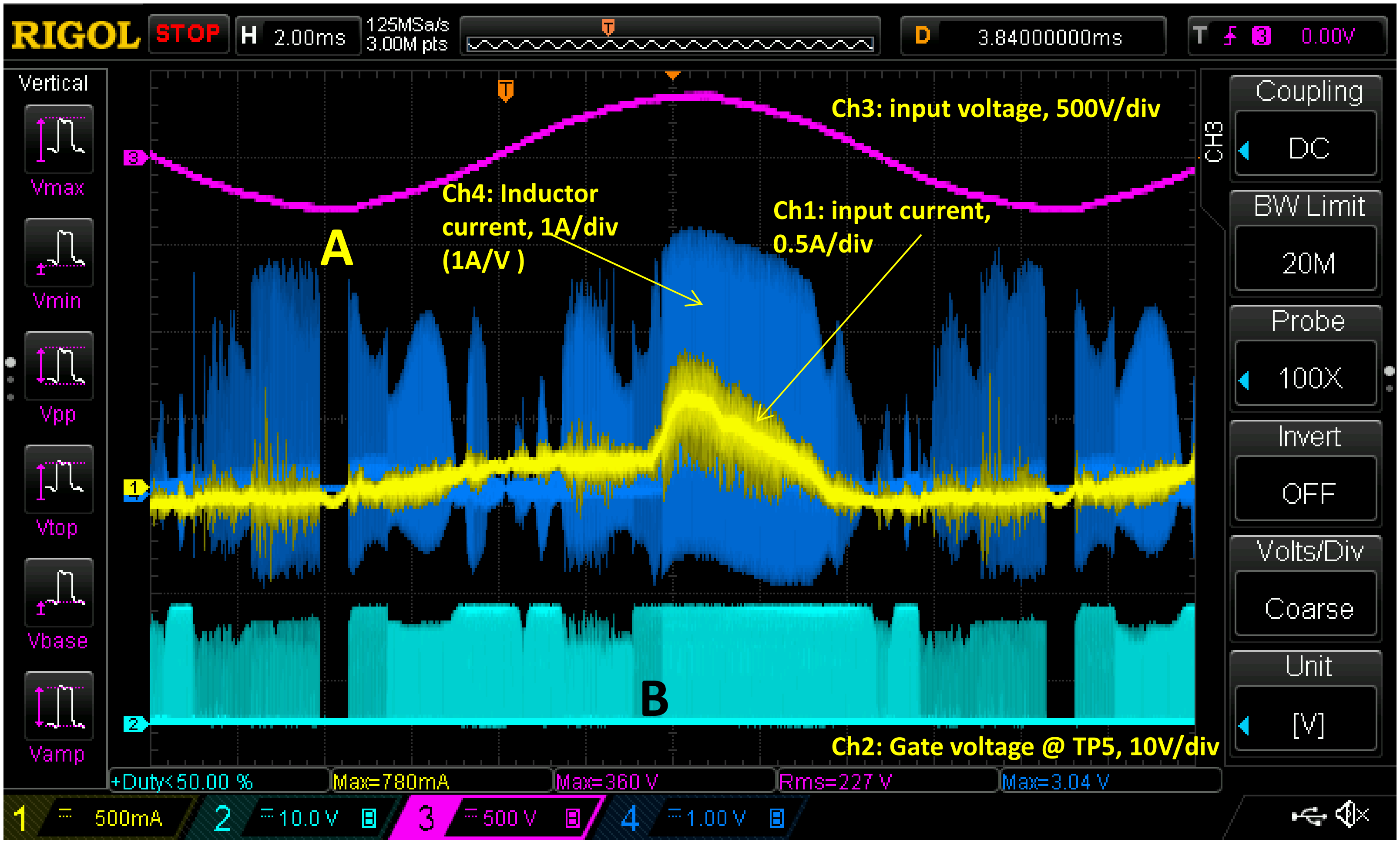
At 85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

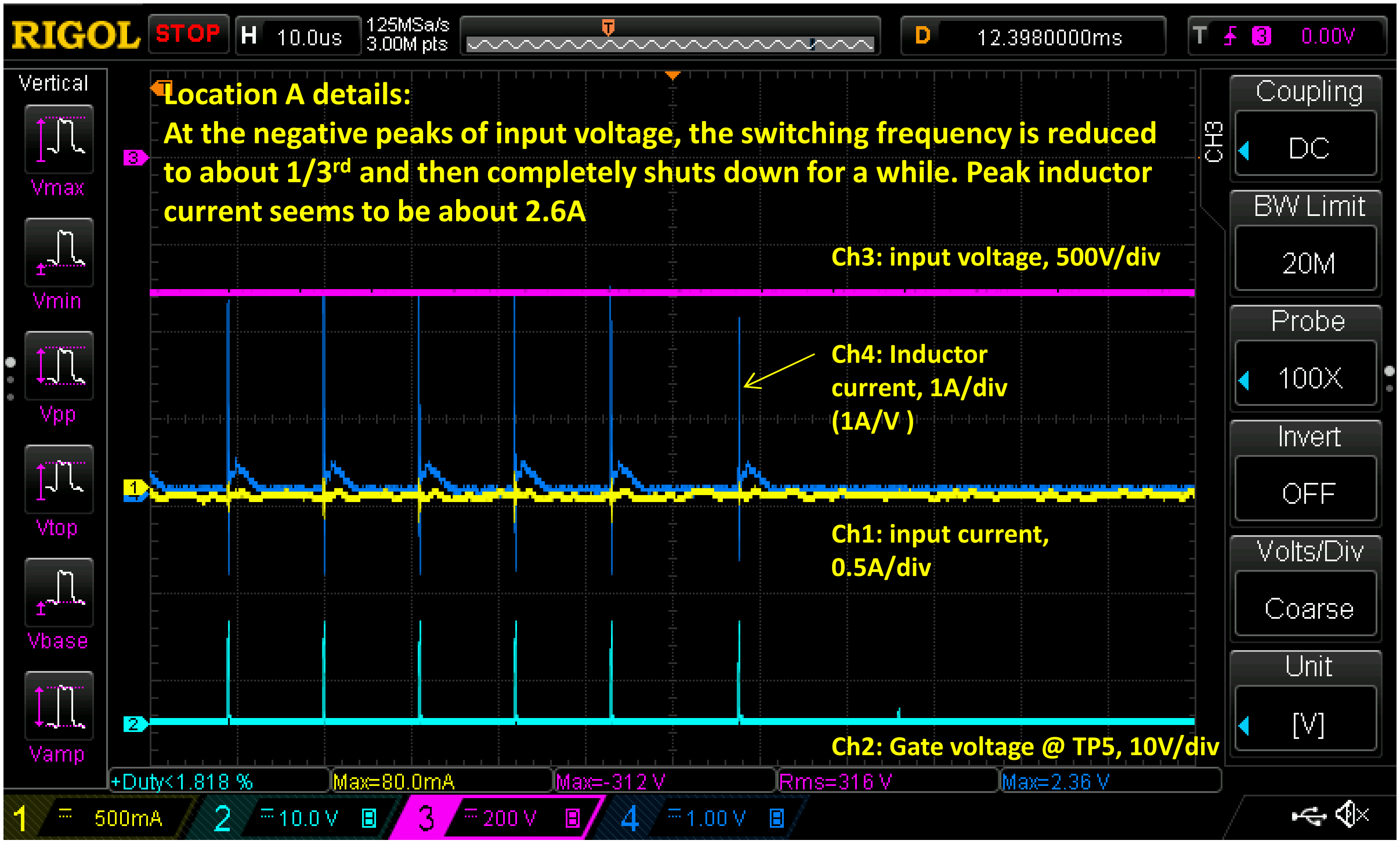
At ~230Vac input voltage and ~25W external load, distortions observed. See next slides for location A, B details



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

At ~230Vac input voltage and ~25W external load, distortions observed.

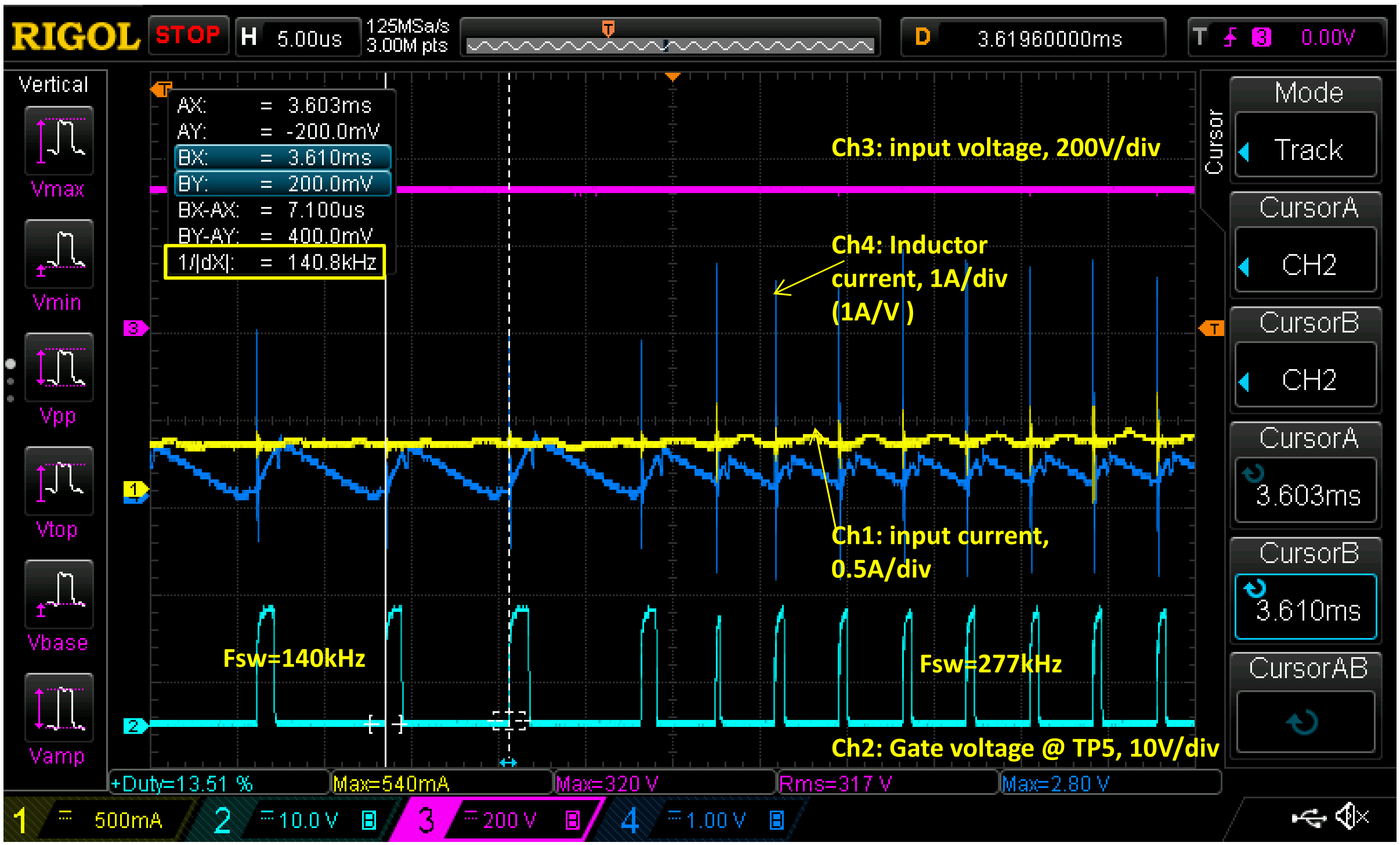


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

<u>Location B details:</u>

At the positive peaks of input voltage, the switching frequency is reduced to about ½ and this results in "flat top" on the current waveform. After that the switching frequency is raised and around that time the current surge is observed

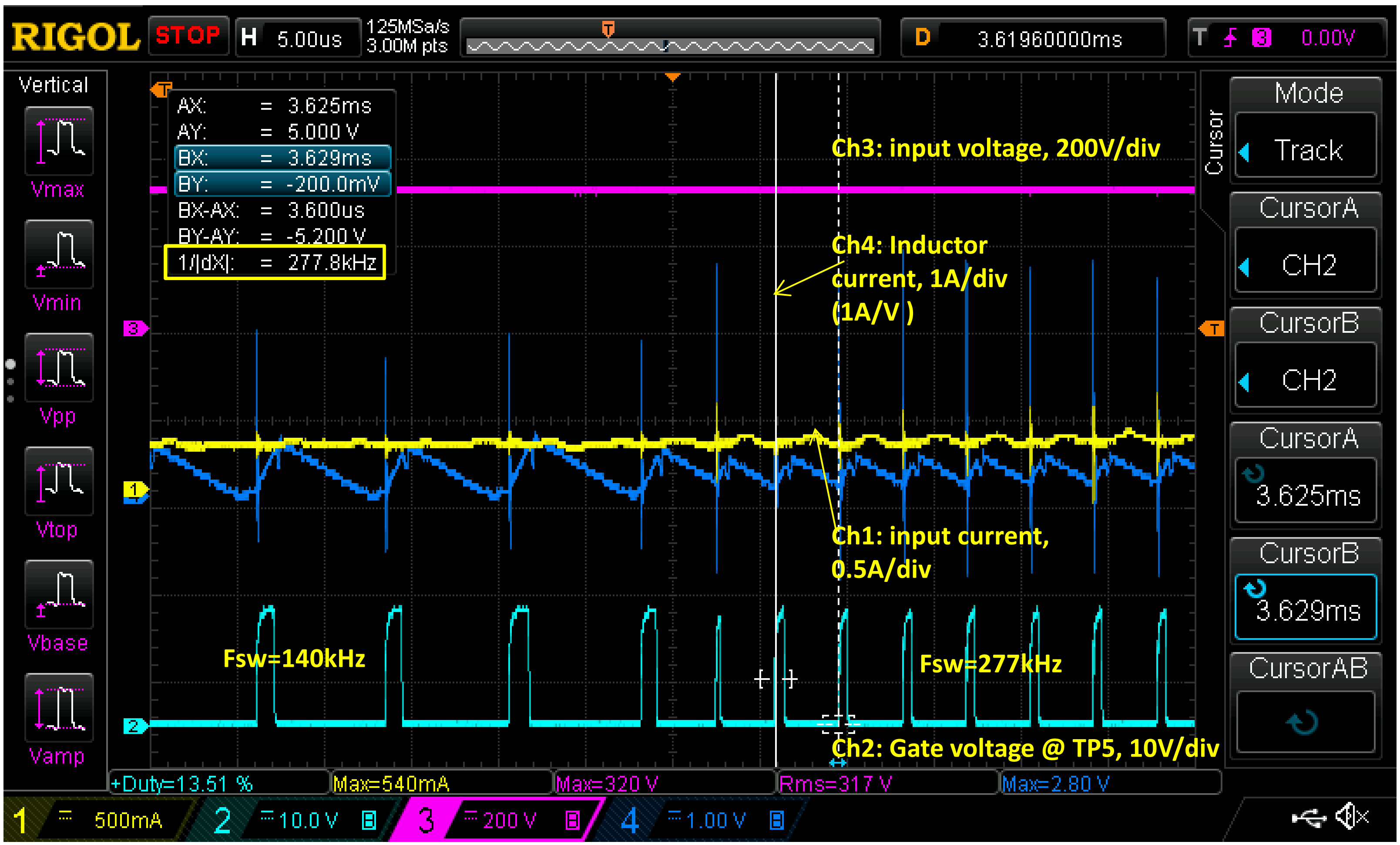


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

<u>Location B details:</u>

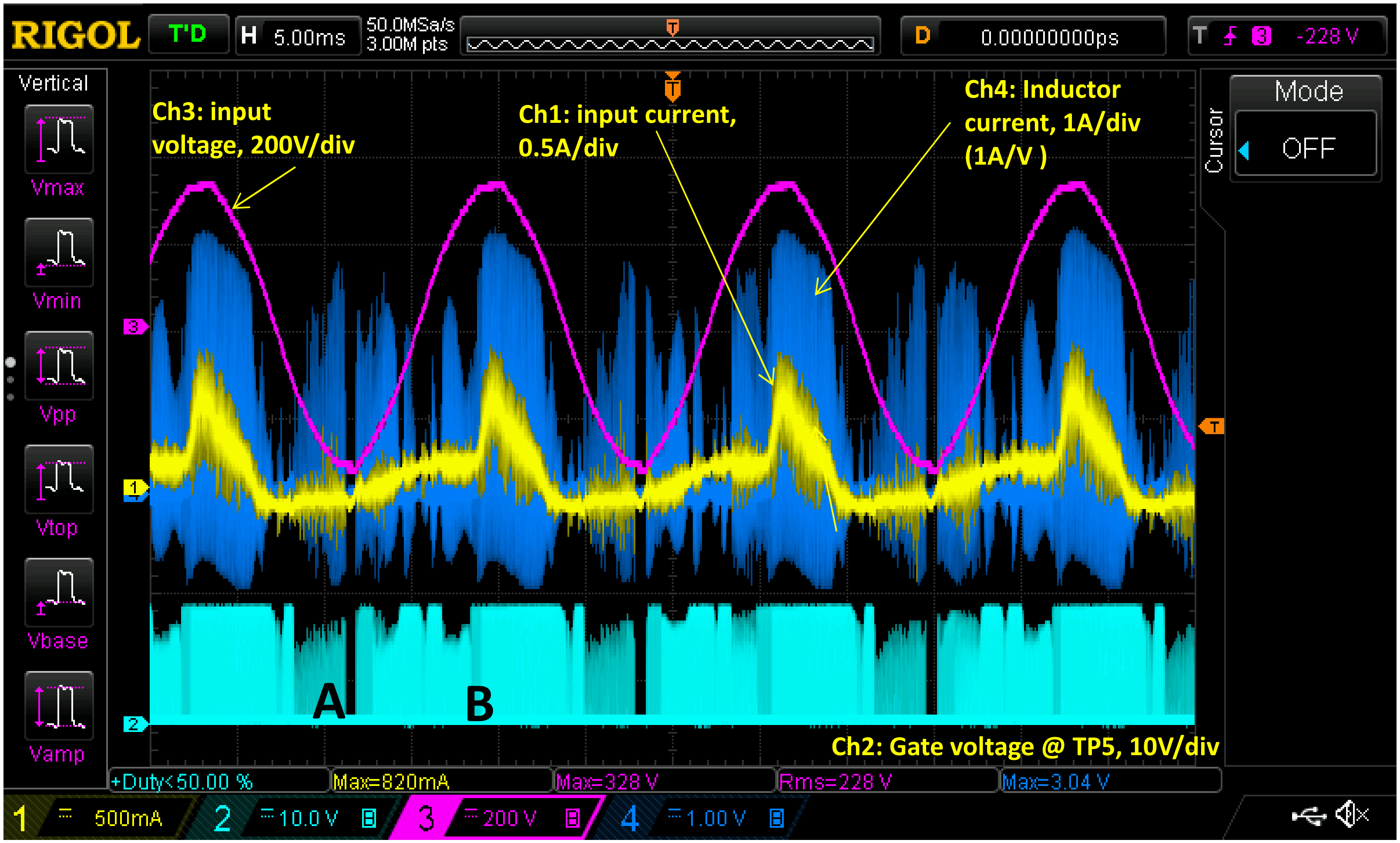
At the positive peaks of input voltage, the switching frequency is reduced to about ½ and this results in "flat top" on the current waveform. After that the switching frequency is raised and around that time the current surge is observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

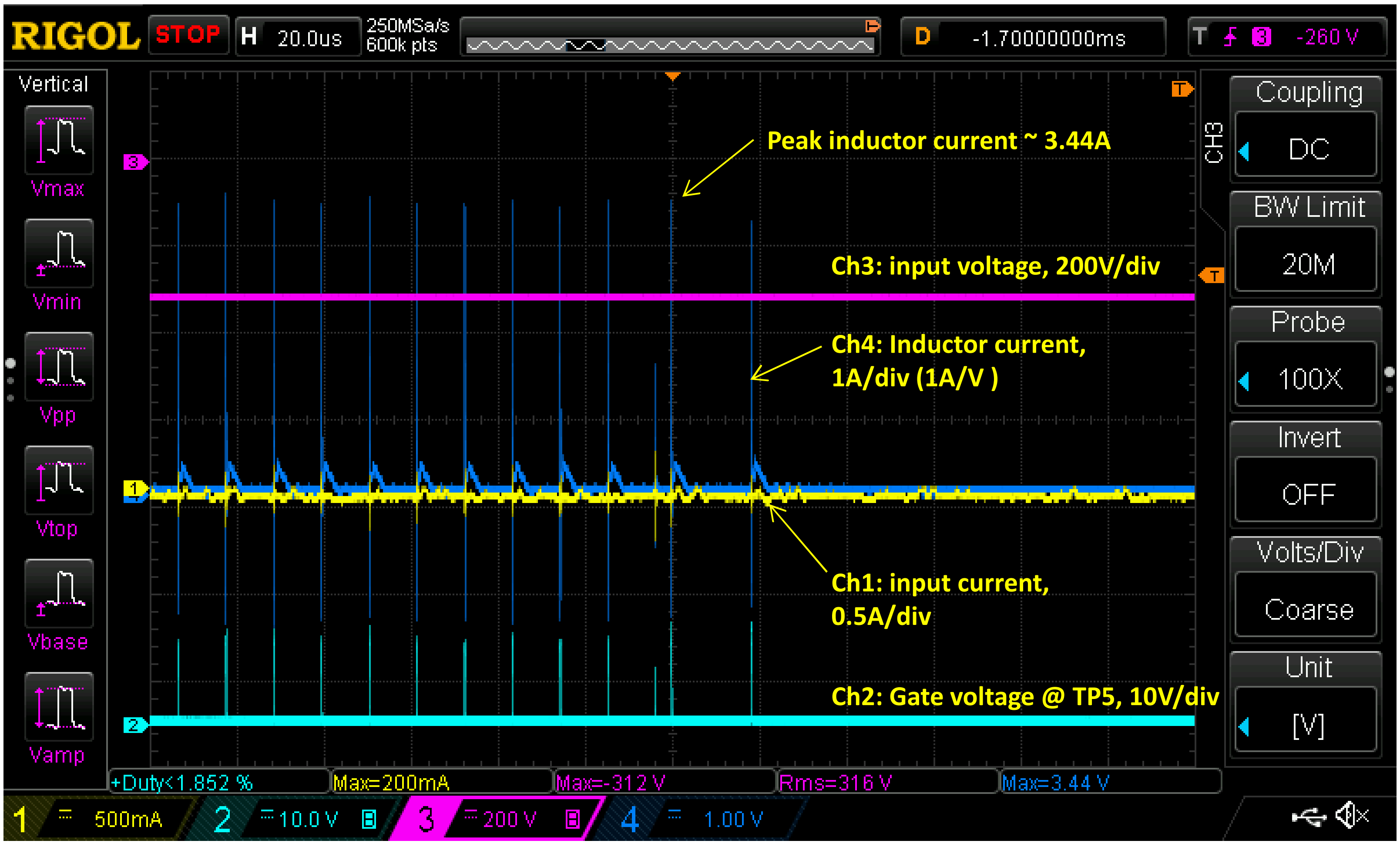
At 230Vac input, 25W external load, the view of locations A (negative peak) and location B (positive peak)



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

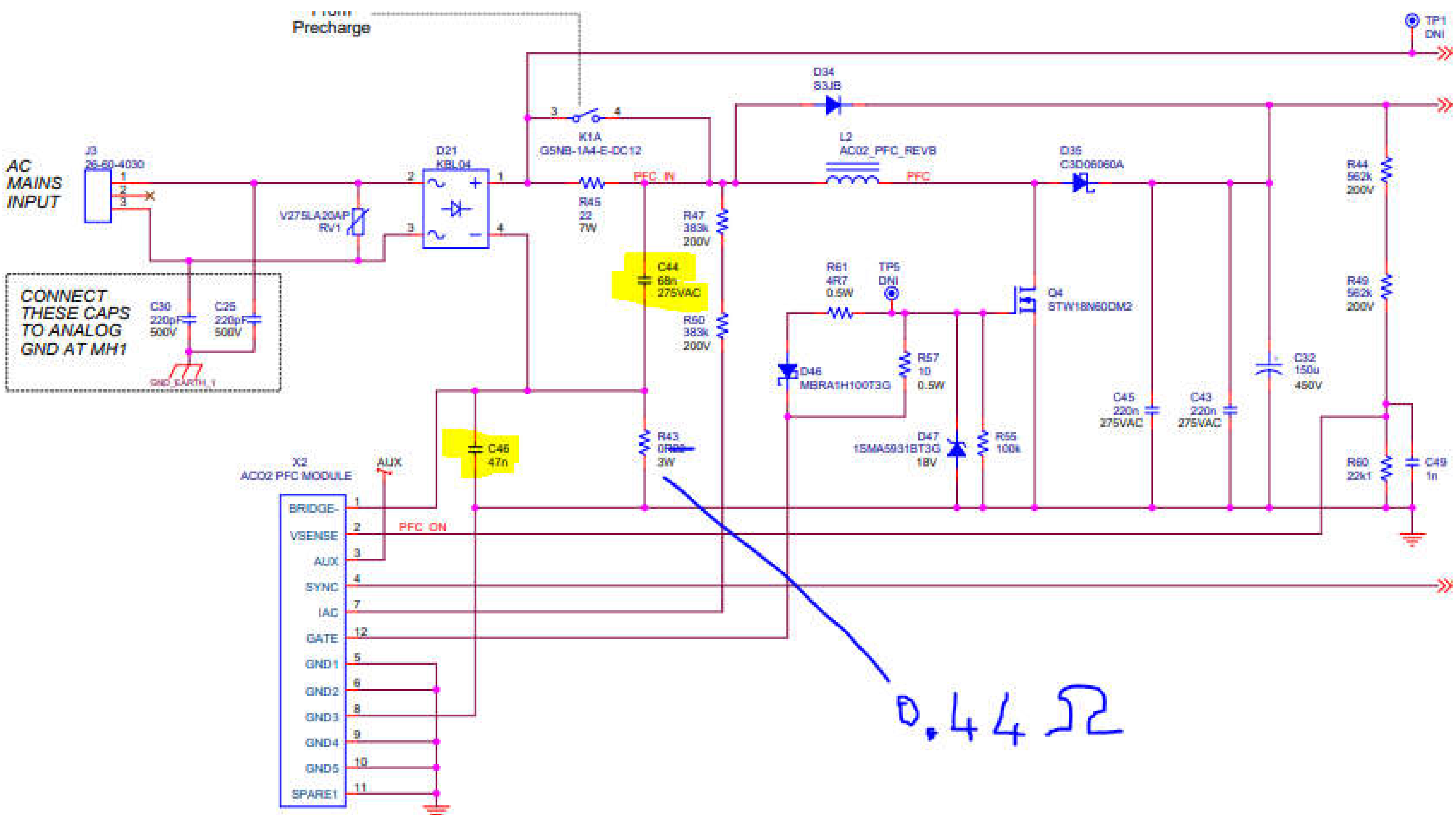
Location A: Current probe on Ch1 has low BW and is used to measure input current only.



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

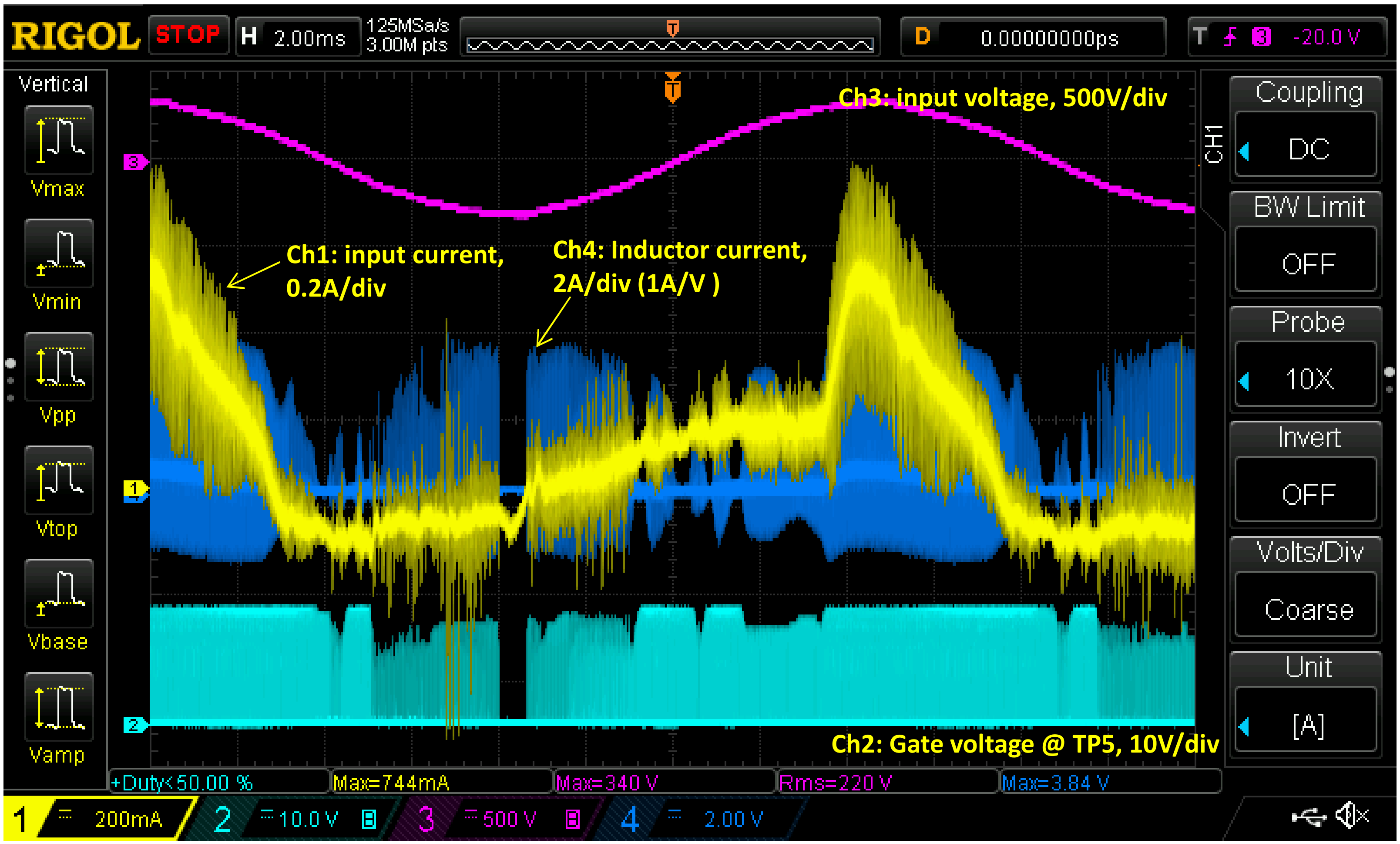
There is a 68nF cap after the rectifier. It is increased to 2x68=136nF, did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

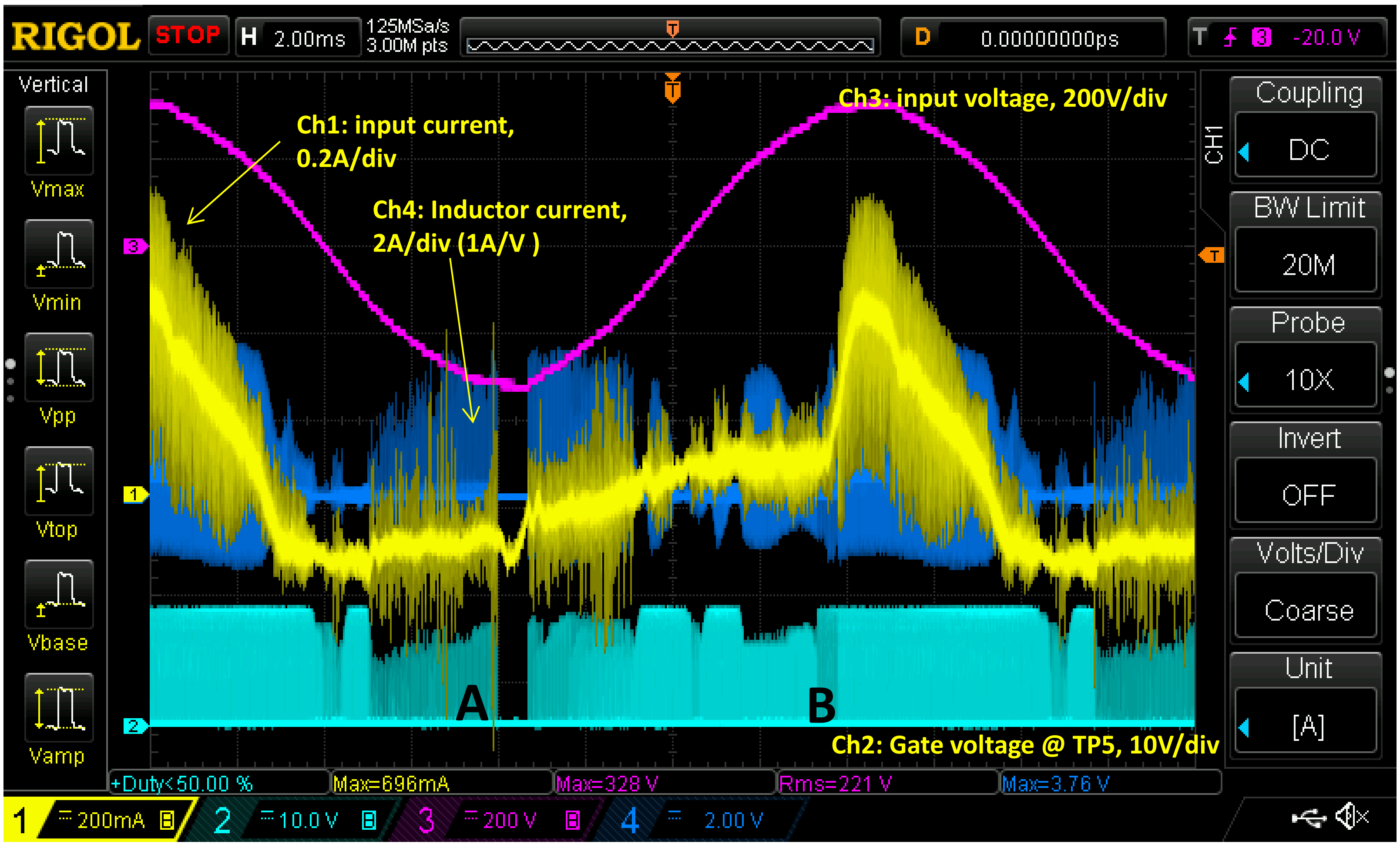
There is a 68nF cap after the rectifier. It is increased to 2x68=136nF, did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

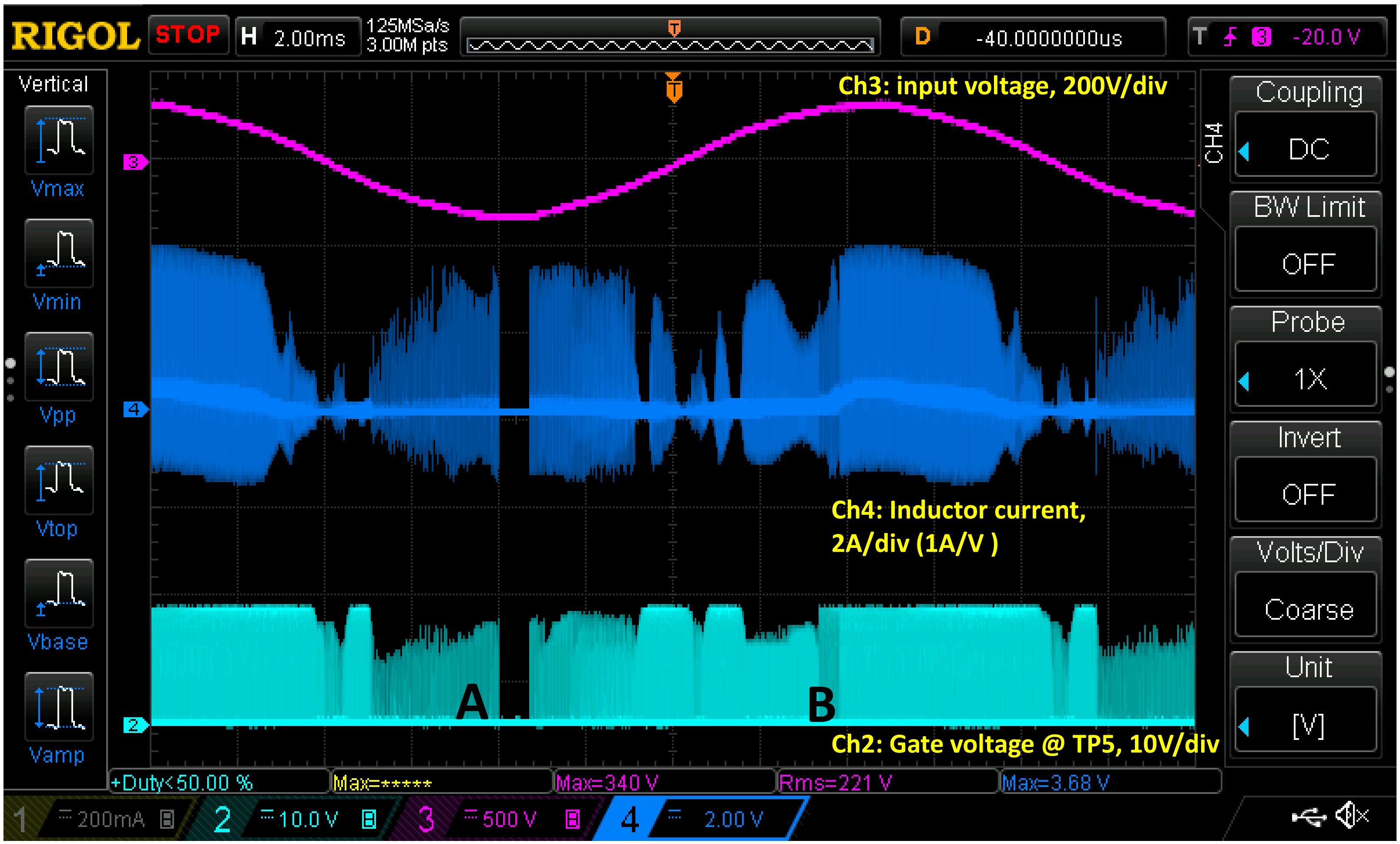
Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

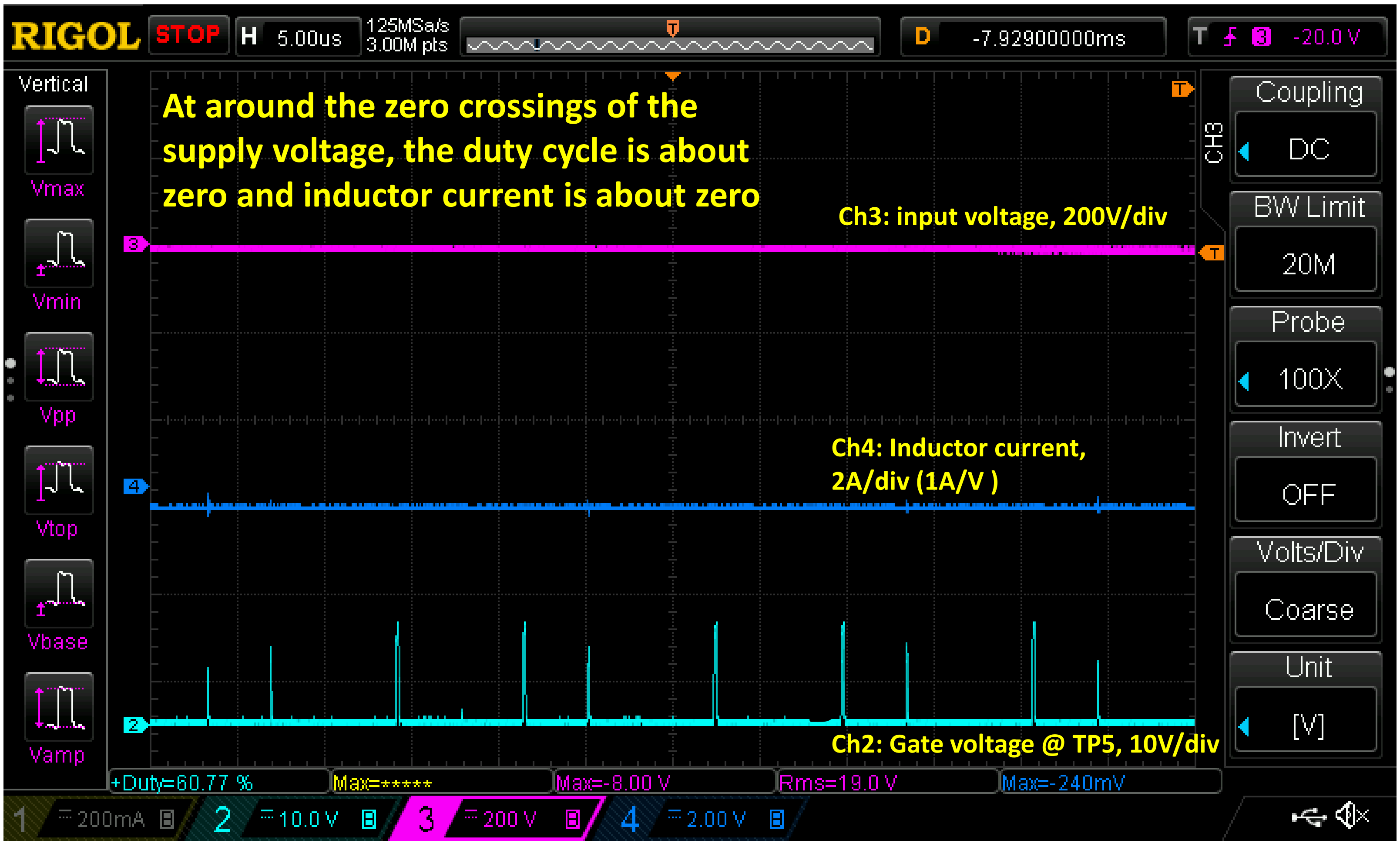
Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

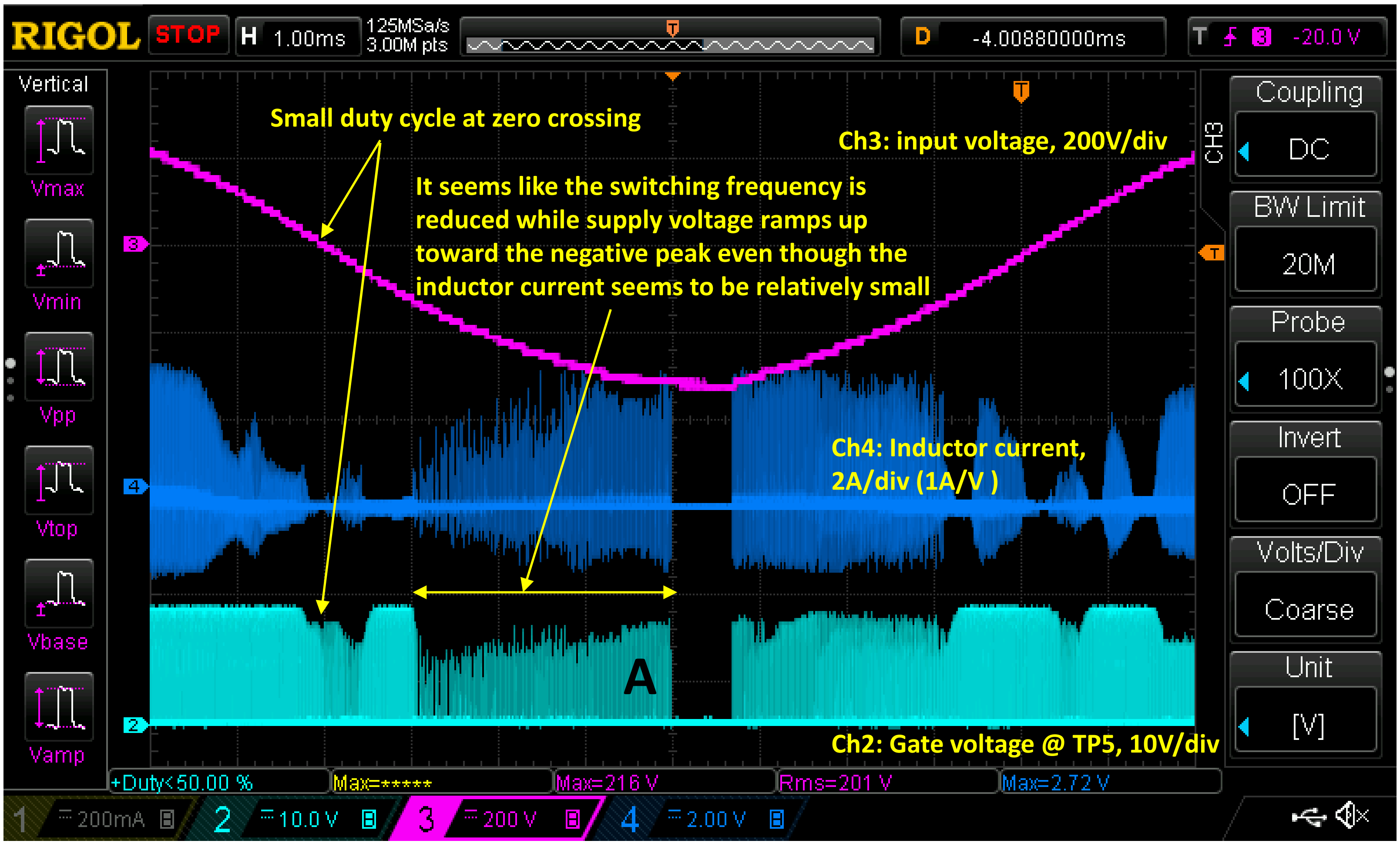
Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

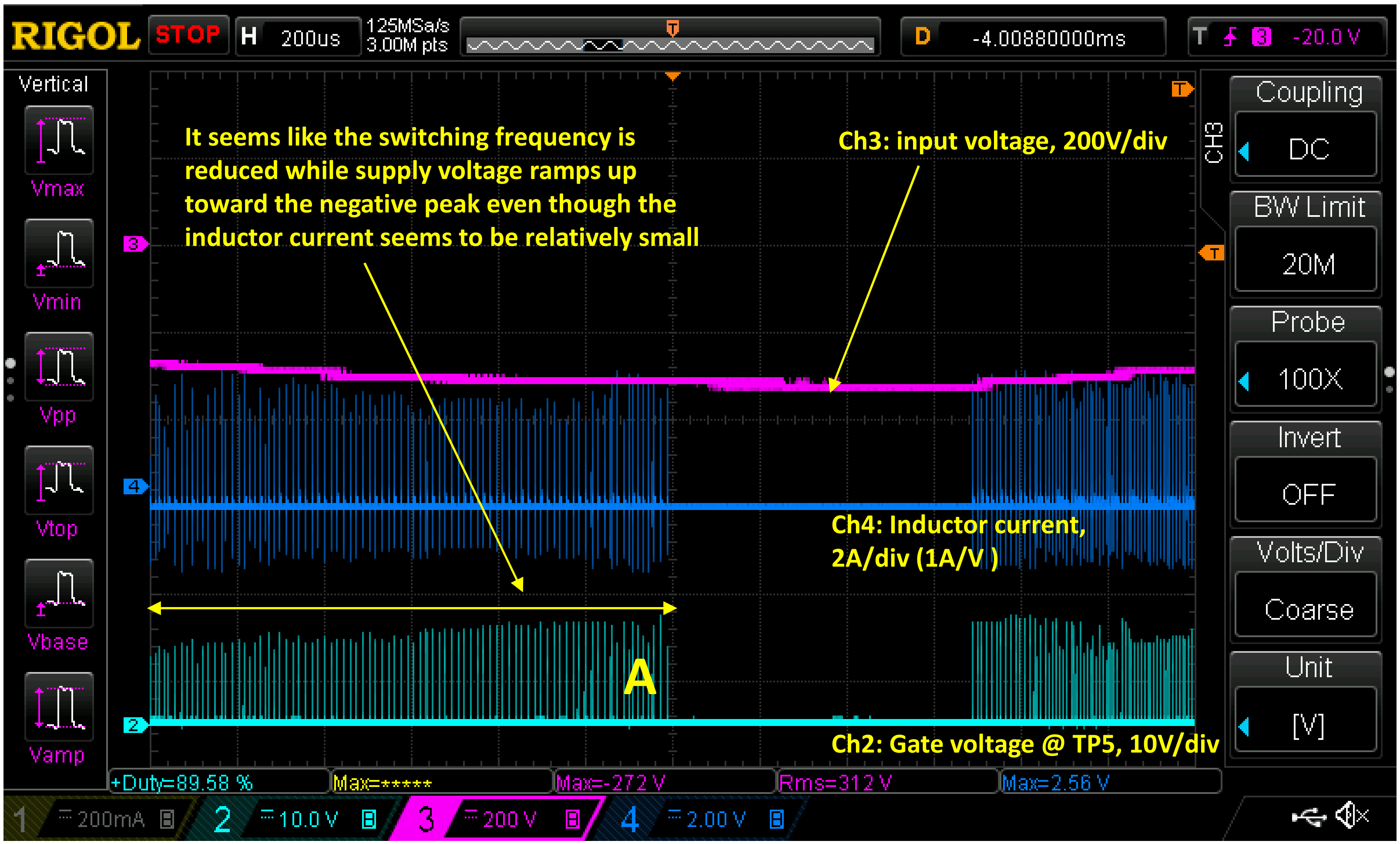
Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

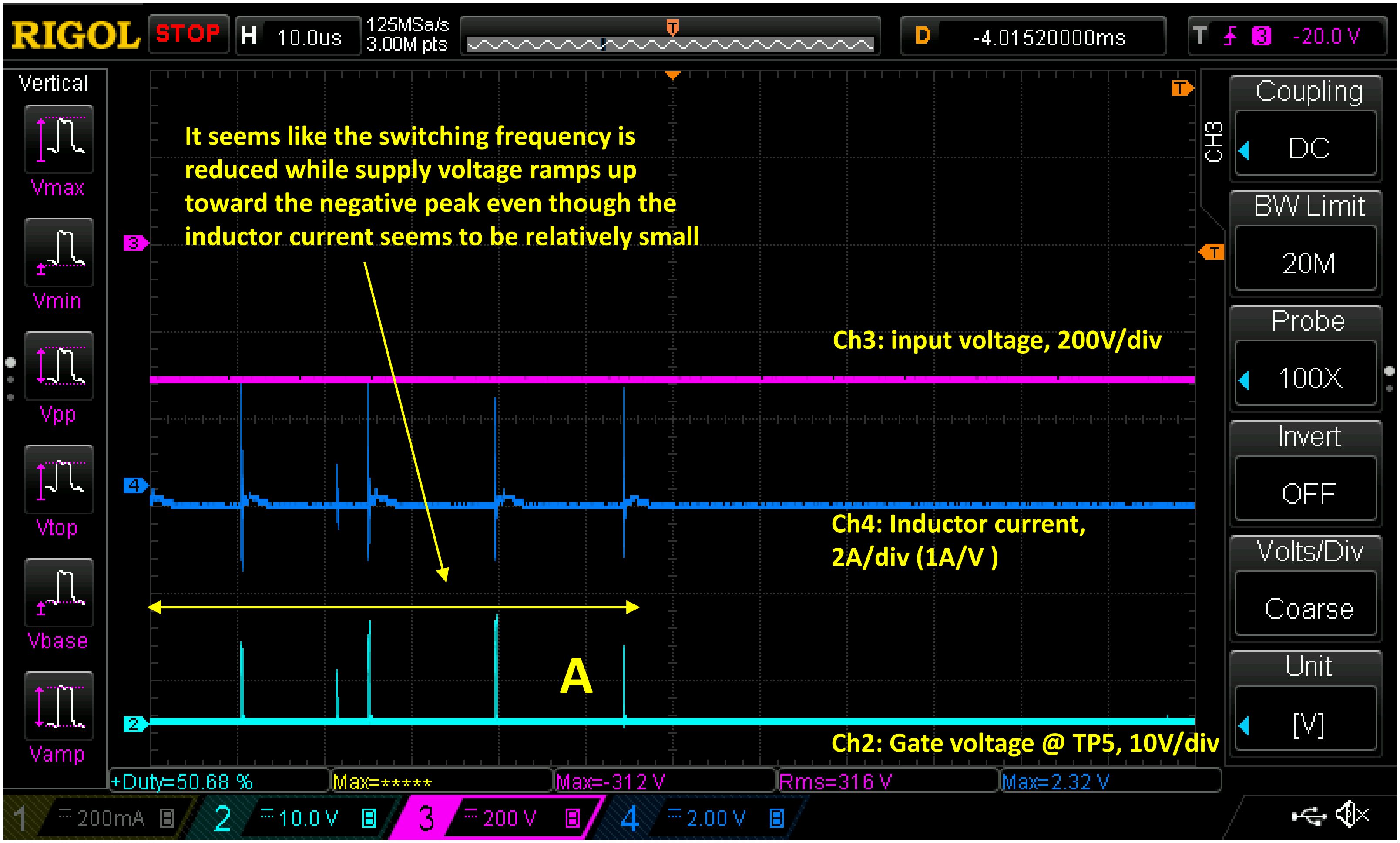
Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Observations:

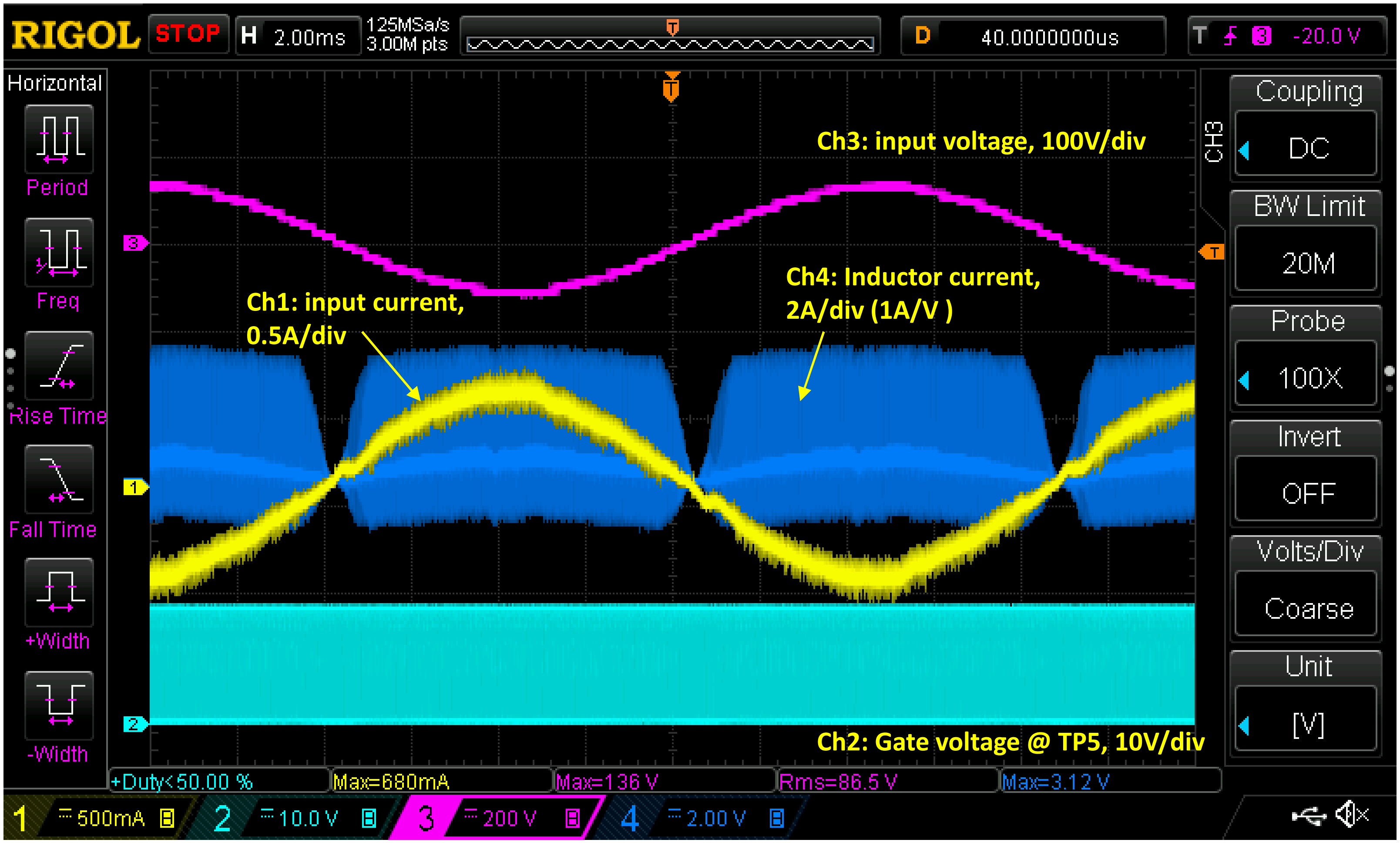
1) Location A: While the supply voltage ramps up toward the negative peak, the switching frequency is reduced significantly and then MOSFET shuts down for a while at the negative peak. It seems like the inductor current is relatively small and this may not be current limit initiated turn off.
2) Location B: While the supply voltage ramps up toward the positive peak, the switching frequency is reduced by about 50%. It is observed this corresponds to "flat top" on supply current. At around the peak of supply voltage, the switching frequency suddenly snaps back to normal frequency and this corresponds to surge in peak of the supply voltage. It is not clear if this phenomenon is caused by activation of current limit.
3) Adding an other 68nF cap after rectifier did not improve the issue
4) Adding 100nF cap across R5 (R7 on data sheet) did not improve the issue

Measuring inductor current vs gate voltages, 12/25

PCB	RefDes on datasheet	RefDes in design	12/11/2022 Fci=44kHz, Gci=5.6	12/25/2022 Fci=11kHz, Gci=1.6
PSB-04	R1	R47, R50	383K	383K
	R2	R43	**0.44**	0.44
	L1	L2	660uH	660uH
PFC-03	R8, R12	R4, R9	**2.74K**	2.74K
	R13	R10	**15.8K**	**4.7K**
	C6	C6	**233pF (200p//33p)**	**3.3n**
	C7	C8	**33pF**	**150pF**
	R15	R11	30.1K	30.1K
	C8	C9	4.7uF	4.7uF
	C10	C1	1.5uF	1.5uF
	C11	C2	150nF	150nF
	R21	R1	48.7K	48.7K
	R14	R13	10K	10K
	R7	R5	**1.50K (3.3K//2.74K) +100pF**	1.50K (3.3K//2.74K) **+ 100pF**
	C9	C4	1uF	1uF

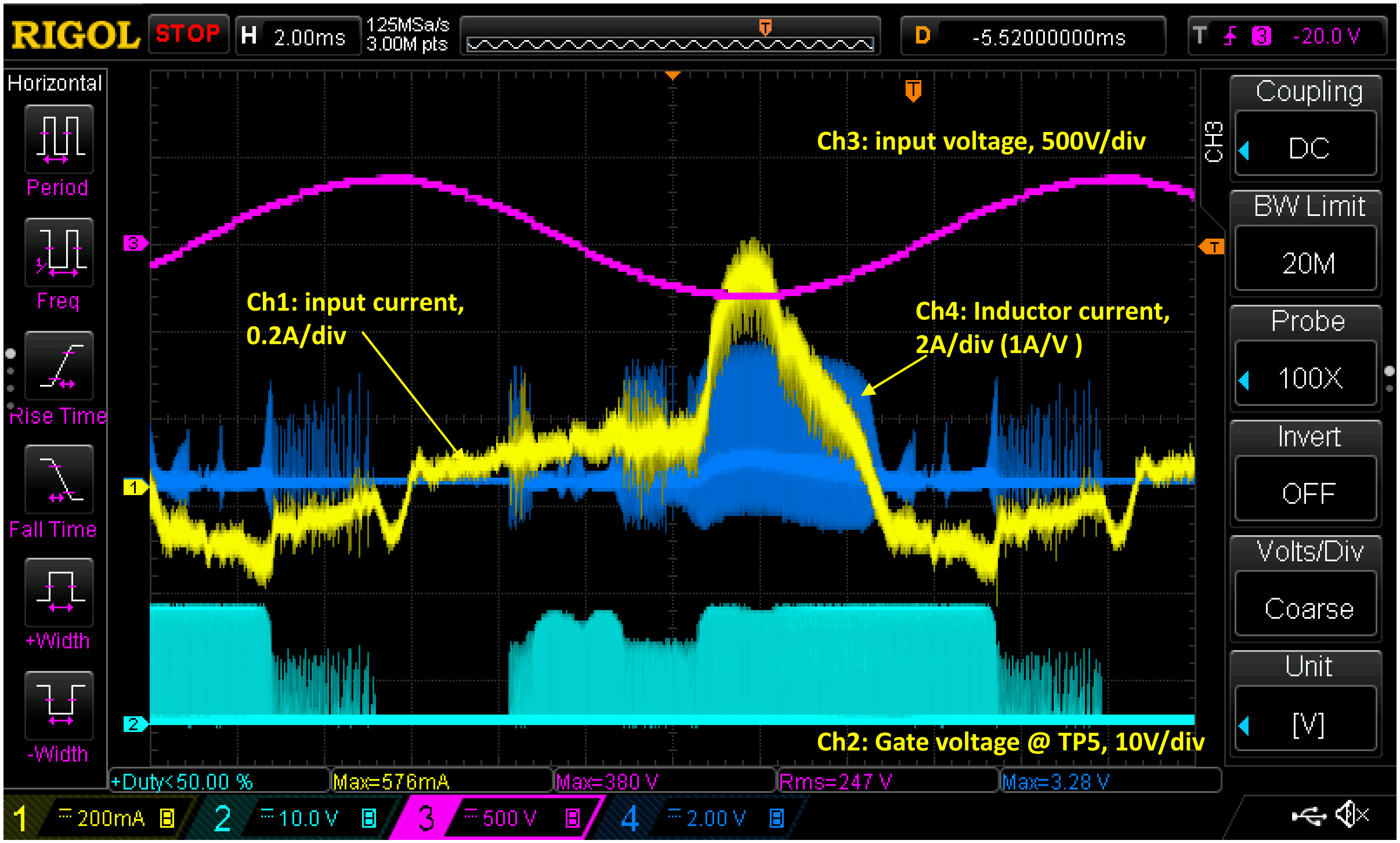
Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55
At ~85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55
At ~230Vac input voltage and ~25W external load, major distortions observed



Measuring inductor current vs gate voltages, 12/28

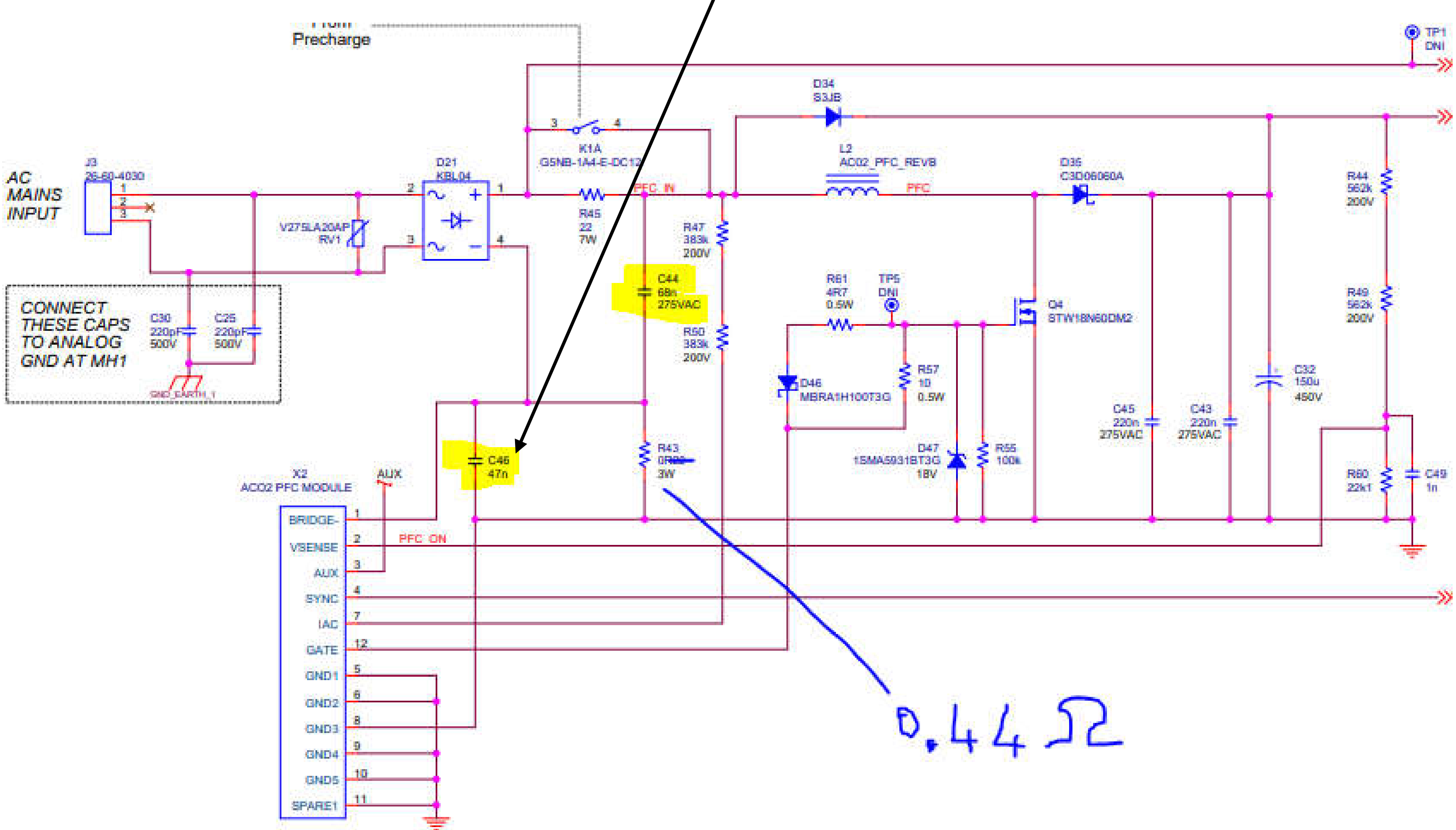
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage and ~25W external load, major distortions observed

Investigating the effect of C46 on input current distortions



Measuring inductor current vs gate voltages, 12/28

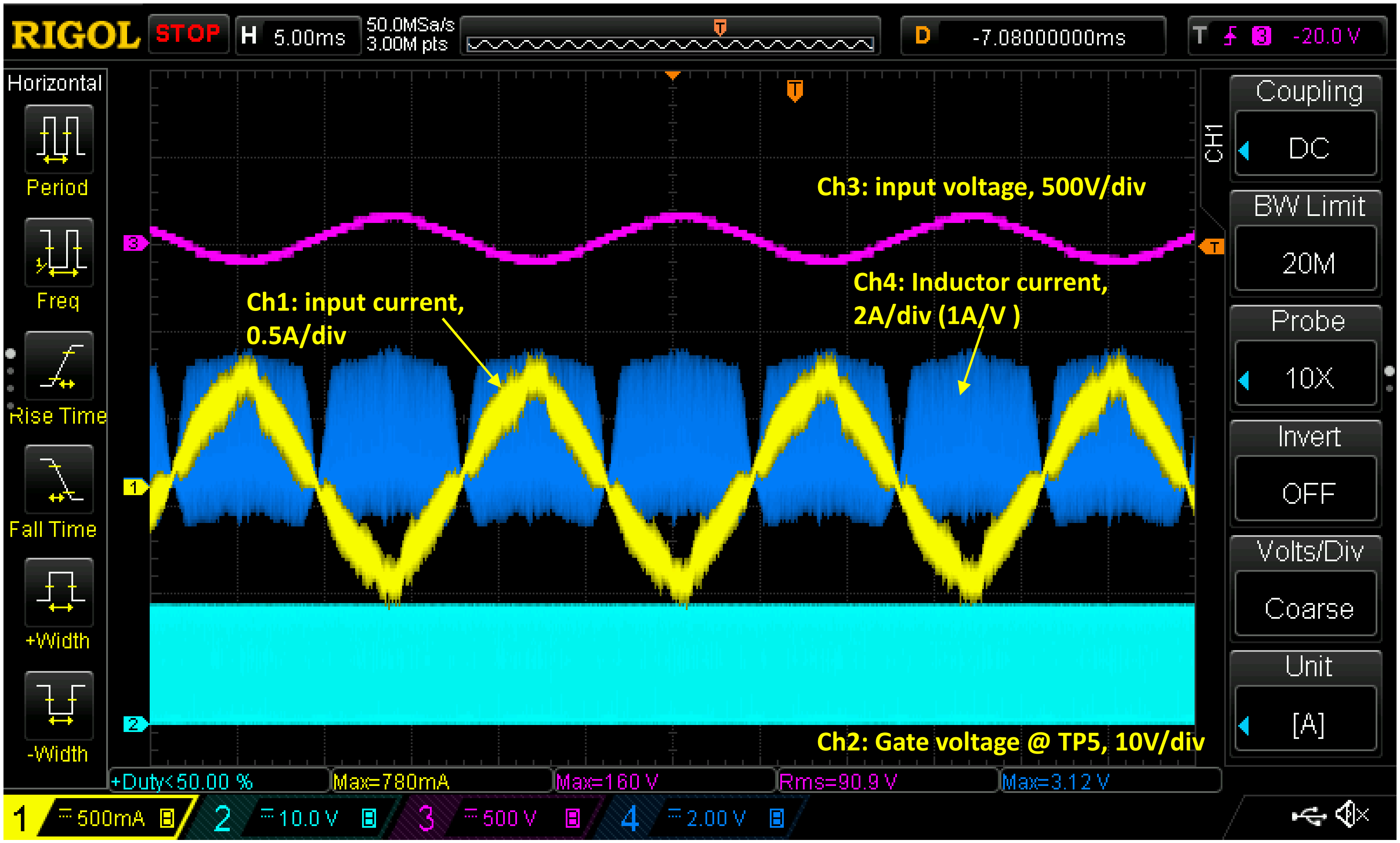
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At 90Vac input voltage, no C46, no major distortions observed

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

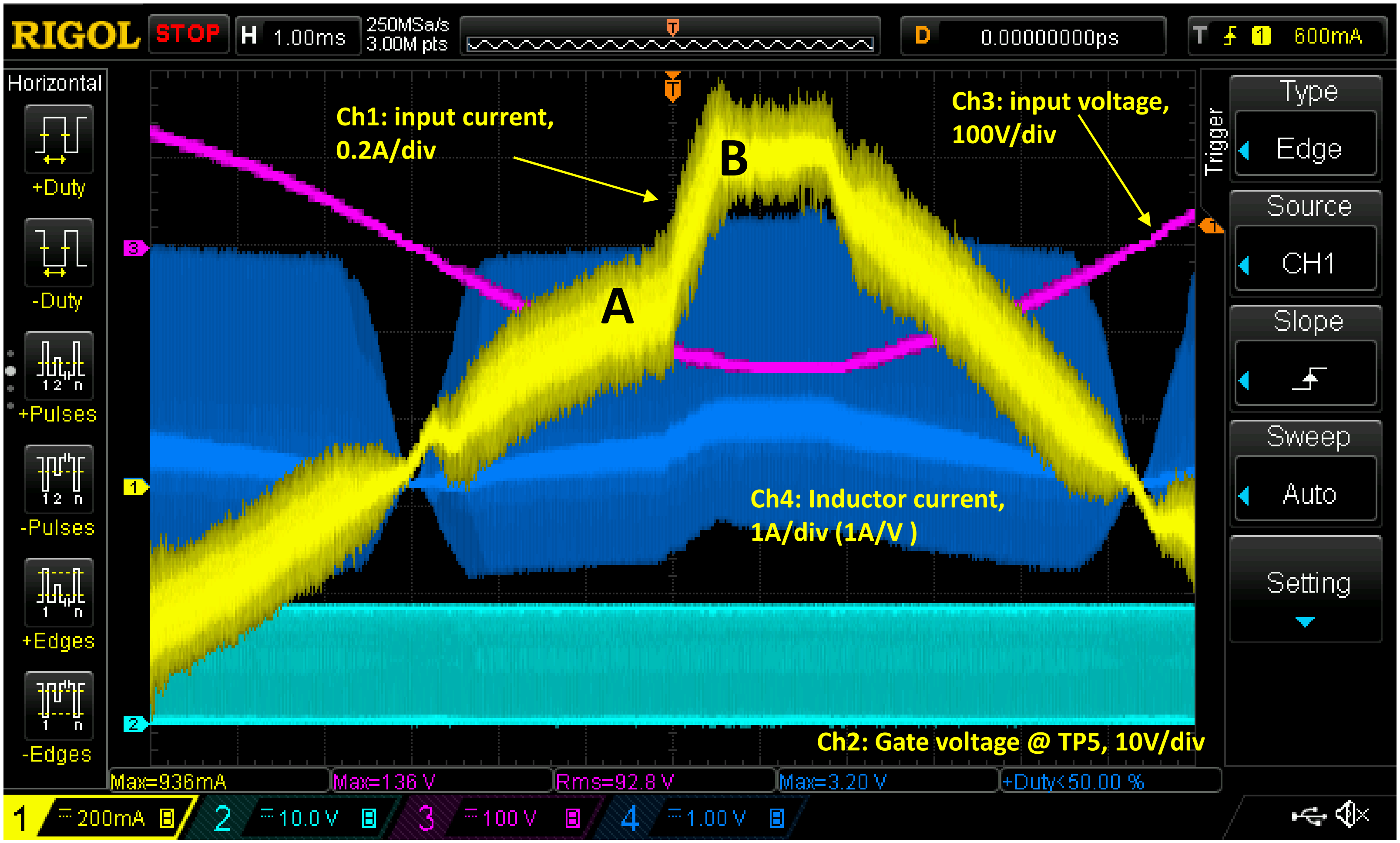
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~100Vac input voltage, <u>no C46</u>, distortions started, notice the current surge from location A to B

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

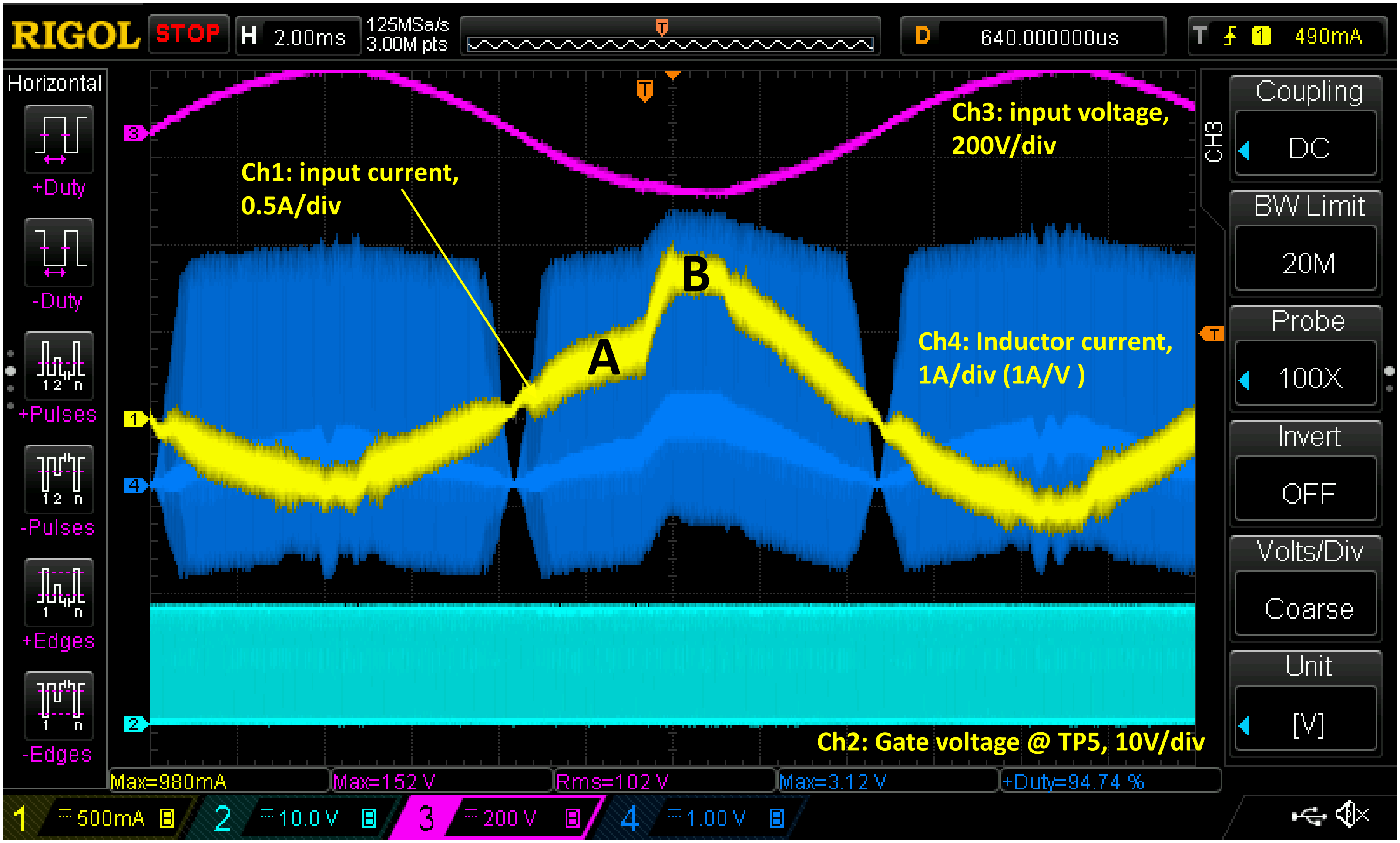
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~100Vac input voltage, no C46, distortions started

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

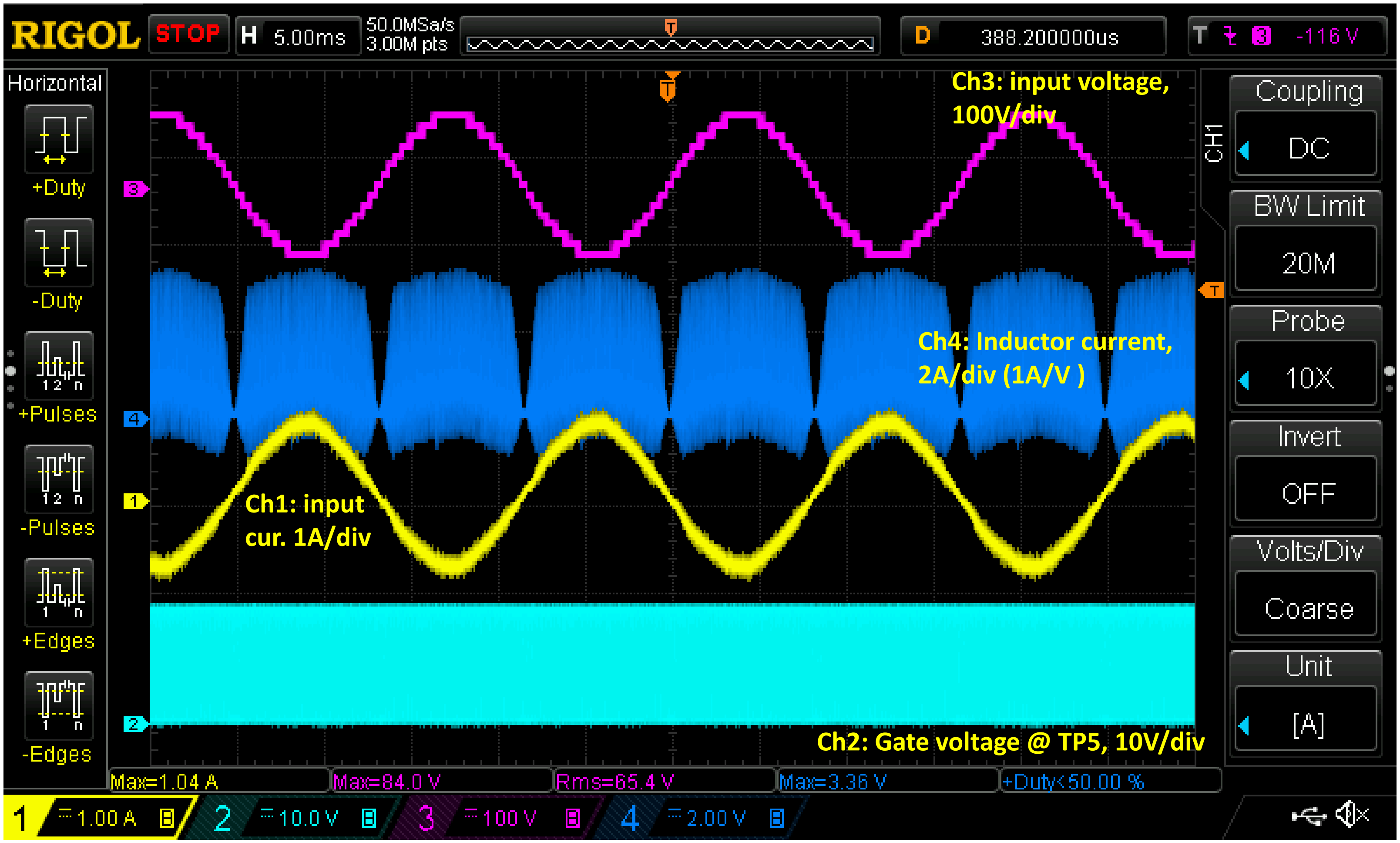
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~85Vac input voltage, <u>C46=100nF</u>, no major distortions

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

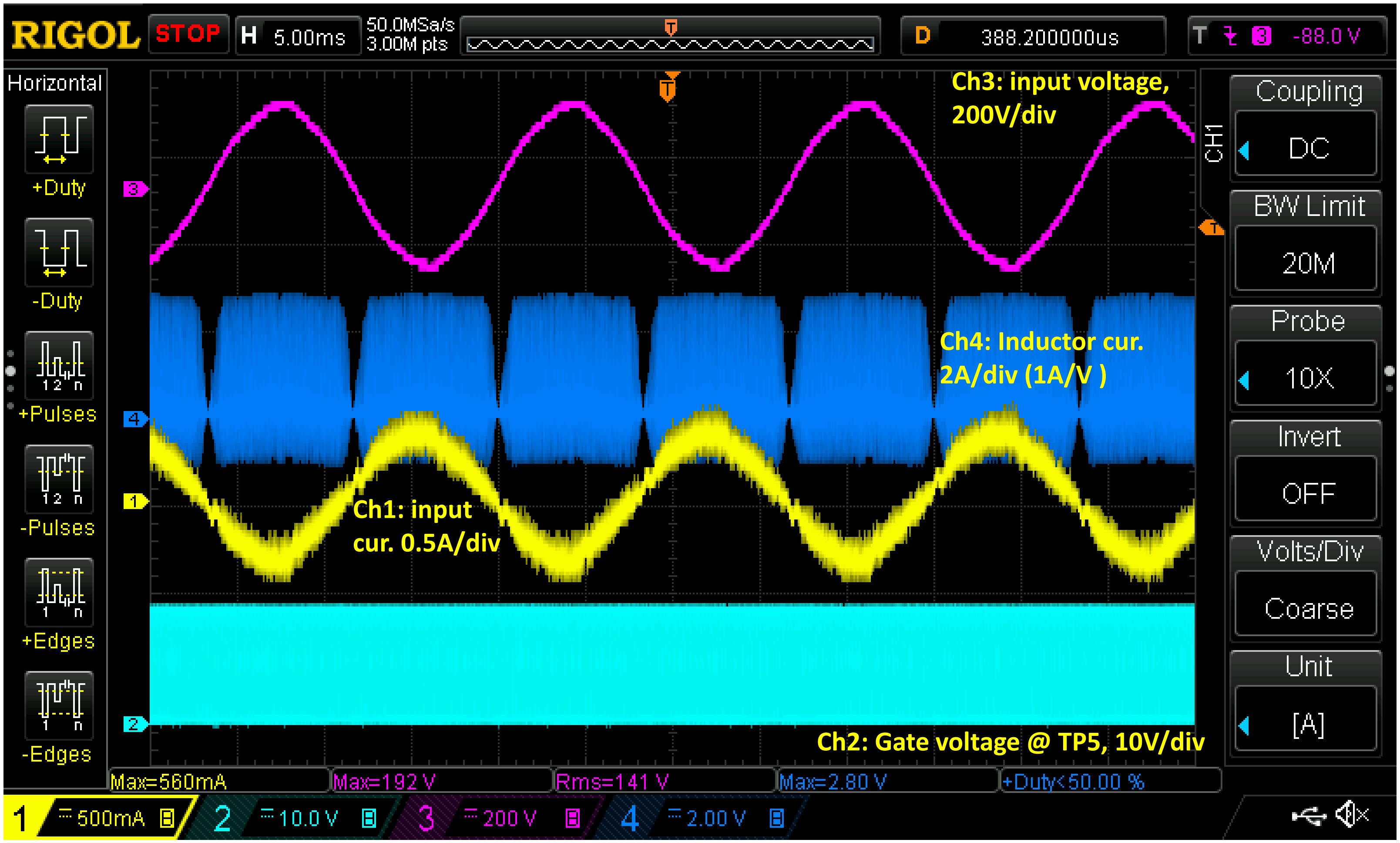
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~140Vac input voltage, <u>C46=100nF</u>, no major distortions

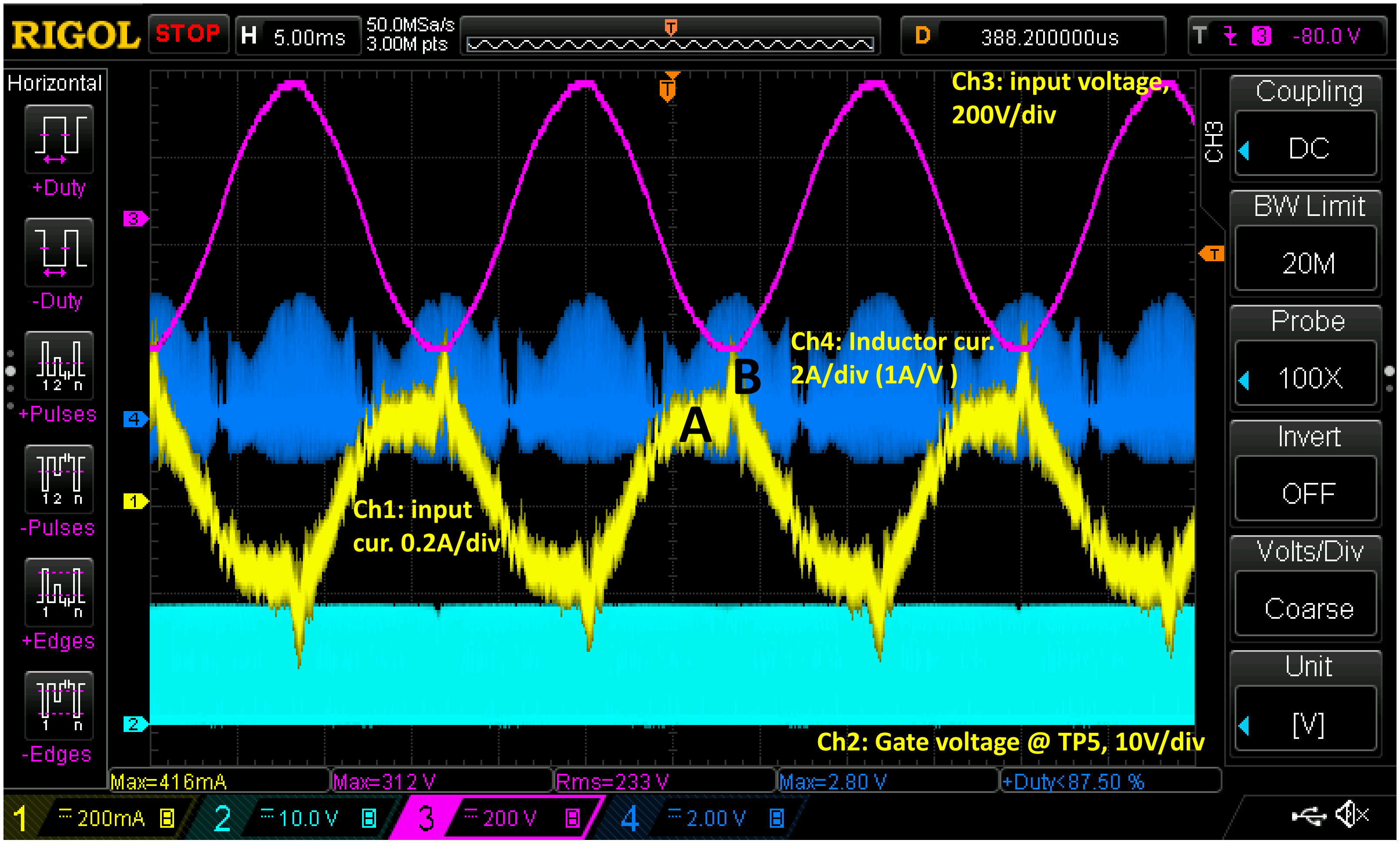
Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55

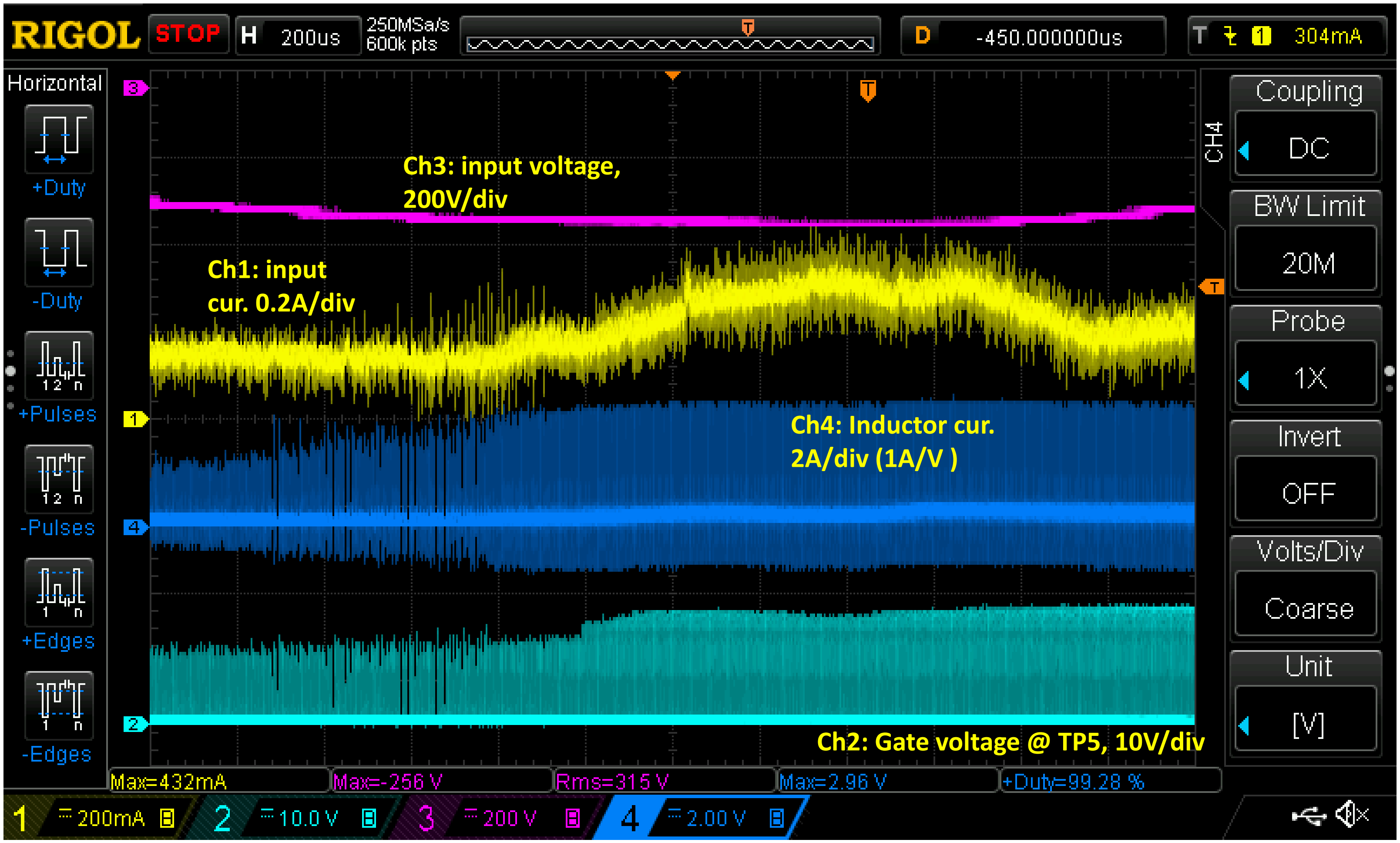
At ~230Vac input voltage, C46=100nF, symmetric distortions show up on peaks of voltage waveform
Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55

At ~230Vac input voltage, C46=100nF, location A; ON times gets very small & pulses start to drop
Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

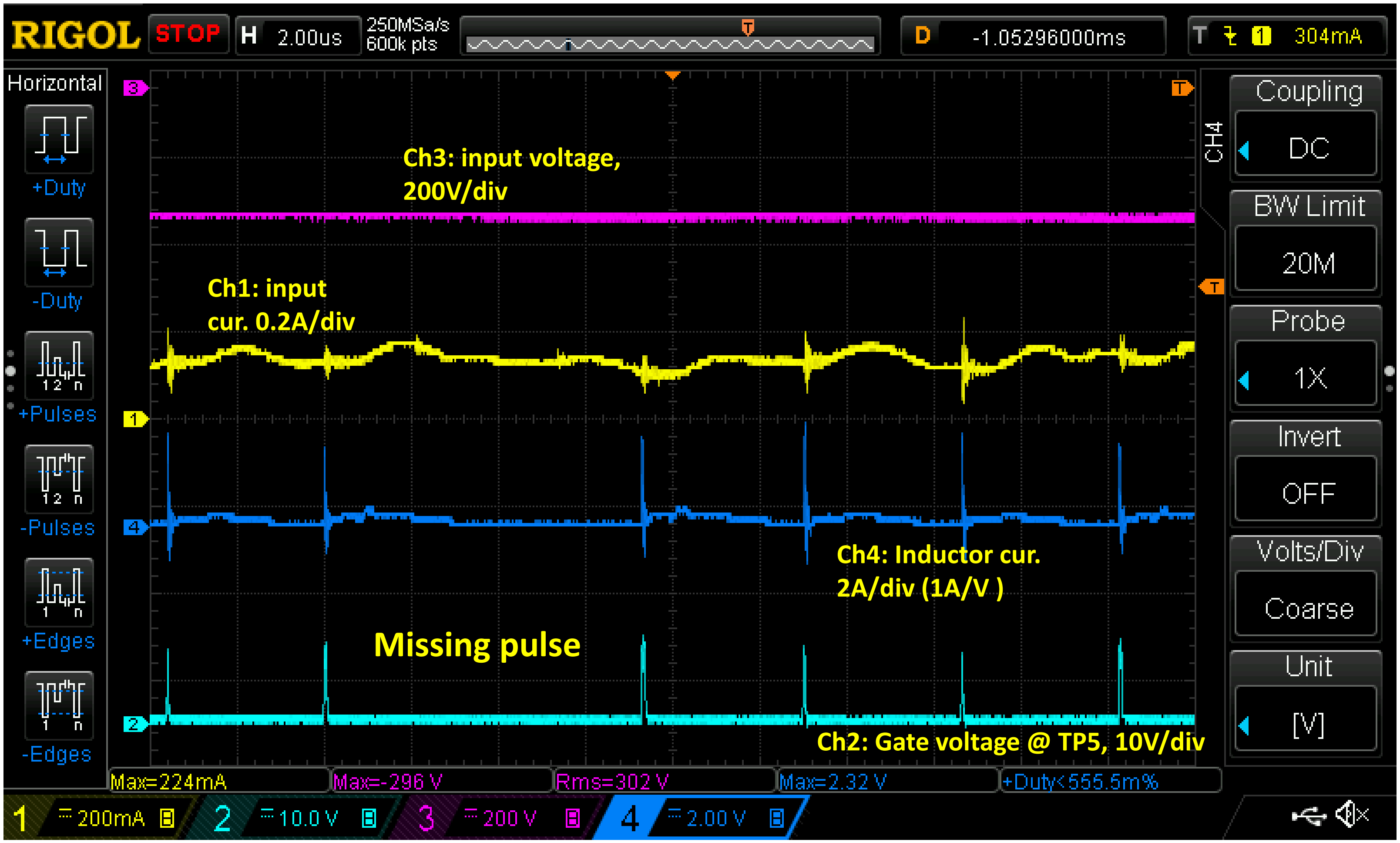
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage, C46=100nF, location A; ON times gets very small & pulses start to drop

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55

Conclusions on 12/28:

1) Removing the 47nF cap across the sense resistor made the issue worse that the current became more unstable and distortions started even at low voltages of ~100Vac

2) Replacing the capacitor across the sense resistor (C46) with 100nF, did not improve the problem that the current waveform was stable up to ~ 230Vac and distortions started above this voltage, as it was the case with C46=47nF

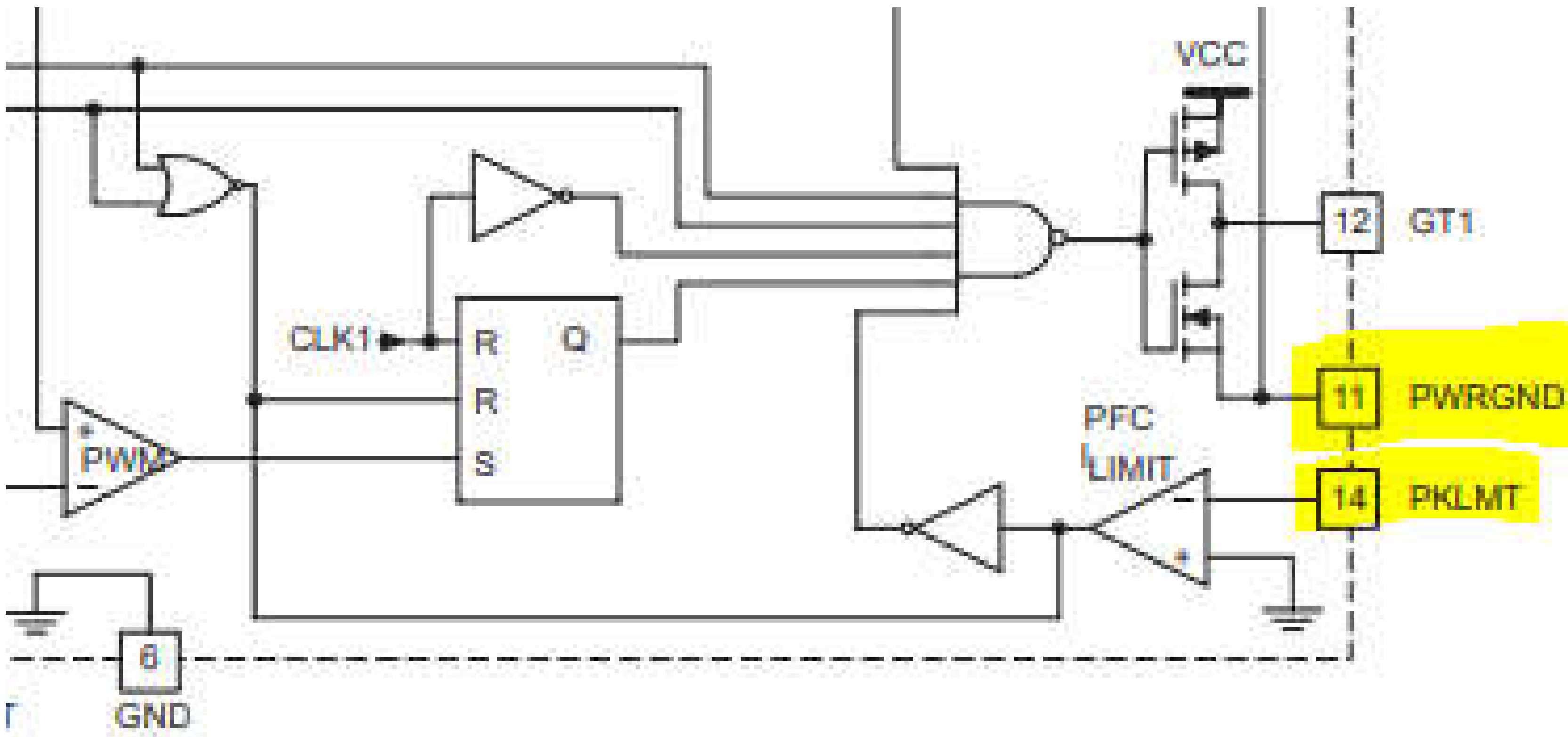
3) Referring to location A; it appears that the duty cycle gets very small and even some pulses were dropped even though the current through the inductor does not appear to be the max. This suggests that the event is not initiated by peak current limit

4) Referring to location B; at this point no pulse dropping is observed. On the contrary, the duty-cycle increases which results in surge in inductor current.

Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

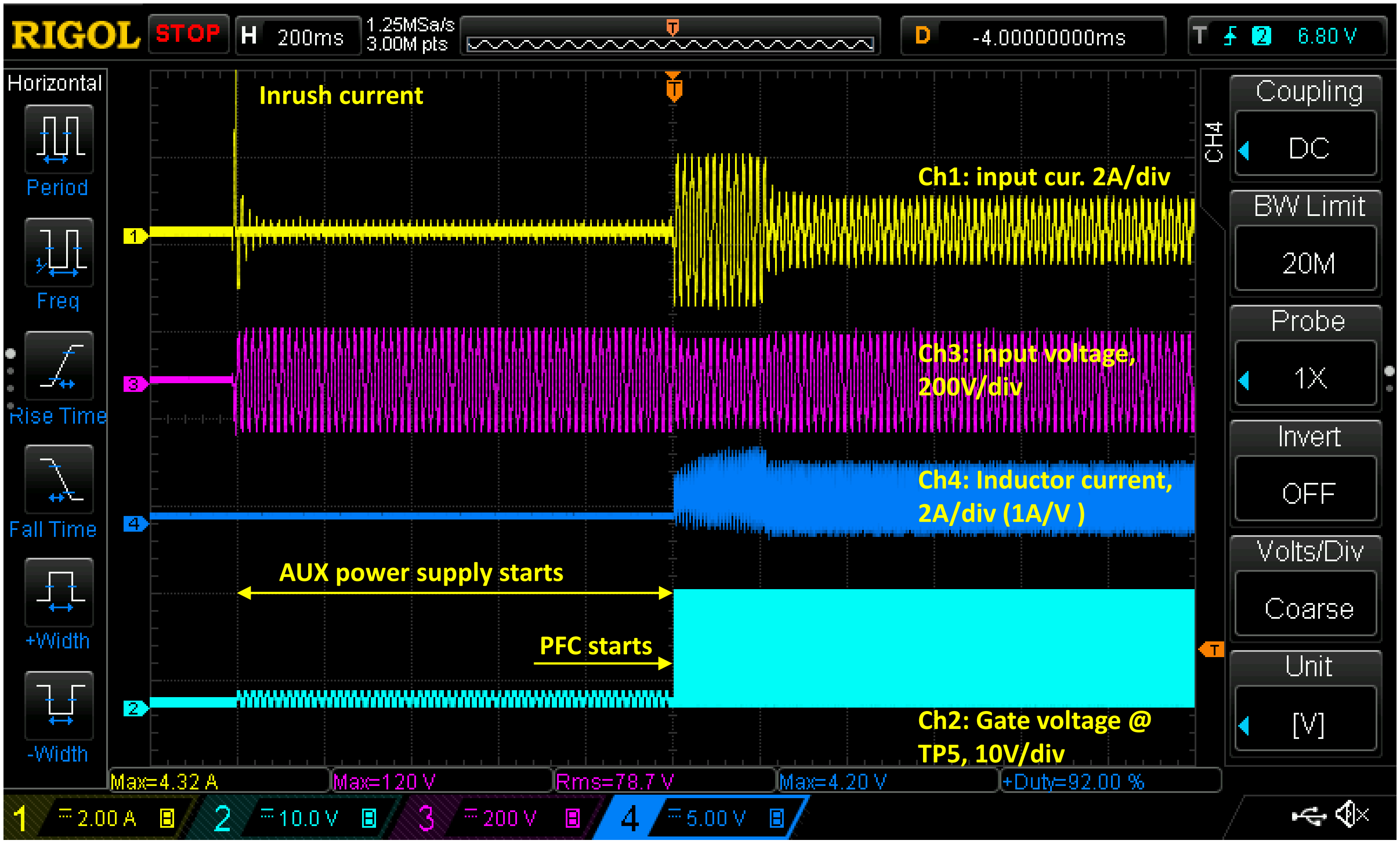
100pF leaded ceramic capacitor was connected from pin14 (PKLMT) to pin11 (PWRGND). No improve observed
After that, a 1nF capacitor was added from pin14 to pin11, and again no improvements were observed



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Start-up timing of PFC stage



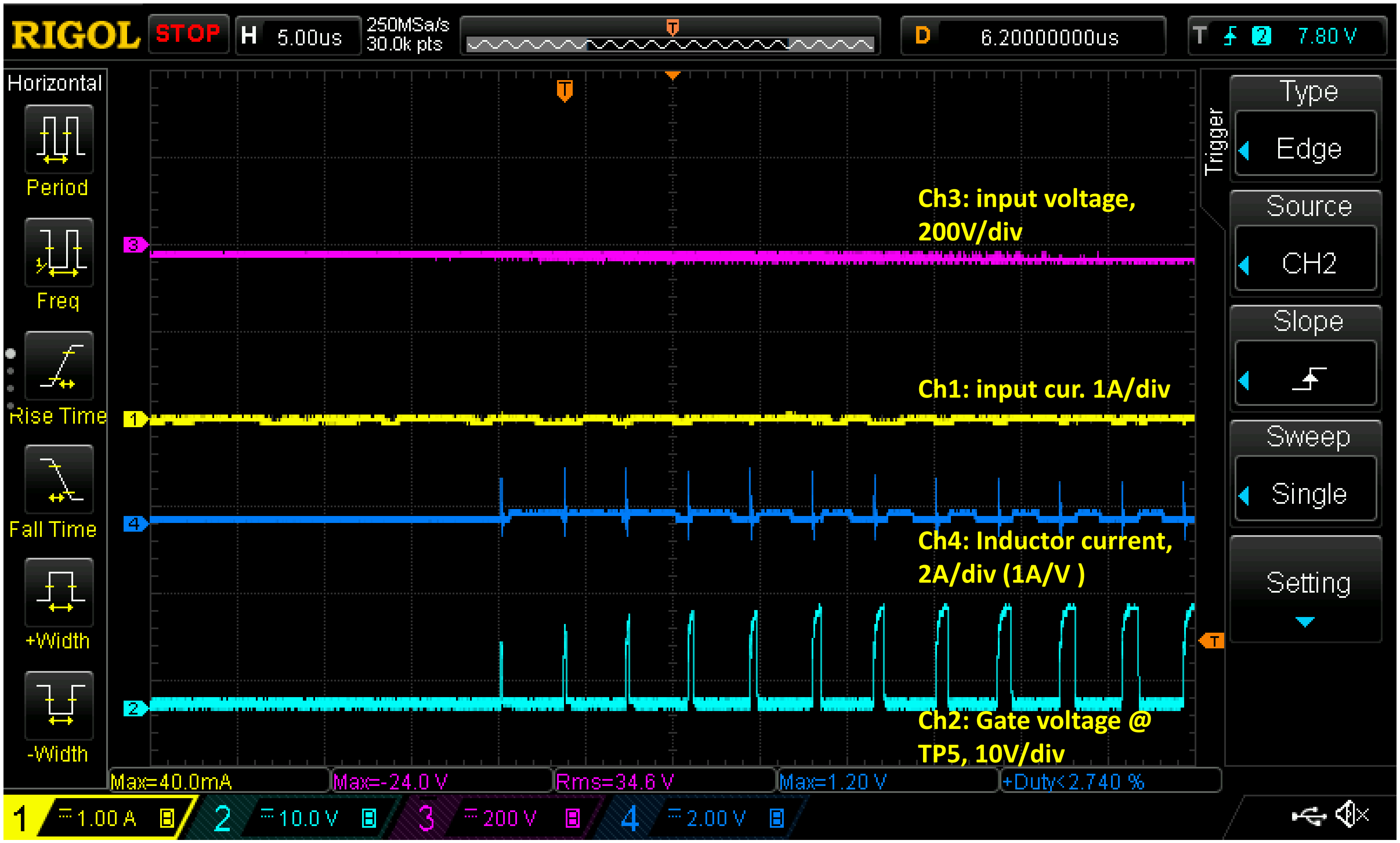
Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

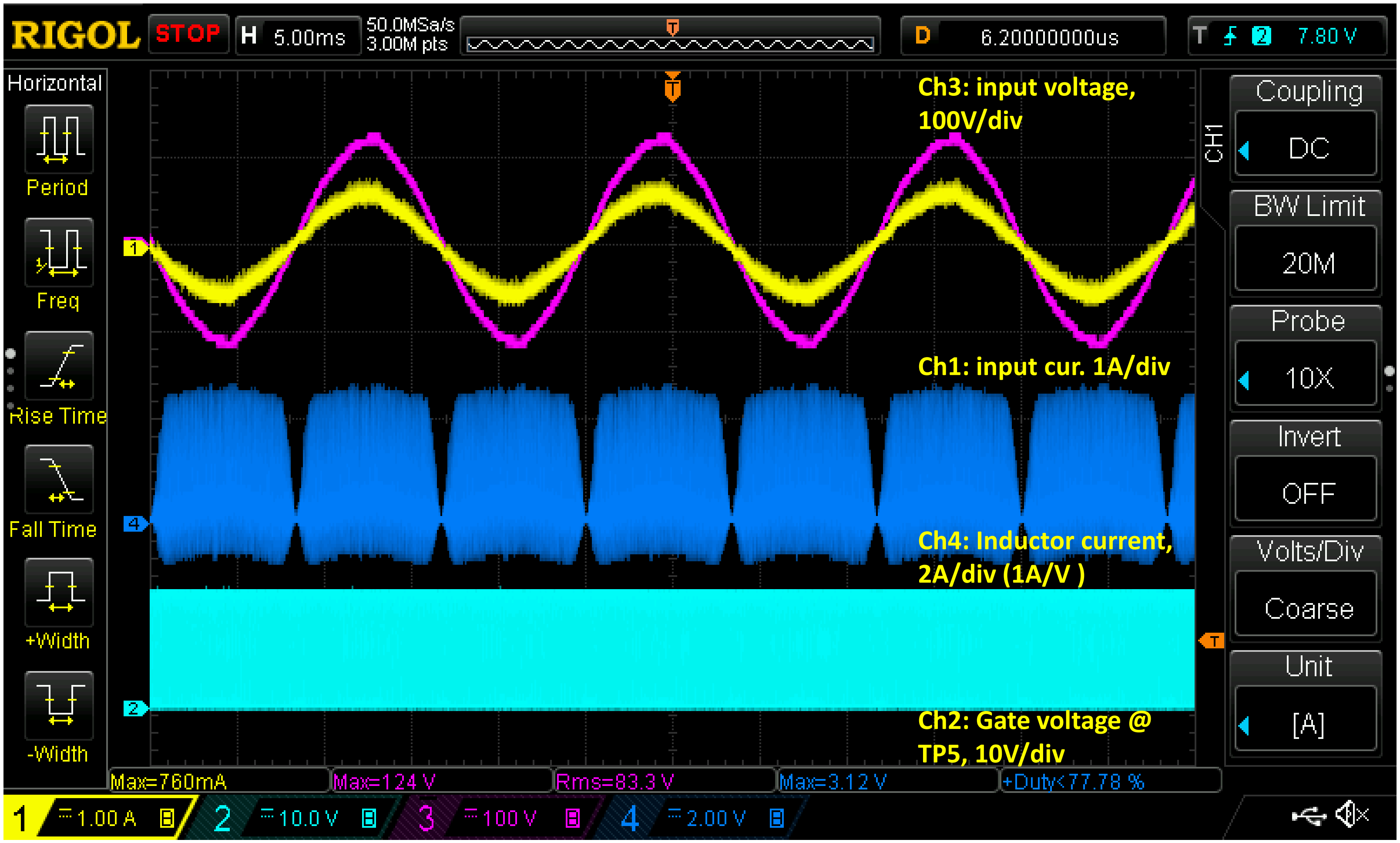
At the time when PFC stage starts operating, it seems like the ON time pulse-width starts from zero and increases slowly



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

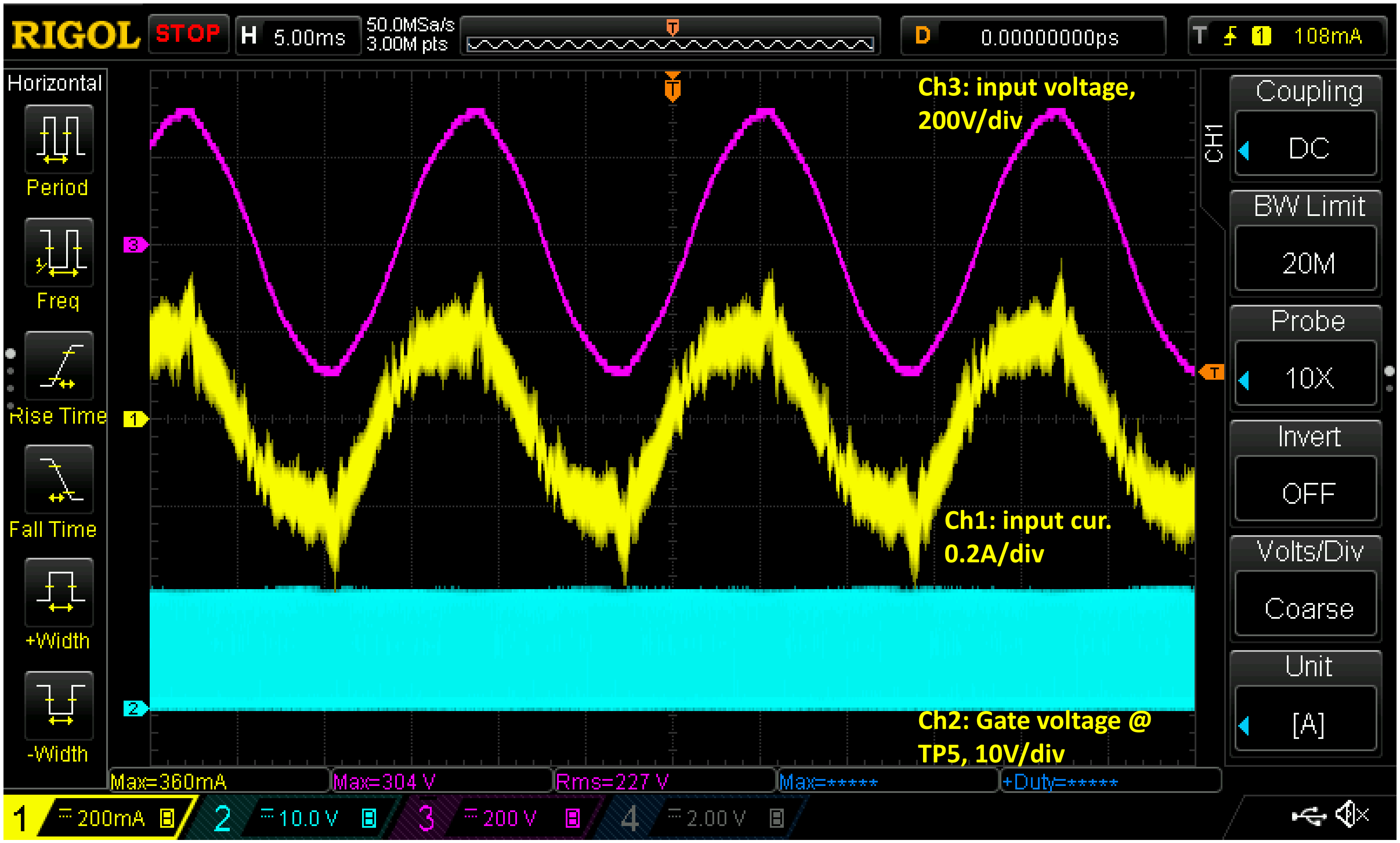
With 1nF from PKLMT (pin14) to GND (pin11), no major distortions at 85Vac



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

With 1nF from PKLMT (pin14) to GND (pin11), distortions start at around 220Vac
(also tried 100pF from pin14 to pin11, no improvements were observed)

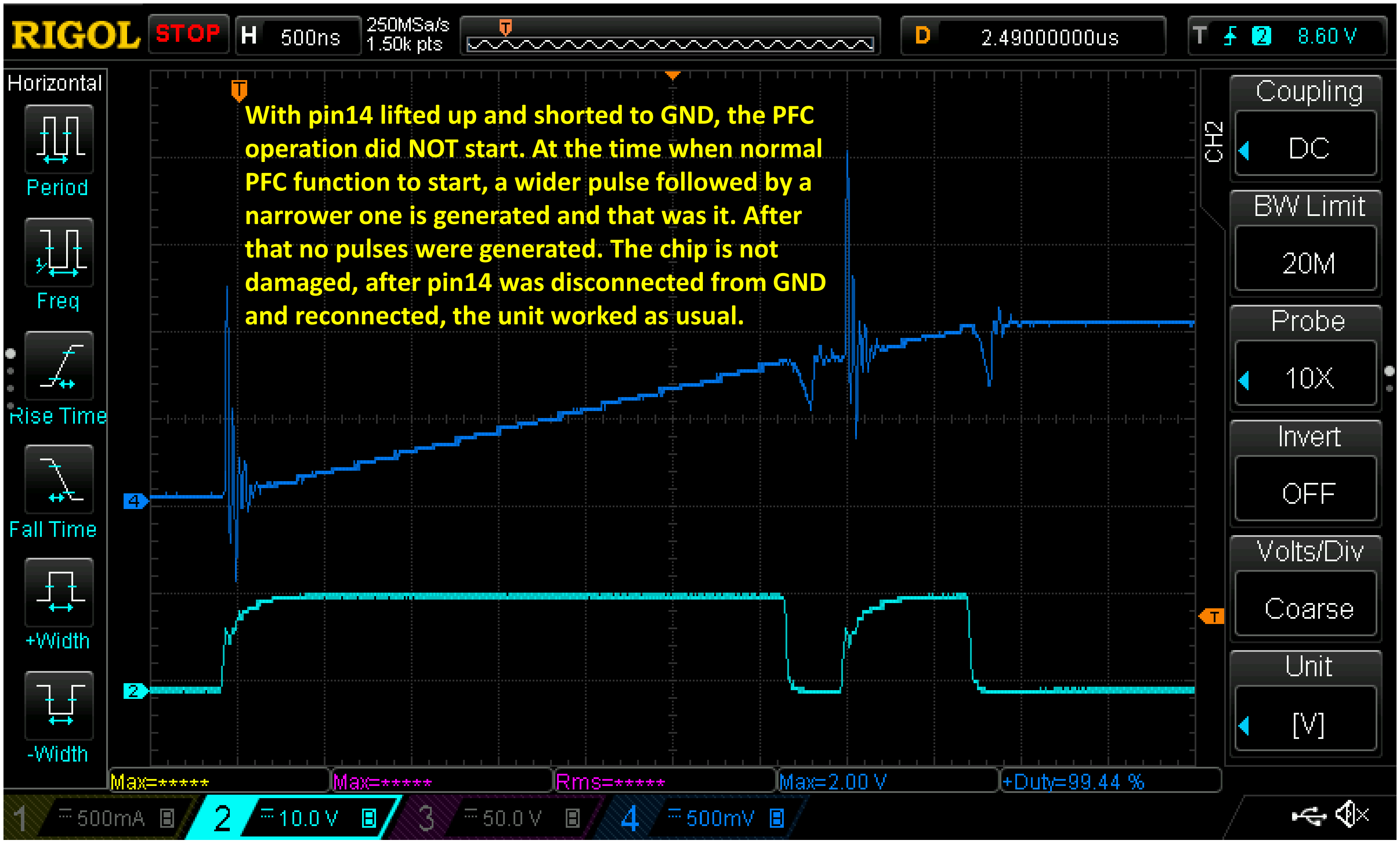


Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Conclusions on 1/8:

1) Connecting 100pF and then 1nF capacitor from pin14 (PKLMT) and pin11 (GND), right on the control chip, did not result in any improvements and that input current started to get distorted at around 230Vac
2) When PFC chip starts to operate, after AUX power supply is established, it seems like the ON time of the MOSFET starts from zero and is increased slowly. This makes sense, as doing so would reduce the chance of triggering PKLMT while DC-link cap is charged.
3) When pin14 is lifted up and shorted to pin11, at the time when it normally starts, the PFC chip generated a wider single pulse followed by a narrower one. The PFC chip did not go through the normal ramp up sequence. It is not clear why shorting the PKLMT to GND disables the ramp up function. And, since PKLMT is shorted to GND, it is presumed that the interruption of PFC function is not due to activation of PKLMT function.

SS2 (pin 13): A capacitor between SS2 and GND programs the softstart duration of the PWM stage gate drive. When the UVLO2 comparator enables the PWM stage, an internal 10.5-µA current source charges the external capacitor at SS2 to 3 V to ramp the voltage at VERR during startup. This allows the GT2 duty cycle to increase from 0% to the maximum clamped by the duty cycle comparator over a controlled time delay t_{SS} given by:

$$C_{SS2} = \frac{t_{SS} \times 10.5 \times 10^{-6} \times \text{Amp}}{3\text{ V}}$$

C_{SS2} is in Farads

In the event of a disable command or a UVLO2 dropout, SS2 quickly discharges to ground to disable the PWM stage gate drive.

CAOUT (Pin 15): This is the output of a wide-bandwidth operational amplifier that senses line current and commands the PFC stage PWM comparator to force the correct duty cycle. This output can swing close to GND to command maximum duty cycle, and above the PFC ramp peak voltage to force zero duty cycle when necessary. Connect current loop compensation components between CAOUT and MOUT.

Measuring inductor current vs gate voltages, 1/15/2023

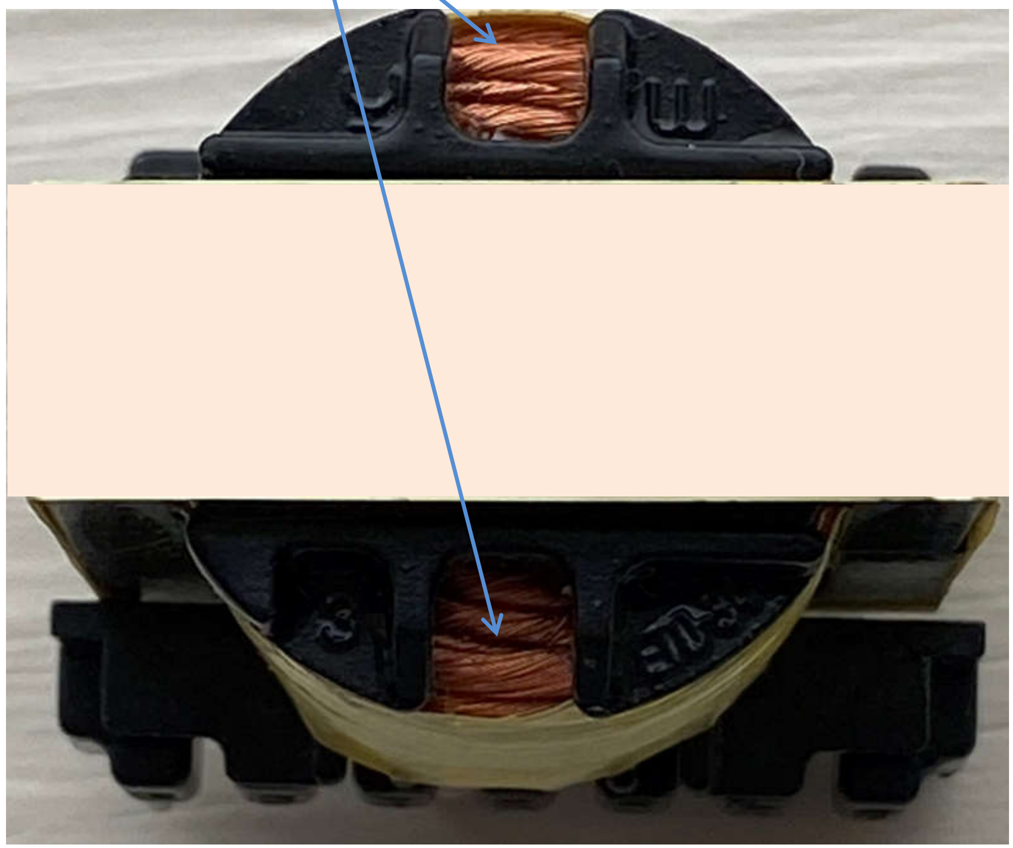
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings

Original PFC inductor has overlapping layers of winding

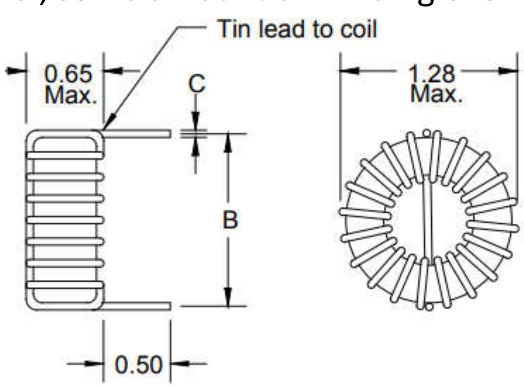


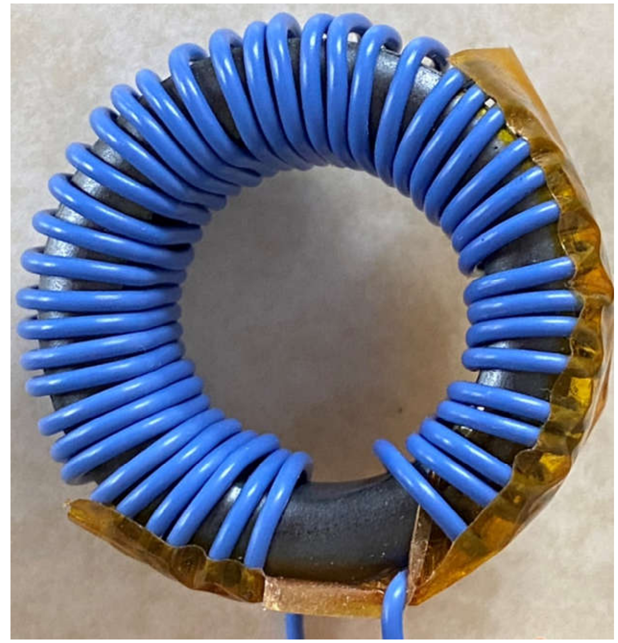
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings

Inductor #1: Bourns PN: 2300LL-681-H-RC, 680uH
Built by using toroid core, single layer winding.
However, some amount of winding overlapping is visible.



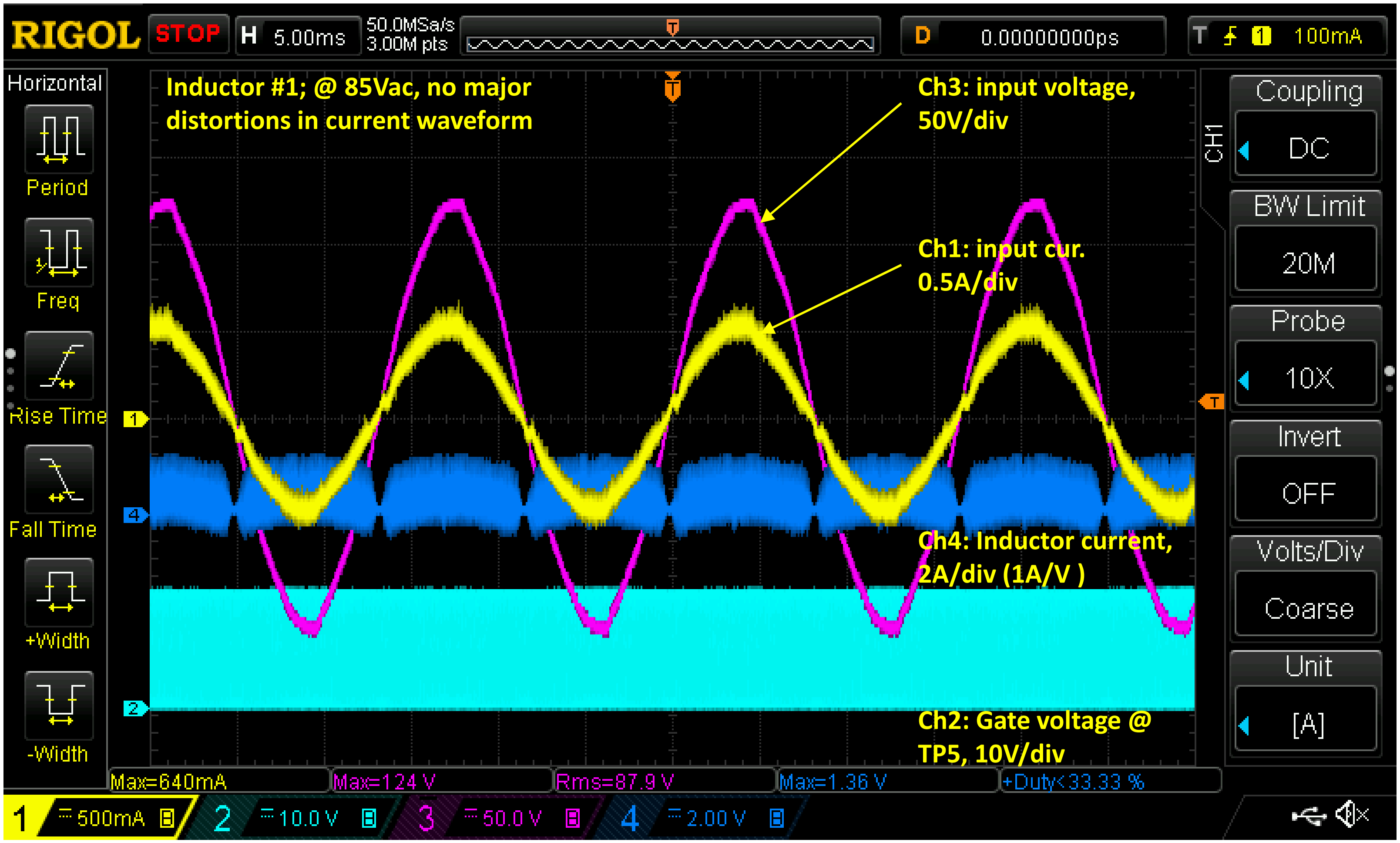


Inductor #2: Homemade by using toroid core Wurth PN: 7427015 and 43 turns of single layer winding.
Inductance measured at 1.39mH @ 300kHz.

Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



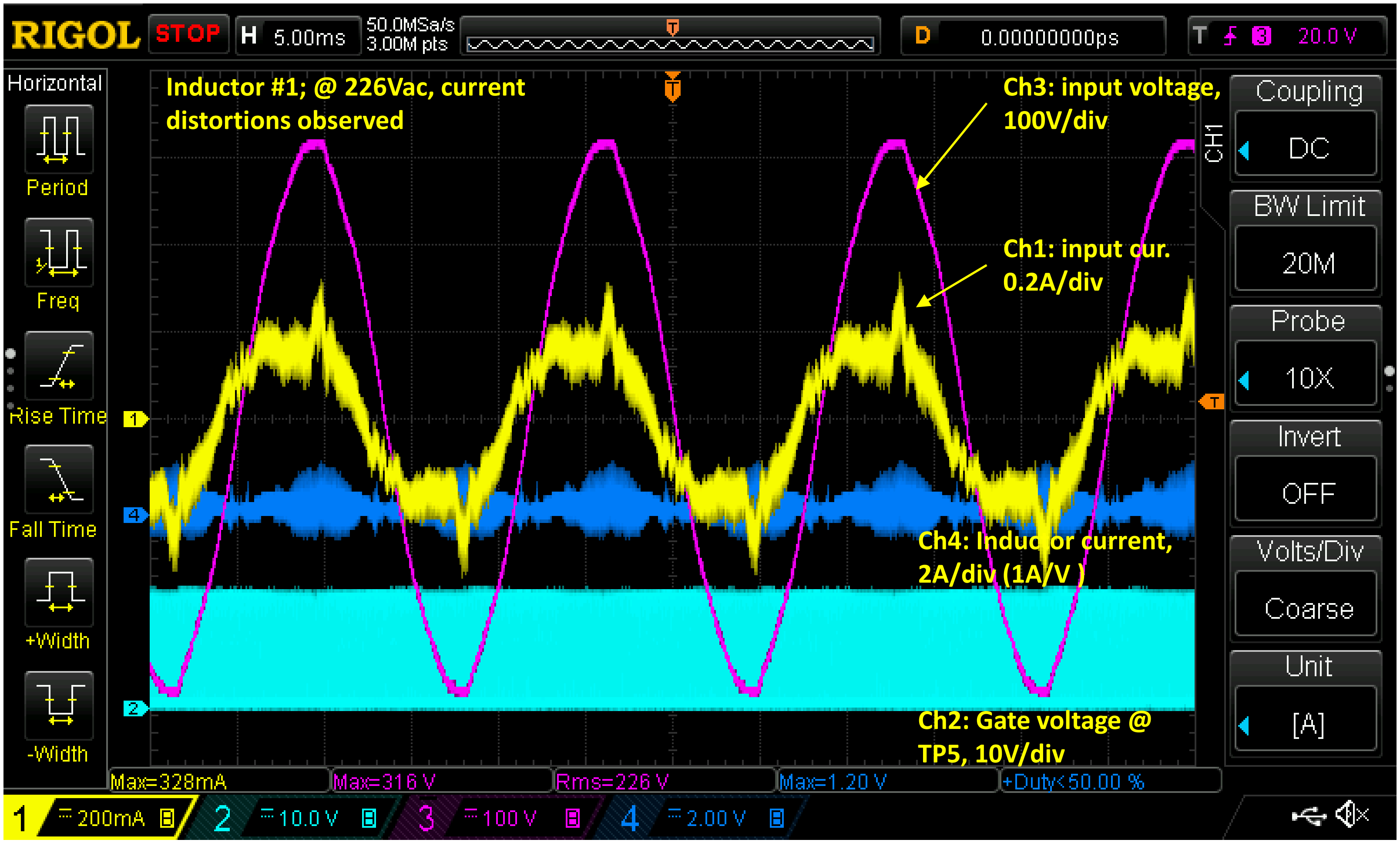
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



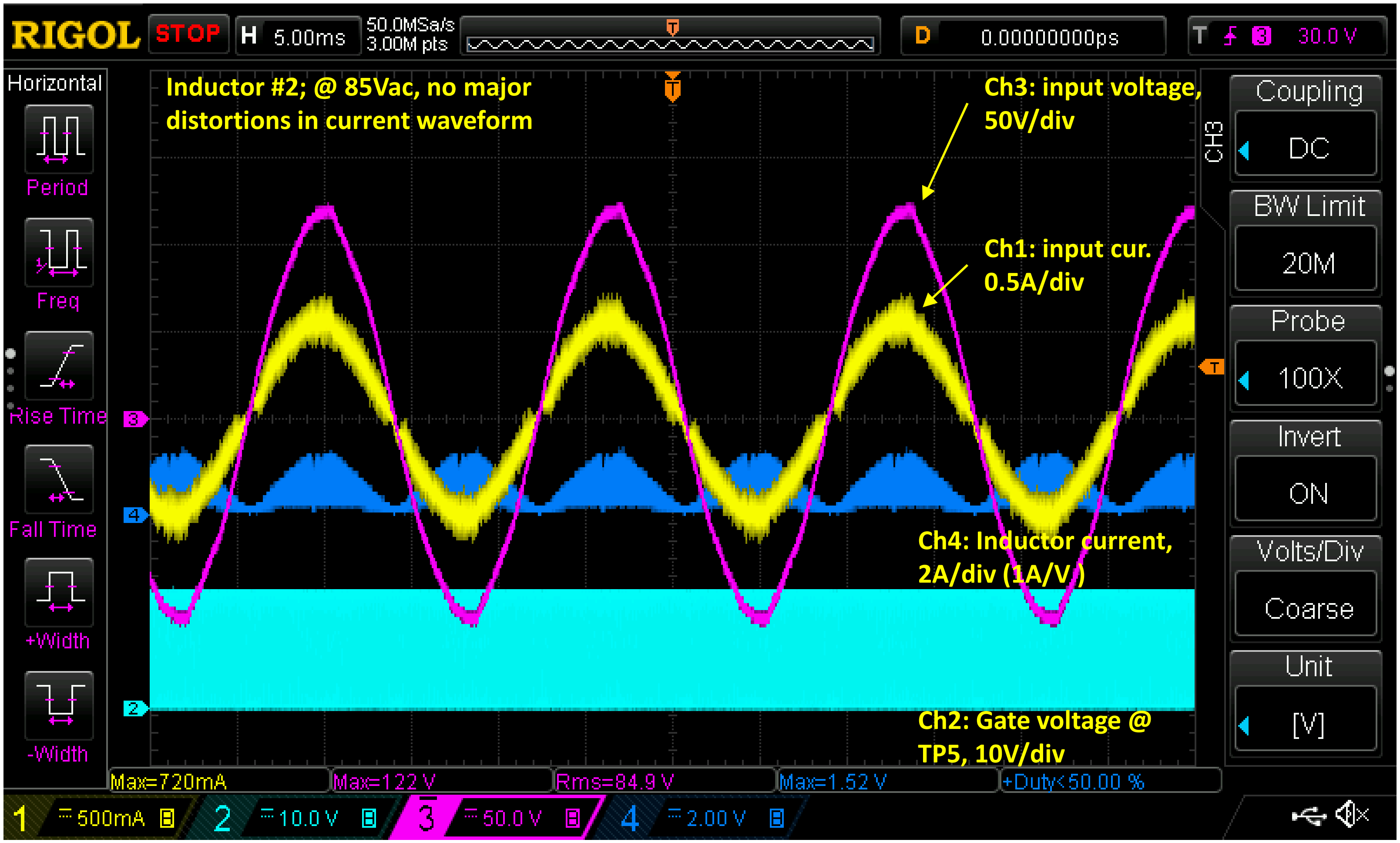
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

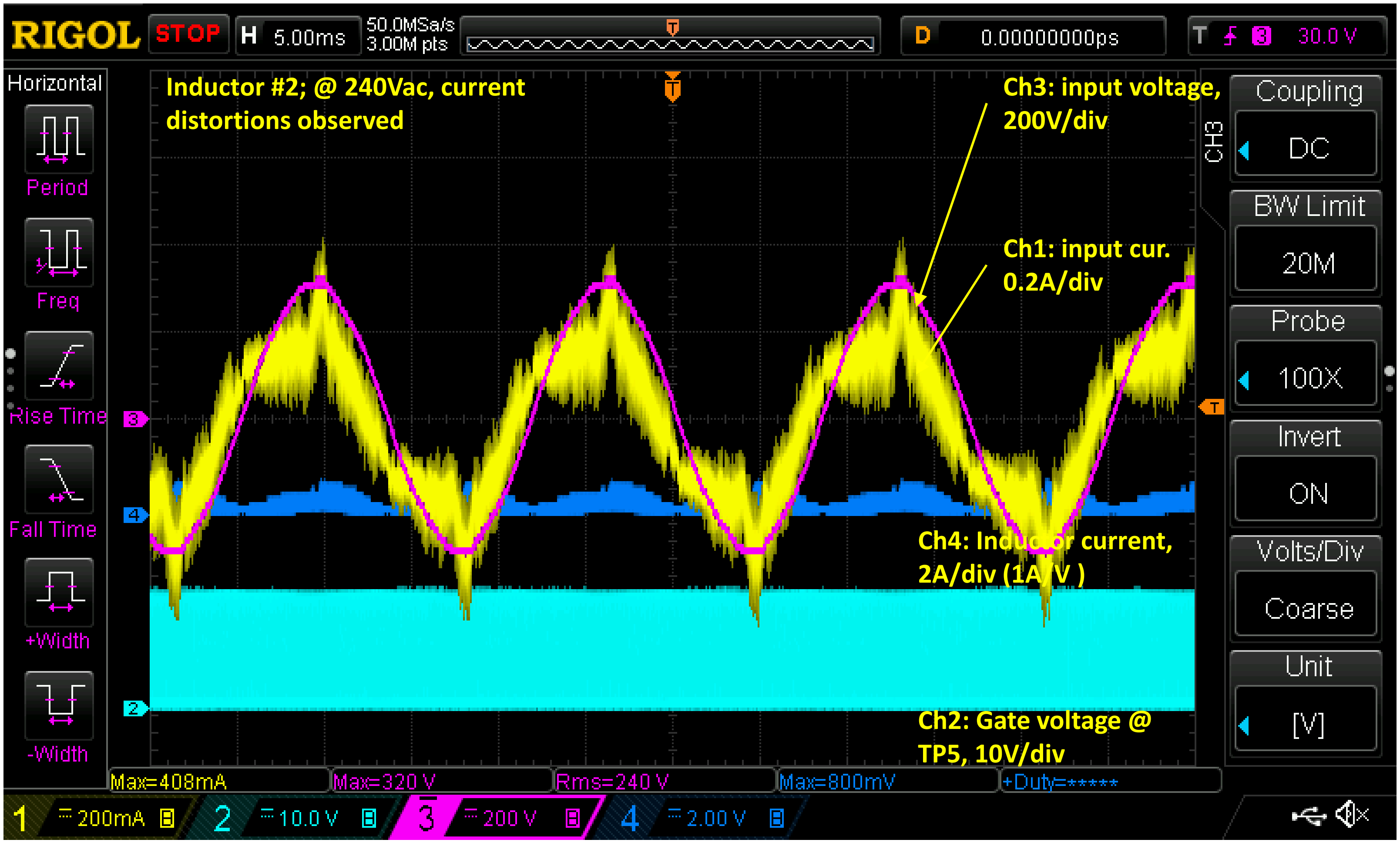
Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings

Conclusions on 1/15:

1) Two different inductors with no or minimal winding overlapping are tried out. Current distortions at high voltages were observe in both case.
2) Original inductor has overlapping windings and new ones do not. Even though the winding to winding capacitance is not measured, it is assumed that a single layer toroid inductor would result in lowest inter-winding capacitance.
3) Is there any practical way to measure the inter-winding capacitance?
4) Is there any rule of thumb as to how much inter-winding capacitance would be too much?