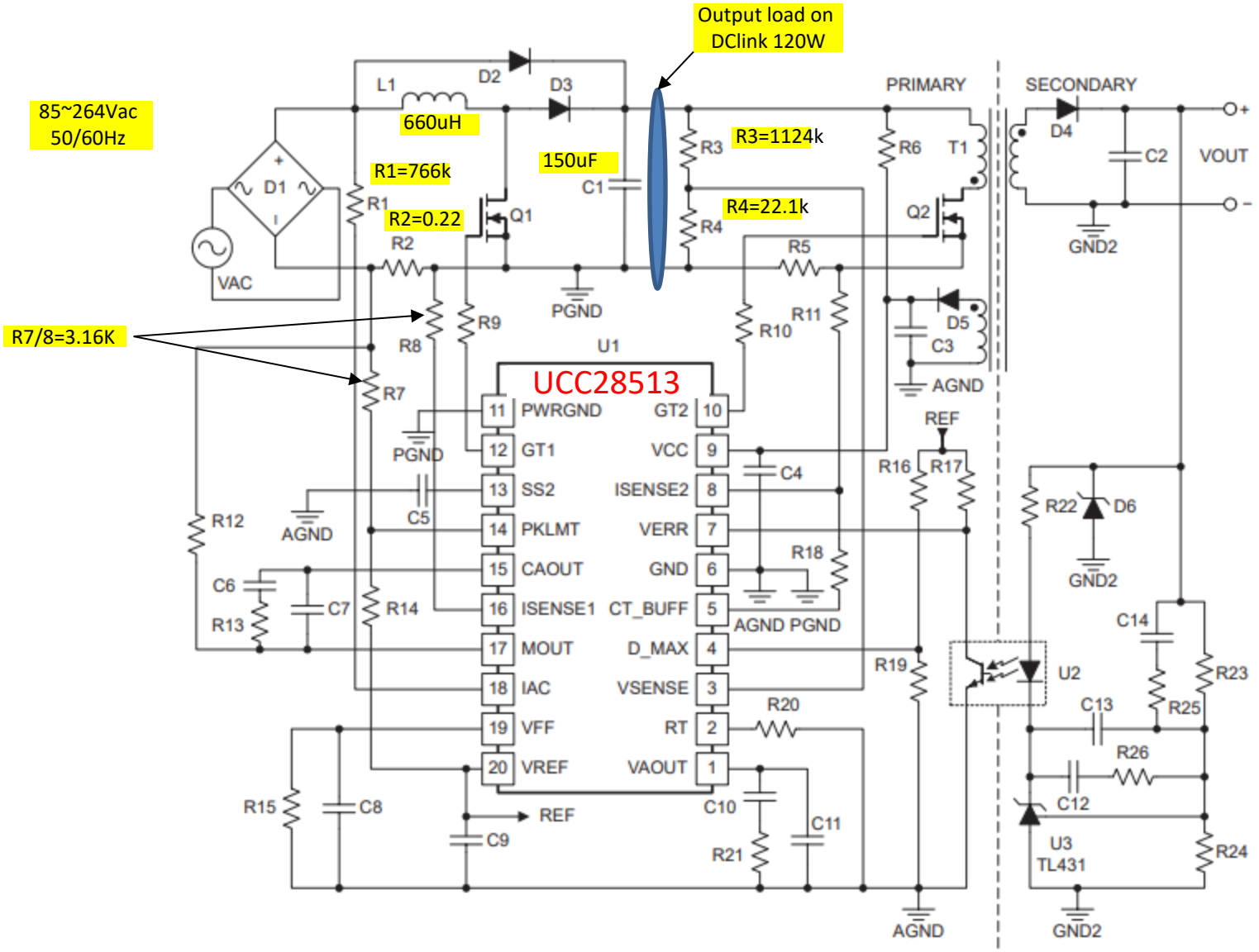
UCC28513 questions, Alex W., 11/17/2022

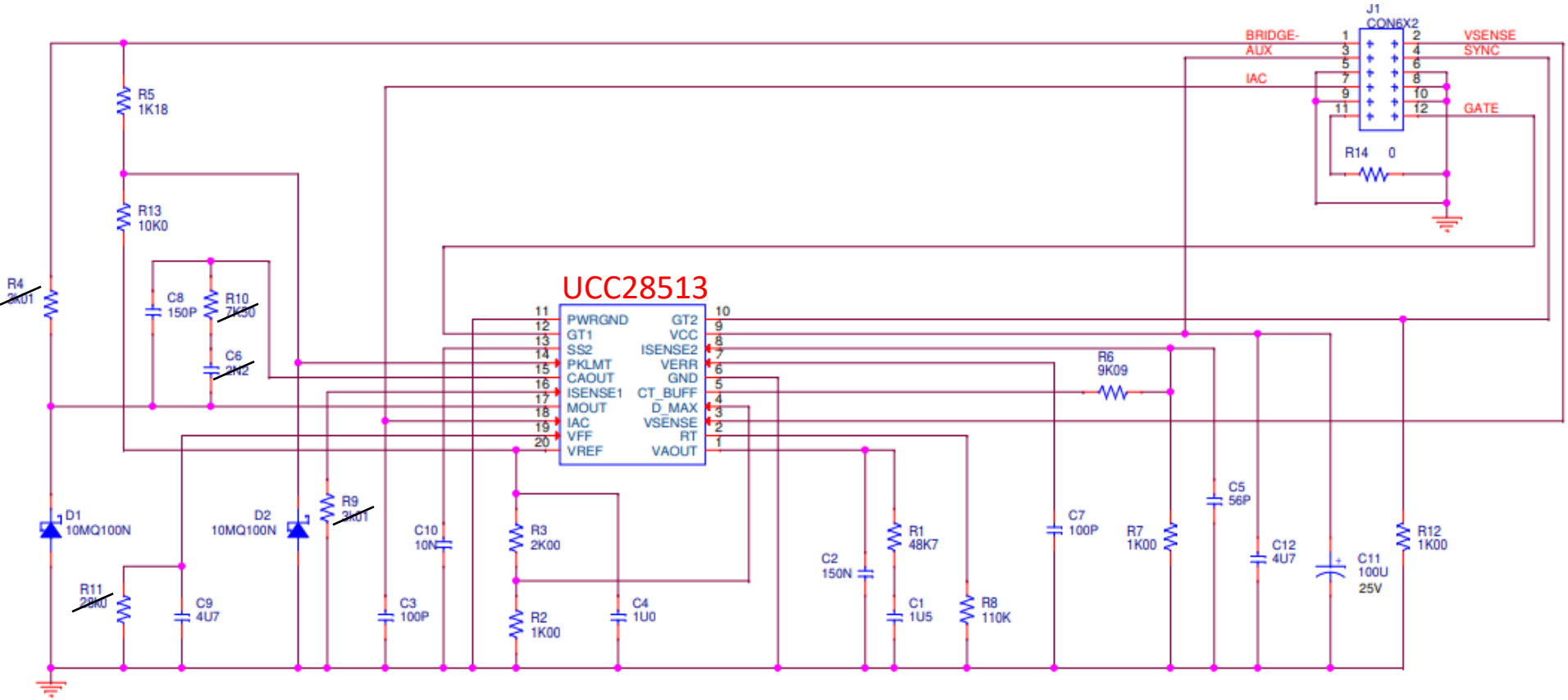
- The boost stage design is based on UCC28513. The PFC stage works well up to 200-220Vac input. Above this voltage range there are significant distortions at the points where sinusoidal input voltage reaches to its positive and negative peaks
- Output voltage is 385Vac
- Input voltage range is 85-264Vac; 50/60Hz
- The load on DC link output is 120W max
- Boost stage switching frequency is 277kHz
- Verified that the Vcc aux supply and Vref are stable
- Observed that the AC ripple on DC link goes up at around 200Vac but not sure it this is the reason or the result
- Observed that the duty cycle is about 70% at the peak sine wave at 85Vac but drops down to ~15% at the peaks of 220Vac at which point I start get distortions on the input current.
- The provided test results are at ~30W output power. It was observed that changing the load did not affect the behavior at around 220Vac.

Questions:

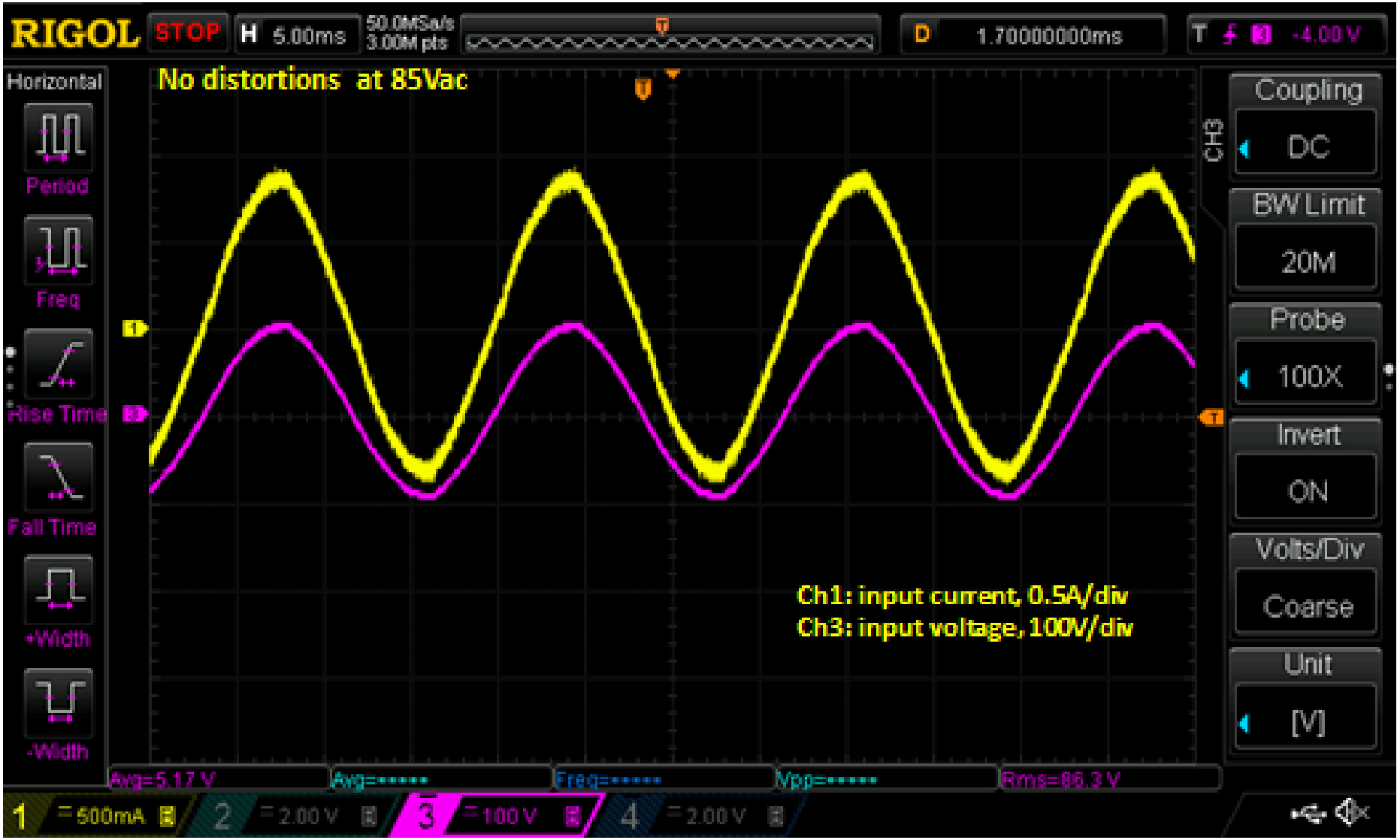
1. Based on the design values, what could potentially cause the distortions at the peak of sine waves at and above ~ 200Vac?
2. Fig. 36 on data sheet talks about max capacitance vs min duty cycle. What capacitor is referred in Fig 36?

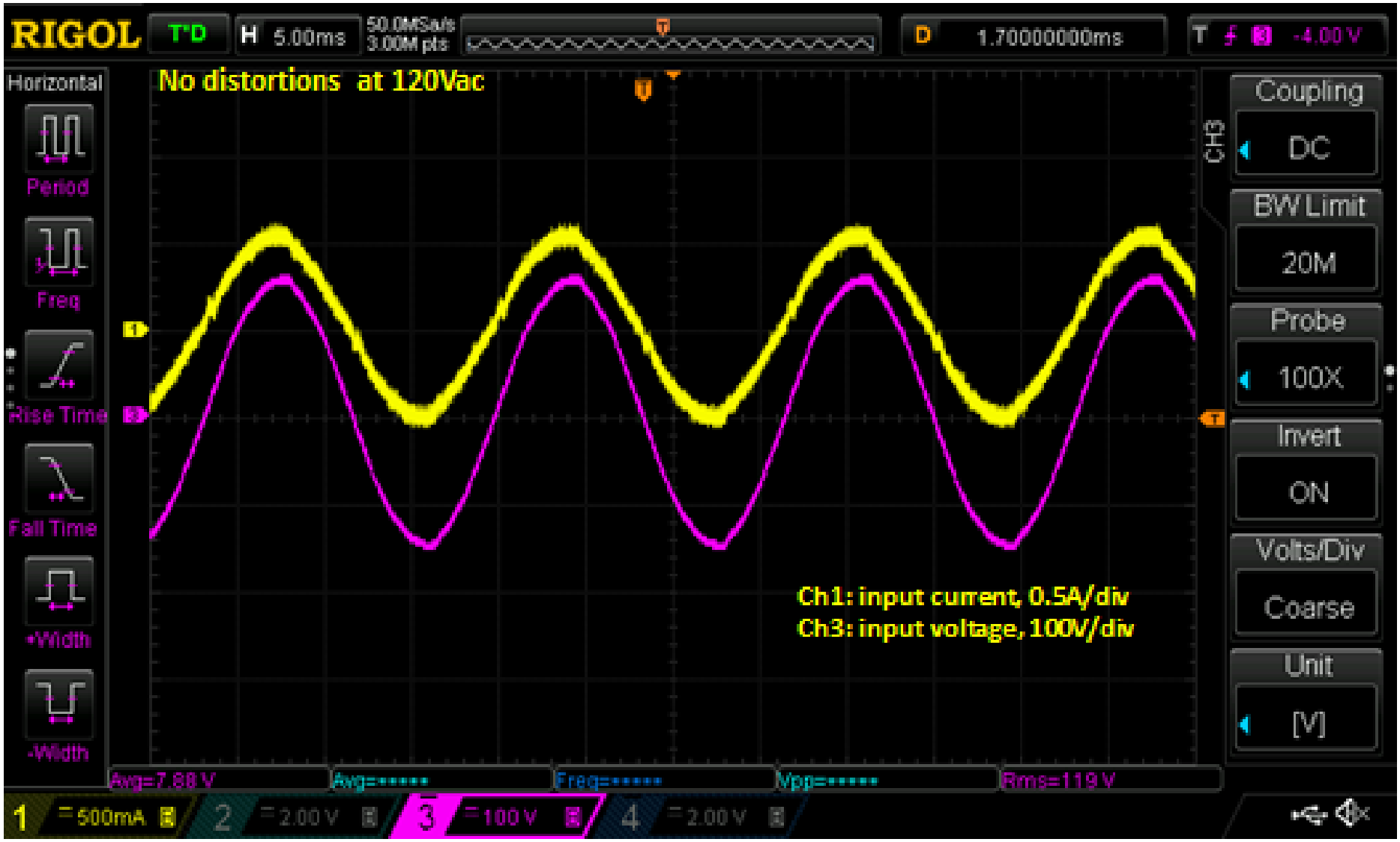

Output load on DClink 120W
85~264Vac 50/60Hz
L1
660uH
D2
D3
R1=766k
R2=0.22
150uF
C1
R3
R3=1124k
R4
R4=22.1k
R5
R6
T1
Q1
Q2
PRIMARY
SECONDARY
D4
C2
VOUT
GND2
D1
VAC
R1
R2
PGND
R7/8=3.16K
R8
R9
R10
R11
U1
UCC28513
D5
C3
AGND
R7
11 PWRGND
12 GT1
13 SS2
14 PKLMT
15 CAOUT
16 ISENSE1
17 MOUT
18 IAC
19 VFF
20 VREF
GT2 10
VCC 9
ISENSE2 8
VERR 7
GND 6
CT_BUFF 5
D_MAX 4
VSENSE 3
RT 2
VAOUT 1
REF
R16
R17
C4
R18
AGND PGND
R12
C5
C6
R13
C7
R14
R15
C8
C9
R20
C10
C11
R21
R19
U2
R22
D6
C14
R23
R25
C13
R26
C12
U3
TL431
R24
AGND
GND2

RefDes on data sheet	RefDes in design	values
R1	R47+R50	766K
R2	R43	0.22
R8/R12	R4/R9	3.16K
R3	R44+R49	1124K
R4	R60	22.1k
C1	C32	150uF
L1	L2	660uH
R13	R10	15.8K
C6	C6	680pF
C7	C8	150pF
R15	R11	30.1K
C8	C9	4.7uF
C10	C1	1.5uF
C11	C2	150nF
R21	R1	48.7K
R14	R13	10K
R7	R5	1.18K
C9	C4	1uF

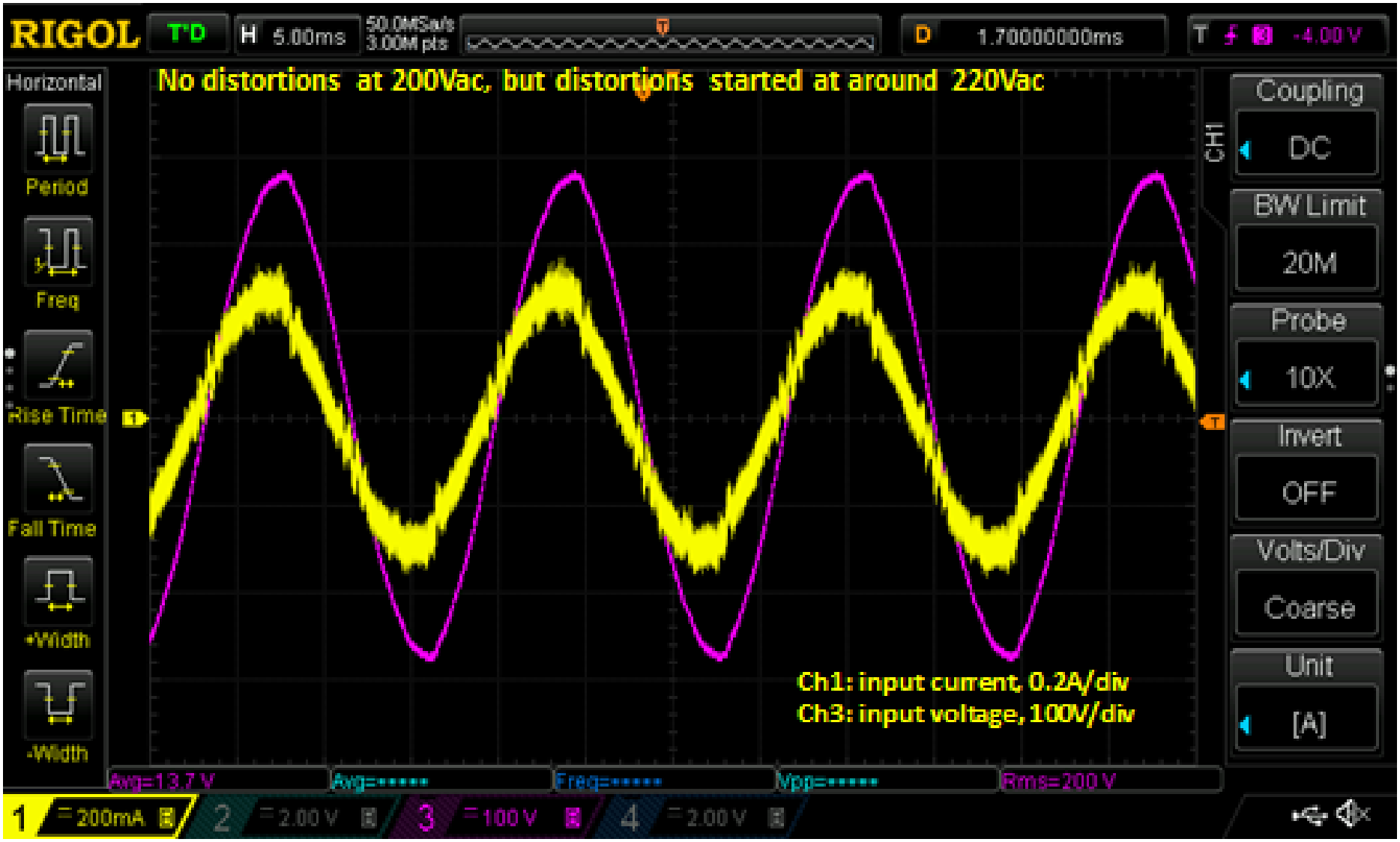


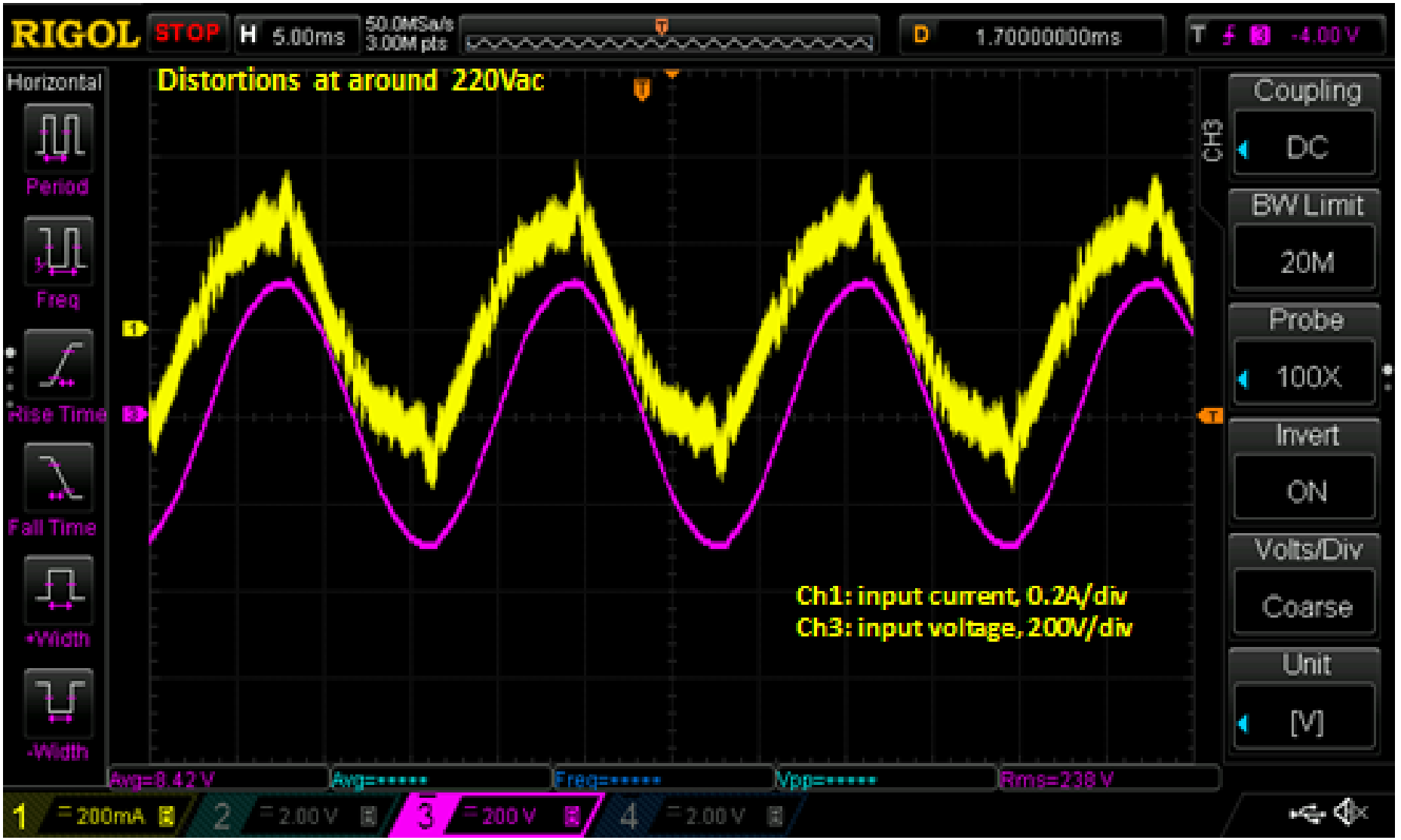
RefDes on data sheet	RefDes in design	values
R8/R12	R4/R9	3.16K
R13	R10	15.8K
C6	C6	680pF
R15	R11	30.1K

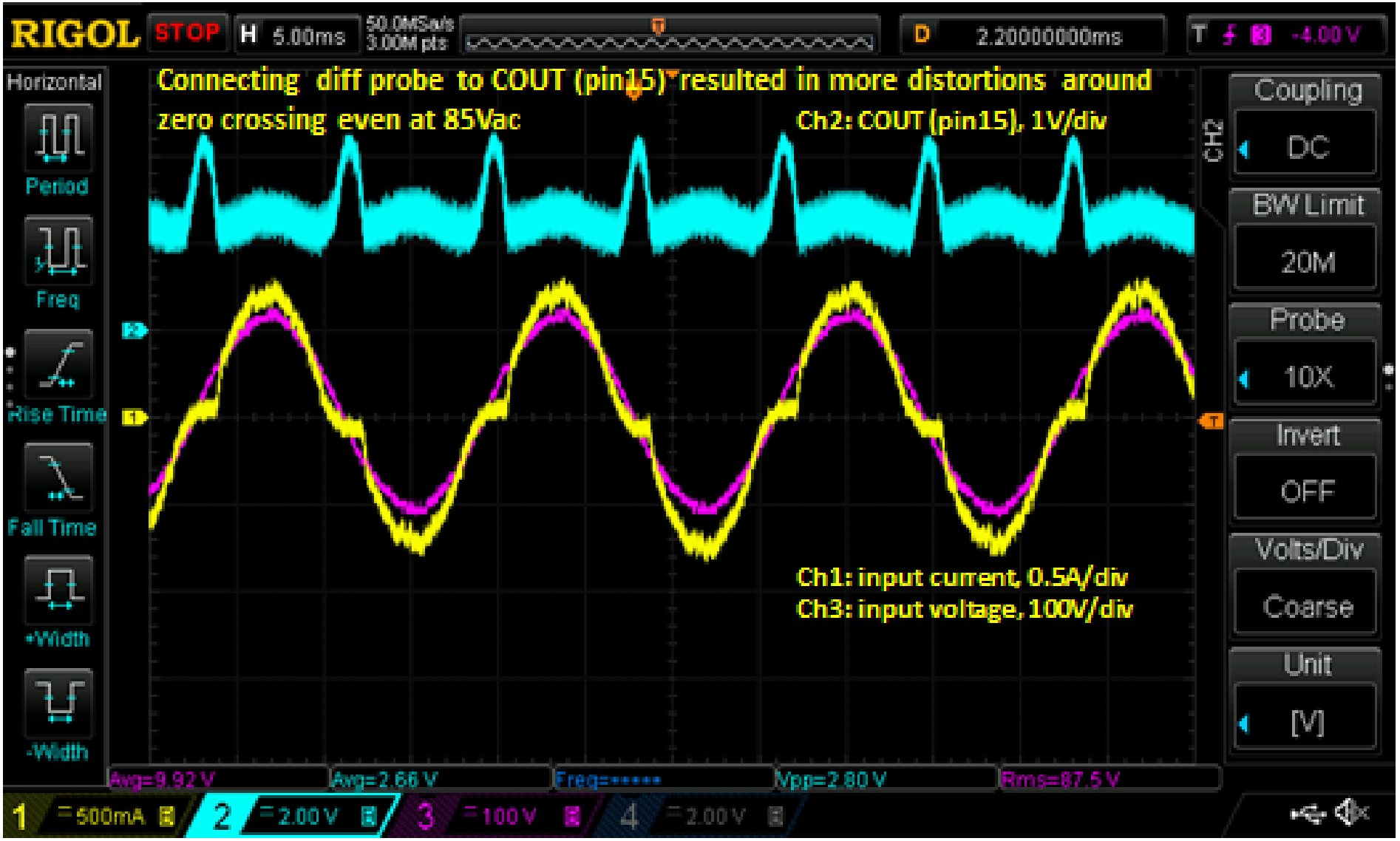

RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
T -4.00 V
Horizontal
No distortions at 85Vac
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH3
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
Avg=5.17 V
Avg=******
Freq=******
Vpp=******
Rms=86.3 V
1 500mA
2 2.00 V
3 100 V
4 2.00 V

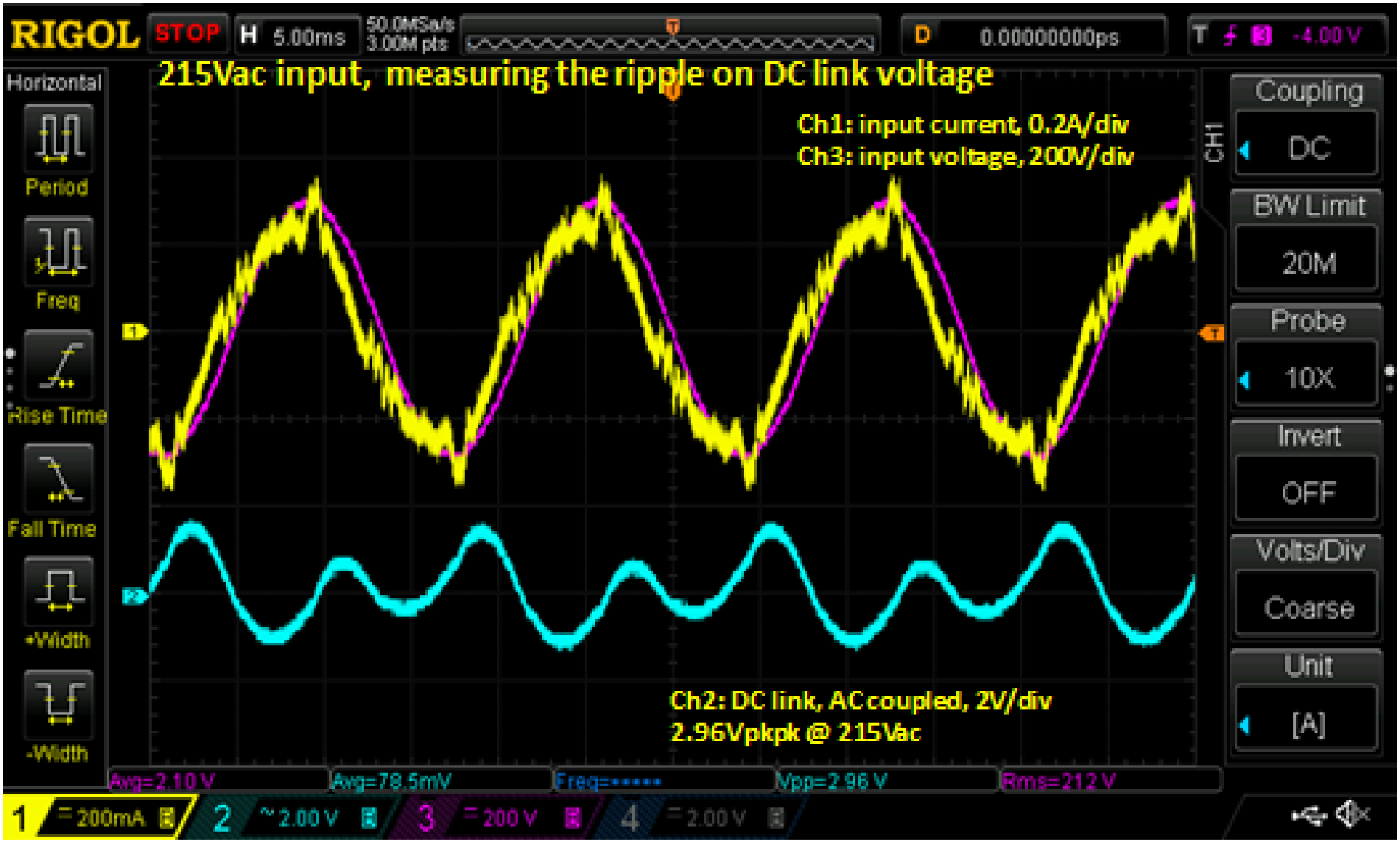

RIGOL
T'D
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
No distortions at 120Vac
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH3
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
Avg=7.88 V
Avg=
Freq=
Vpp=
Rms=119 V
1 500mA
2 2.00 V
3 100 V
4 2.00 V

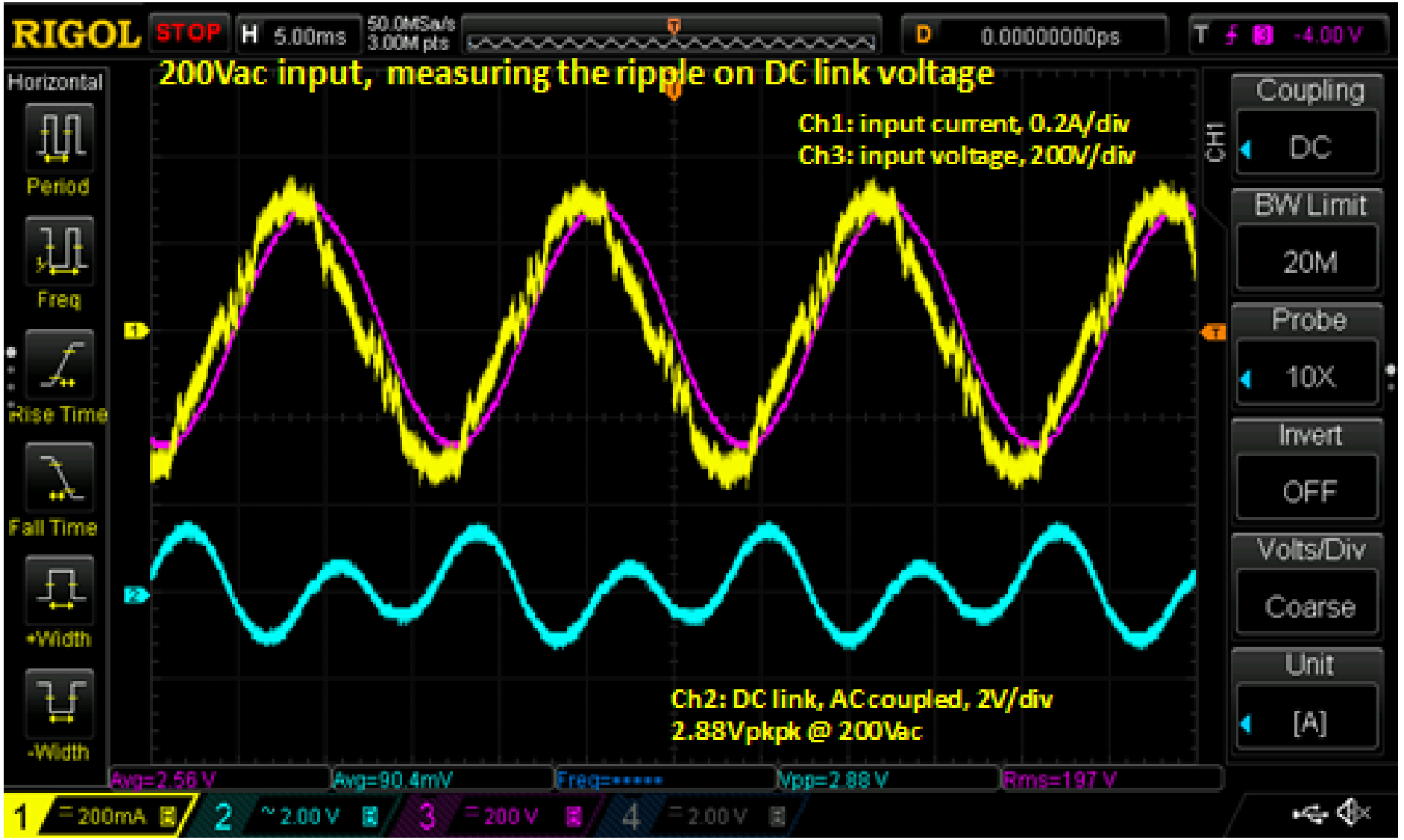
No distortions at 200Vac input, displacement between current and voltage is probably caused by the input capacitors on EMI filter




RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 1.70000000ms
T -4.00 V
Horizontal
Distortions at around 220Vac
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH3
Coupling
DC
BW Limit
20M
Probe
100X
Invert
ON
Volts/Div
Coarse
Unit
[V]
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Avg=8.42 V
Avg=*****
Freq=*****
Vpp=*****
Rms=238 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 2.20000000ms
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
Connecting diff probe to COUT (pin15) resulted in more distortions around zero crossing even at 85Vac
Ch2: COUT (pin15), 1V/div
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH2
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Avg=9.92 V
Avg=2.66 V
Freq=******
Vpp=2.80 V
Rms=87.5 V
1 500mA
2 2.00 V
3 100 V
4 2.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.000000000ps
T -4.00 V
215Vac input, measuring the ripple on DC link voltage
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Ch2: DC link, AC coupled, 2V/div
2.96Vpkpk @ 215Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Avg=2.10 V
Avg=78.5mV
Freq=
Vpp=2.96 V
Rms=212 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V

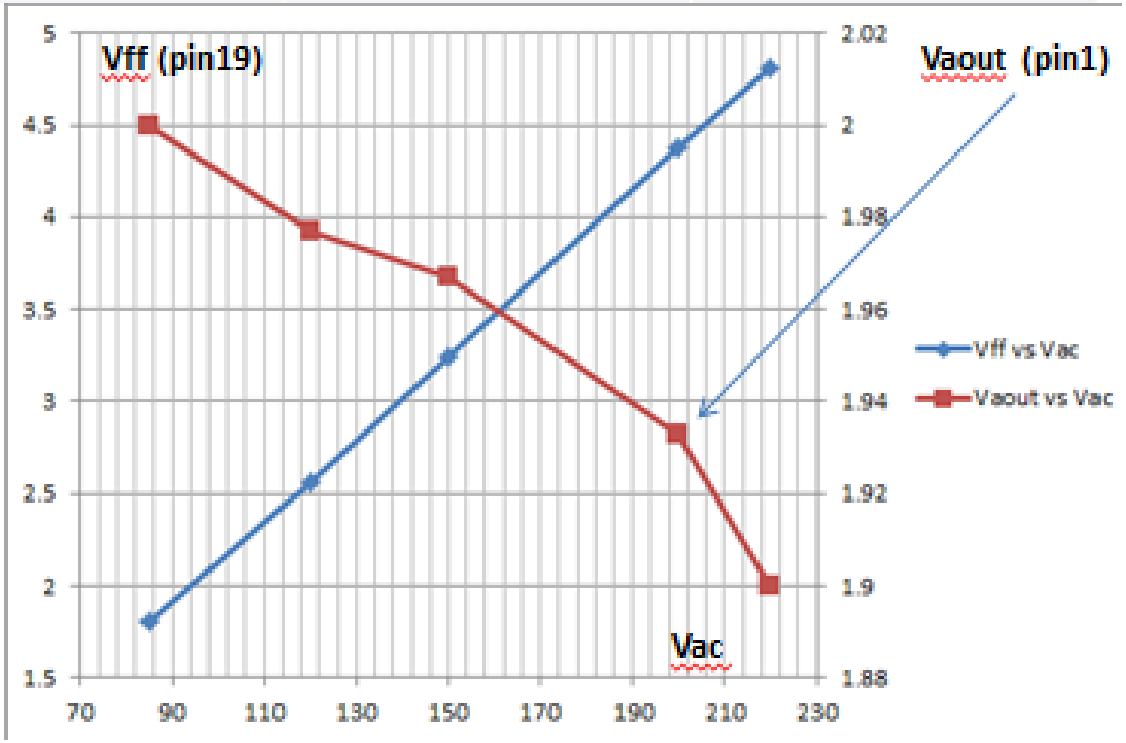

RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.000000000ps
T -4.00 V
200Vac input, measuring the ripple on DC link voltage
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Ch2: DC link, AC coupled, 2V/div
2.88Vpkpk @ 200Vac
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Avg=2.56 V
Avg=90.4mV
Freq=*****
Vpp=2.88 V
Rms=197 V
1 200mA
2 2.00 V
3 200 V
4 2.00 V

Input voltage (Vrms)	Vff on pin19 w/ DiffProbe (Vdc)	Vaout on pin1 w/ DVM (Vdc)
85	1.80	2.000
120	2.56	1.977
150	3.24	1.967
200	4.38	1.933
220	4.81	1.900

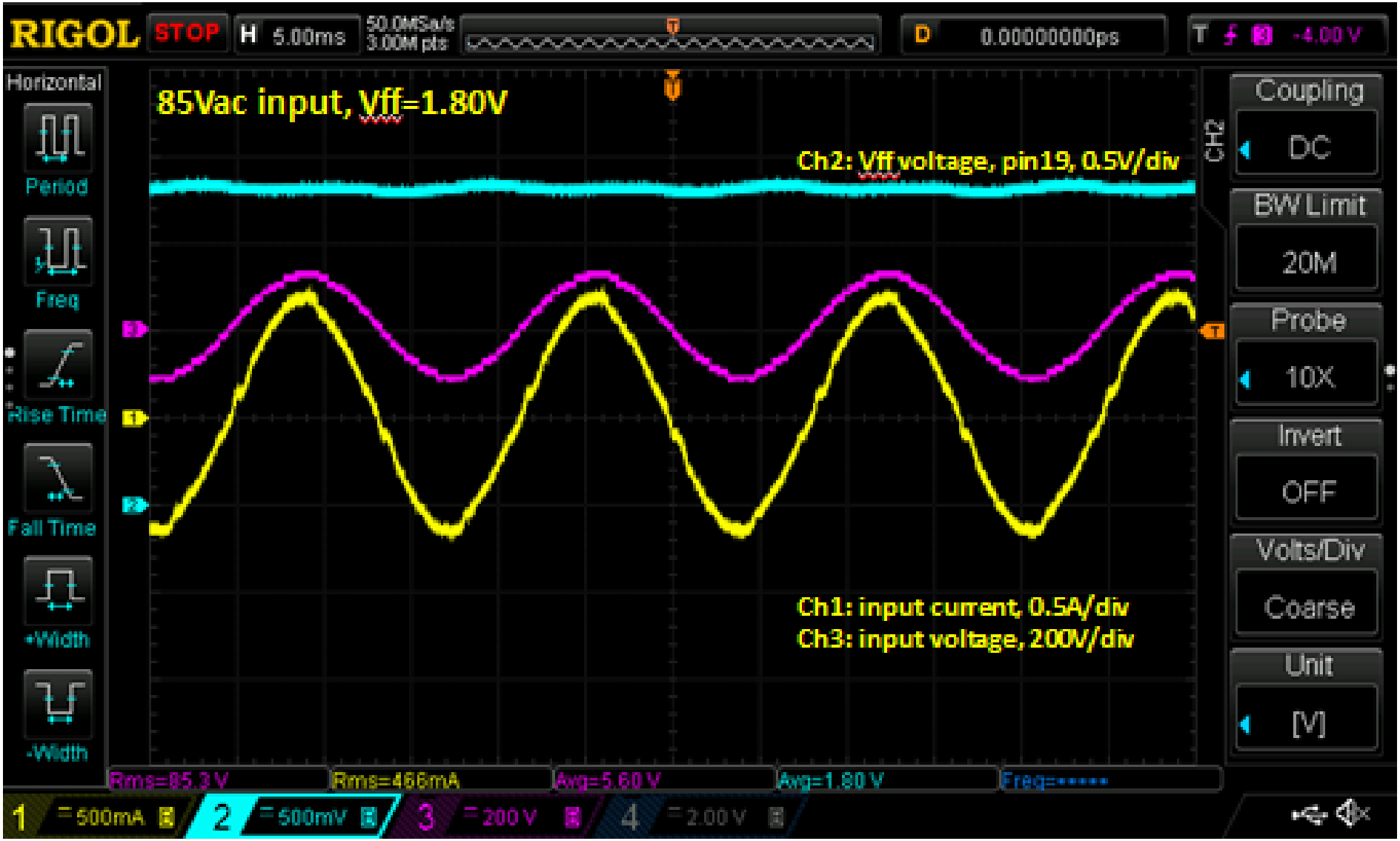
$0 \le i_{IAC}(t) \le 500\ \mu A,$

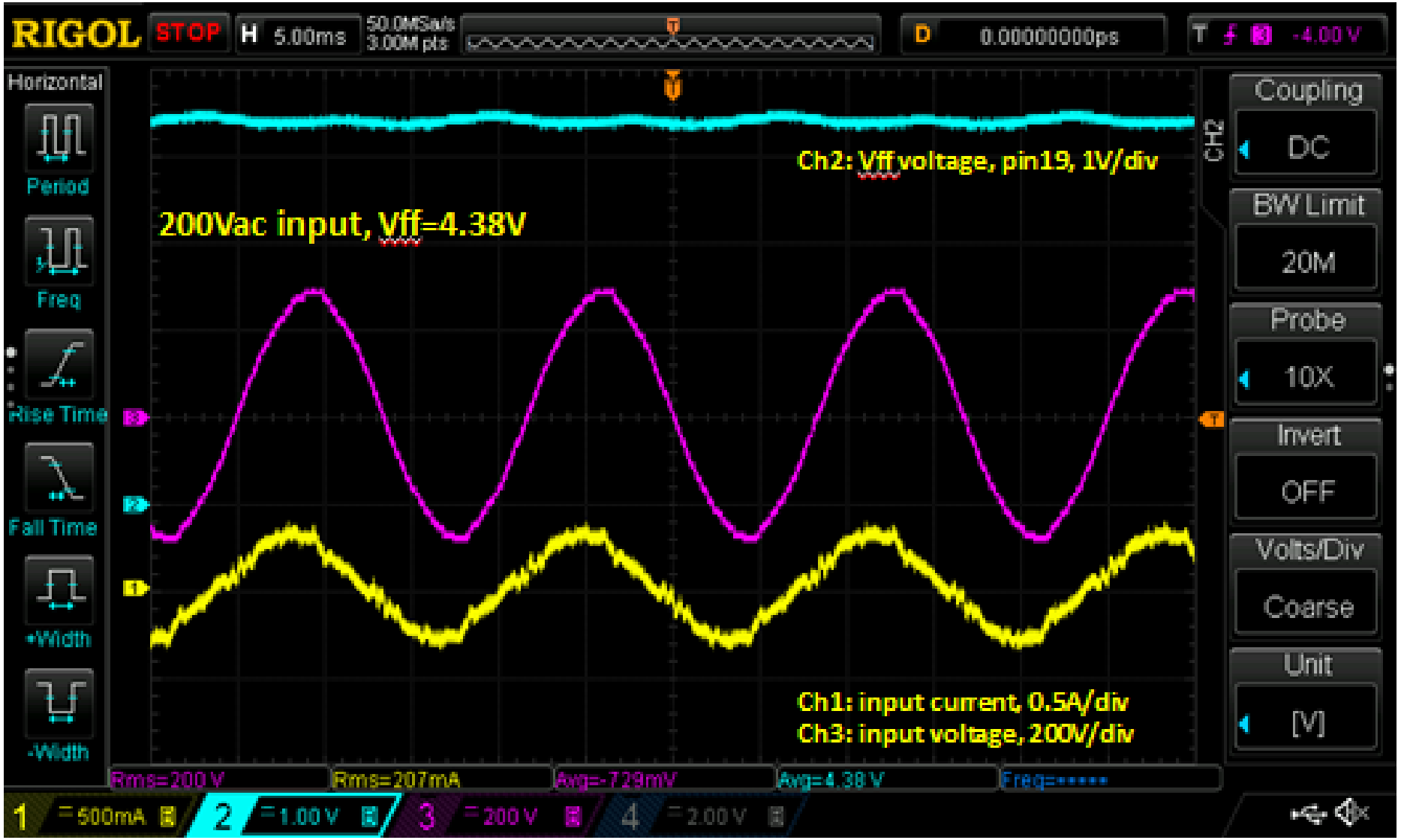
$0 \le V_{VAOUT}(t) \le 5\ V,$

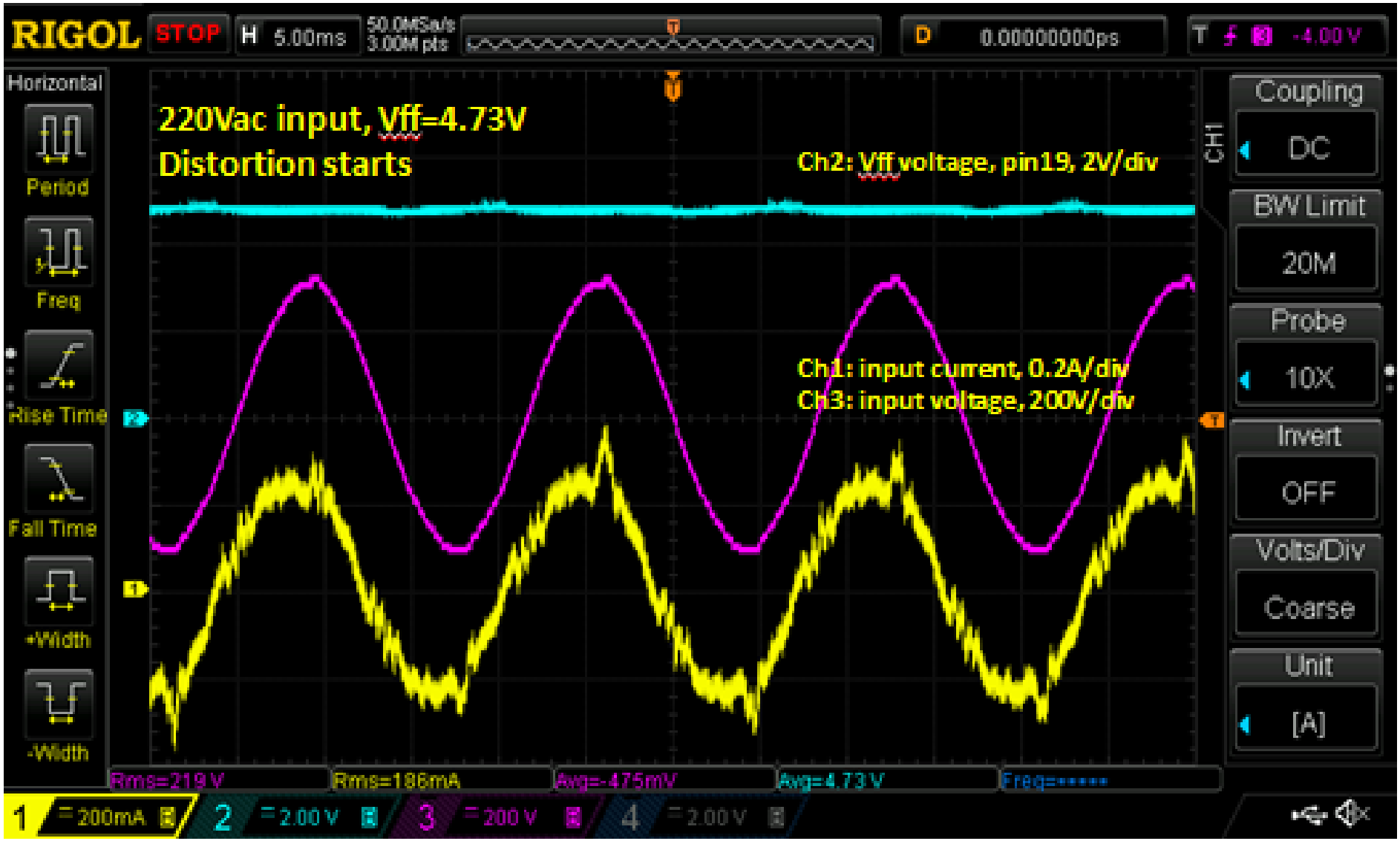
$1.4\ V \le V_{VFF} \le V_{VREF} - 1.4\ V$



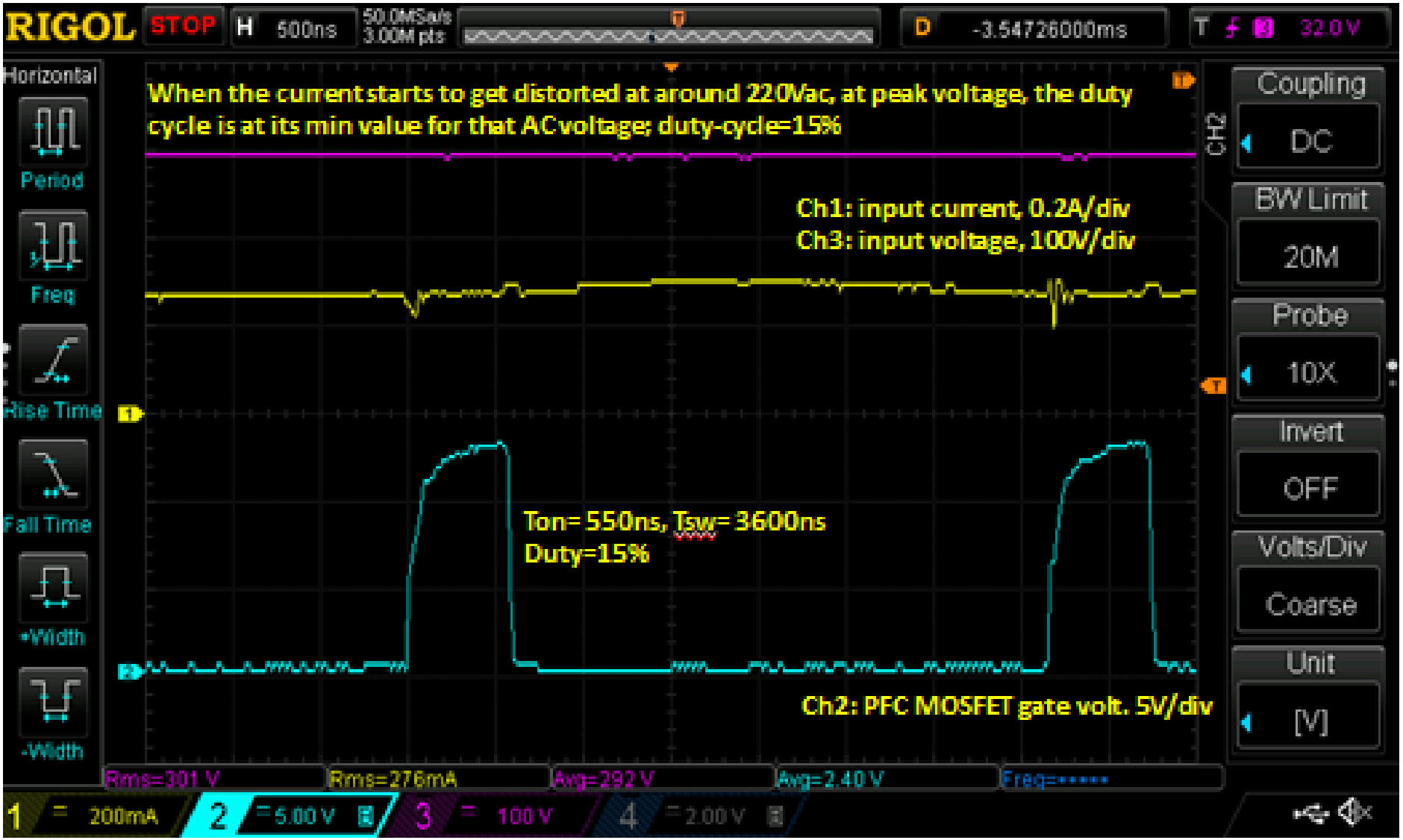
- Vff increases proportionally and Vaout drops inversely as Vac increases.
- Vaout seems to start low at 2V and not varying within its full range of 0-5V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.000000000ps
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
85Vac input, Vff=1.80V
Ch2: Vff voltage, pin19, 0.5V/div
Ch1: input current, 0.5A/div
Ch3: input voltage, 200V/div
CH2
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Rms=85.3 V
Rms=466mA
Avg=5.60 V
Avg=1.80 V
Freq=*****
1 =500mA
2 =500mV
3 =200 V
4 =2.00 V

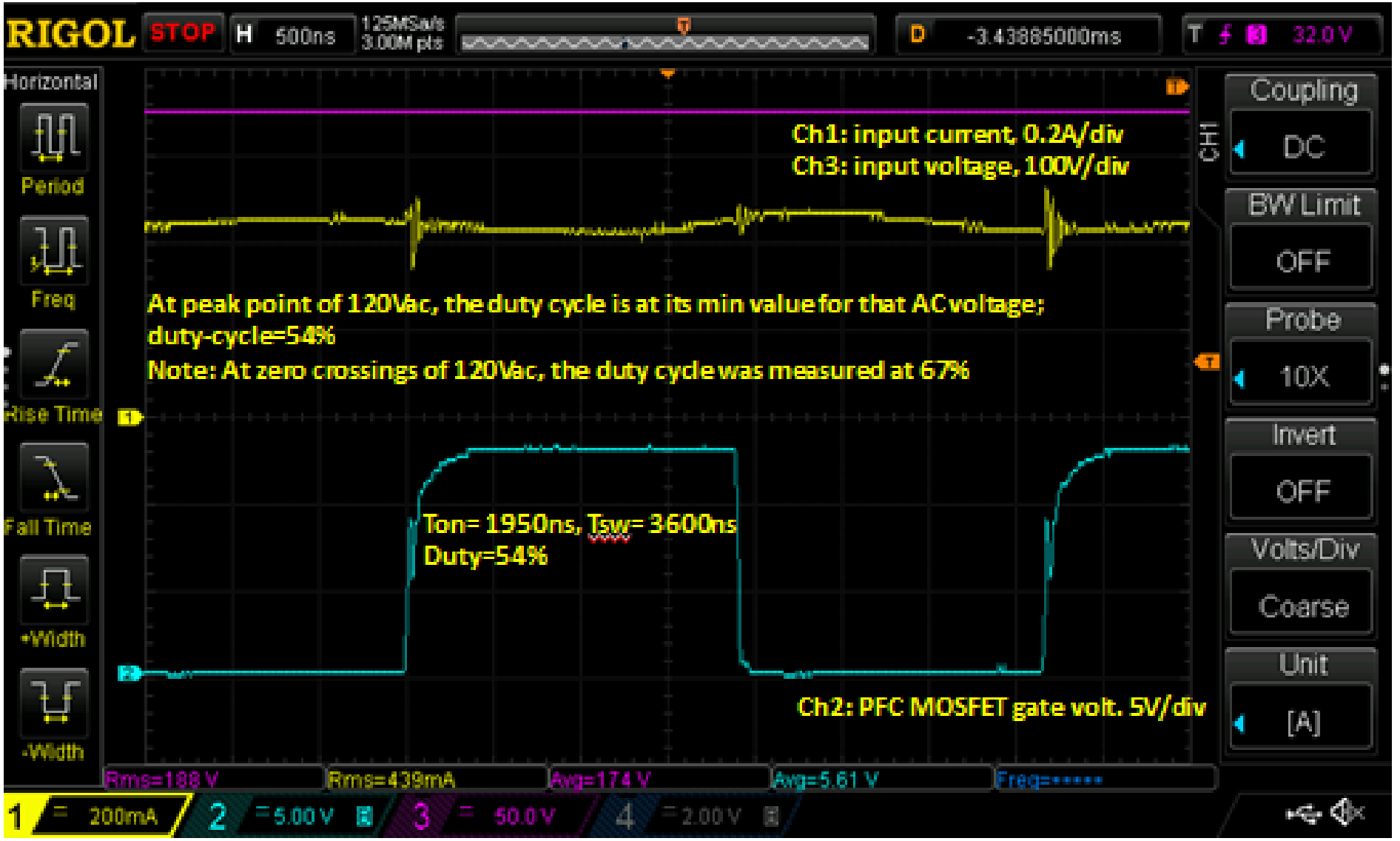

RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.000000000ps
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
Ch2: Vff voltage, pin19, 1V/div
200Vac input, Vff=4.38V
Ch1: input current, 0.5A/div
Ch3: input voltage, 200V/div
CH2
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Rms=200 V
Rms=207mA
Avg=-729mV
Avg=4.38 V
Freq=*****
1 500mA
2 1.00 V
3 200 V
4 2.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 0.00000000ps
T -4.00 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
220Vac input, Vff=4.73V
Distortion starts
Ch2: Vff voltage, pin19, 2V/div
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
CH1
Coupling
DC
BW Limit
20M
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Rms=219 V
Rms=186mA
Avg=-475mV
Avg=4.73 V
Freq=*****
1 200mA
2 2.00 V
3 200 V
4 2.00 V

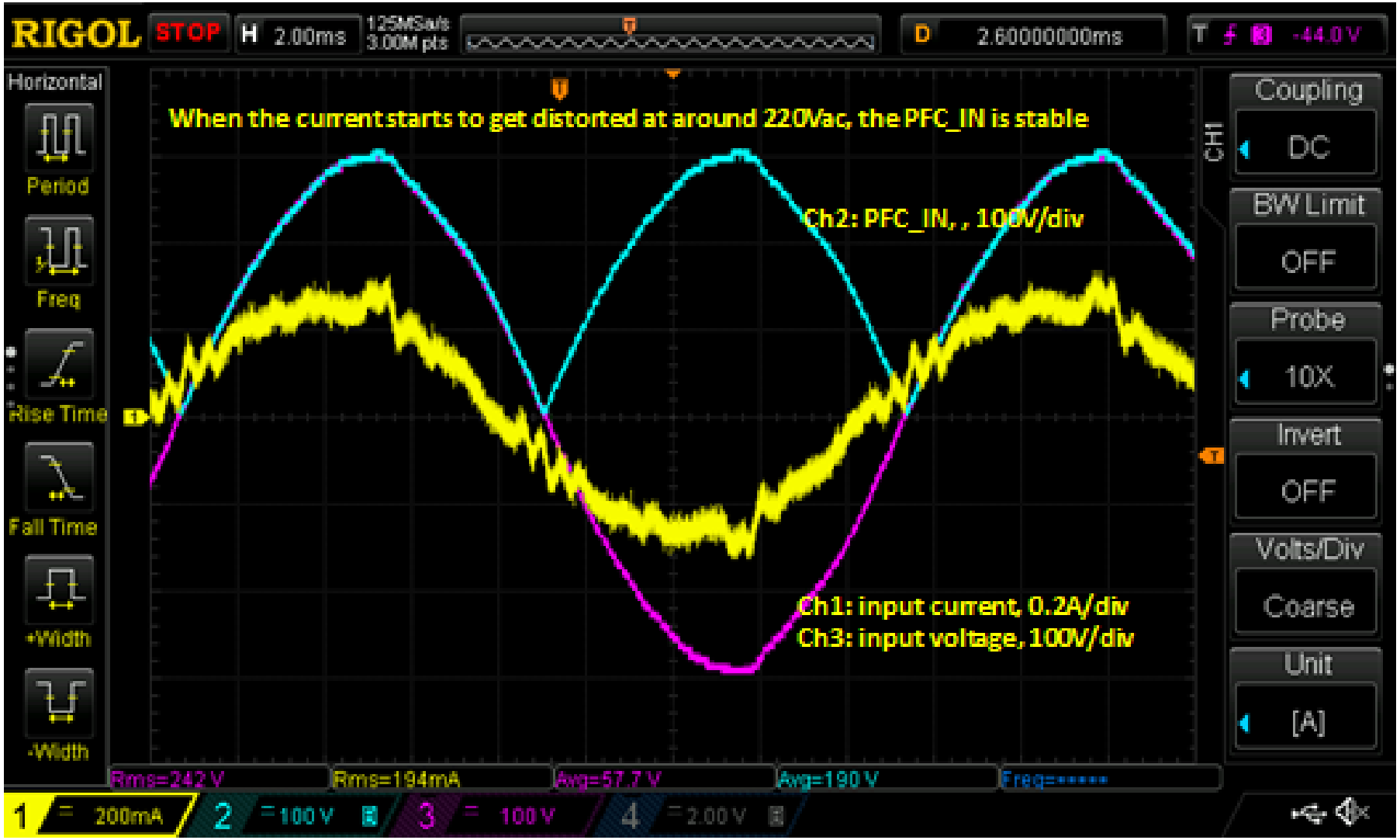
At the peak of sinewaves when distortion starts, the duty cycle of boost MOSFET is about 15%



At the peak of sinewaves at 120Vac, the duty cycle of boost MOSFET is about 54%



At 220Vac when distortions starts, the rectified input voltage (used for Vff) is shown below



Referring to Fig 36 in the data sheet of UCC28513DW, what specific capacitor controls the min duty cycle?

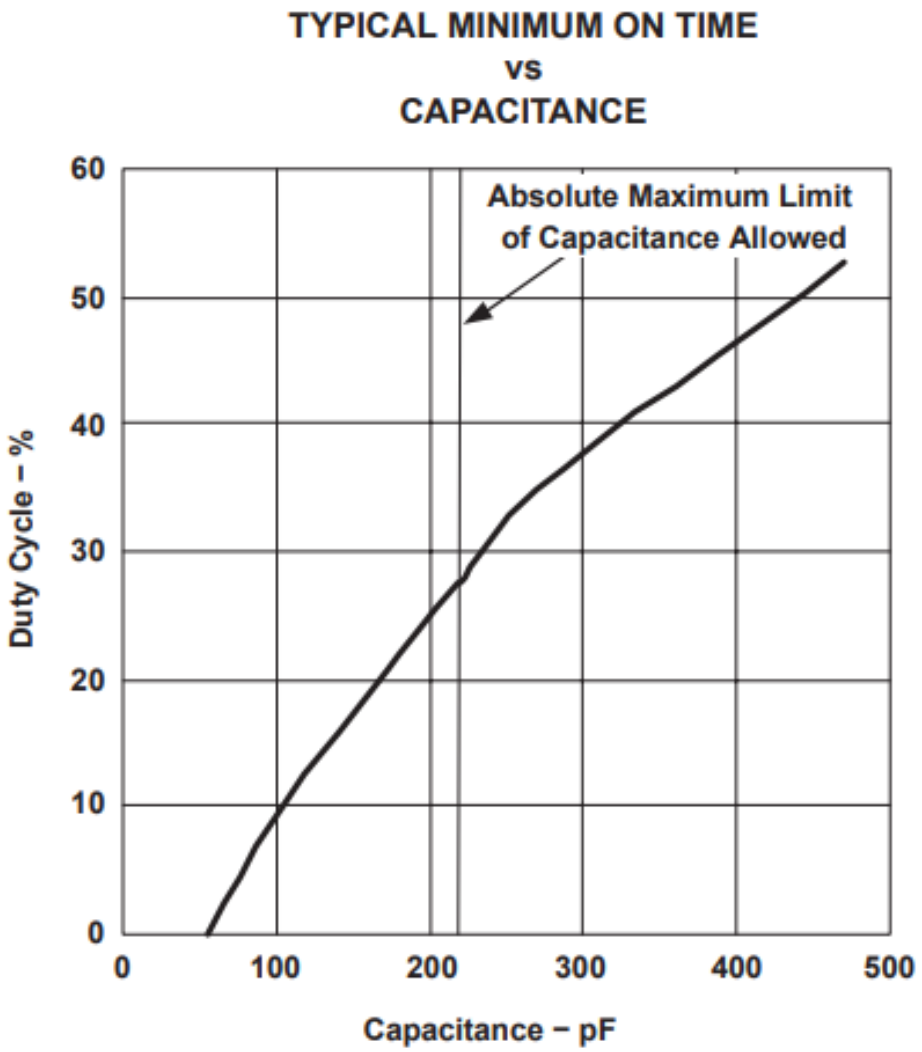
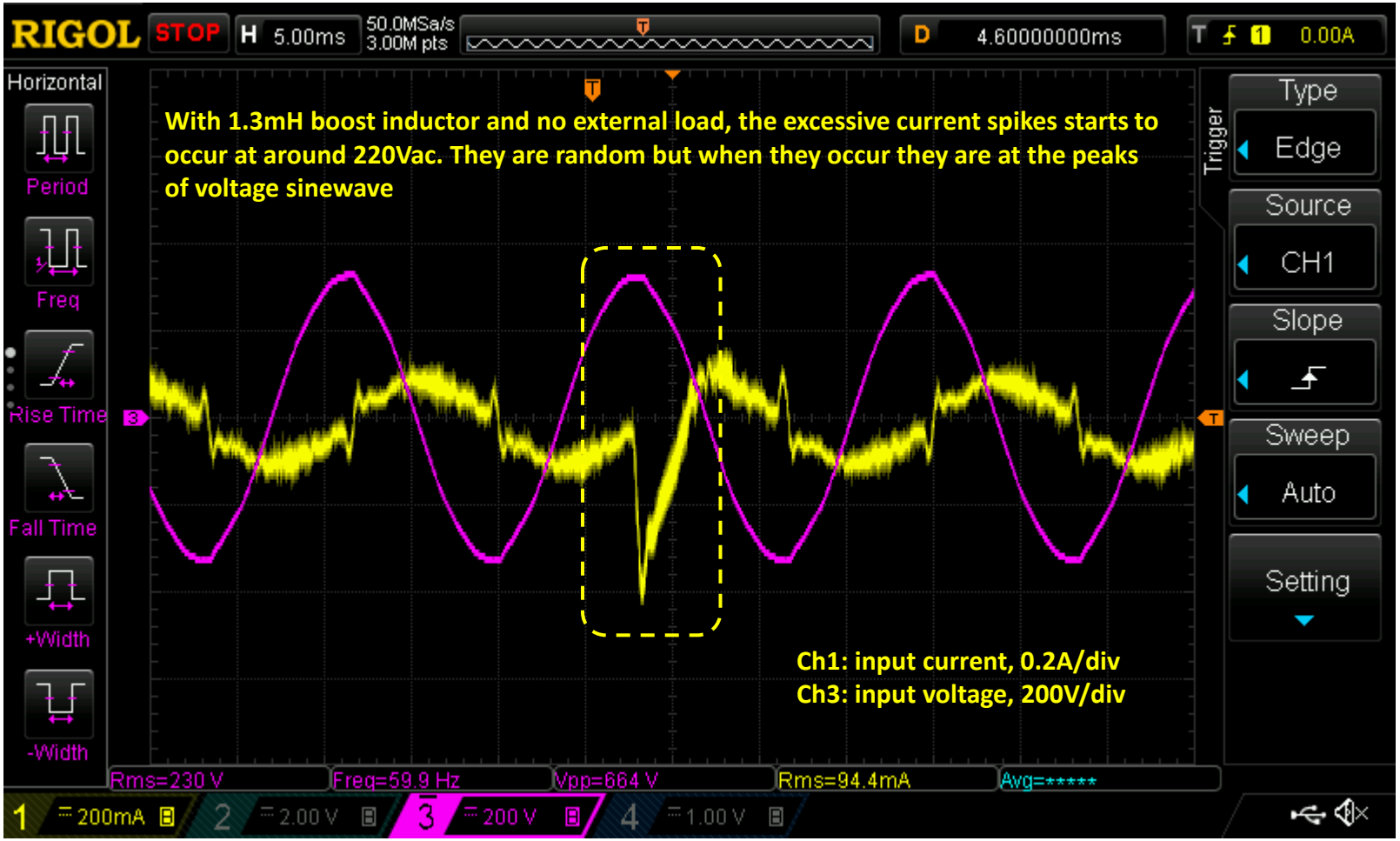


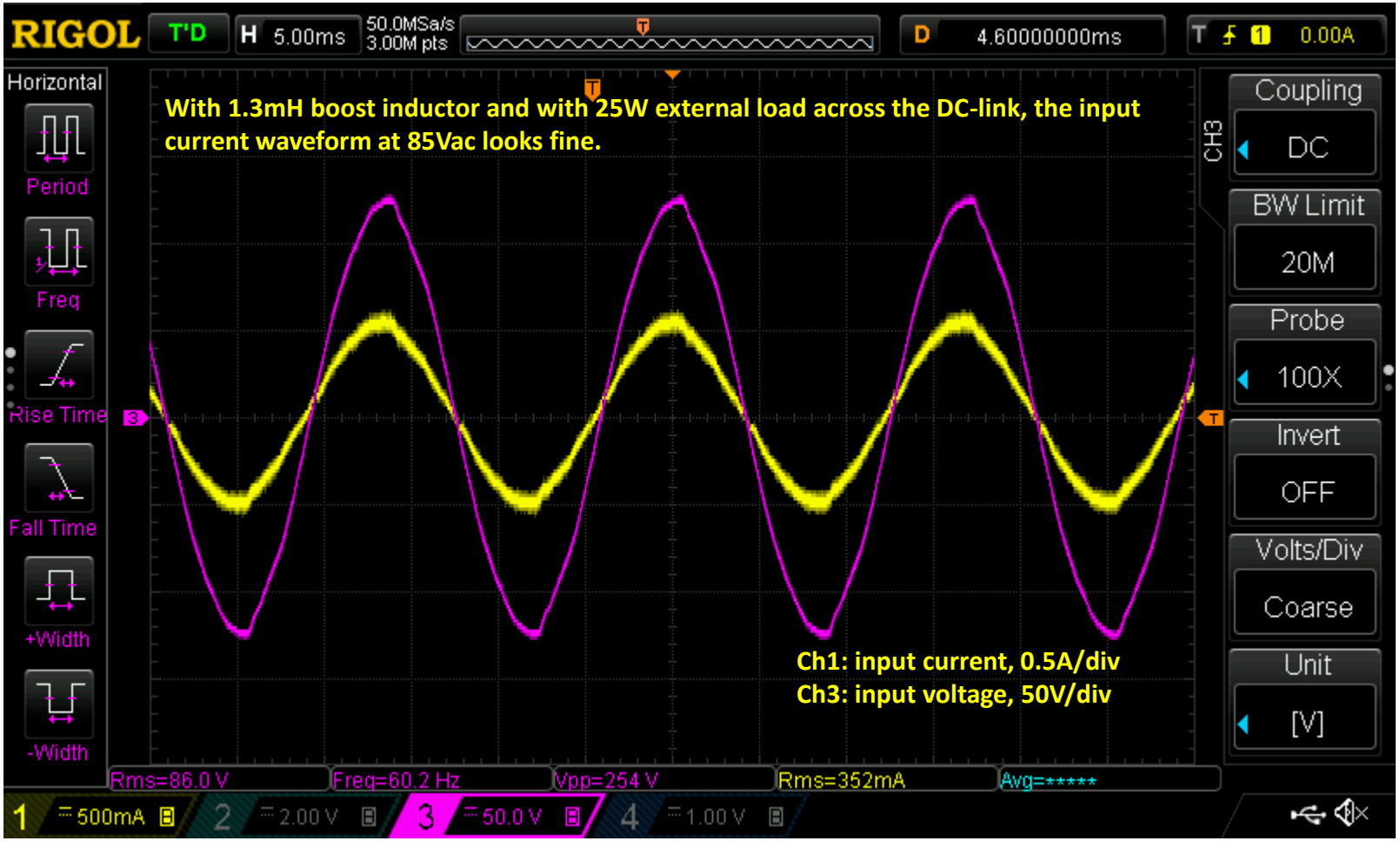
Figure 36

Note: The capacitor on Isense2 affects the min duty cycle on GATE2 output, PFC is on GATE1 output

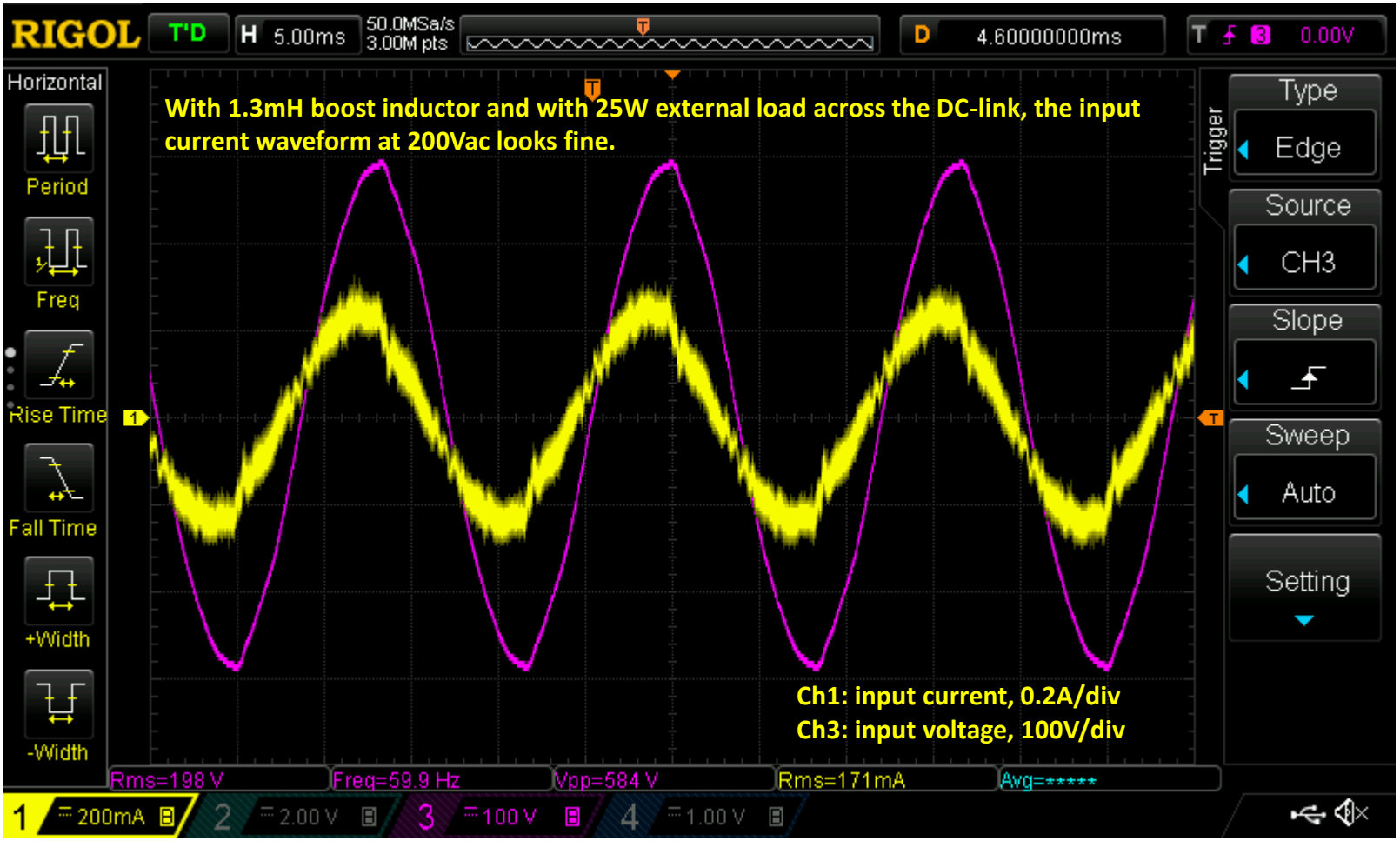
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



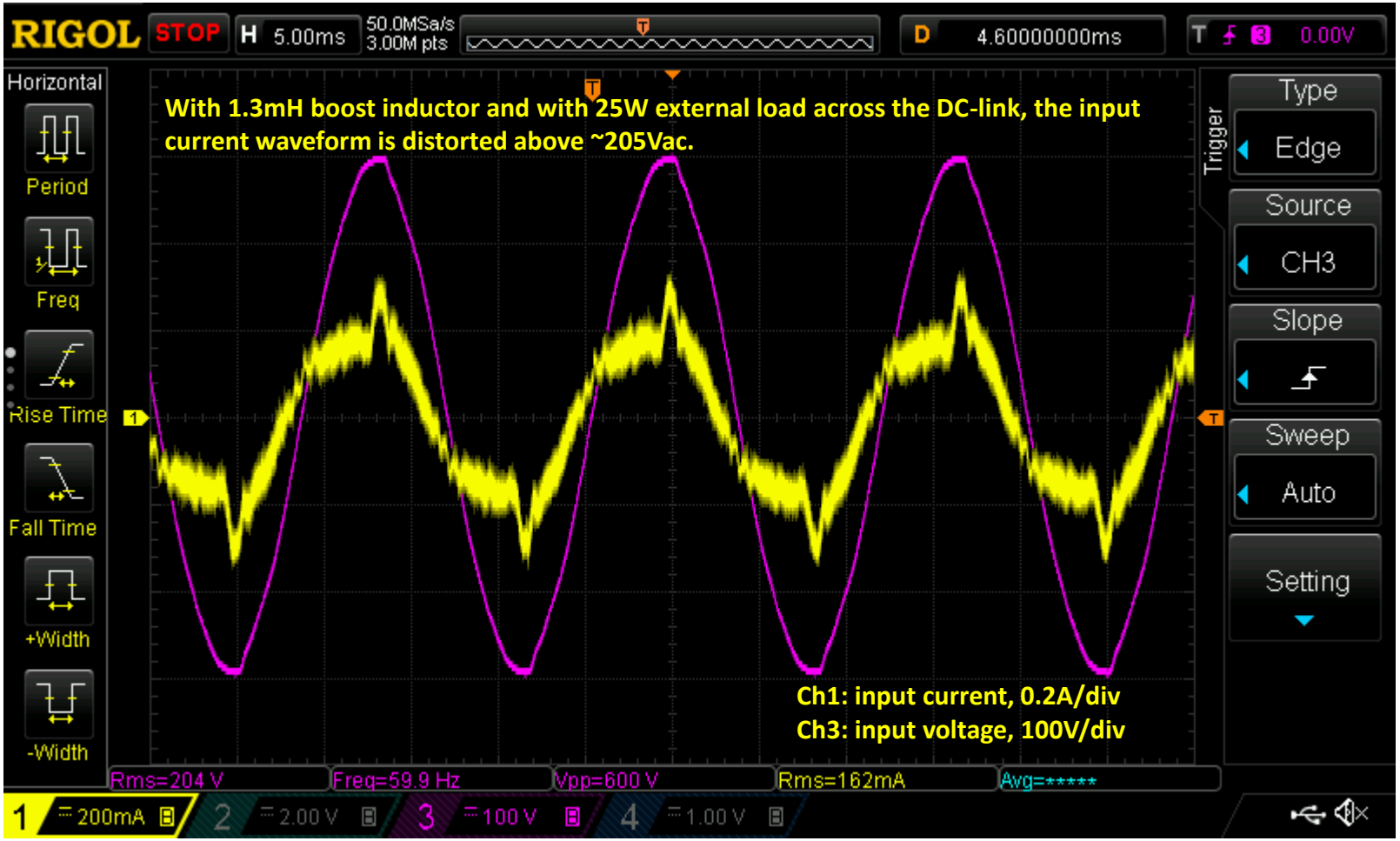
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



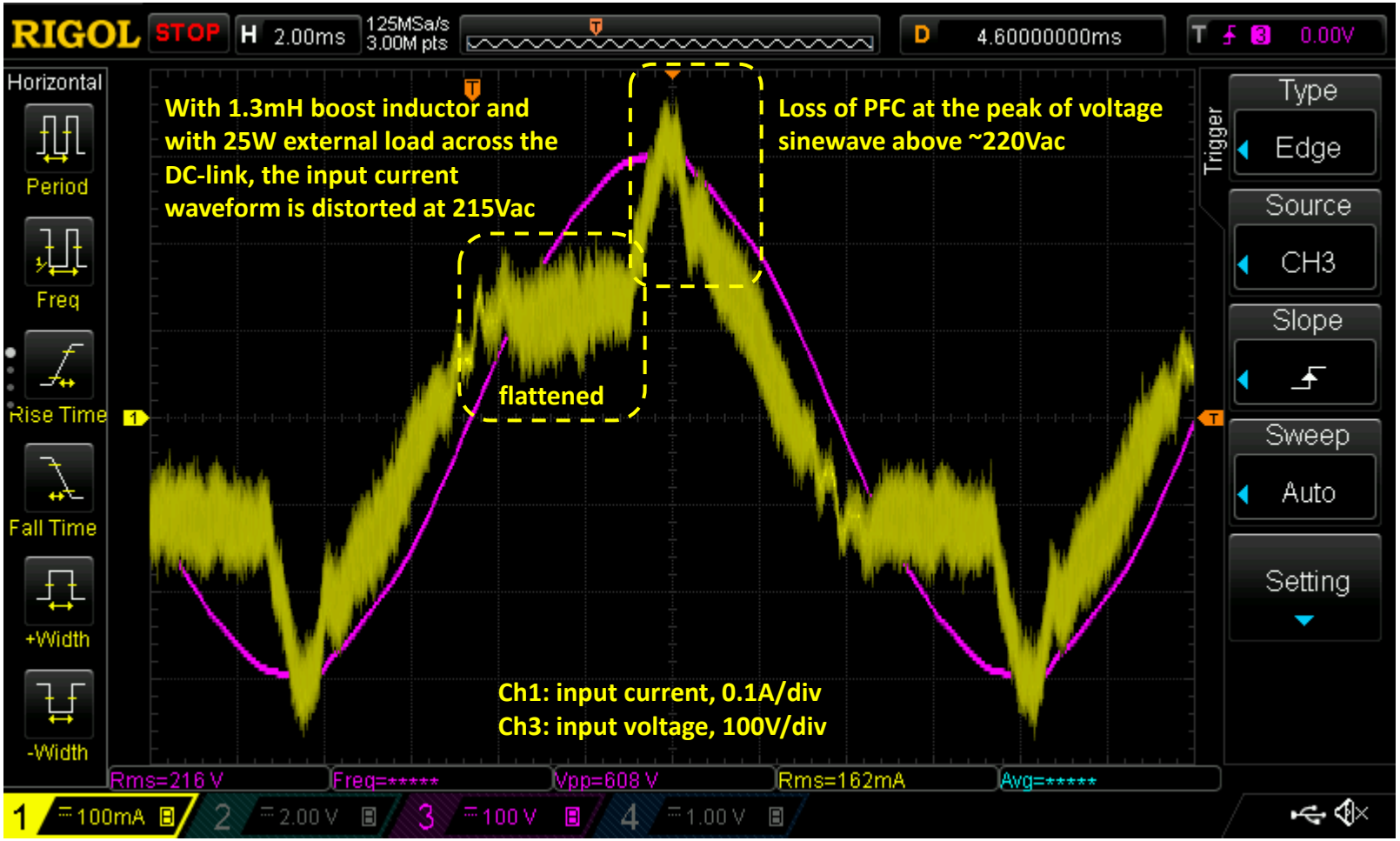
Boost inductor is changed from 660uH to 2x660uH= 1.32mH



Boost inductor is changed from 660uH to 2x660uH= 1.32mH



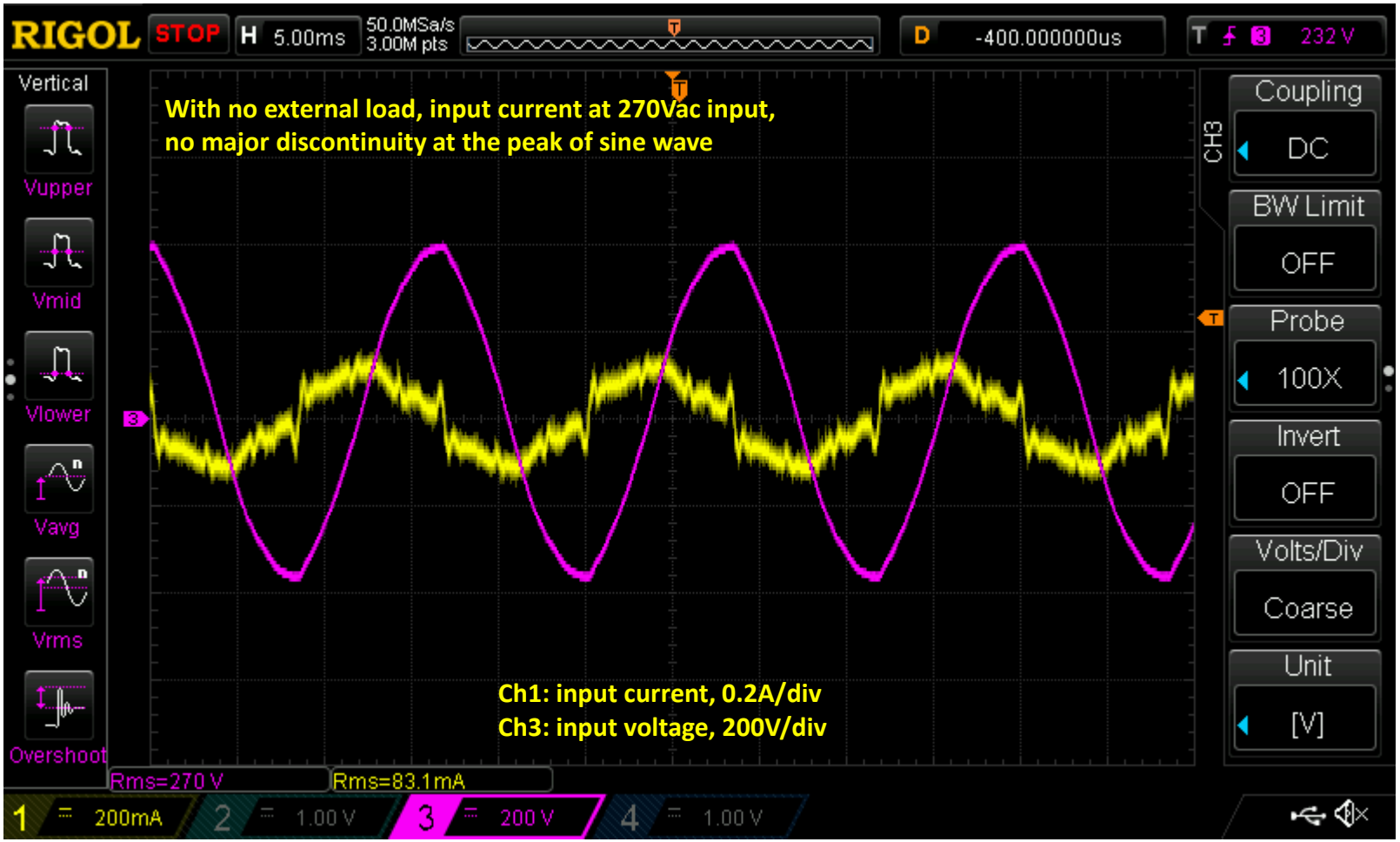
Boost inductor is changed from 660uH to 2x660uH= 1.32mH

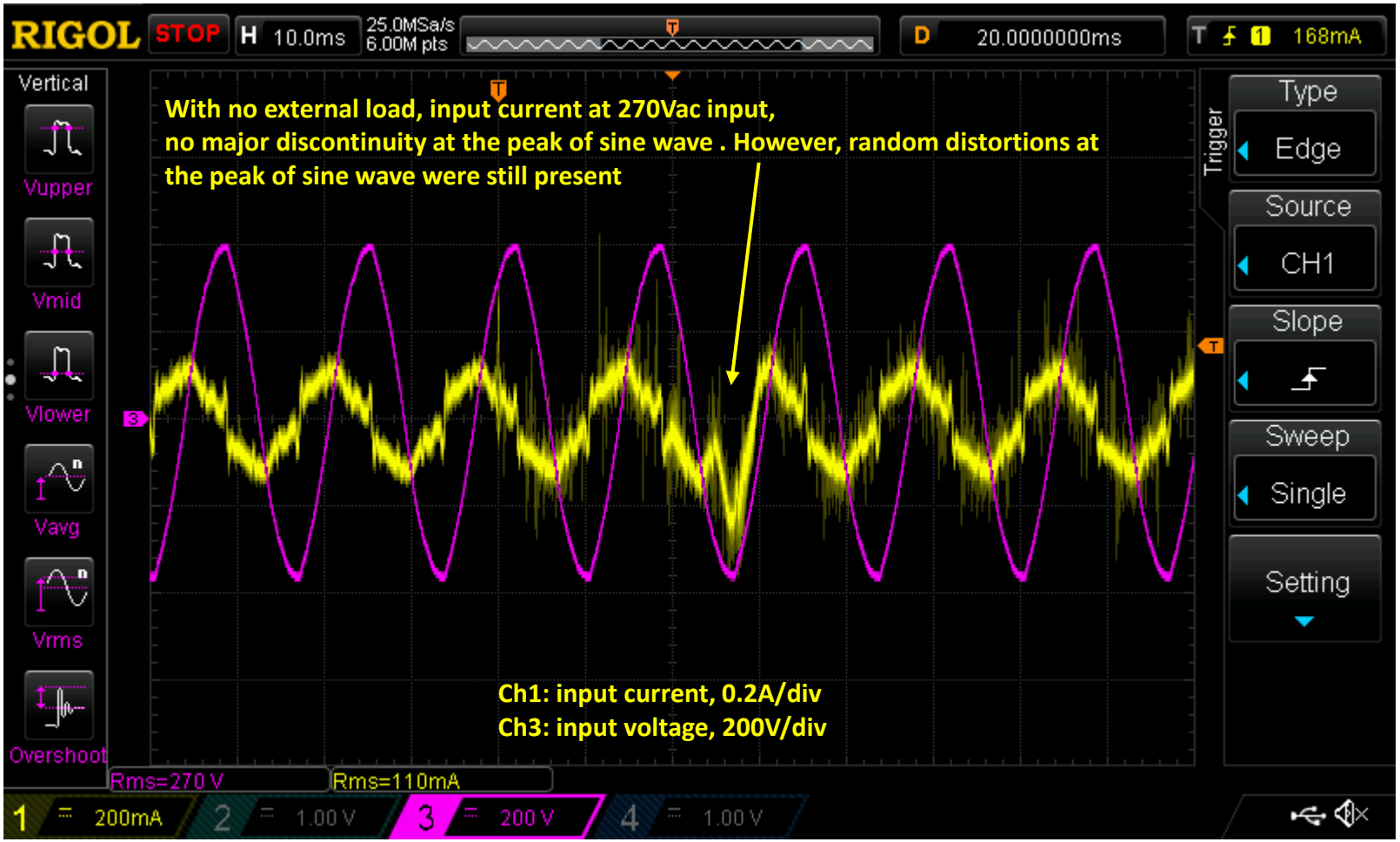


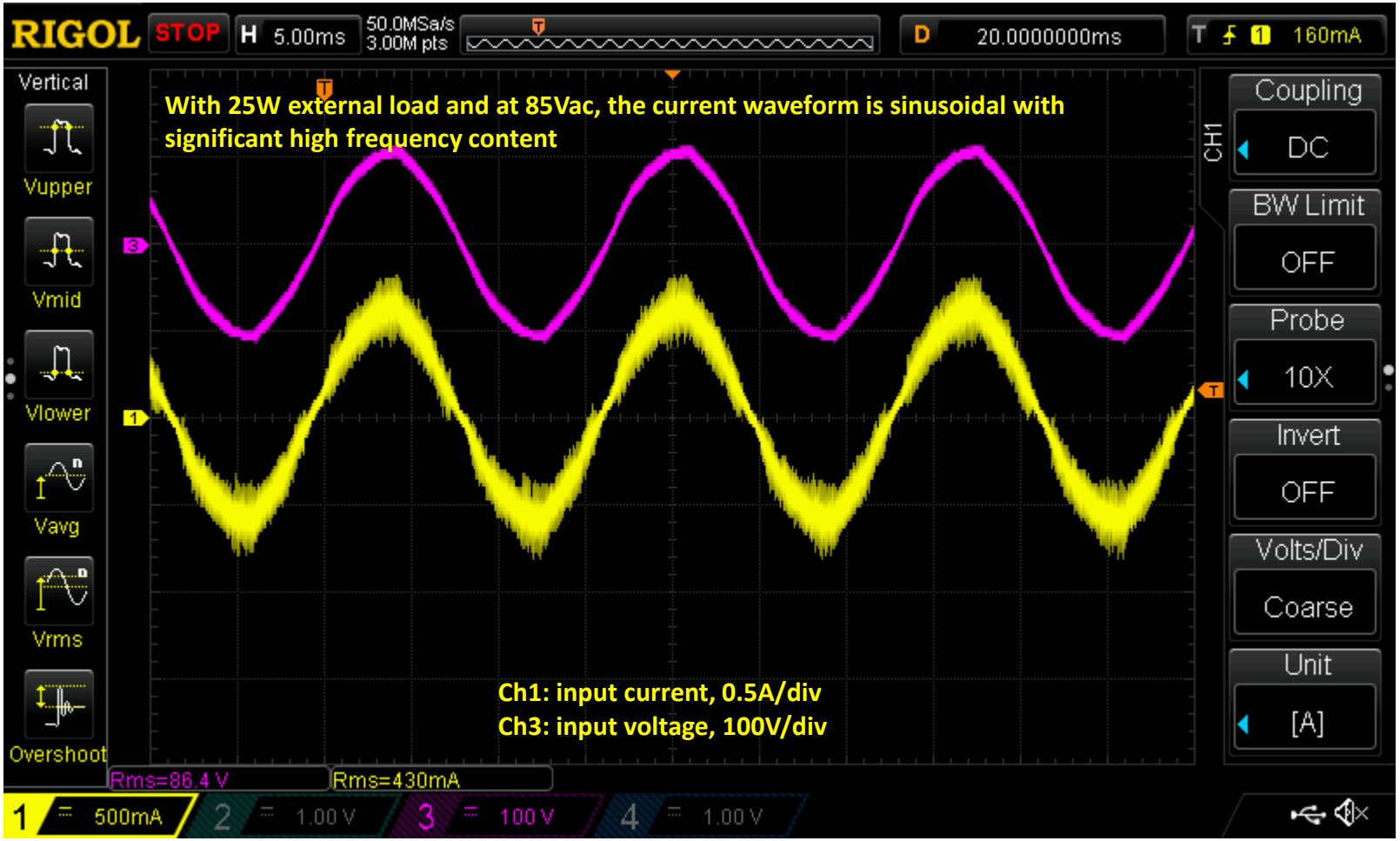
RefDes on data sheet	RefDes in design	values	Values on 12/11/2022
R1	R47+R50	766K	
R2	R43	0.22	**0.44**
R8/R12	R4/R9	3.16K	**2.74K**
R3	R44+R49	1124K	
R4	R60	22.1k	
C1	C32	150uF	
L1	L2	660uH	
R13	R10	15.8K	**55K (56K//3.3Meg)**
C6	C6	680pF	**233pF (200p//33p)**
C7	C8	150pF	**33pF**
R15	R11	30.1K	
C8	C9	4.7uF	
C10	C1	1.5uF	
C11	C2	150nF	
R21	R1	48.7K	
R14	R13	10K	
R7	R5	1.18K	**1.50K (3.3K//2.74K)**
C9	C4	1uF	

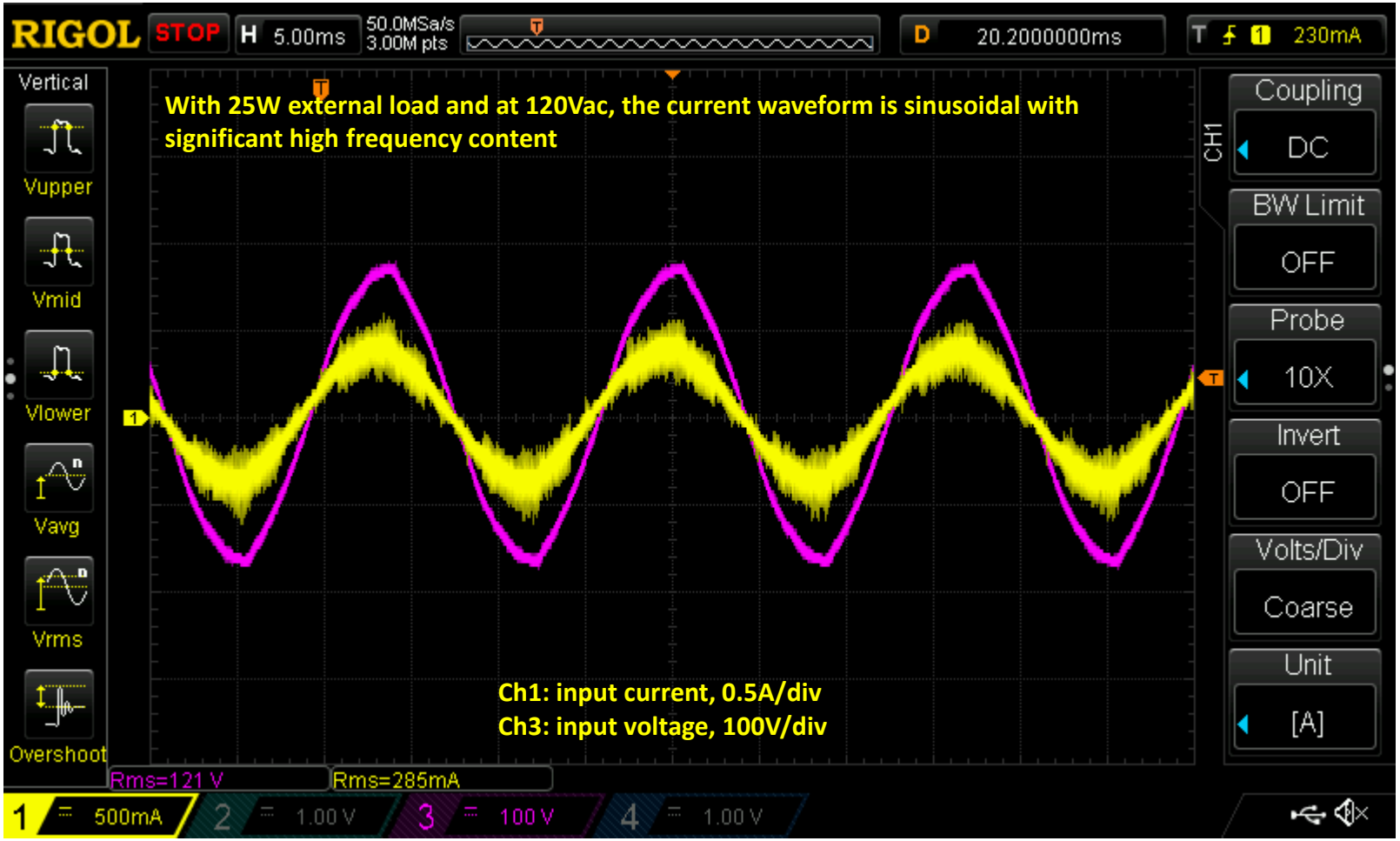
Changes made on 12/11 are highlighted

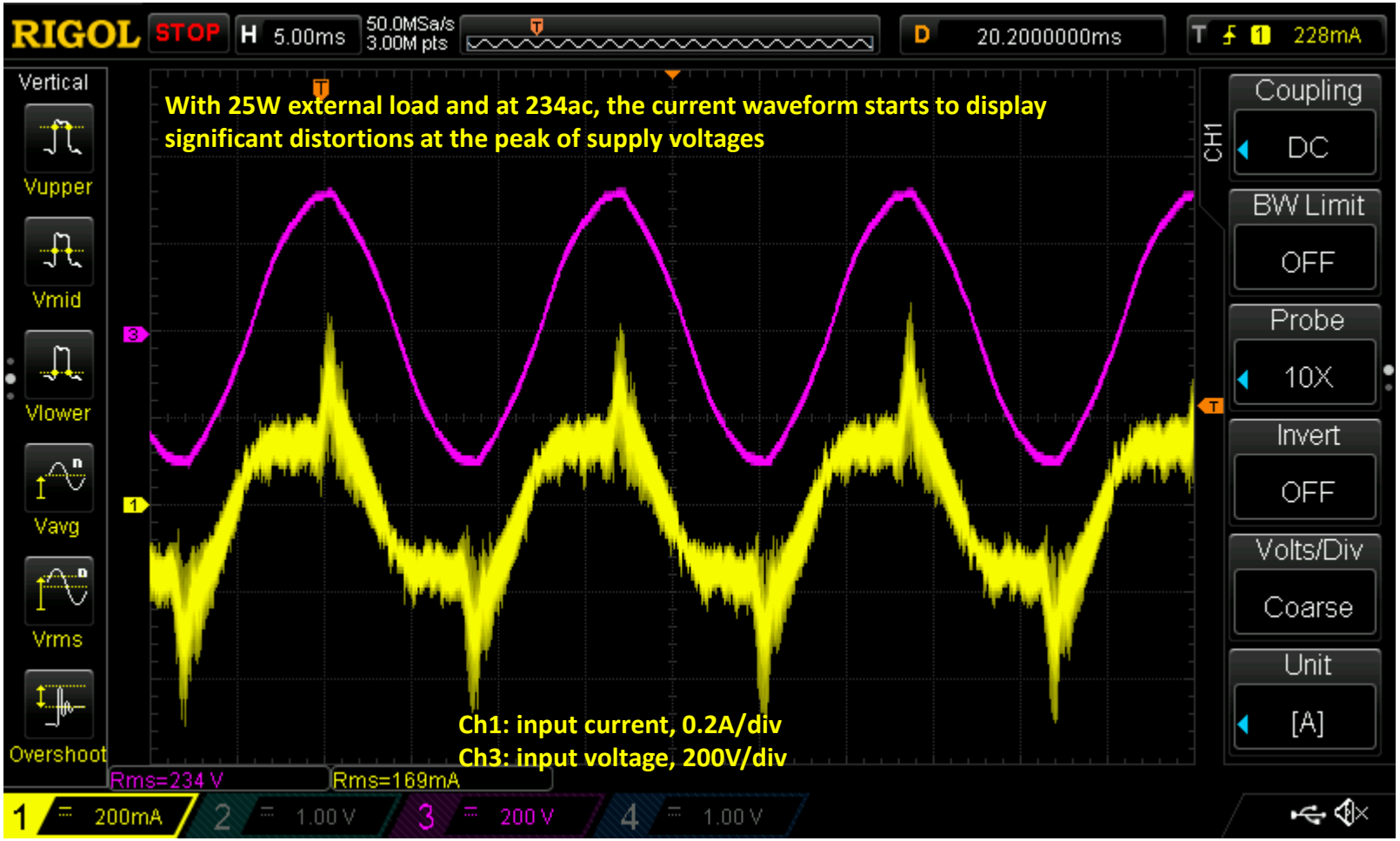
Also tried 15.8k


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D -400.000000us
T 232 V
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With no external load, input current at 270Vac input,
no major discontinuity at the peak of sine wave
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Rms=270 V
Rms=83.1mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V
CH3
Coupling
DC
BW Limit
OFF
Probe
100X
Invert
OFF
Volts/Div
Coarse
Unit
[V]


RIGOL
STOP
H 10.0ms
25.0MSa/s
6.00M pts
D 20.0000000ms
T 168mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With no external load, input current at 270Vac input,
no major discontinuity at the peak of sine wave . However, random distortions at
the peak of sine wave were still present
Trigger
Type
Edge
Source
CH1
Slope
Sweep
Single
Setting
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Rms=270 V
Rms=110mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 20.0000000ms
T 160mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 85Vac, the current waveform is sinusoidal with significant high frequency content
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]
Rms=86.4 V
Rms=430mA
1 500mA
2 1.00 V
3 100 V
4 1.00 V


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 20.2000000ms
T 230mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 120Vac, the current waveform is sinusoidal with significant high frequency content
Ch1: input current, 0.5A/div
Ch3: input voltage, 100V/div
Rms=121 V
Rms=285mA
1 500mA
2 1.00 V
3 100 V
4 1.00 V
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]


RIGOL
STOP
H 5.00ms
50.0MSa/s
3.00M pts
D 20.2000000ms
T 228mA
Vertical
Vupper
Vmid
Vlower
Vavg
Vrms
Overshoot
With 25W external load and at 234ac, the current waveform starts to display significant distortions at the peak of supply voltages
Ch1: input current, 0.2A/div
Ch3: input voltage, 200V/div
Rms=234 V
Rms=169mA
1 200mA
2 1.00 V
3 200 V
4 1.00 V
CH1
Coupling
DC
BW Limit
OFF
Probe
10X
Invert
OFF
Volts/Div
Coarse
Unit
[A]

Measuring inductor current vs gate voltages, 12/18

There are only two current probes at the moment:

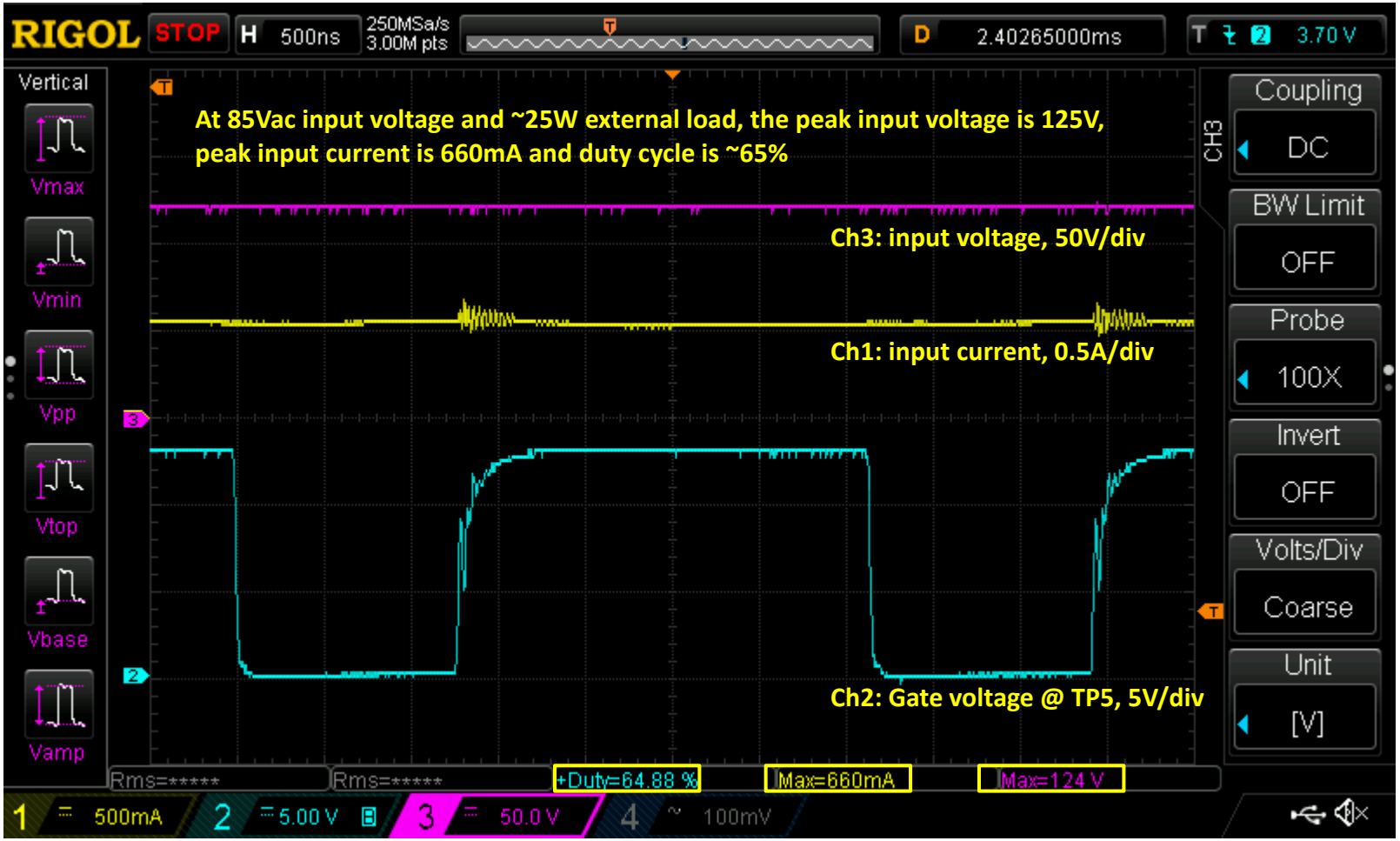
Ch1: Fluke 80i-110S has limited bandwidth and is used to measure 60Hz input current only.

Ch4: Rogowski probe, CWTUM-015-B, is used to measure the high frequency switching ripple only.

In addition, a 100mΩ and 20mΩ sense resistor was connected in series with inductor and the voltage across the resistor was measured with a differential probe. However, doing so resulted in further instability and distortion and therefore abandoned.

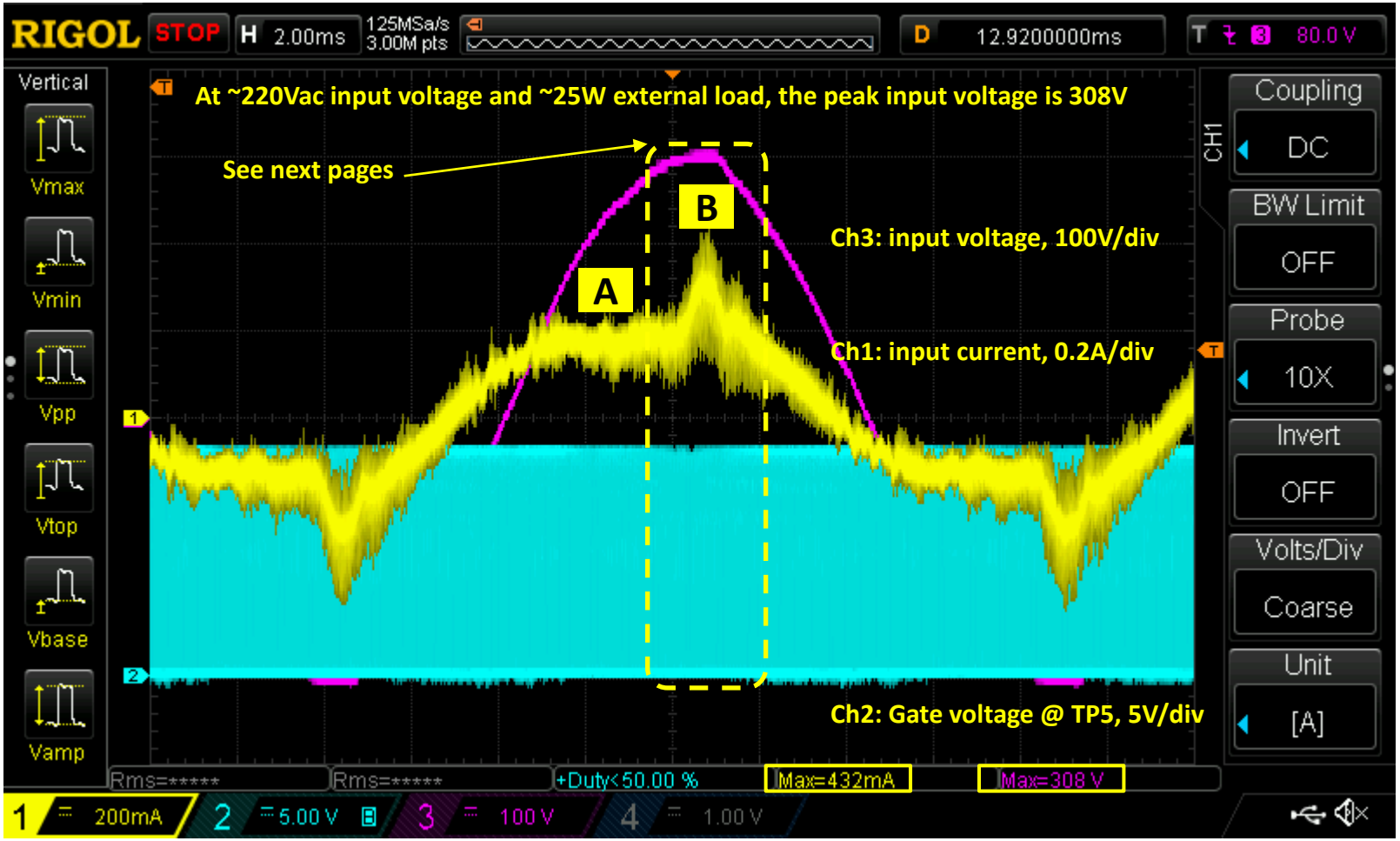
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



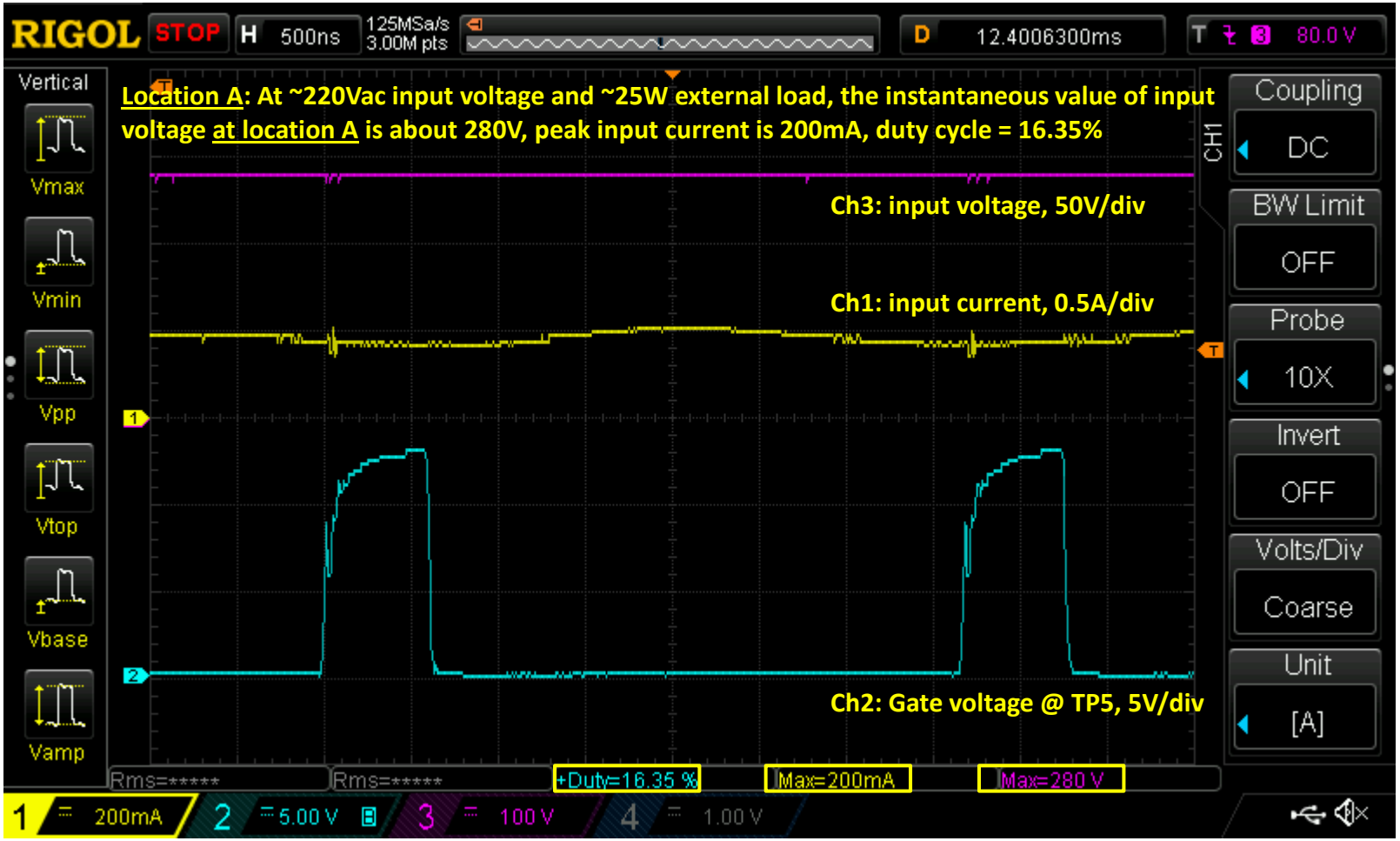
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



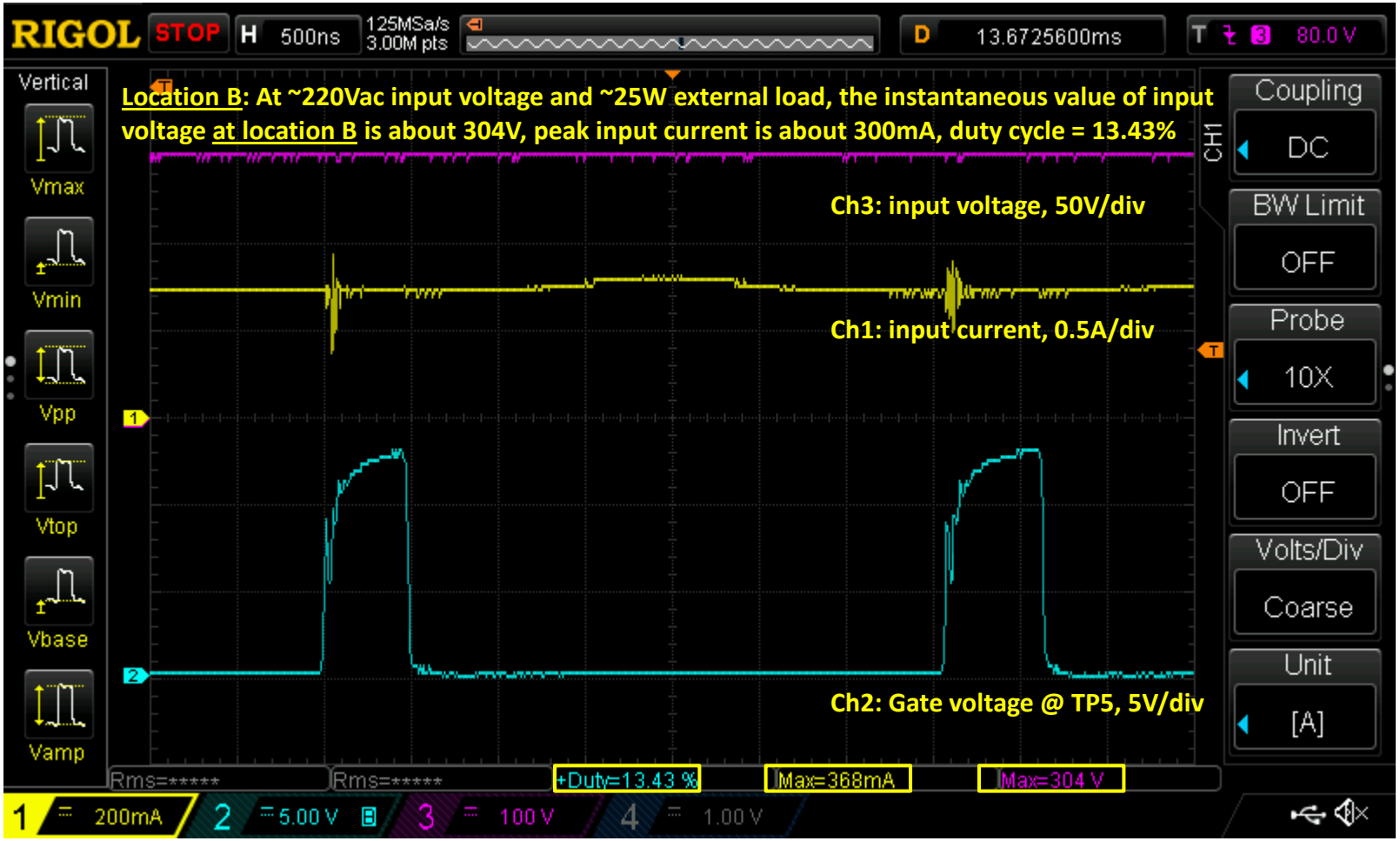
Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current



Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current

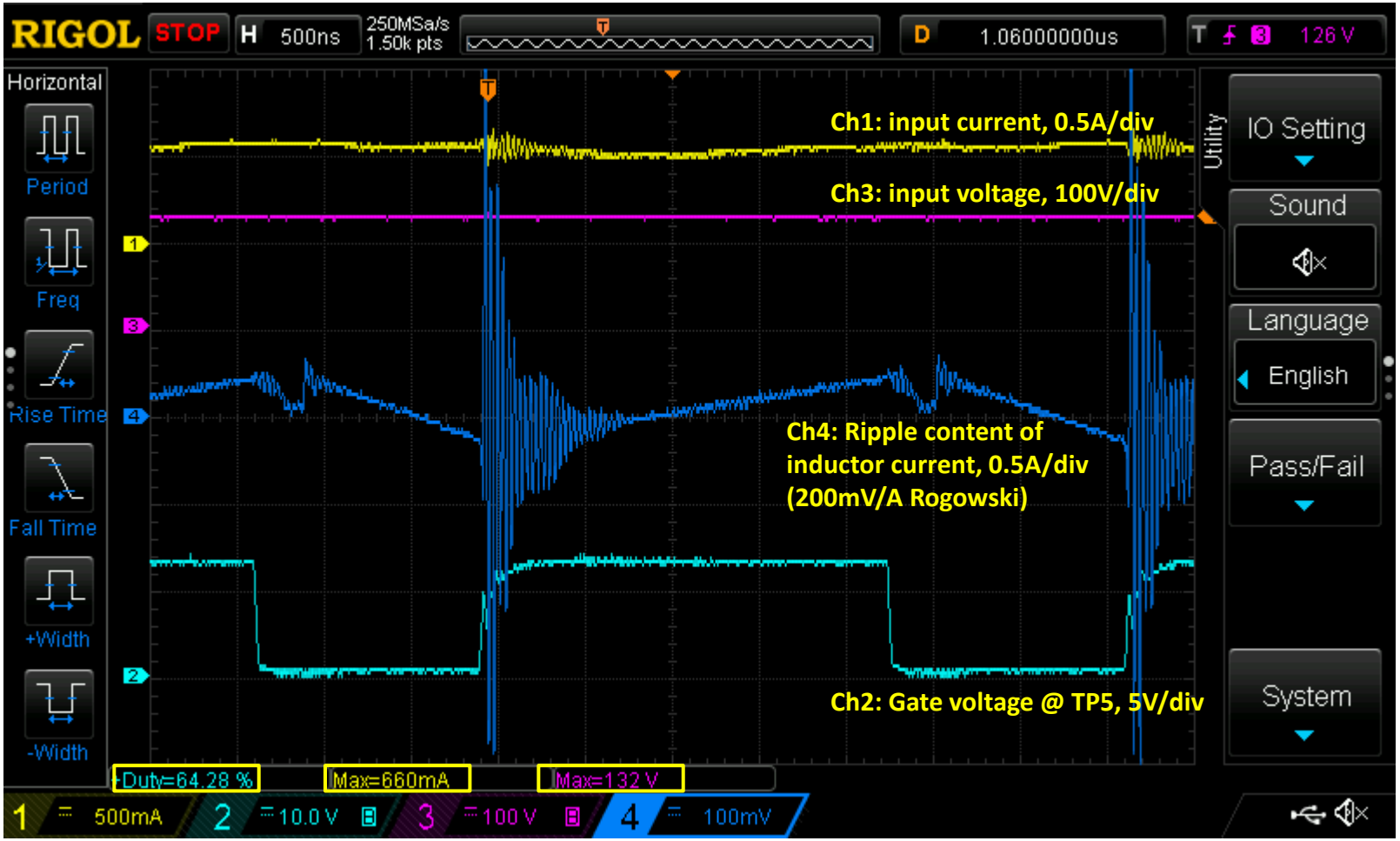


Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current

Ch4: Current probe is Rogowski CWTUM-015-B, which can measure high frequency only.

At the peak of 85Vac input voltage and ~25W external load, the instantaneous value of input voltage is 132V, peak input current is 660mA, duty cycle = 64.28%

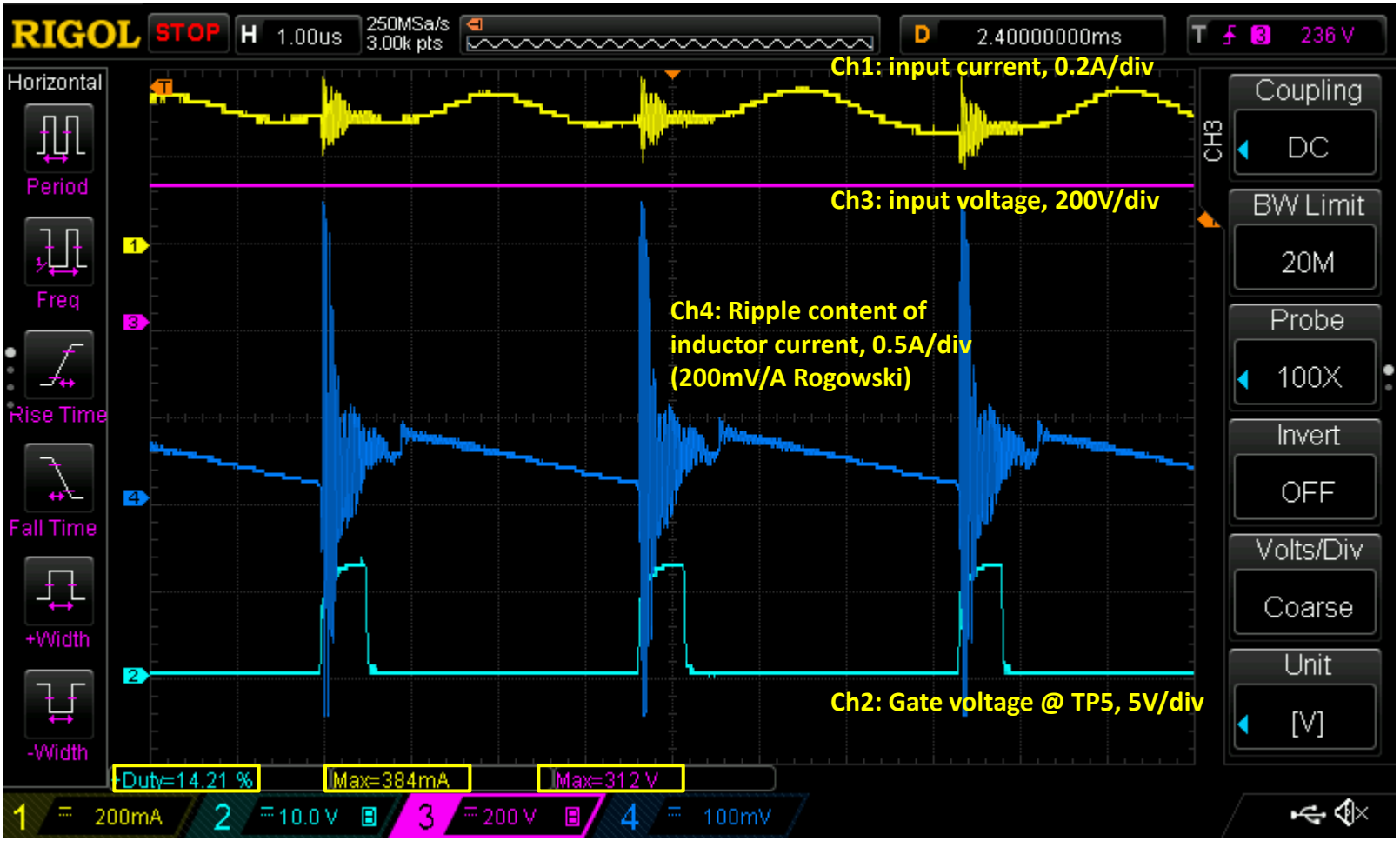


Measuring inductor current vs gate voltages, 12/18

Ch1: Current probe is Fluke 80i-110S, which has limited bandwidth and is used to measure 60Hz input current

Ch4: Current probe is Rogowski CWTUM-015-B, which can measure high frequency only.

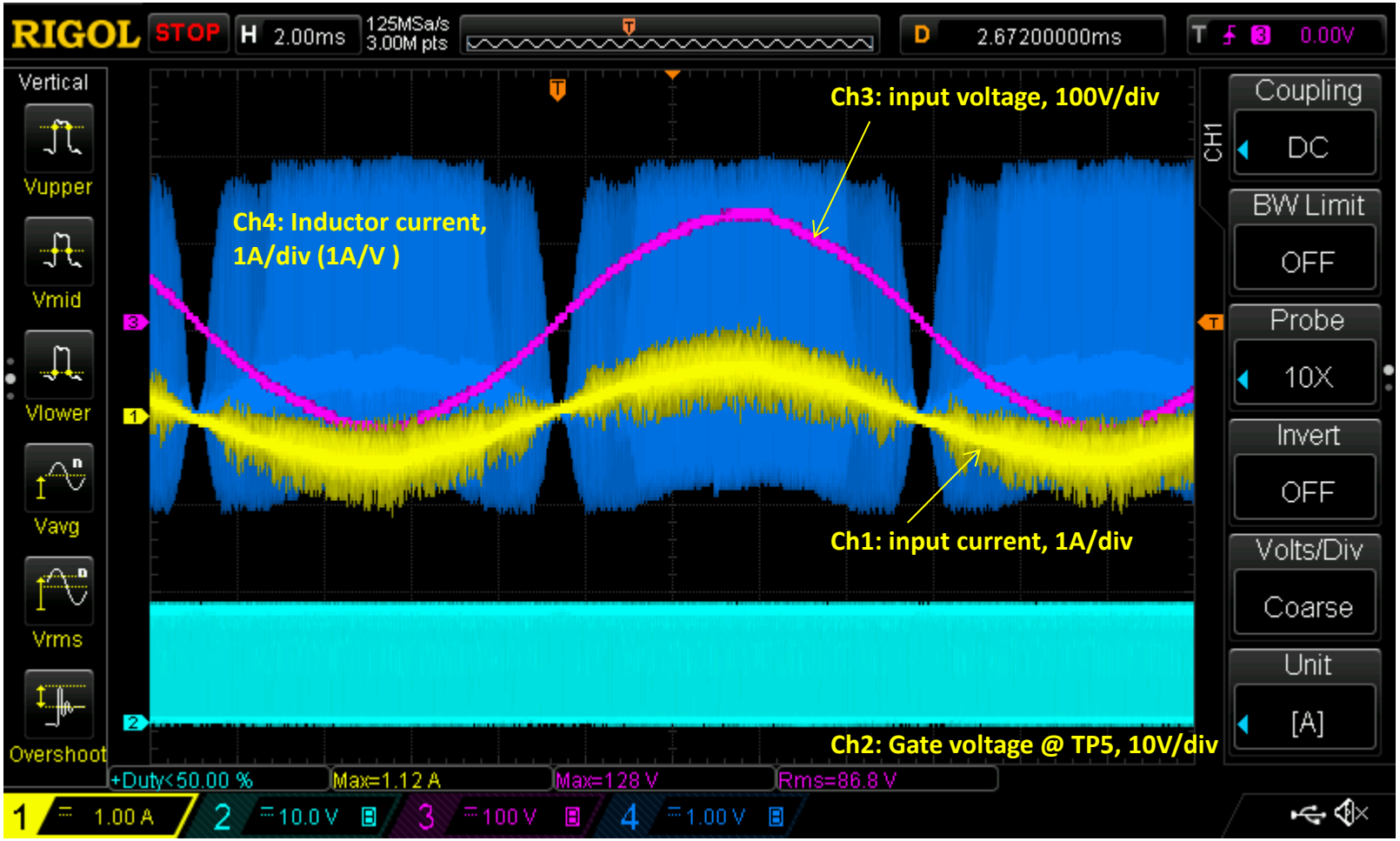
At the peak of 220Vac input voltage and ~25W external load, the instantaneous value of input voltage is 312V, peak input current is ~300mA (location B), duty cycle is about 14.2%



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

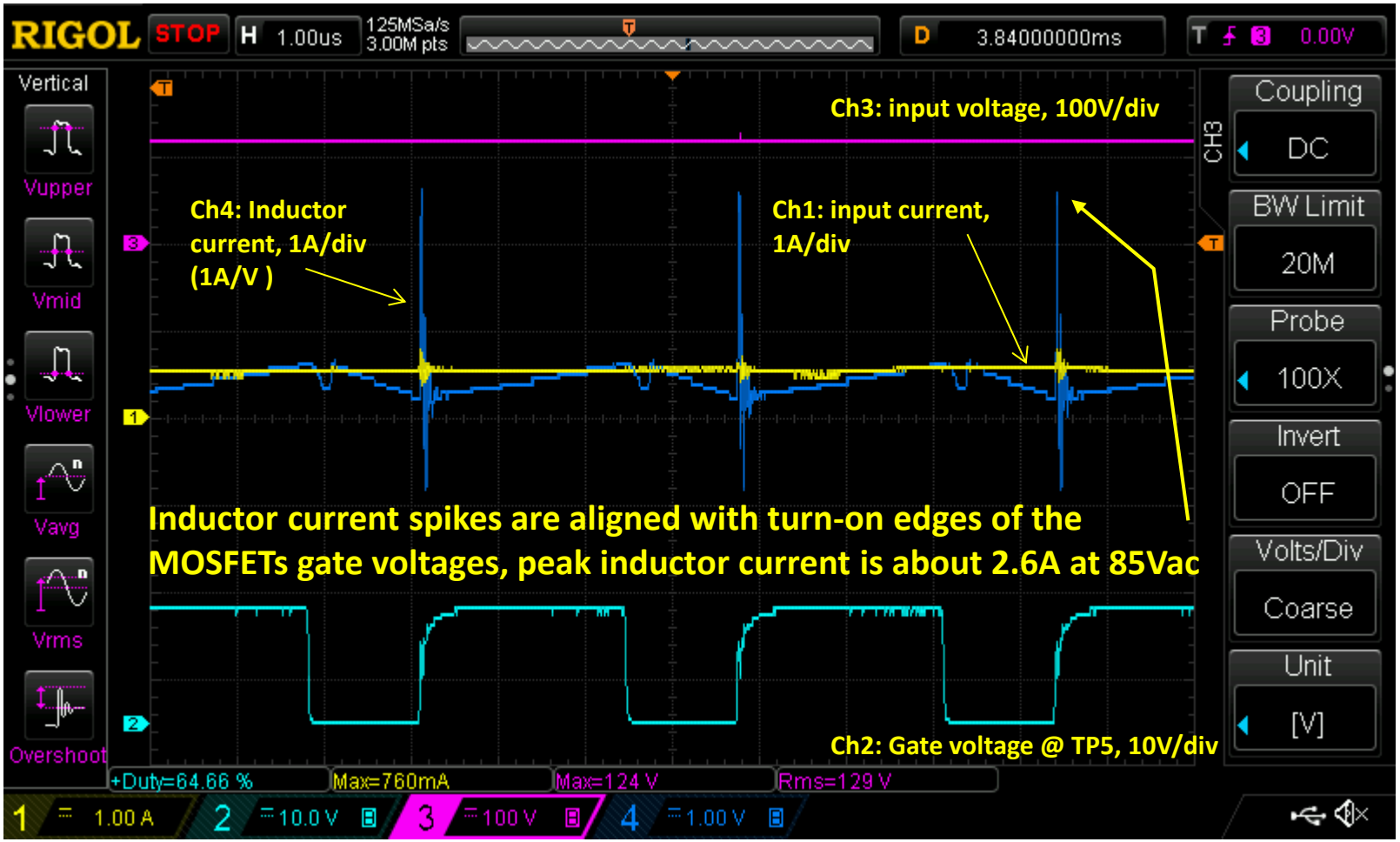
At 85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

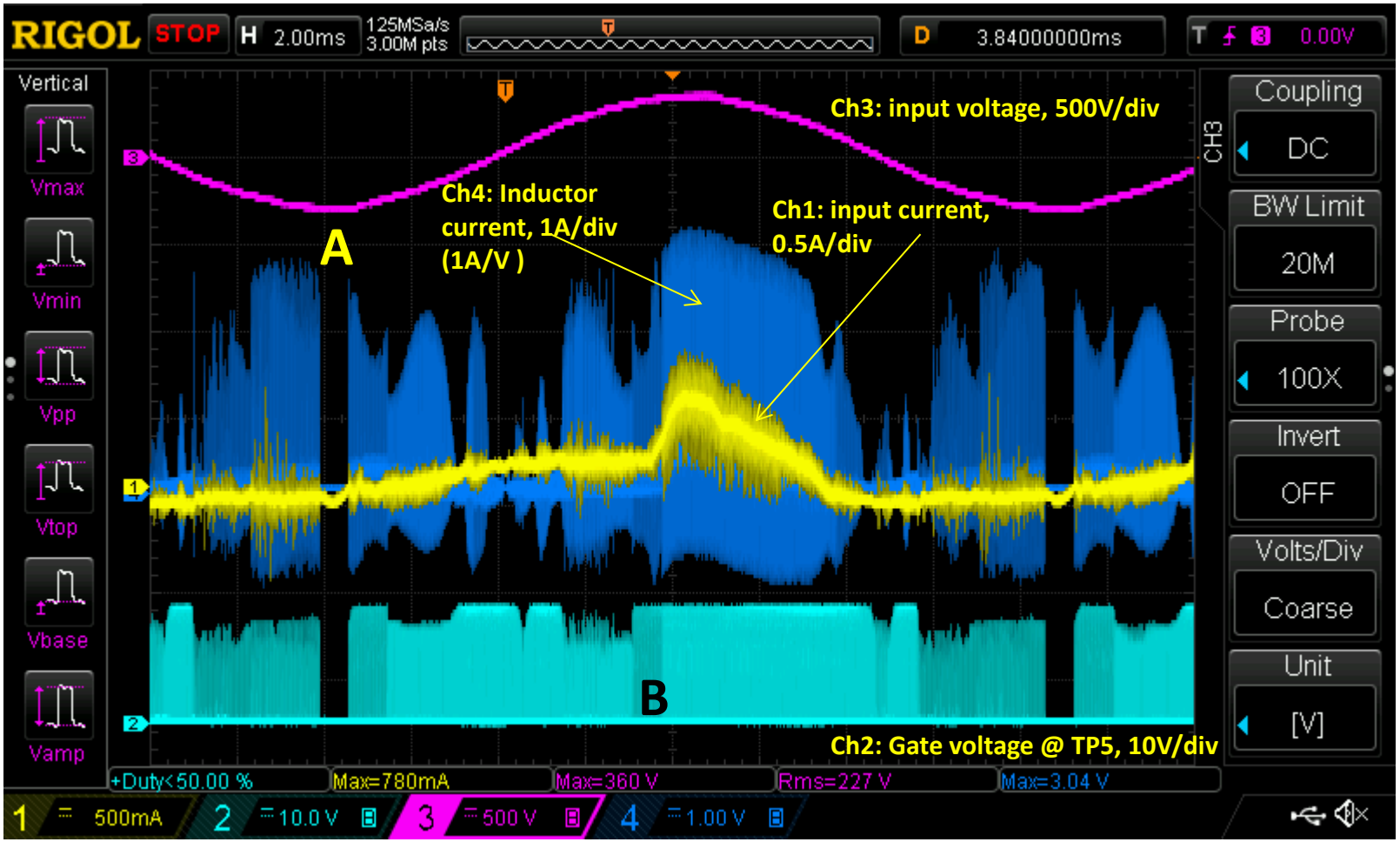
At 85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

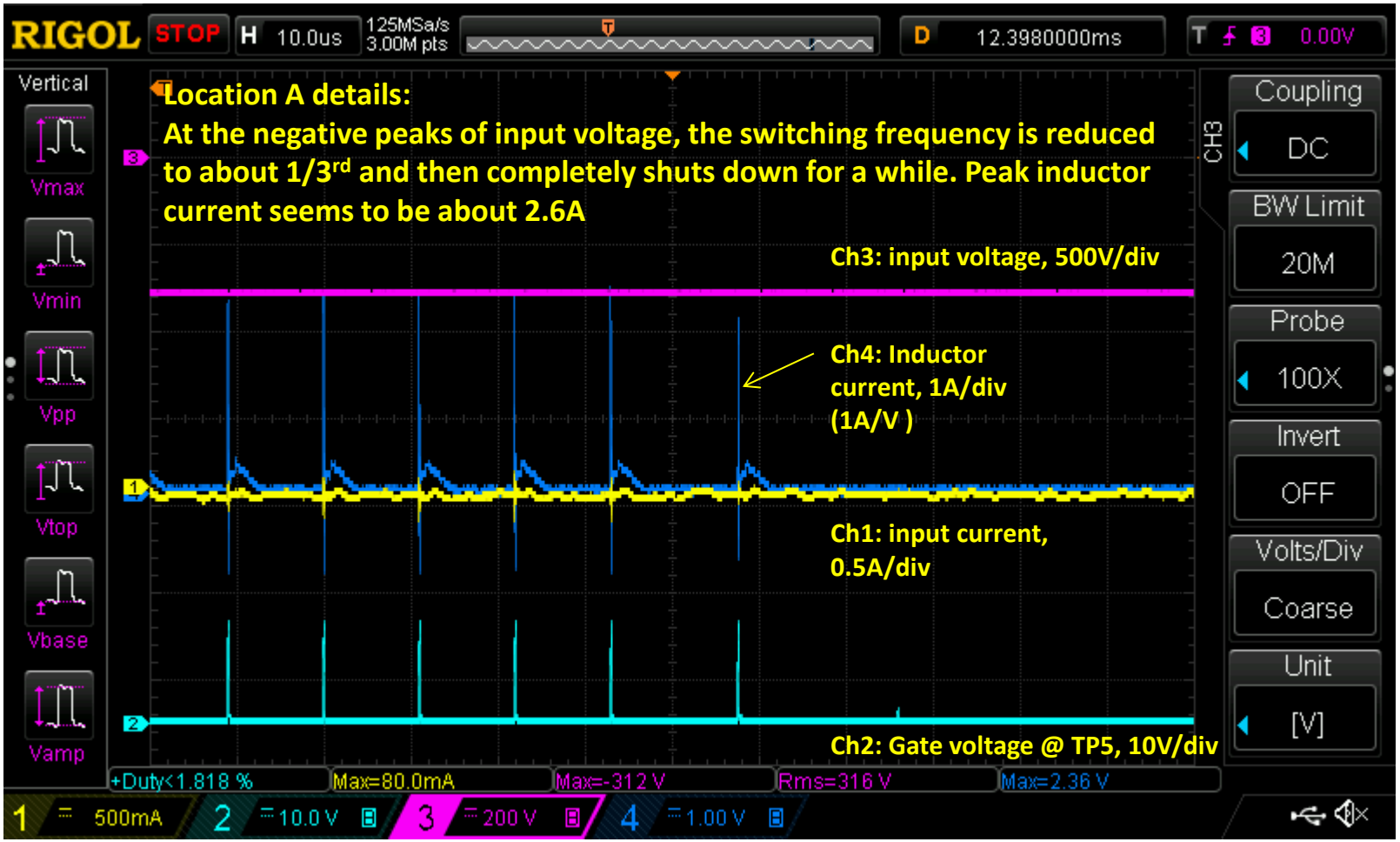
At ~230Vac input voltage and ~25W external load, distortions observed. See next slides for location A, B details



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe

At ~230Vac input voltage and ~25W external load, distortions observed.

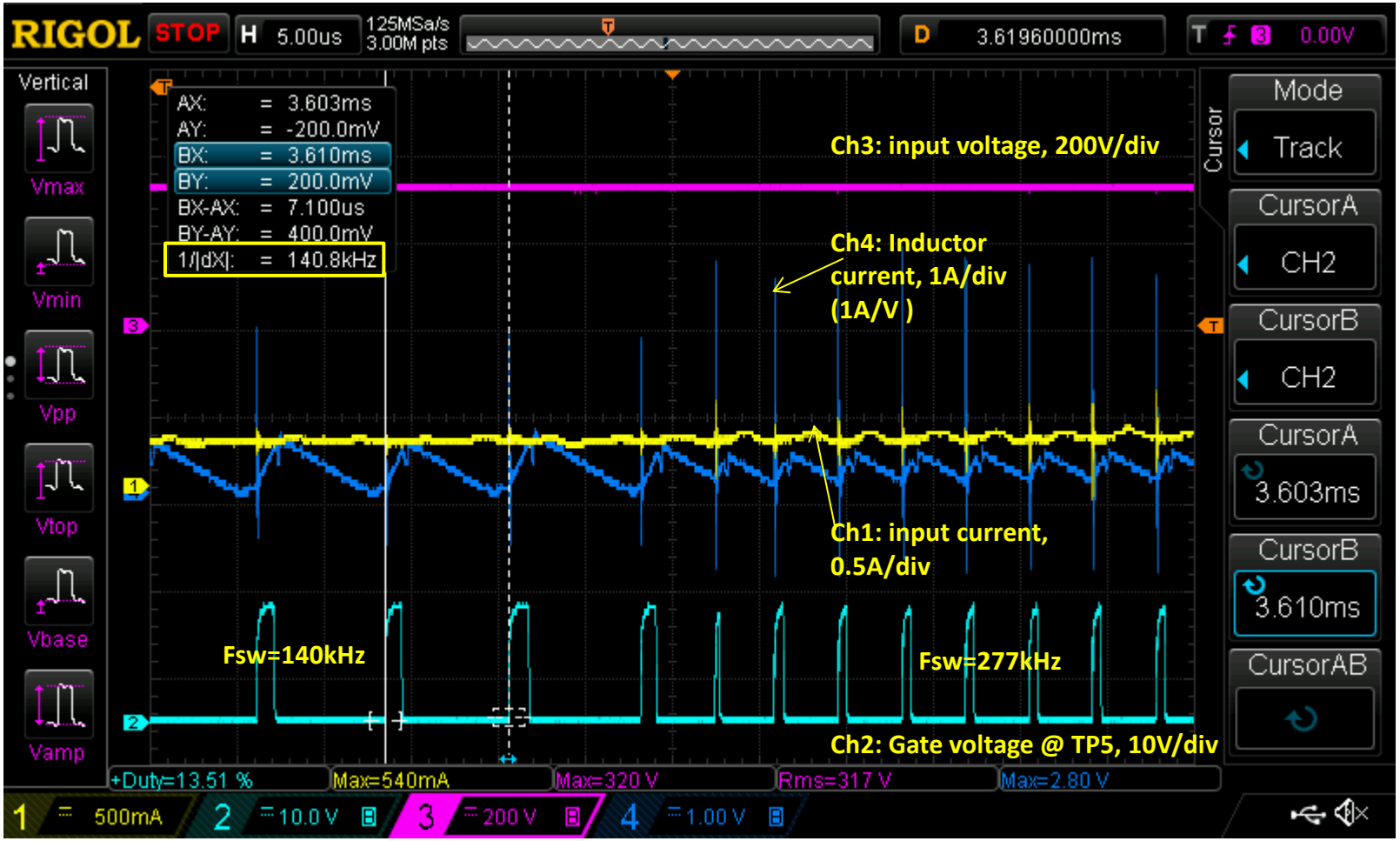


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Location B details:

At the positive peaks of input voltage, the switching frequency is reduced to about ½ and this results in "flat top" on the current waveform. After that the switching frequency is raised and around that time the current surge is observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
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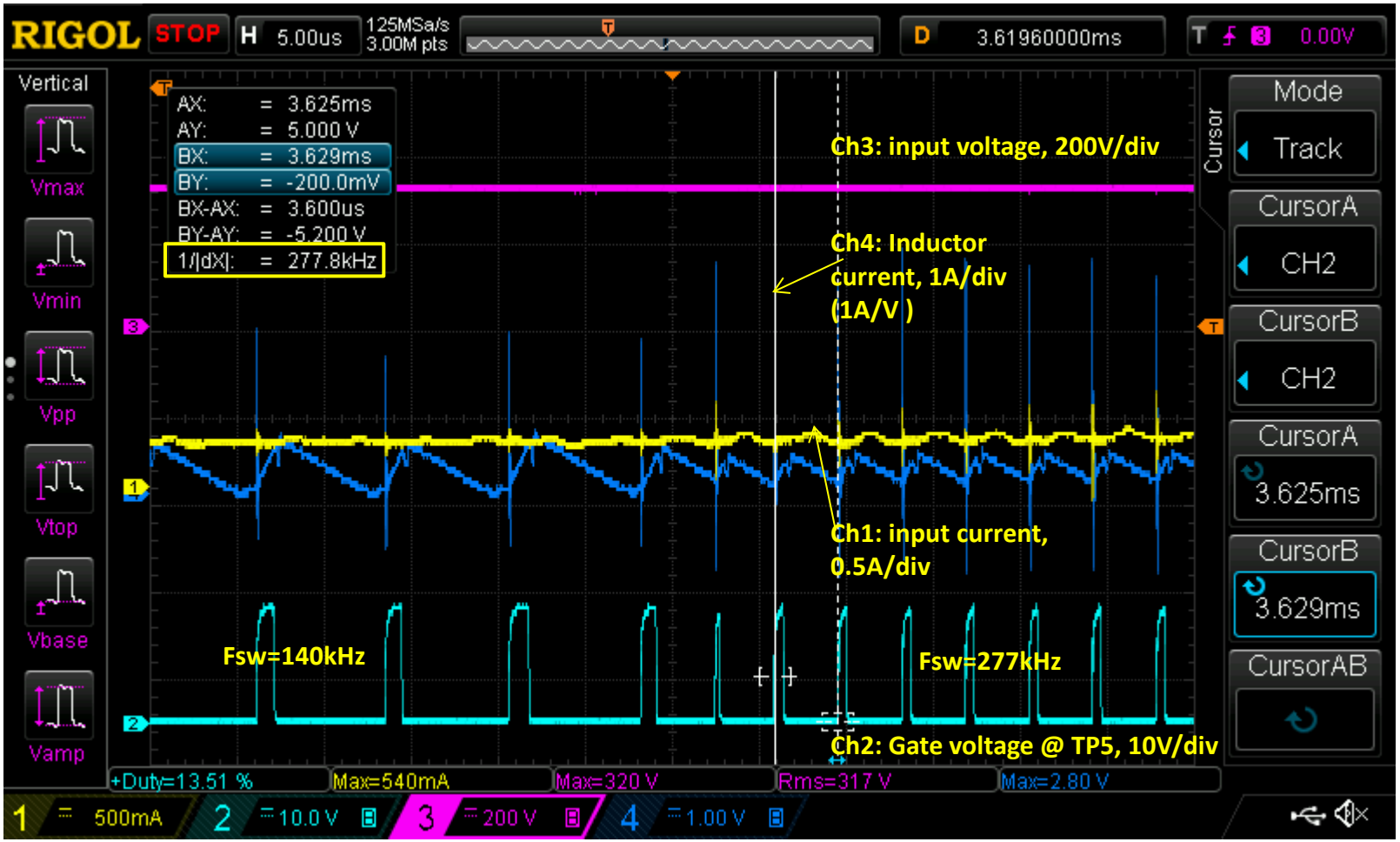
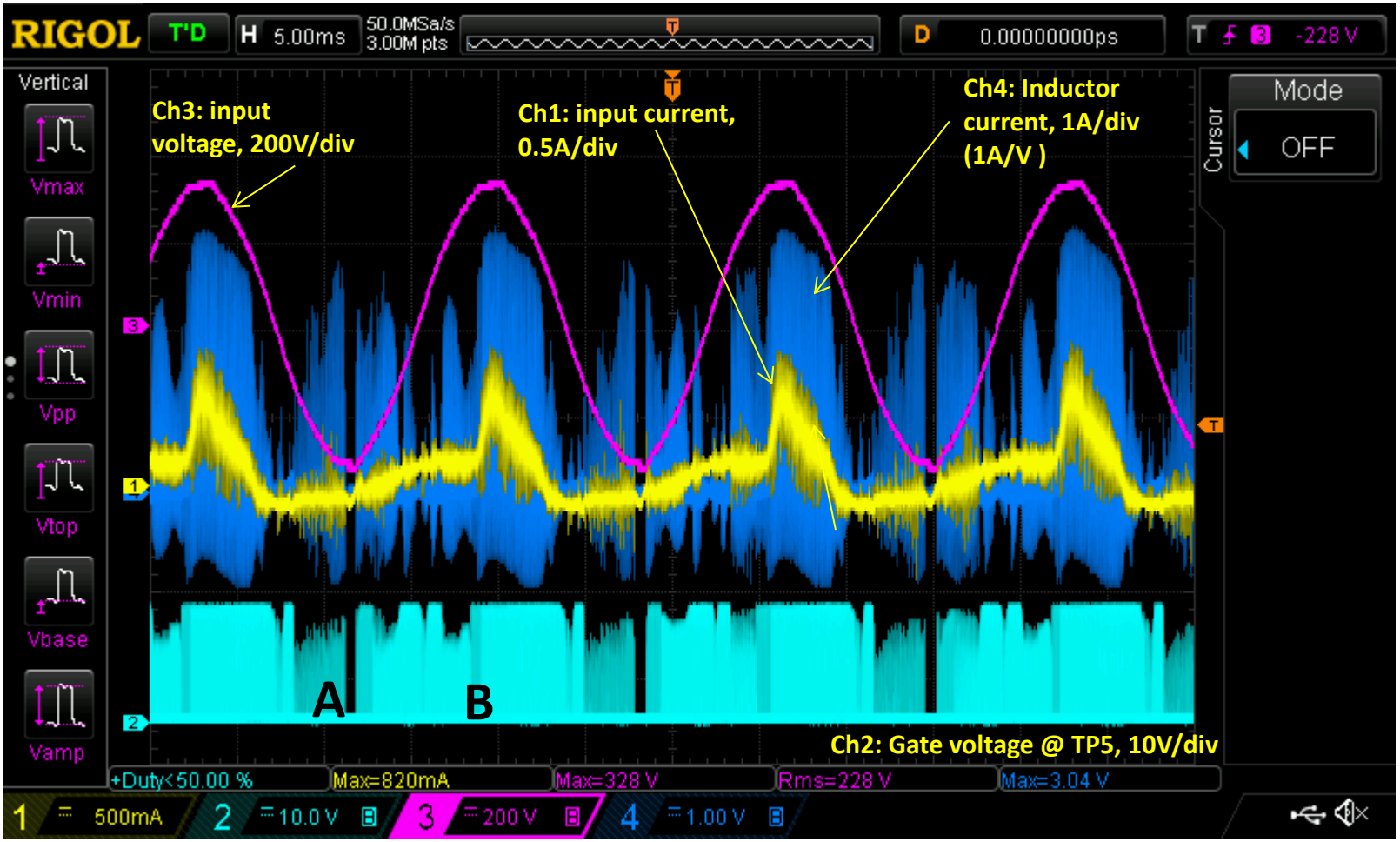
At the positive peaks of input voltage, the switching frequency is reduced to about ½ and this results in "flat top" on the current waveform. After that the switching frequency is raised and around that time the current surge is observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

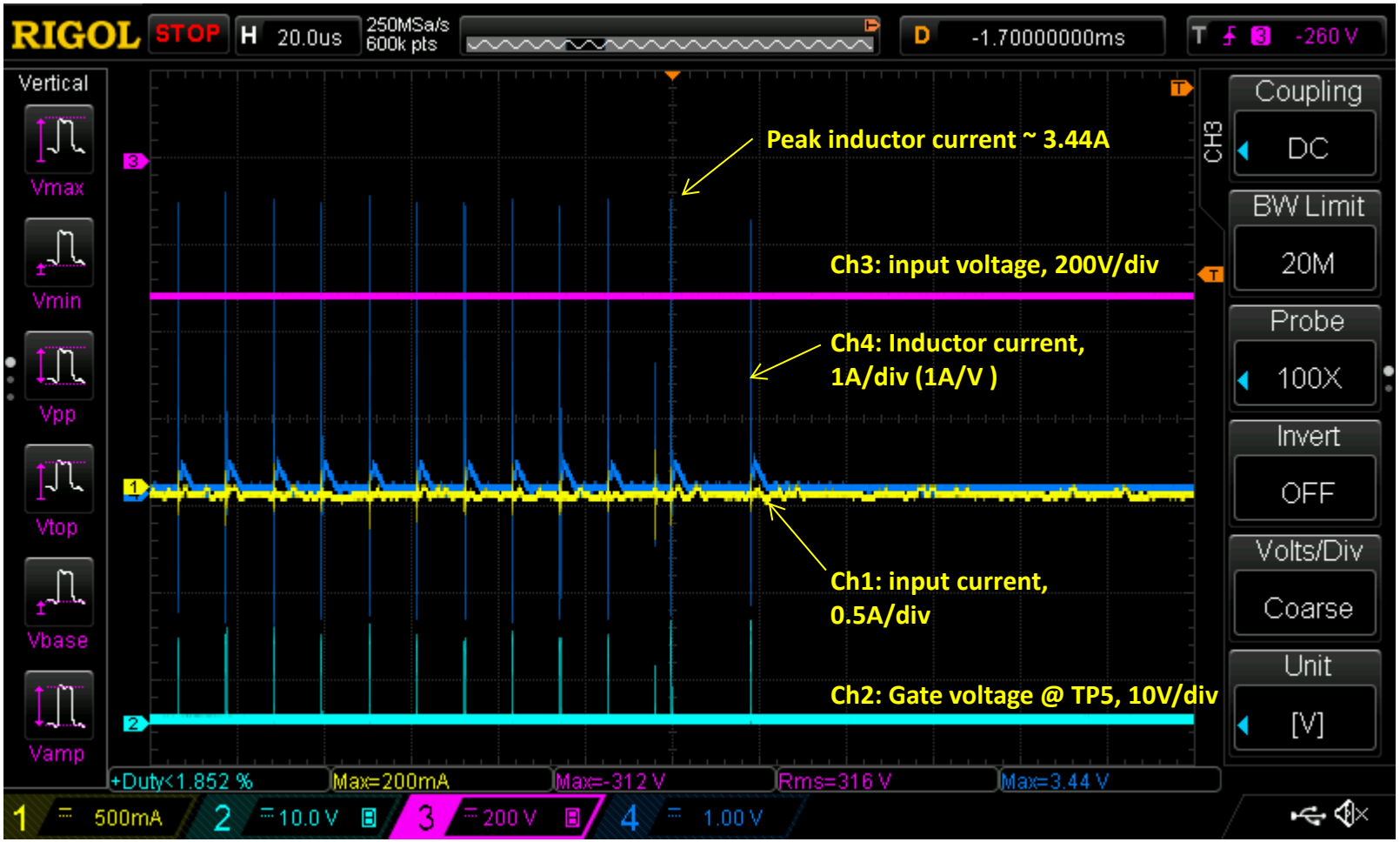
At 230Vac input, 25W external load, the view of locations A (negative peak) and location B (positive peak)



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

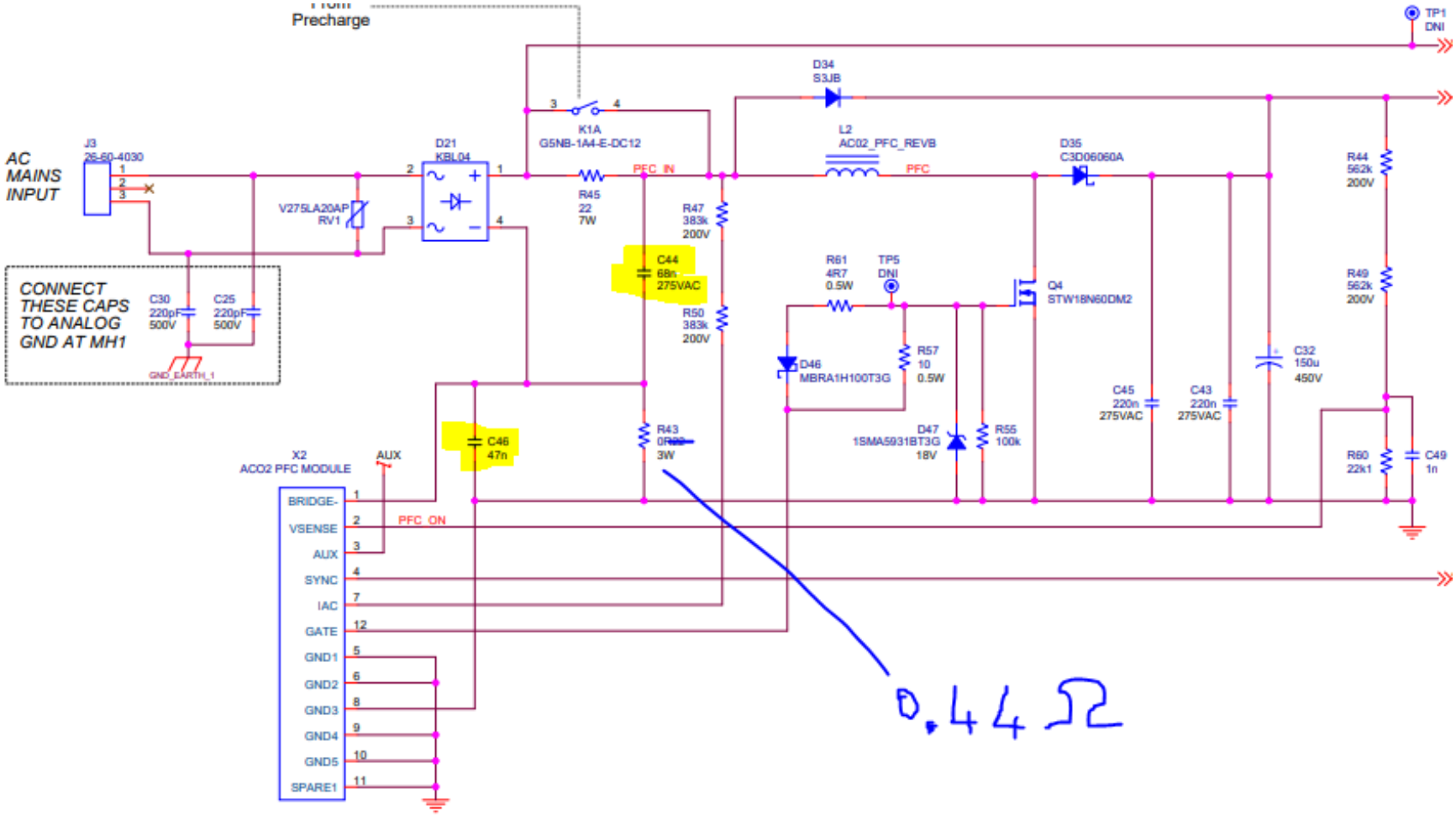
Location A: Current probe on Ch1 has low BW and is used to measure input current only.



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

There is a 68nF cap after the rectifier. It is increased to 2x68=136nF, did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

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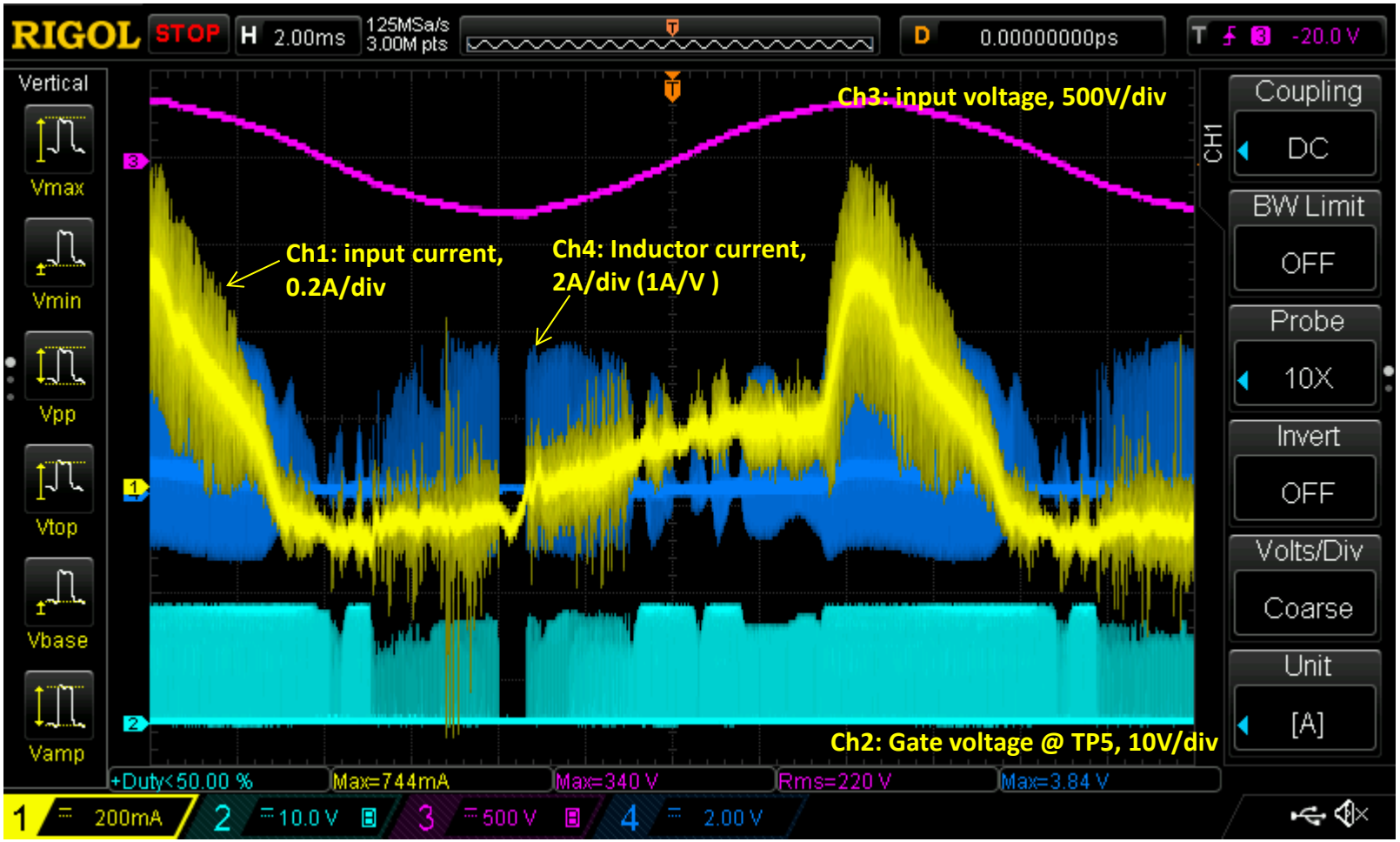
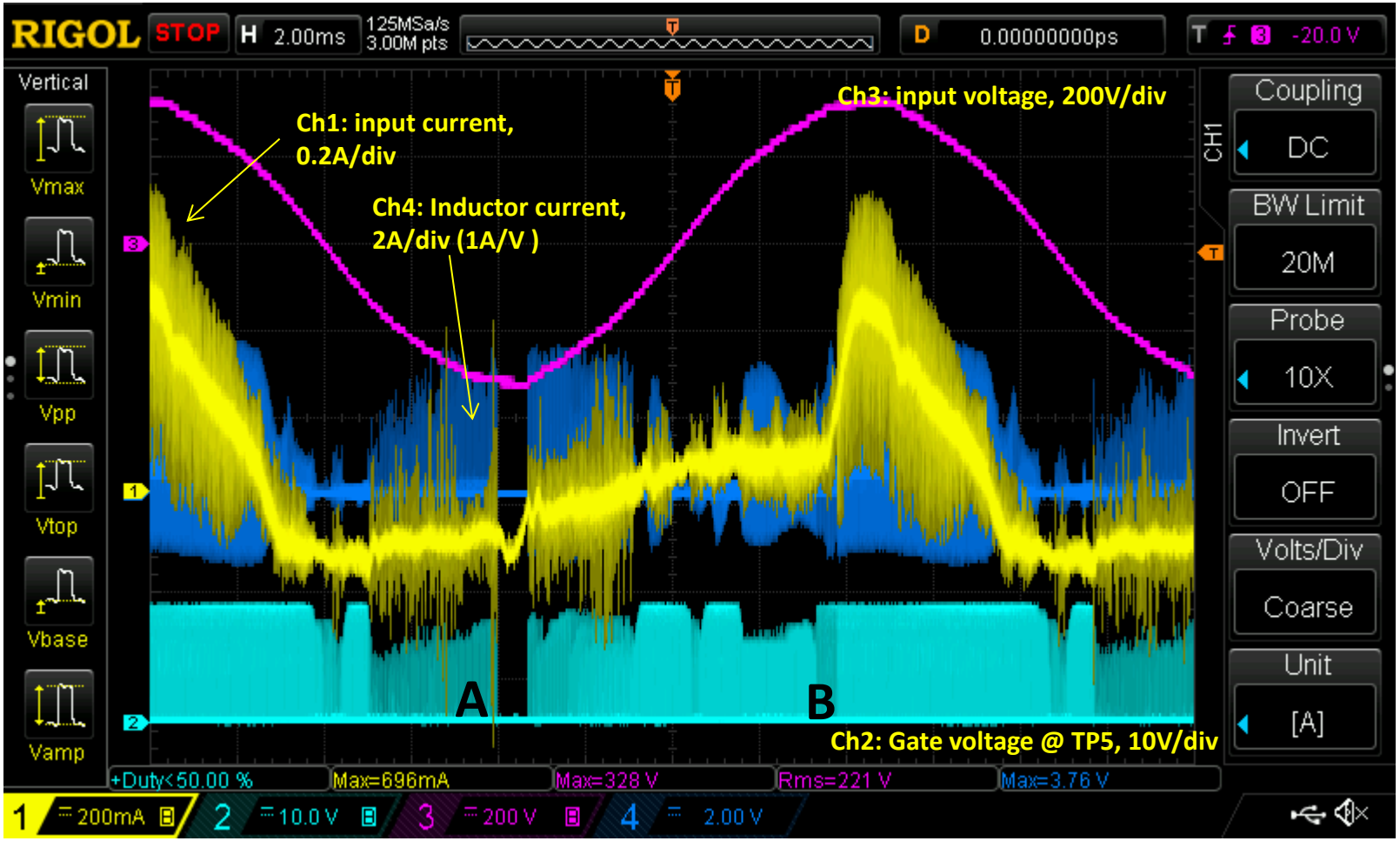


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
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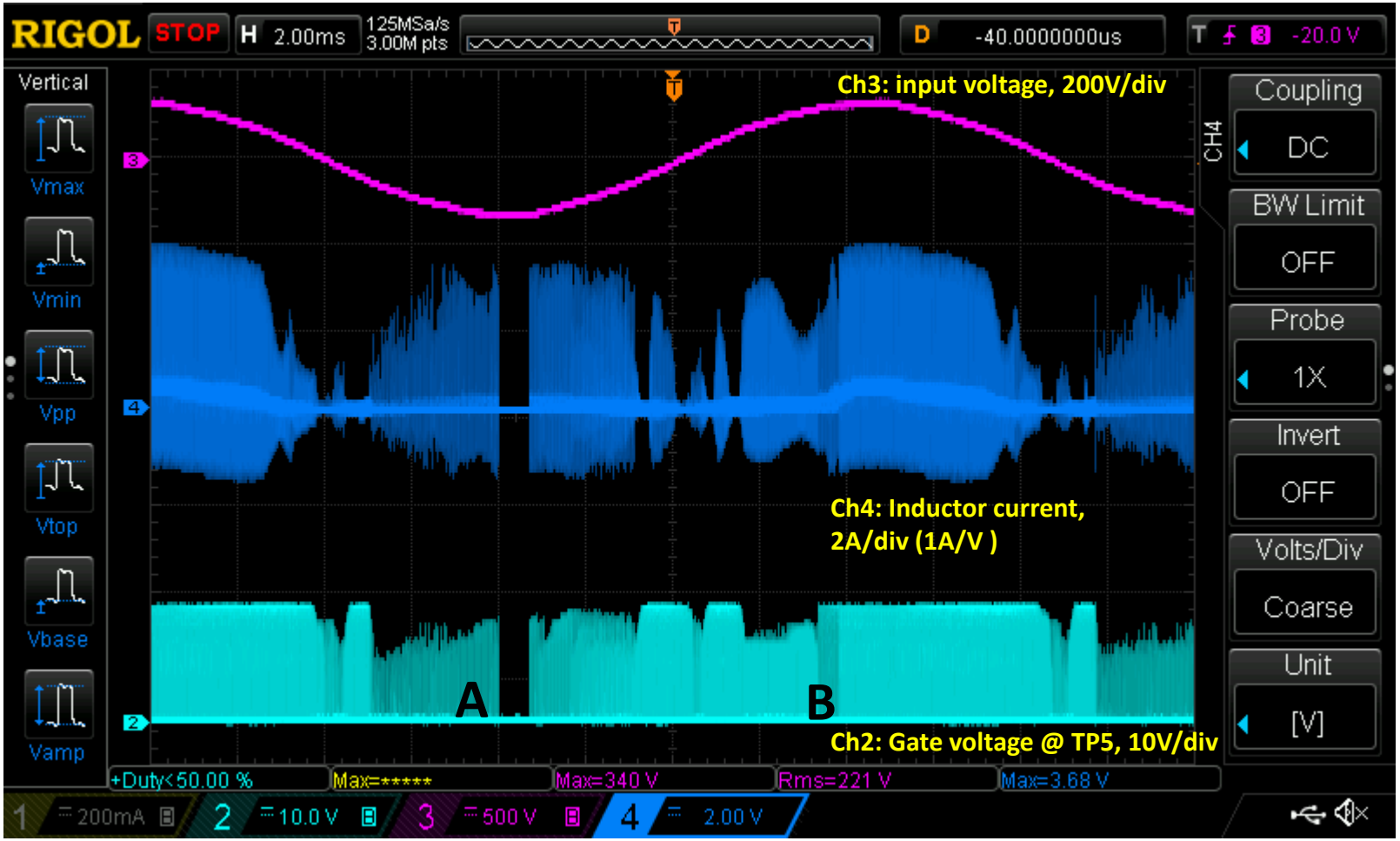

Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
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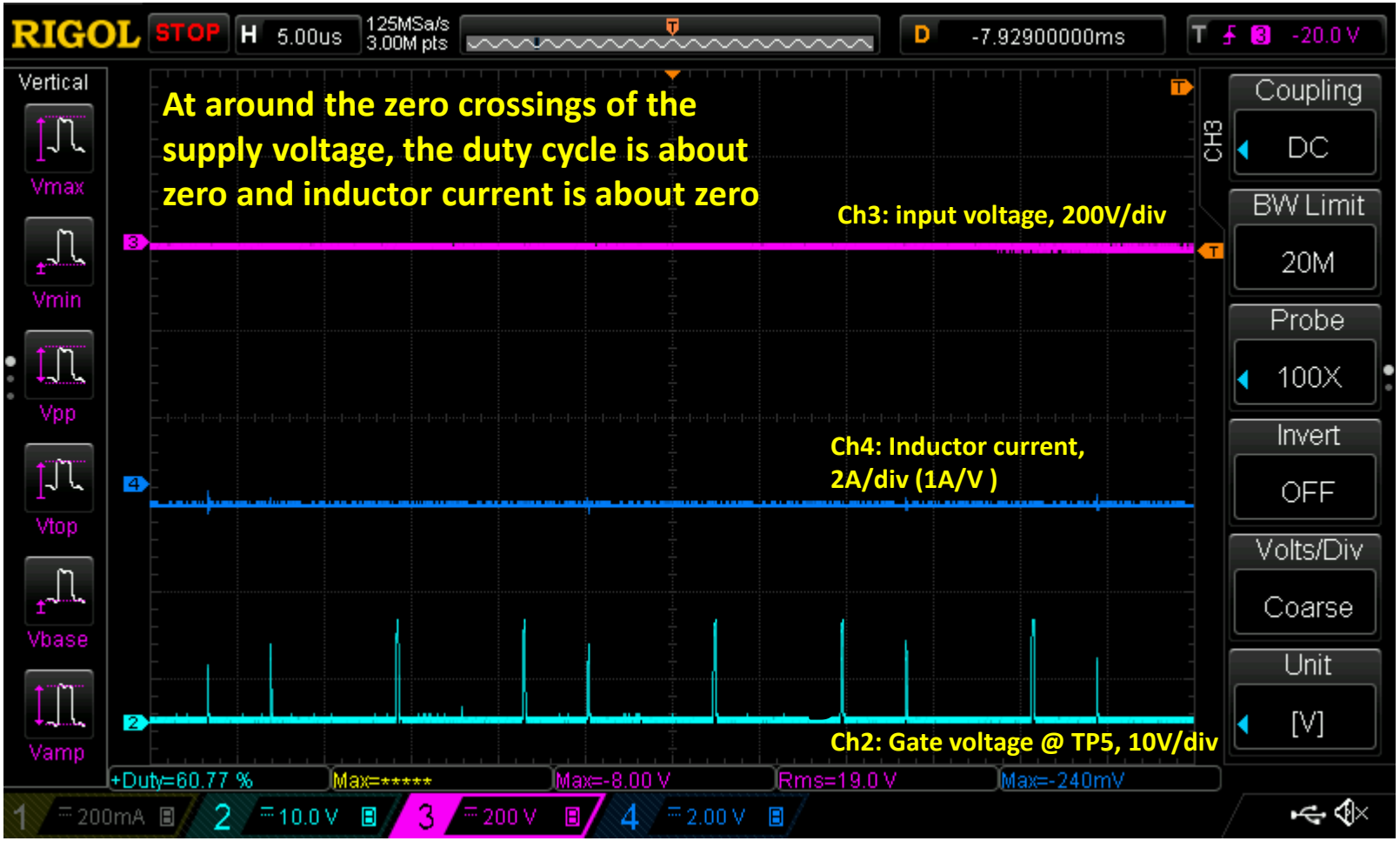

Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
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At ~230Vac input voltage and ~25W external load, distortions observed.

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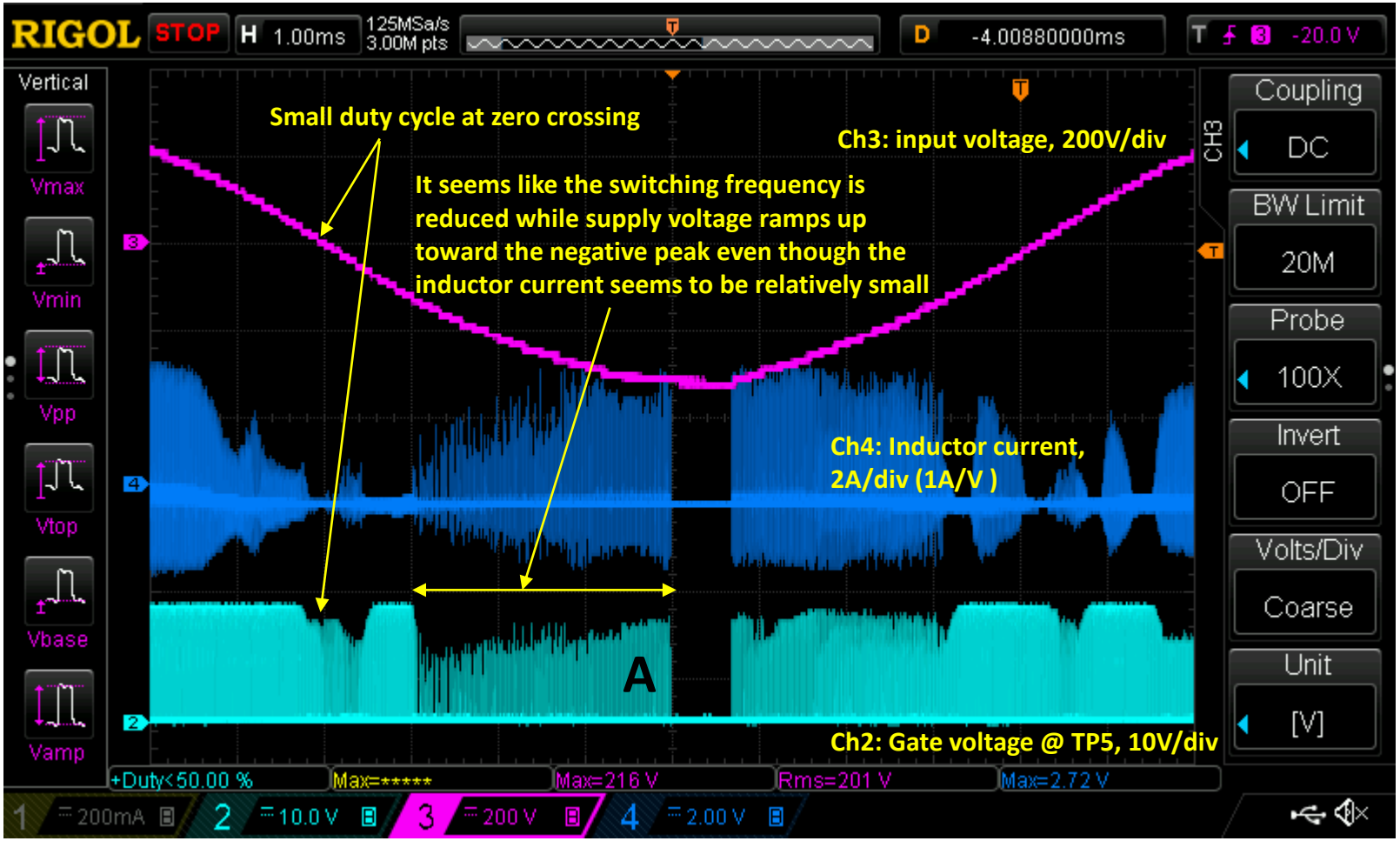
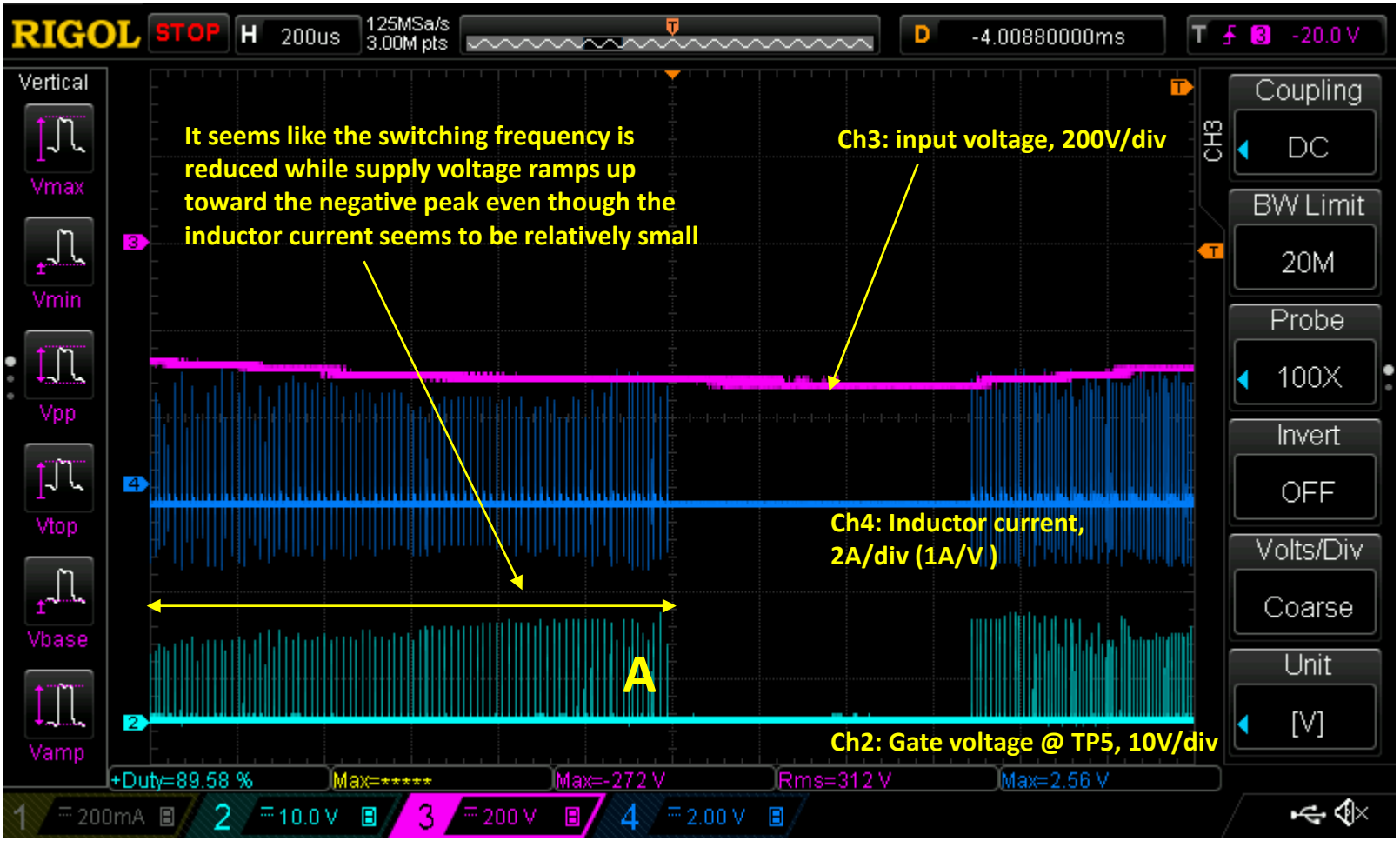


Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
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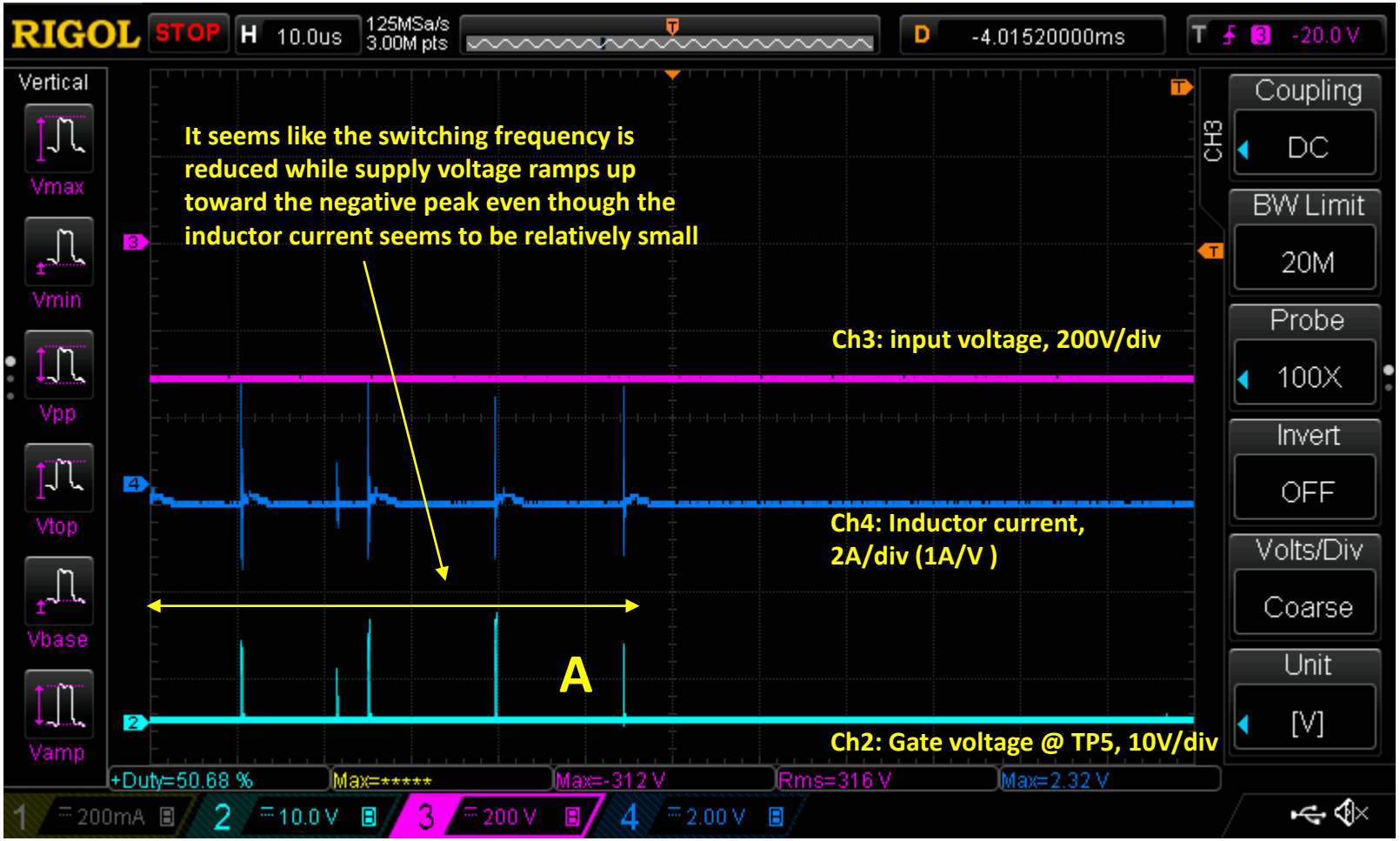
At ~230Vac input voltage and ~25W external load, distortions observed.

Added 100pF across the R5 (R7 on data sheet), did not observe any improvements



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
At ~230Vac input voltage and ~25W external load, distortions observed.

Observations:

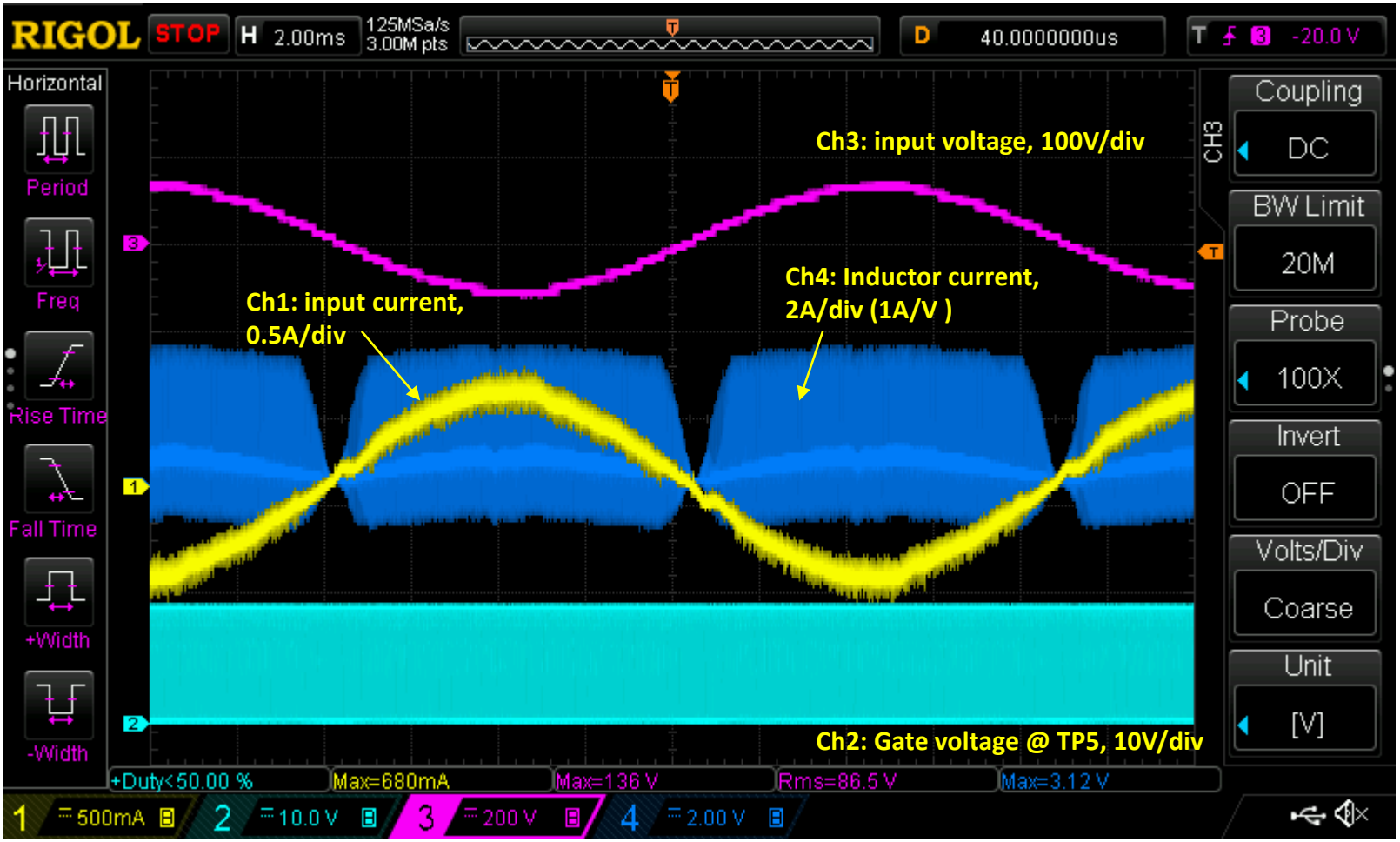
1) Location A: While the supply voltage ramps up toward the negative peak, the switching frequency is reduced significantly and then MOSFET shuts down for a while at the negative peak. It seems like the inductor current is relatively small and this may not be current limit initiated turn off.
2) Location B: While the supply voltage ramps up toward the positive peak, the switching frequency is reduced by about 50%. It is observed this corresponds to “flat top” on supply current. At around the peak of supply voltage, the switching frequency suddenly snaps back to normal frequency and this corresponds to surge in peak of the supply voltage. It is not clear if this phenomenon is caused by activation of current limit.
3) Adding an other 68nF cap after rectifier did not improve the issue
4) Adding 100nF cap across R5 (R7 on data sheet) did not improve the issue

Measuring inductor current vs gate voltages, 12/25

PCB	RefDes on datasheet	RefDes in design	12/11/2022 Fci=44kHz, Gci=5.6	12/25/2022 Fci=11kHz, Gci=1.6
PSB-04	R1	R47, R50	383K	383K
	R2	R43	**0.44**	0.44
	L1	L2	660uH	660uH
PFC-03	R8, R12	R4, R9	**2.74K**	2.74K
	R13	R10	**15.8K**	**4.7K**
	C6	C6	**233pF (200p//33p)**	**3.3n**
	C7	C8	**33pF**	**150pF**
	R15	R11	30.1K	30.1K
	C8	C9	4.7uF	4.7uF
	C10	C1	1.5uF	1.5uF
	C11	C2	150nF	150nF
	R21	R1	48.7K	48.7K
	R14	R13	10K	10K
	R7	R5	**1.50K (3.3K//2.74K) +100pF**	1.50K (3.3K//2.74K) **+ 100pF**
	C9	C4	1uF	1uF

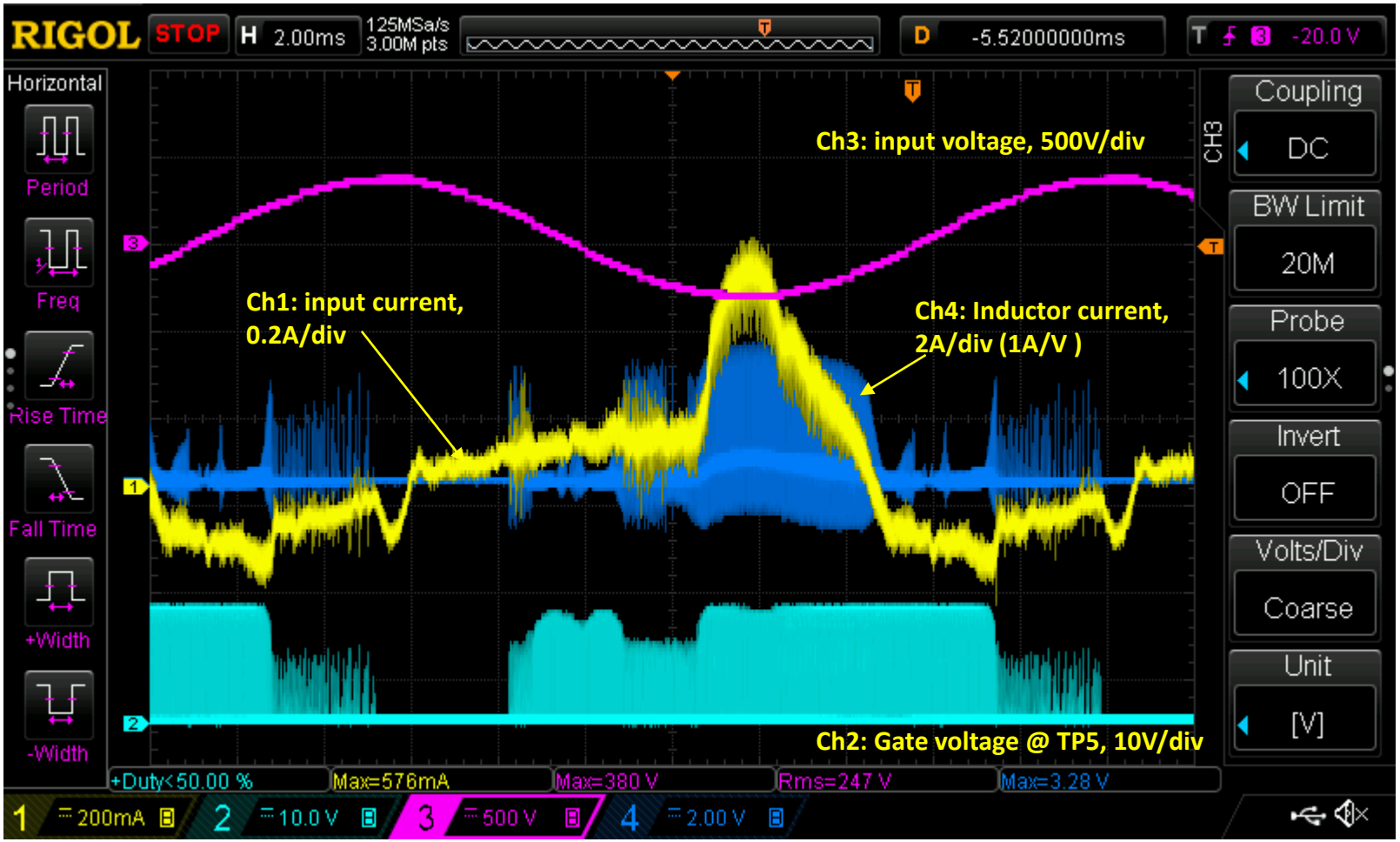
Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55
At ~85Vac input voltage and ~25W external load, no major distortions observed



Measuring inductor current vs gate voltages, 12/25

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55
At ~230Vac input voltage and ~25W external load, major distortions observed



Measuring inductor current vs gate voltages, 12/28

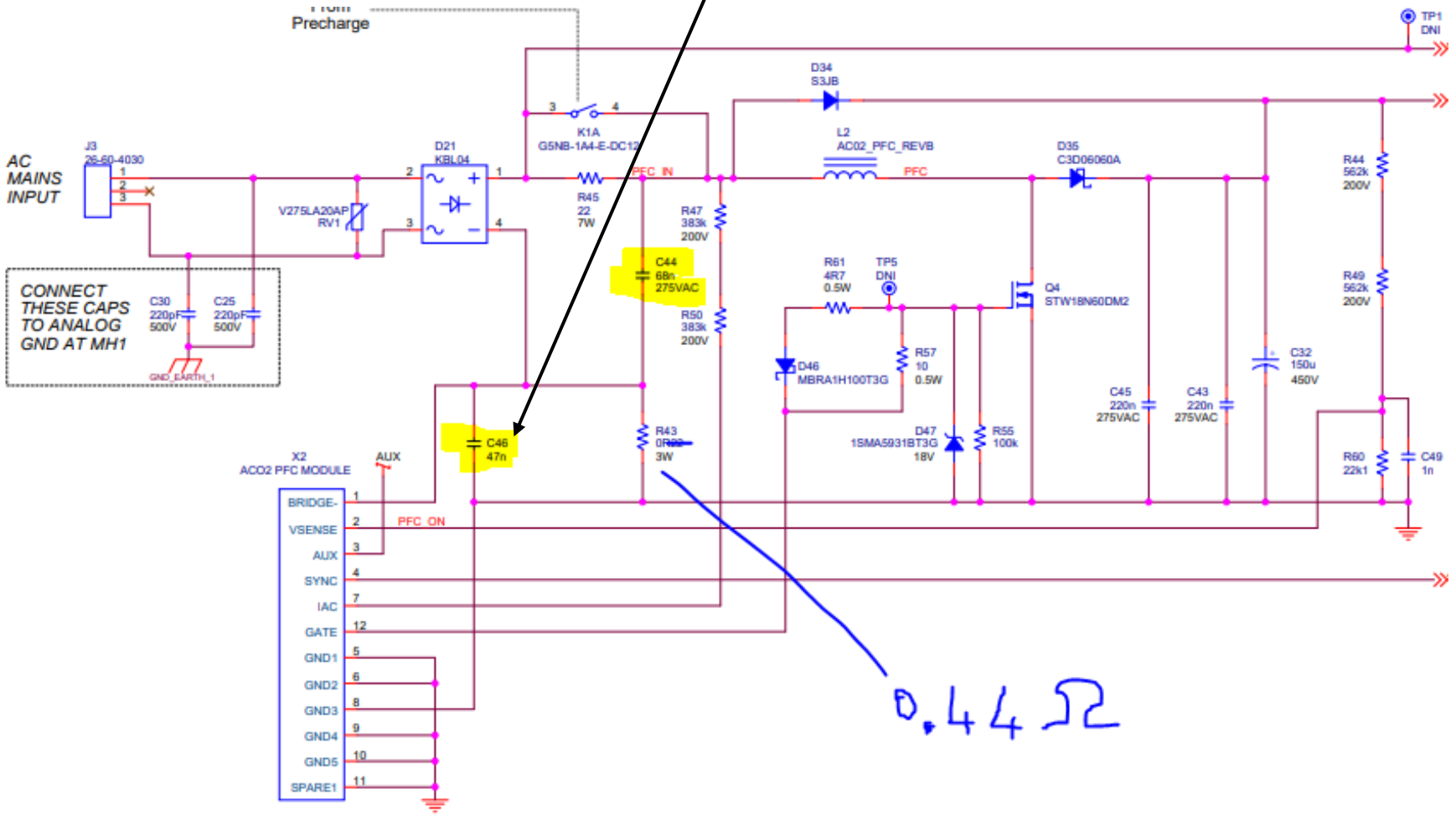
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage and ~25W external load, major distortions observed

Investigating the effect of C46 on input current distortions



Measuring inductor current vs gate voltages, 12/28

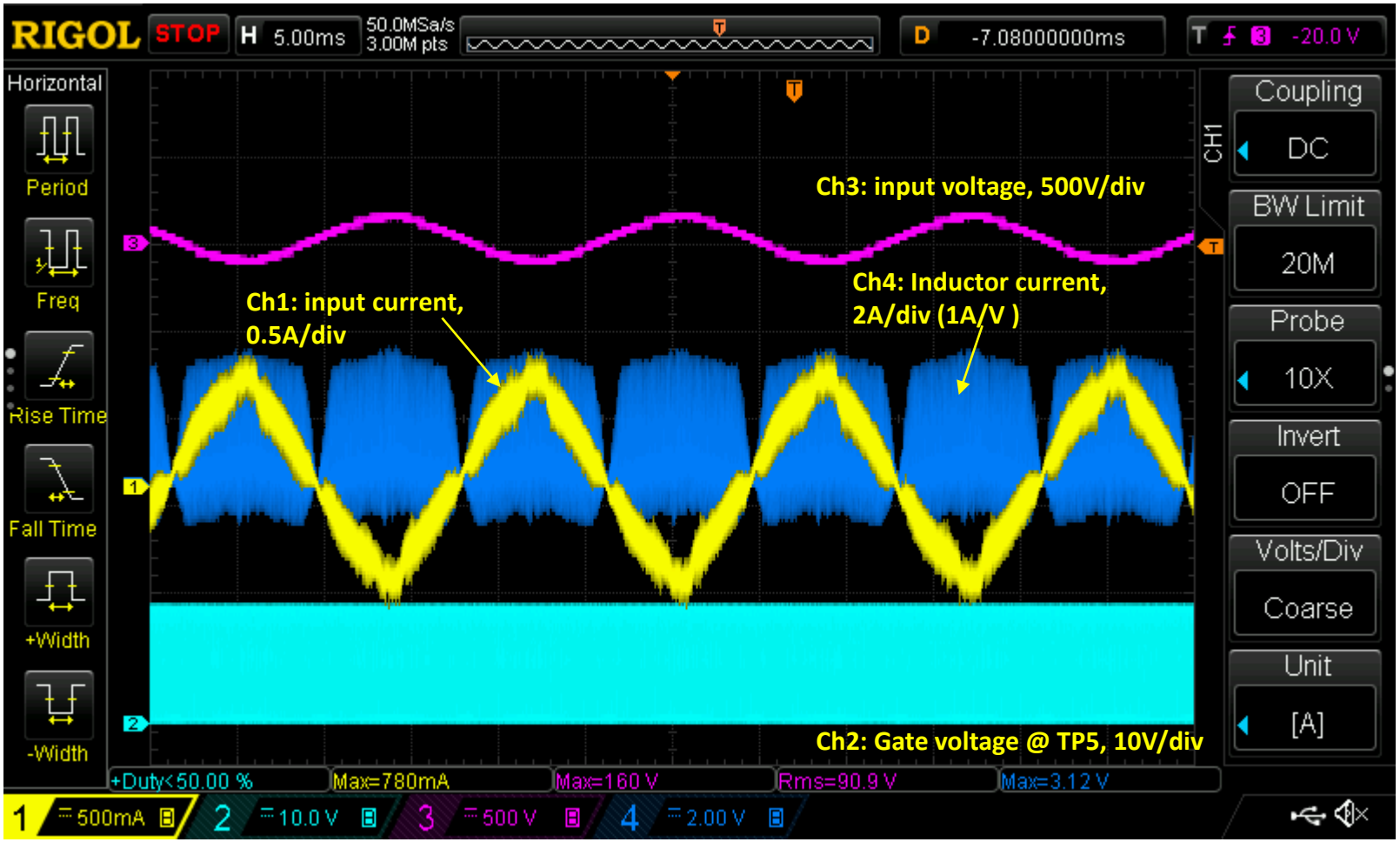
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At 90Vac input voltage, no C46, no major distortions observed

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

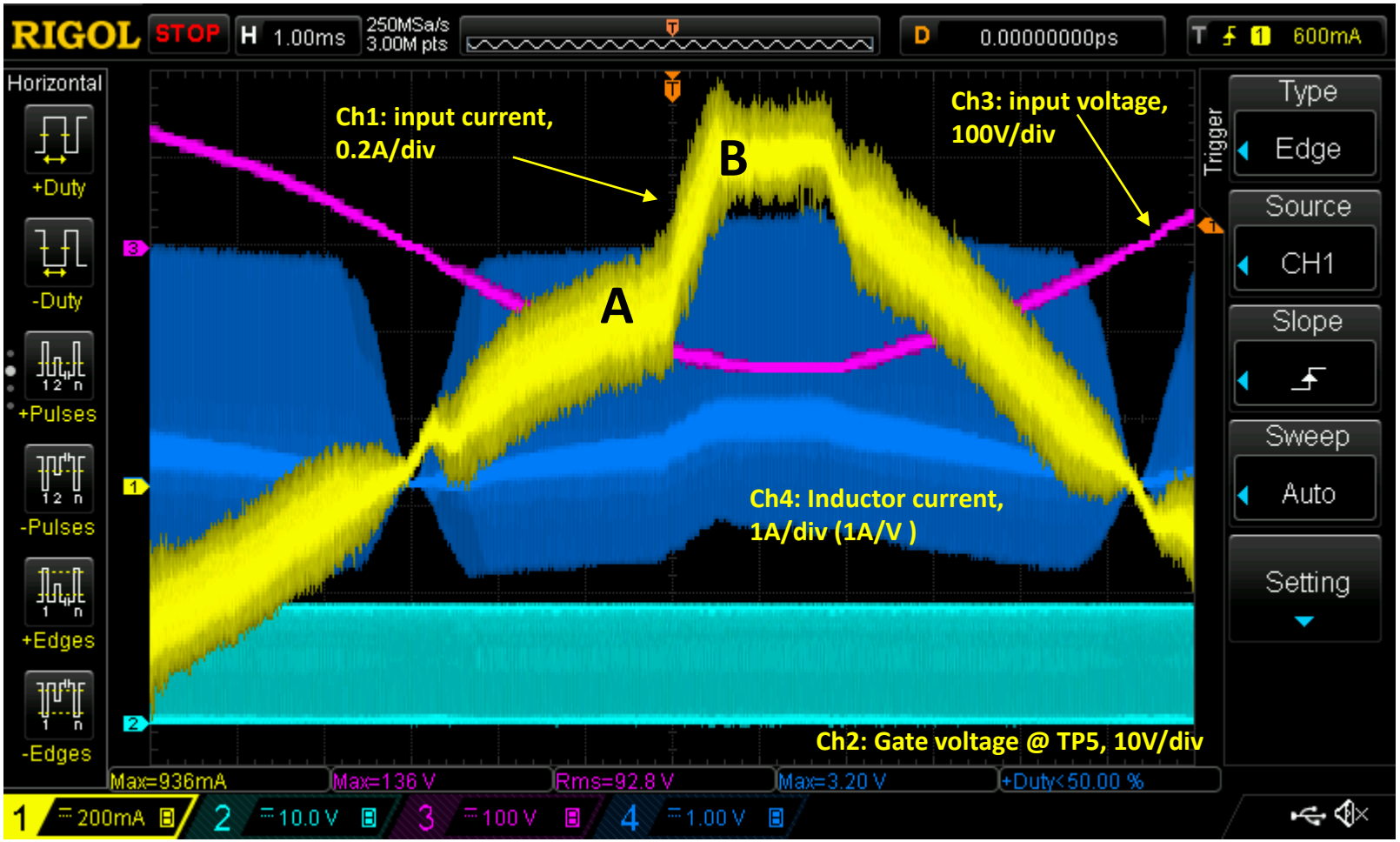
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~100Vac input voltage, no C46, distortions started, notice the current surge from location A to B

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

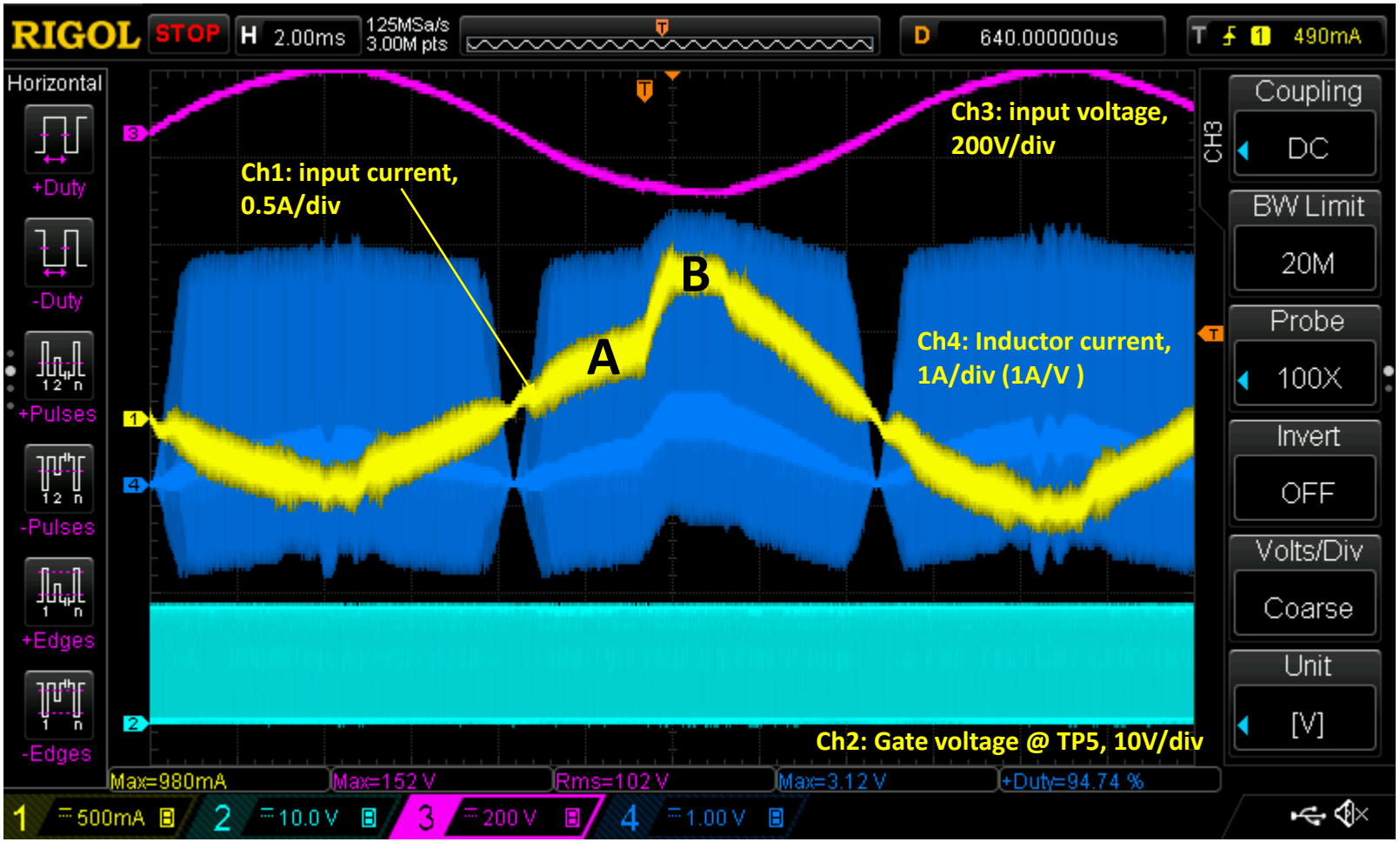
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~100Vac input voltage, no C46, distortions started

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

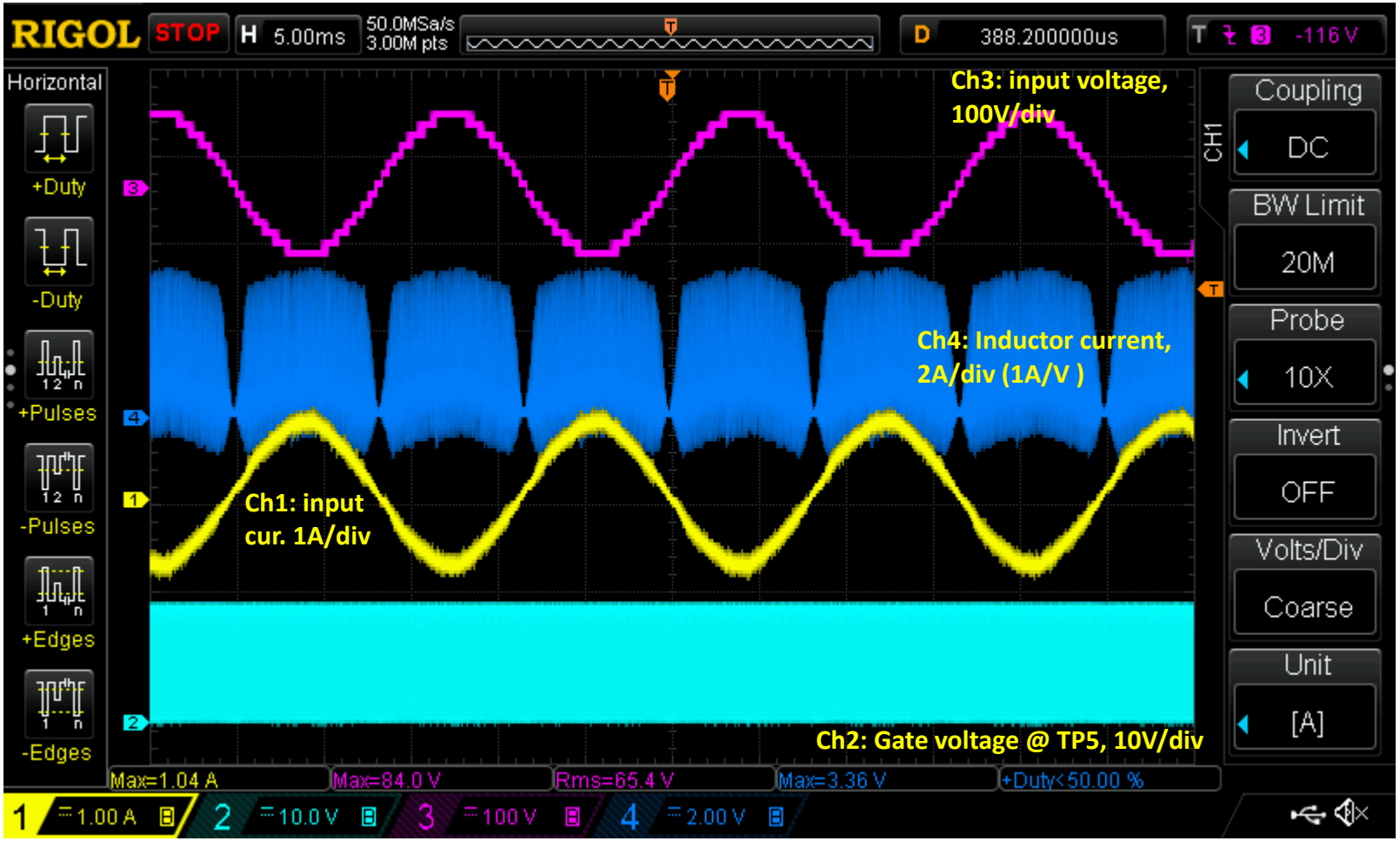
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~85Vac input voltage, <u>C46=100nF</u>, no major distortions

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

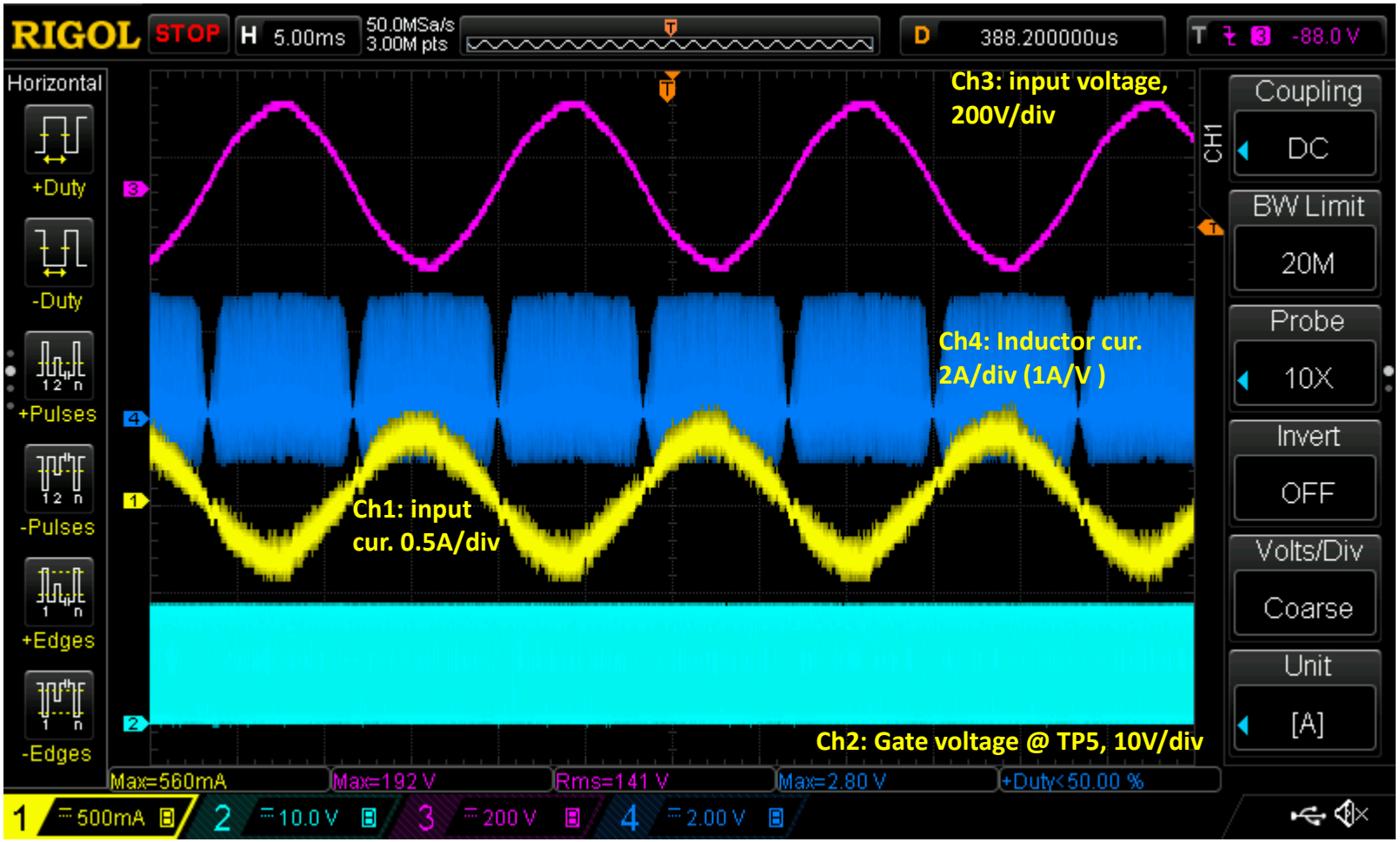
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~140Vac input voltage, C46=100nF, no major distortions

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

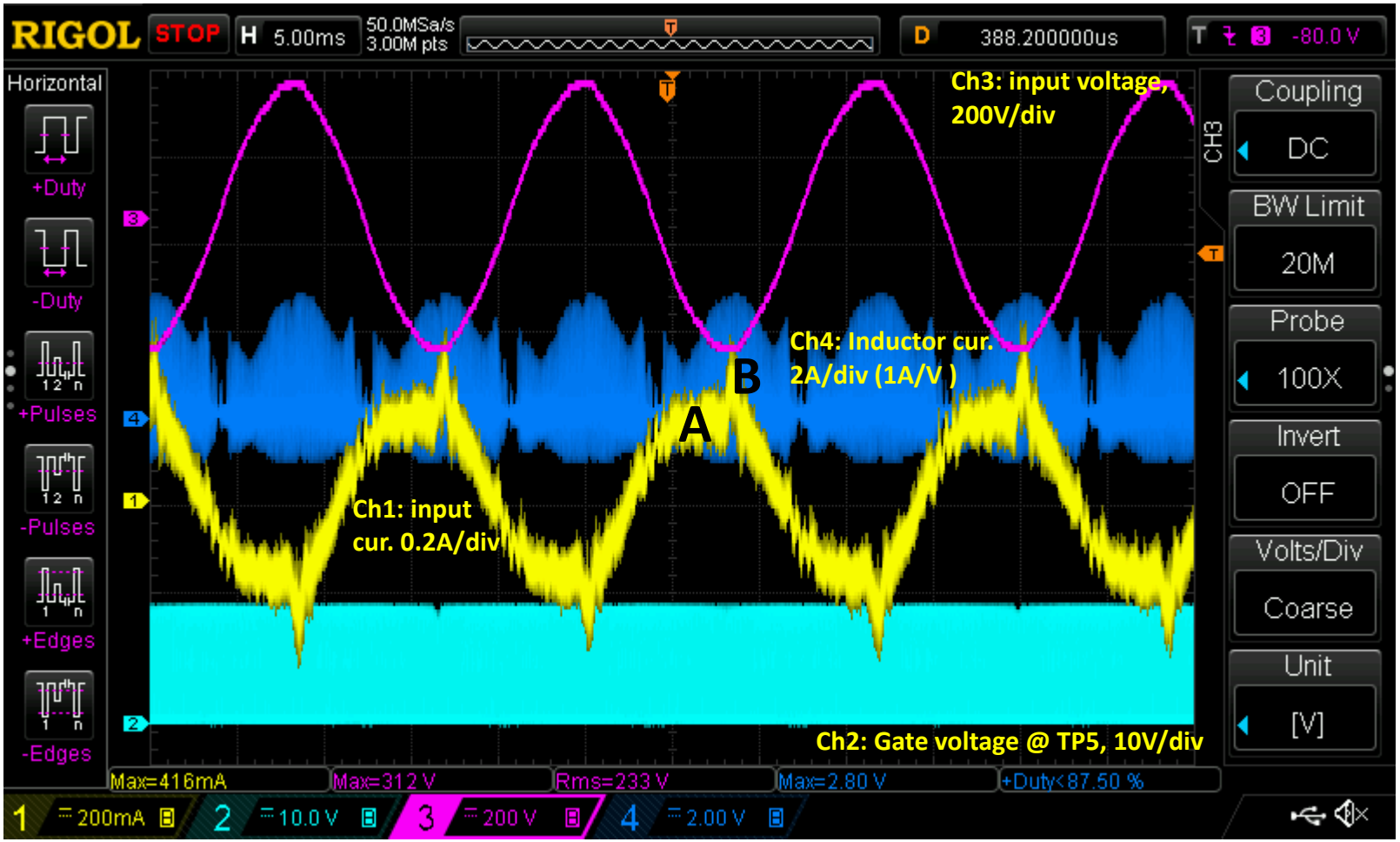
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage, <u>C46=100nF</u>, symmetric distortions show up on peaks of voltage waveform

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

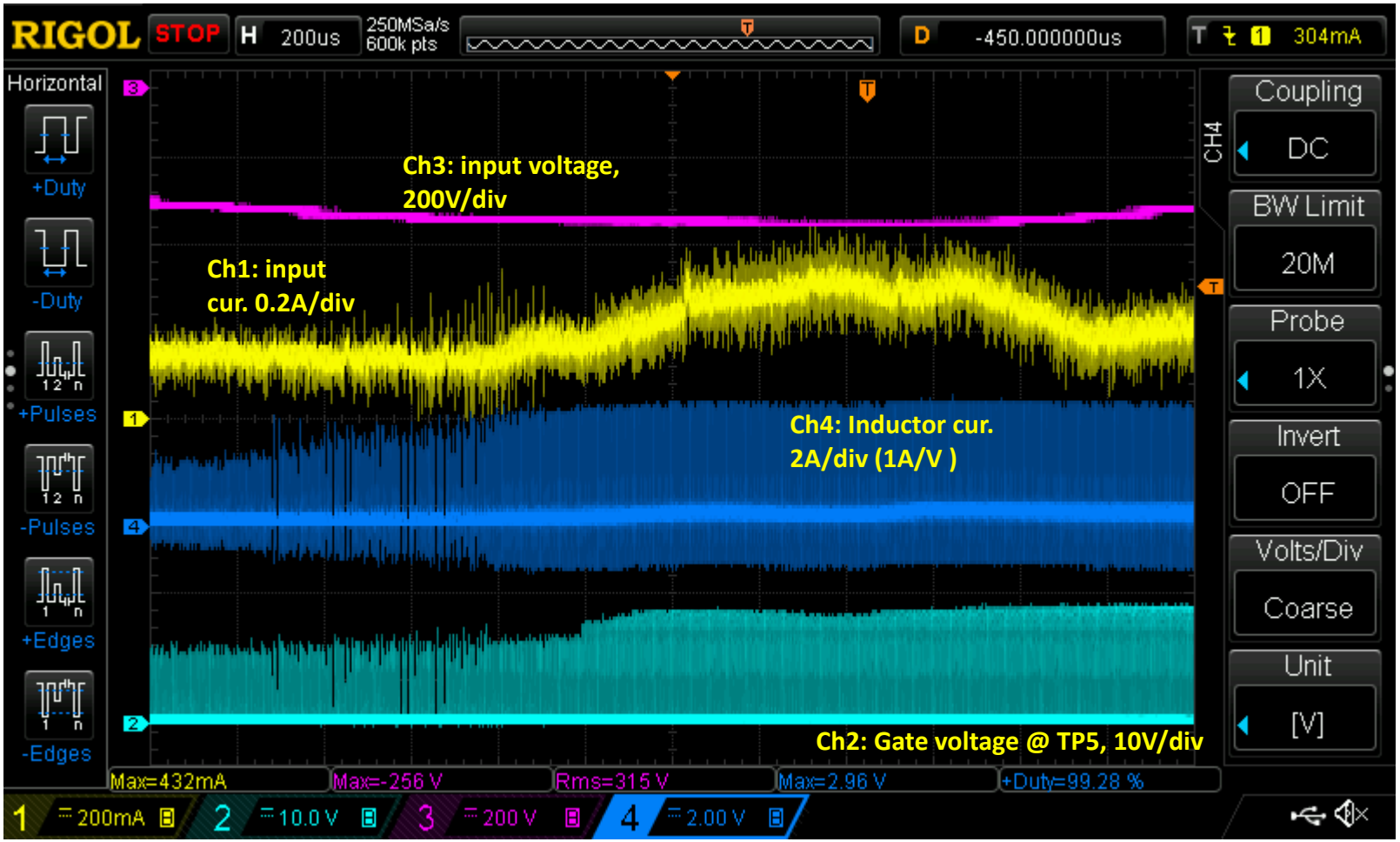
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage, <u>C46=100nF</u>, location A; ON times gets very small & pulses start to drop

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

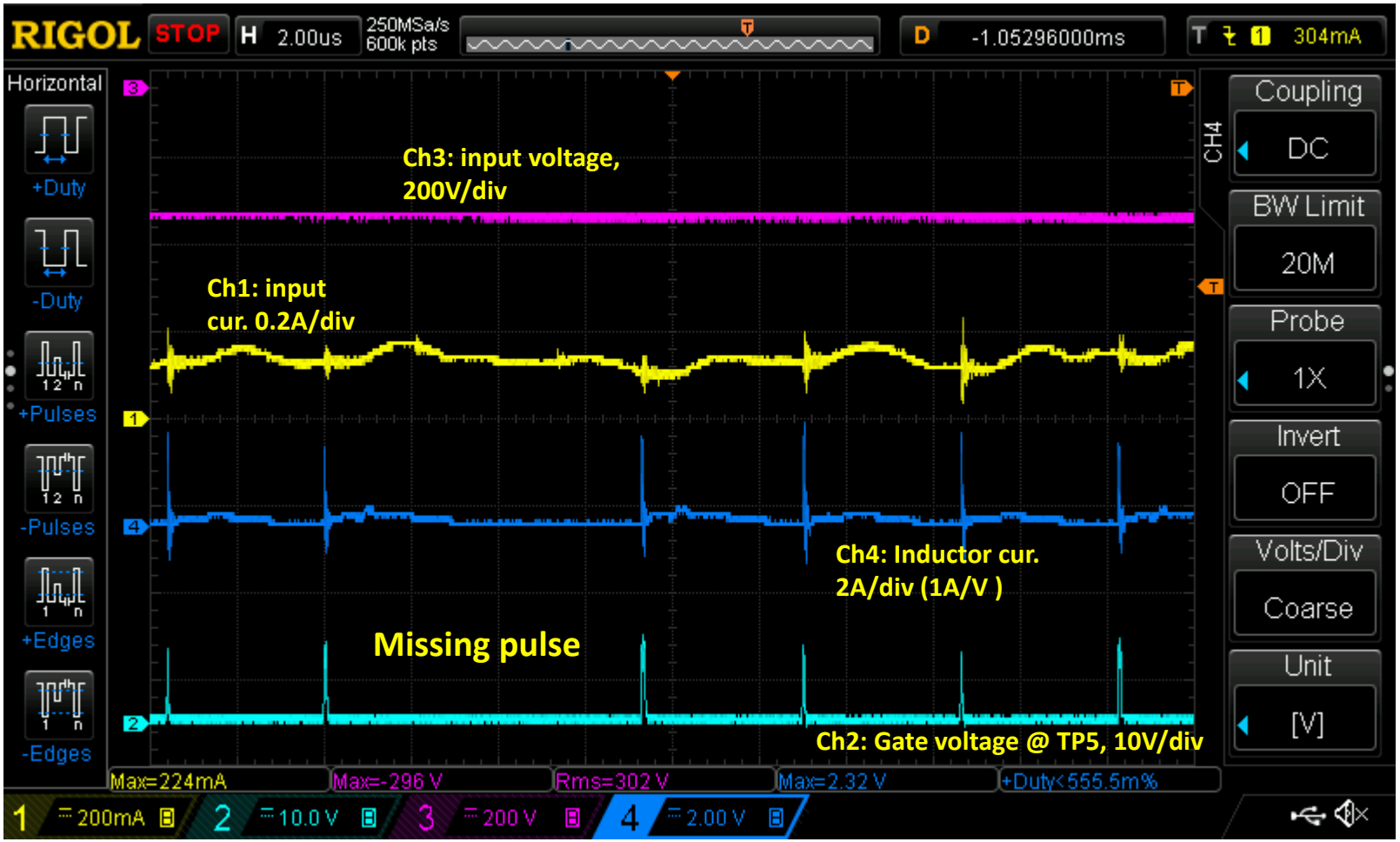
Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55

At ~230Vac input voltage, <u>C46=100nF</u>, location A; ON times gets very small & pulses start to drop

Ch4: Tek TCPA300, Ch1: Fluke 80i-110S



Measuring inductor current vs gate voltages, 12/28

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55

Conclusions on 12/28:

1) Removing the 47nF cap across the sense resistor made the issue worse that the current became more unstable and distortions started even at low voltages of ~100Vac

2) Replacing the capacitor across the sense resistor (C46) with 100nF, did not improve the problem that the current waveform was stable up to ~ 230Vac and distortions started above this voltage, as it was the case with C46=47nF

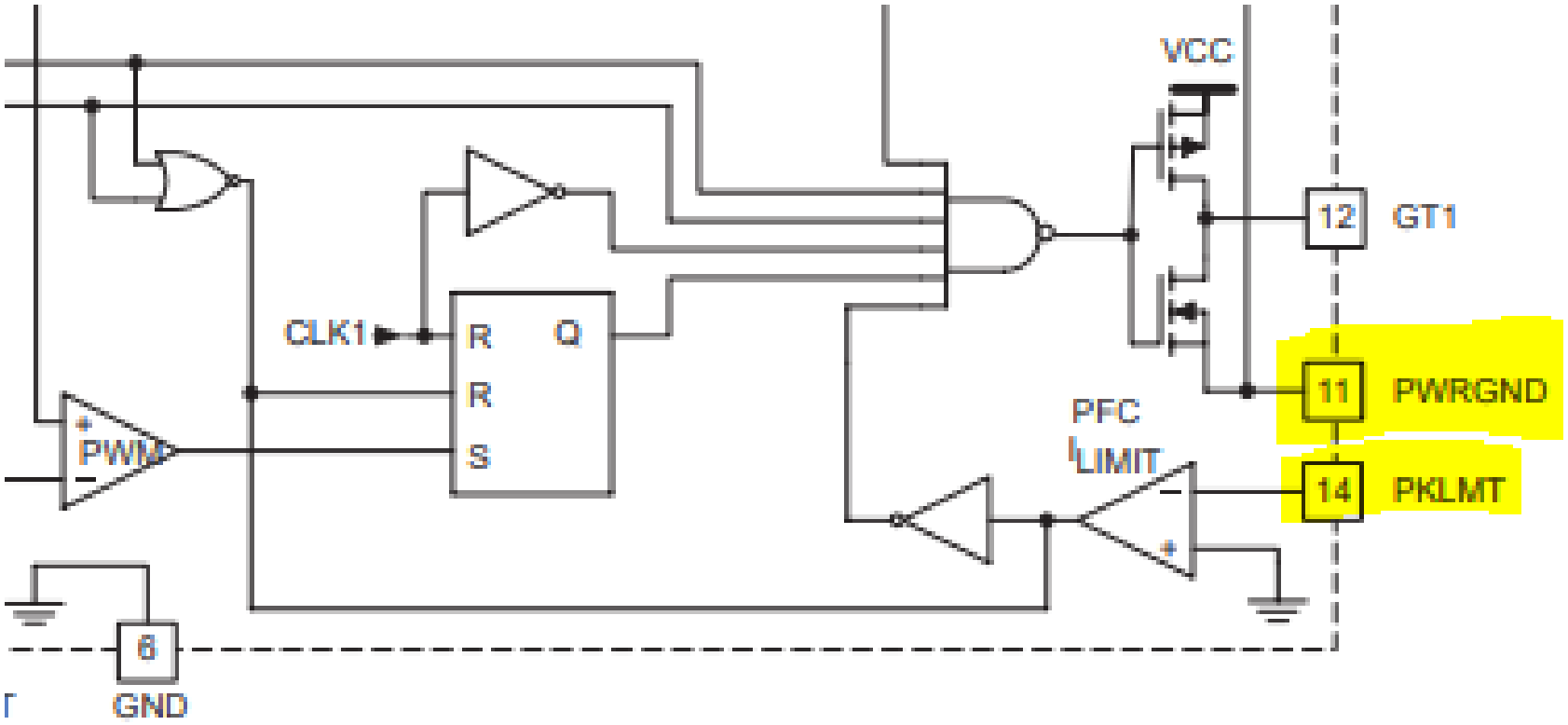
3) Referring to location A; it appears that the duty cycle gets very small and even some pulses were dropped even though the current through the inductor does not appear to be the max. This suggests that the event is not initiated by peak current limit

4) Referring to location B; at this point no pulse dropping is observed. On the contrary, the duty-cycle increases which results in surge in inductor current.

Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

100pF leaded ceramic capacitor was connected from pin14 (PKLMT) to pin11 (PWRGND). No improve observed
After that, a 1nF capacitor was added from pin14 to pin11, and again no improvements were observed



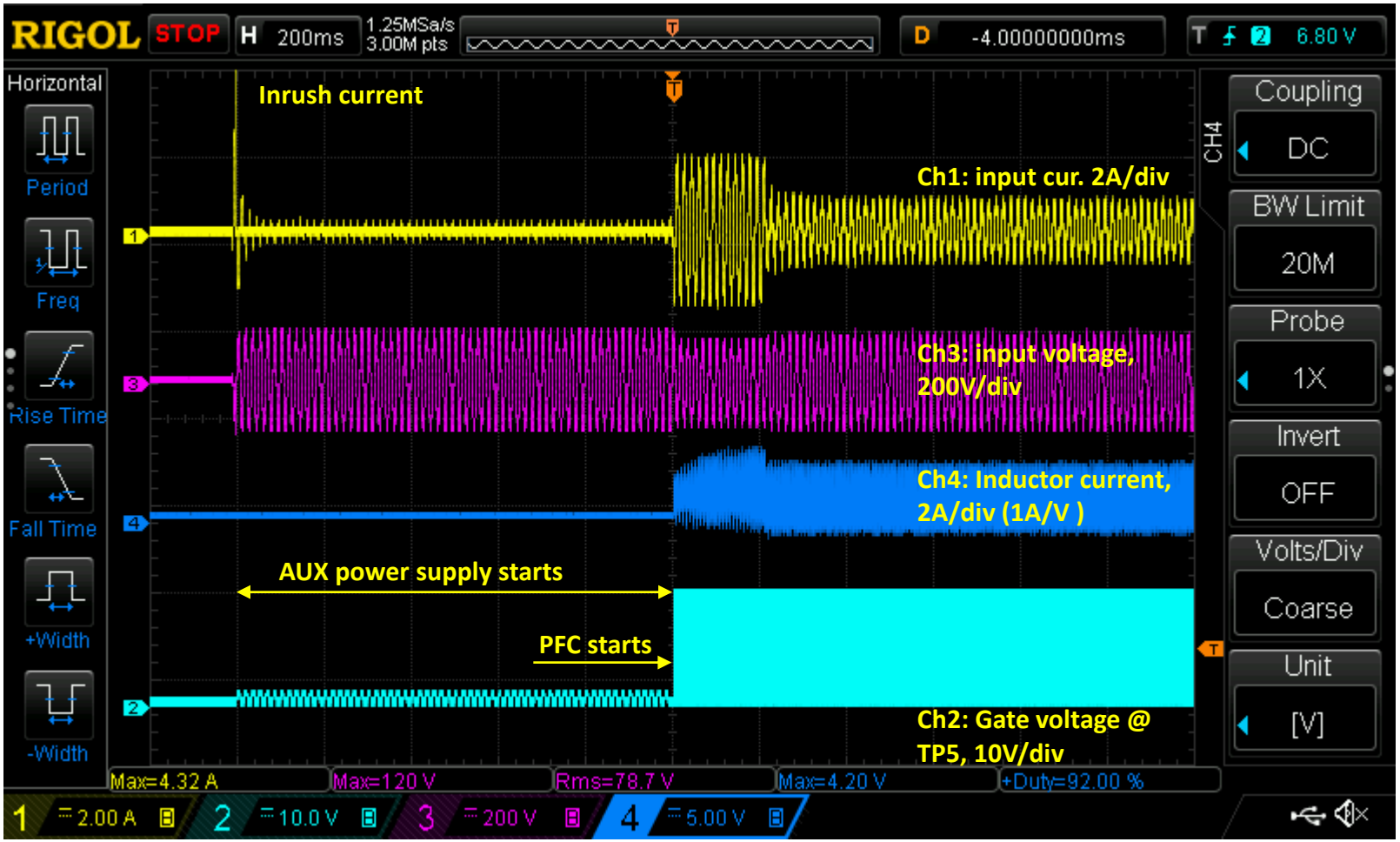
Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Start-up timing of PFC stage



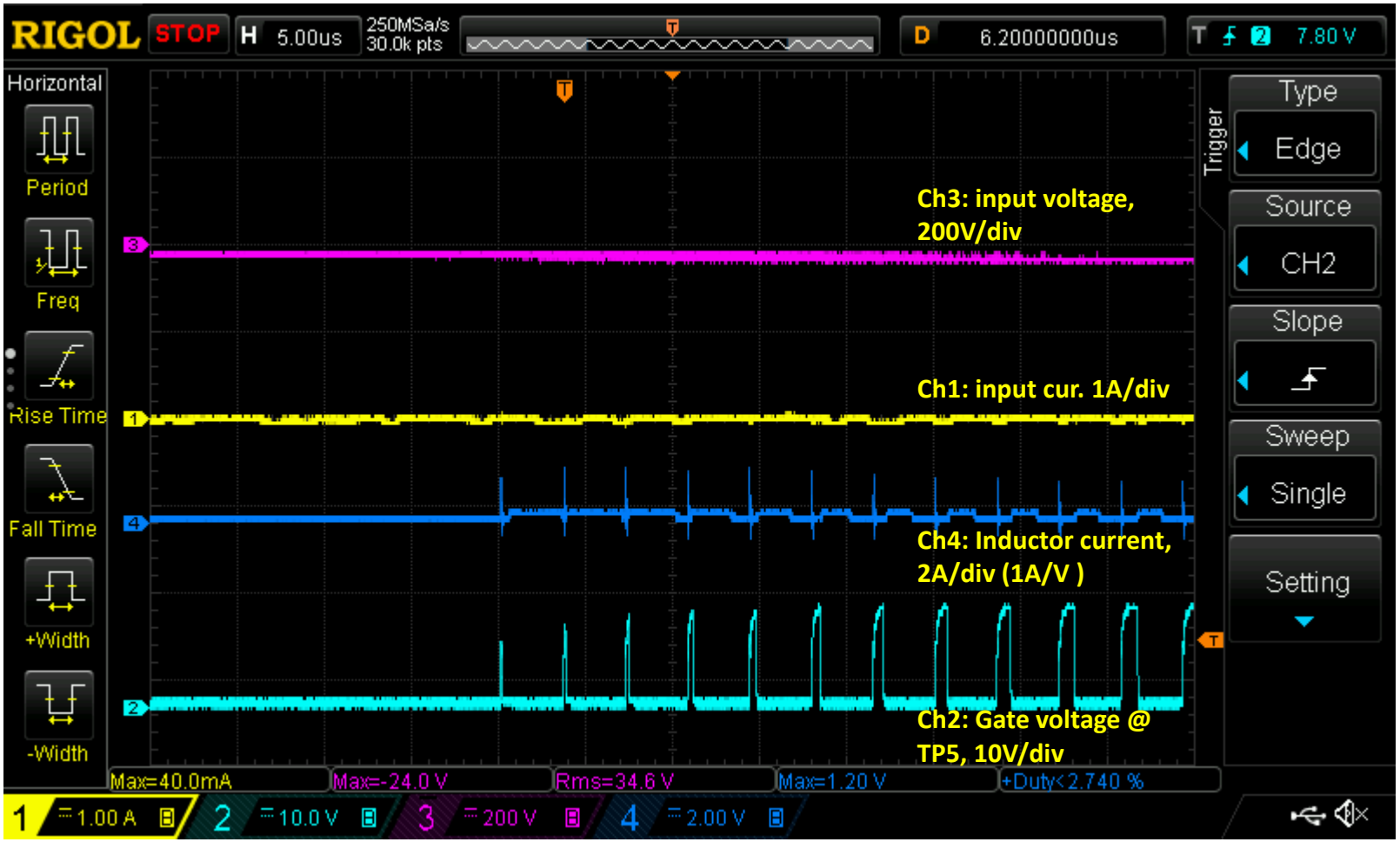
Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

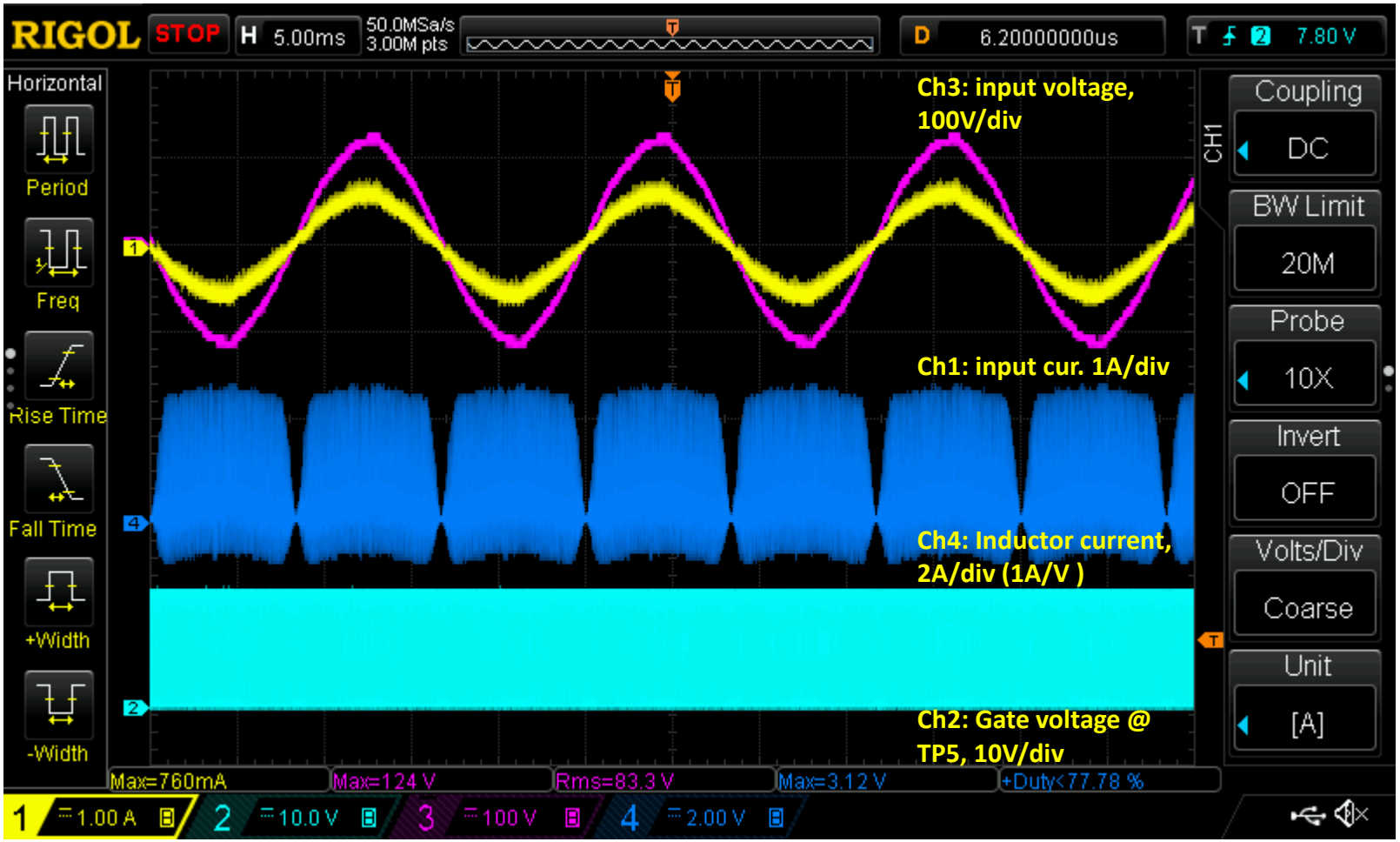
At the time when PFC stage starts operating, it seems like the ON time pulse-width starts from zero and increases slowly



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

With 1nF from PKLMT (pin14) to GND (pin11), no major distortions at 85Vac



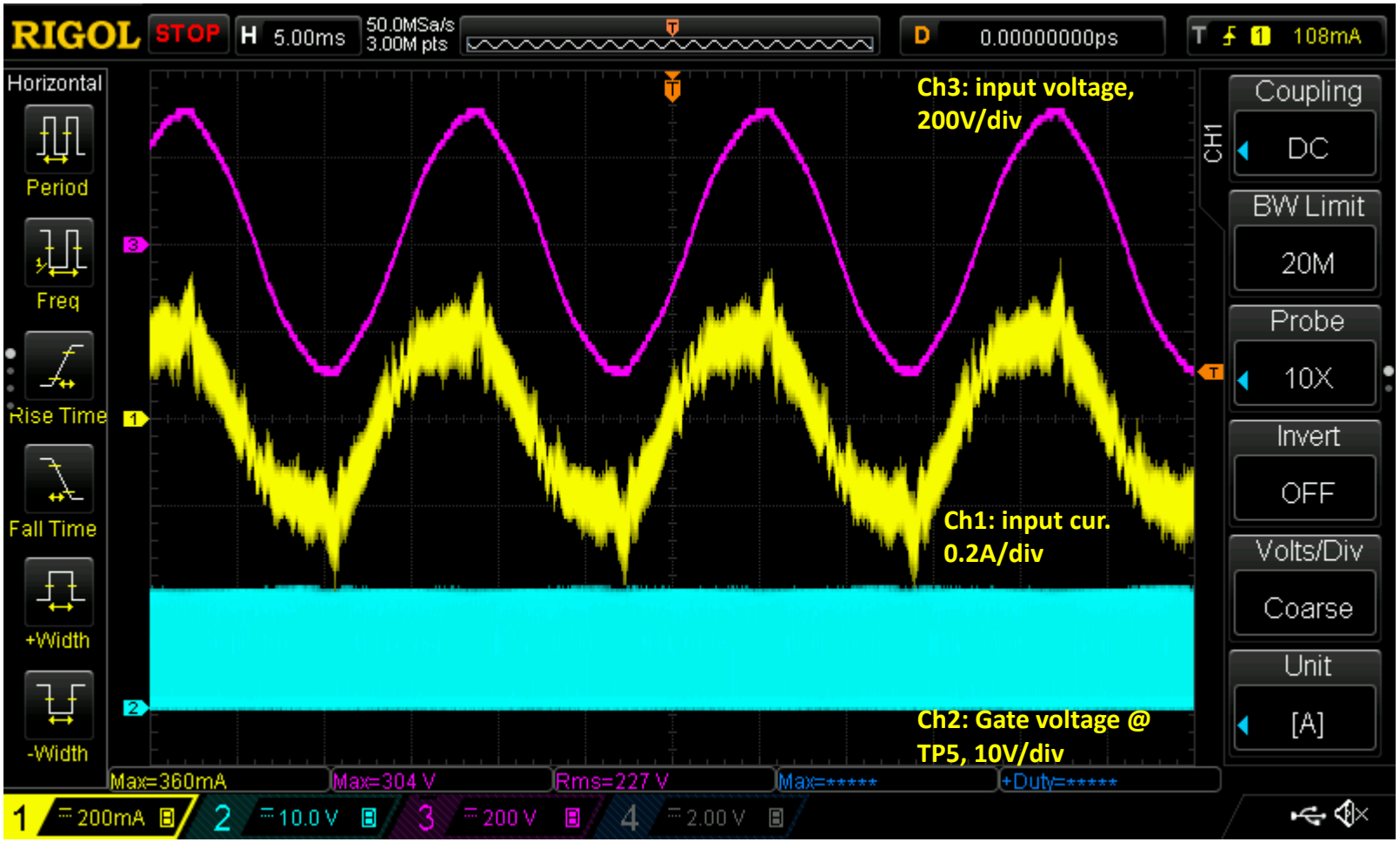
Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

With 1nF from PKLMT (pin14) to GND (pin11), distortions start at around 220Vac (also tried 100pF from pin14 to pin11, no improvements were observed)

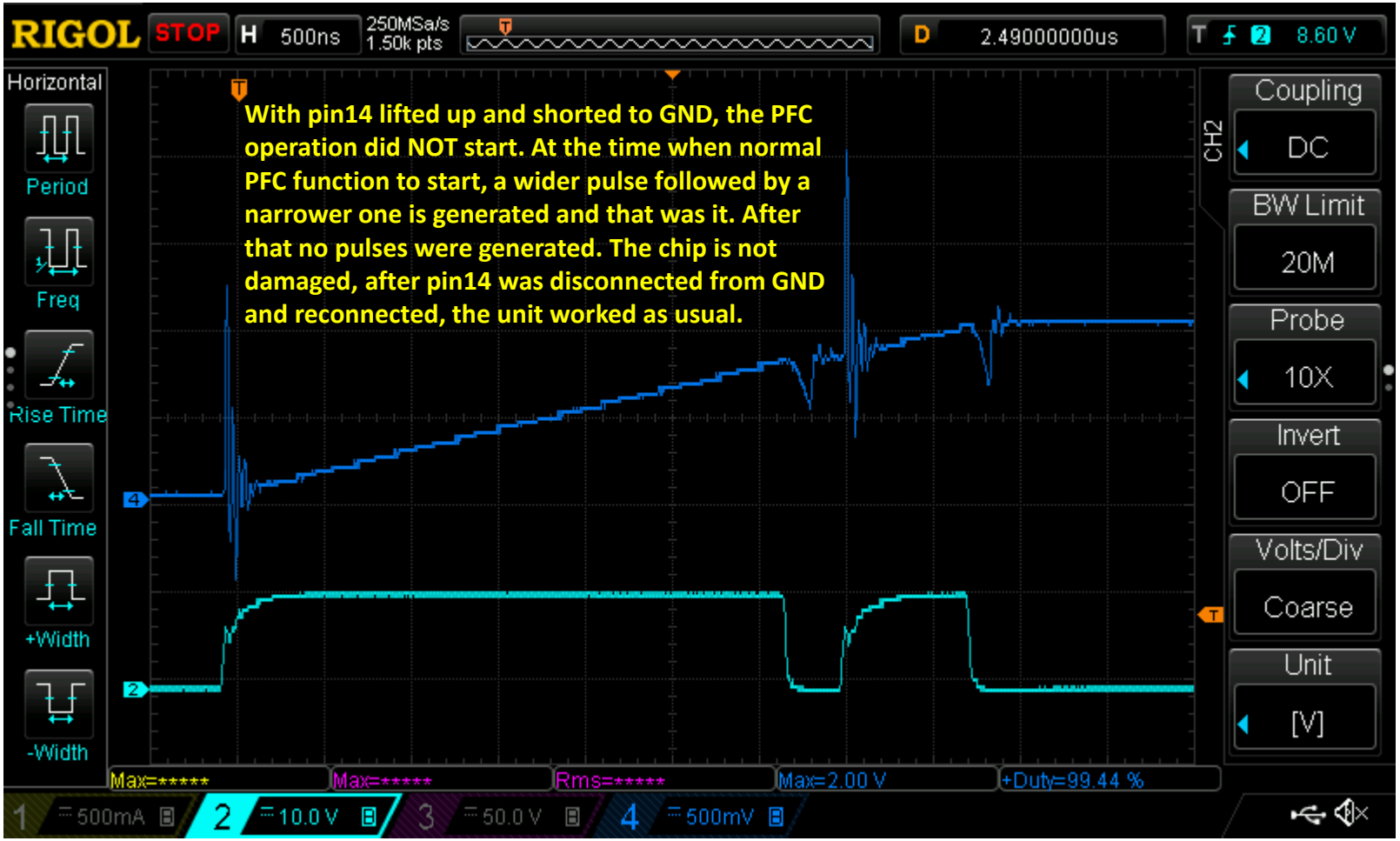


Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5



Measuring inductor current vs gate voltages, 1/8/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Conclusions on 1/8:

1) Connecting 100pF and then 1nF capacitor from pin14 (PKLMT) and pin11 (GND), right on the control chip, did not result in any improvements and that input current started to get distorted at around 230Vac
2) When PFC chip starts to operate, after AUX power supply is established, it seems like the ON time of the MOSFET starts from zero and is increased slowly. This makes sense, as doing so would reduce the chance of triggering PKLMT while DC-link cap is charged.
3) When pin14 is lifted up and shorted to pin11, at the time when it normally starts, the PFC chip generated a wider single pulse followed by a narrower one. The PFC chip did not go through the normal ramp up sequence. It is not clear why shorting the PKLMT to GND disables the ramp up function. And, since PKLMT is shorted to GND, it is presumed that the interruption of PFC function is not due to activation of PKLMT function.

SS2 (pin 13): A capacitor between SS2 and GND programs the softstart duration of the PWM stage gate drive. When the UVLO2 comparator enables the PWM stage, an internal 10.5-µA current source charges the external capacitor at SS2 to 3 V to ramp the voltage at VERR during startup. This allows the GT2 duty cycle to increase from 0% to the maximum clamped by the duty cycle comparator over a controlled time delay t_{SS} given by:

$$C_{SS2} = \frac{t_{SS} \times 10.5 \times 10^{-6} \times Amp}{3\ V}$$

C_{SS2} is in Farads

In the event of a disable command or a UVLO2 dropout, SS2 quickly discharges to ground to disable the PWM stage gate drive.

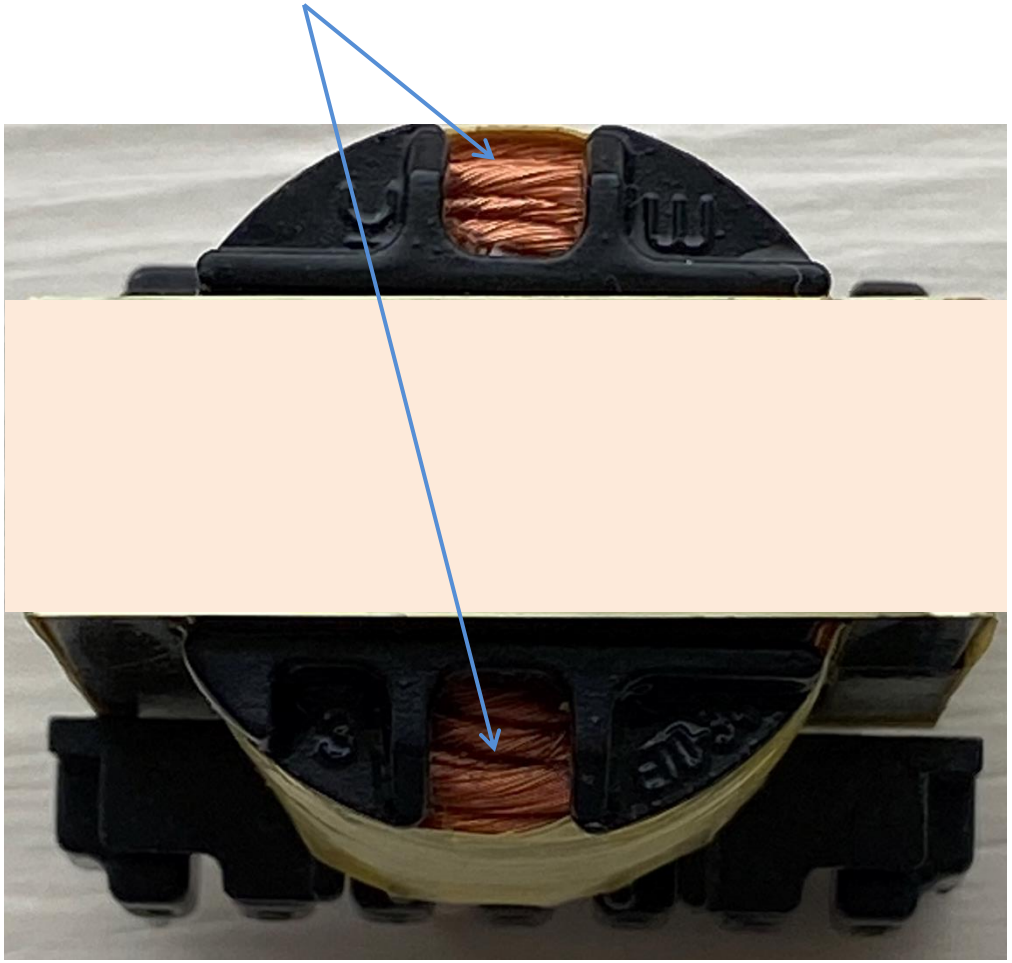
CAOUT (Pin 15): This is the output of a wide-bandwidth operational amplifier that senses line current and commands the PFC stage PWM comparator to force the correct duty cycle. This output can swing close to GND to command maximum duty cycle, and above the PFC ramp peak voltage to force zero duty cycle when necessary. Connect current loop compensation components between CAOUT and MOUT.

Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings

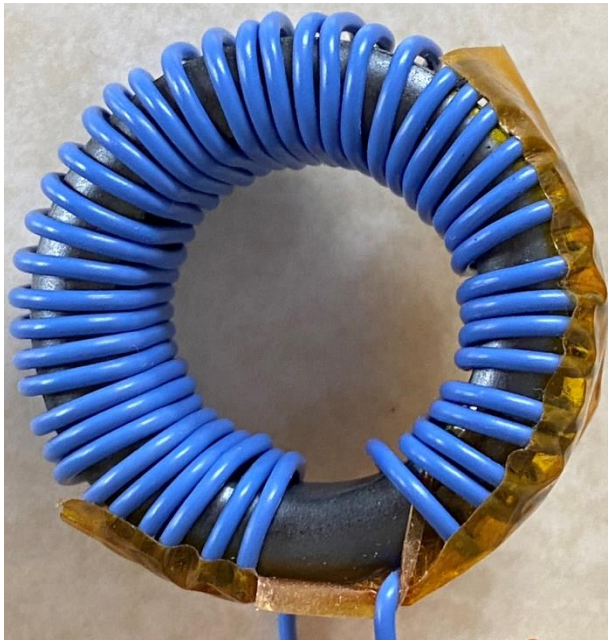
Original PFC inductor has overlapping layers of winding



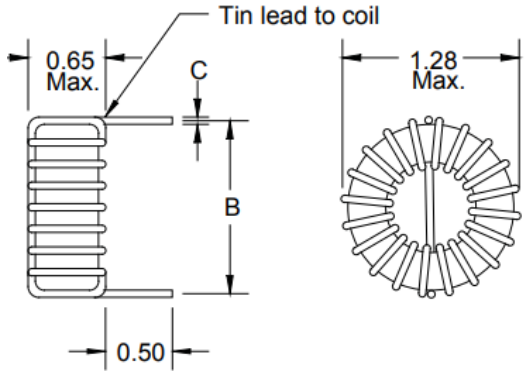
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Inductor #1: Bourns PN: 2300LL-681-H-RC, 680uH
Built by using toroid core, single layer winding.
However, some amount of winding overlapping is visible.



Inductor #2: Homemade by using toroid core Wurth PN: 7427015 and 43 turns of single layer winding.
Inductance measured at 1.39mH @ 300kHz.

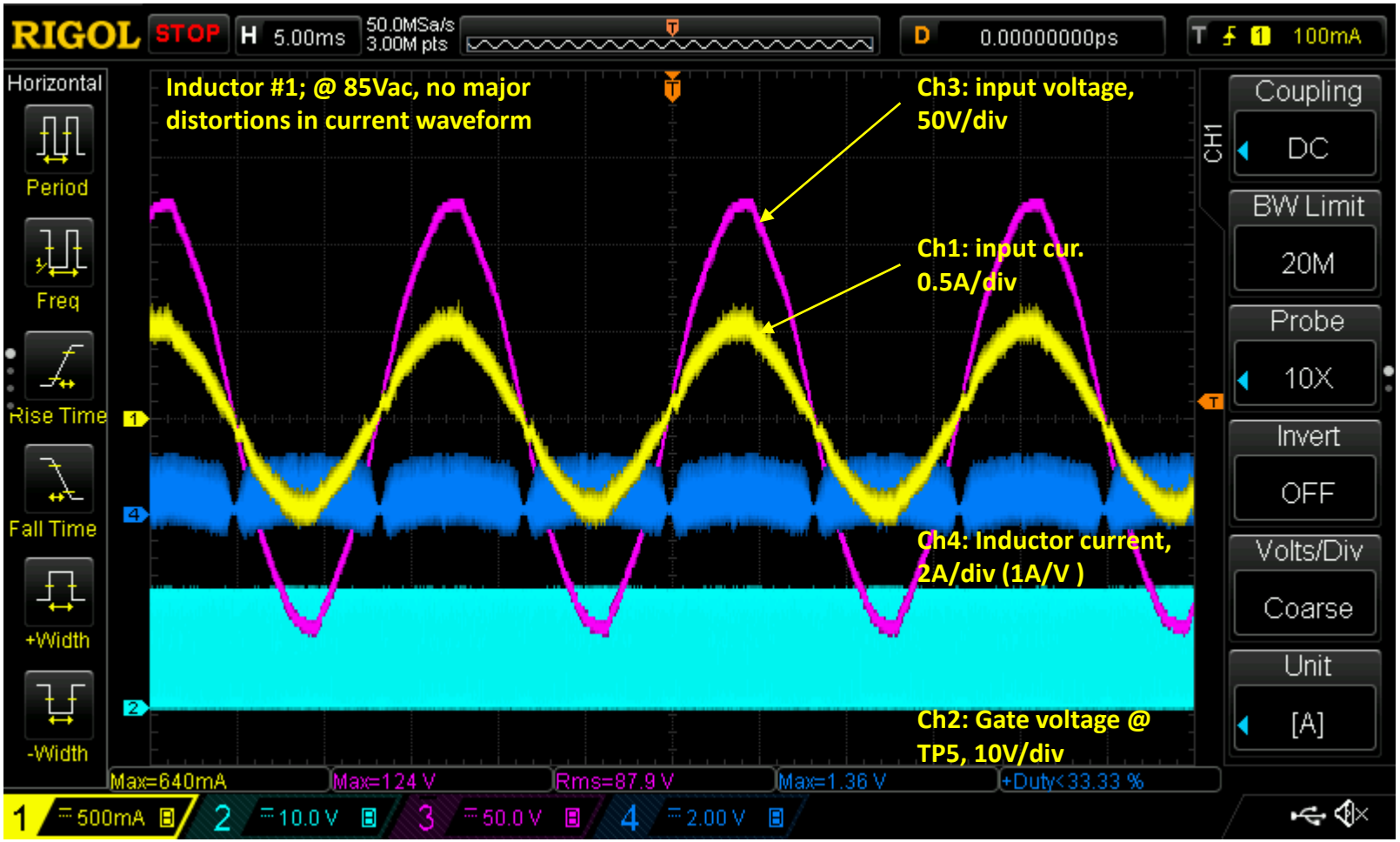
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



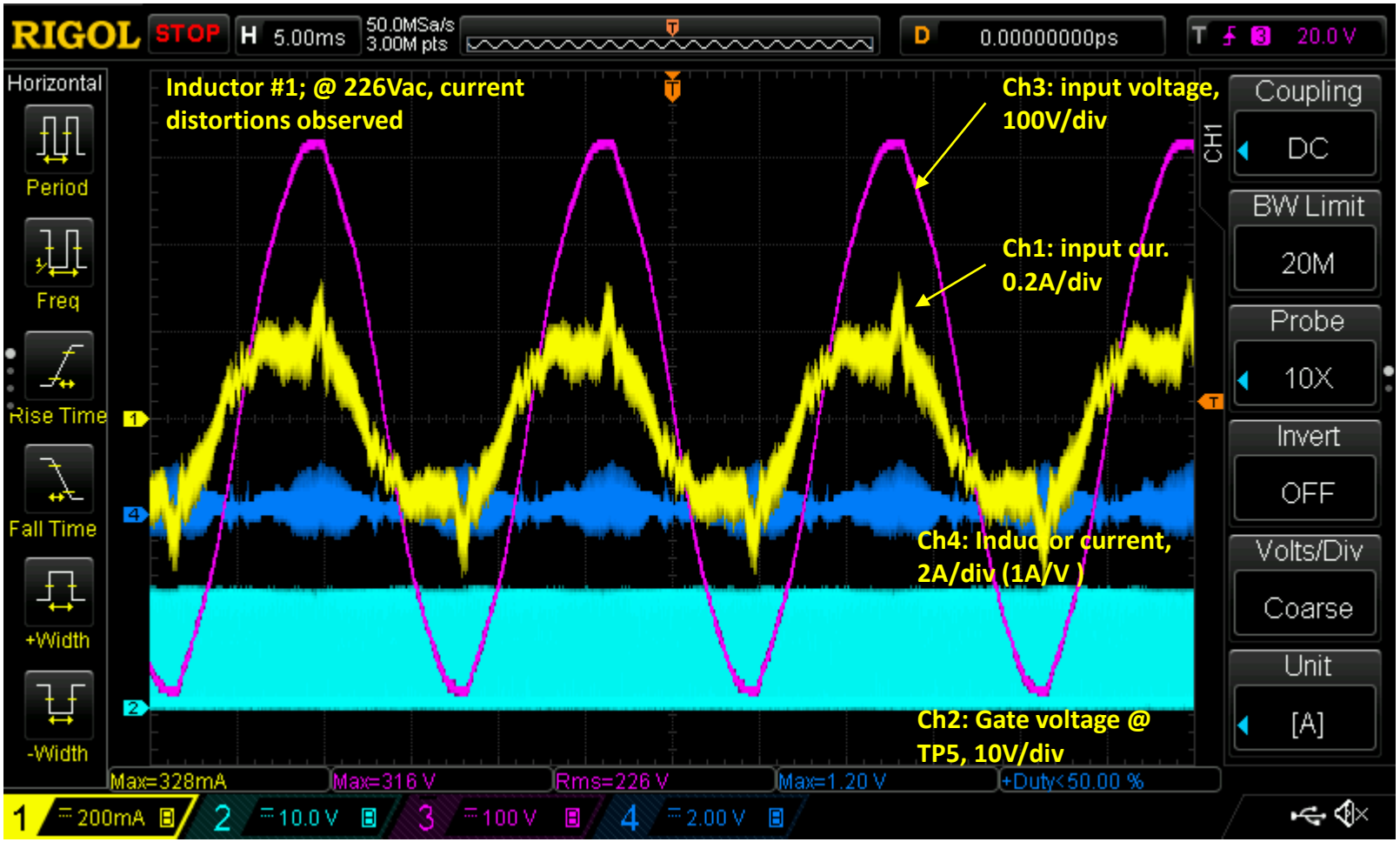
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



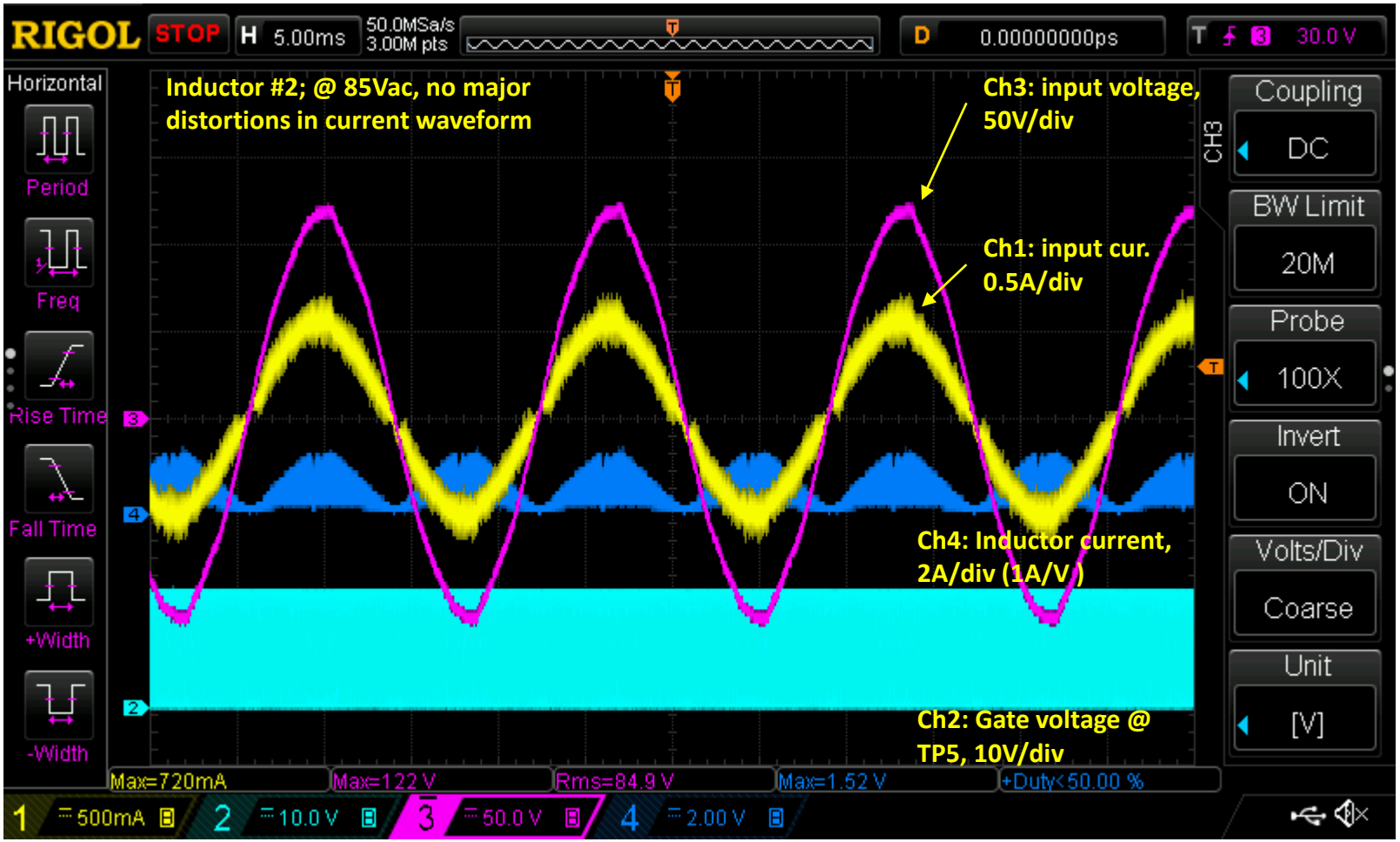
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



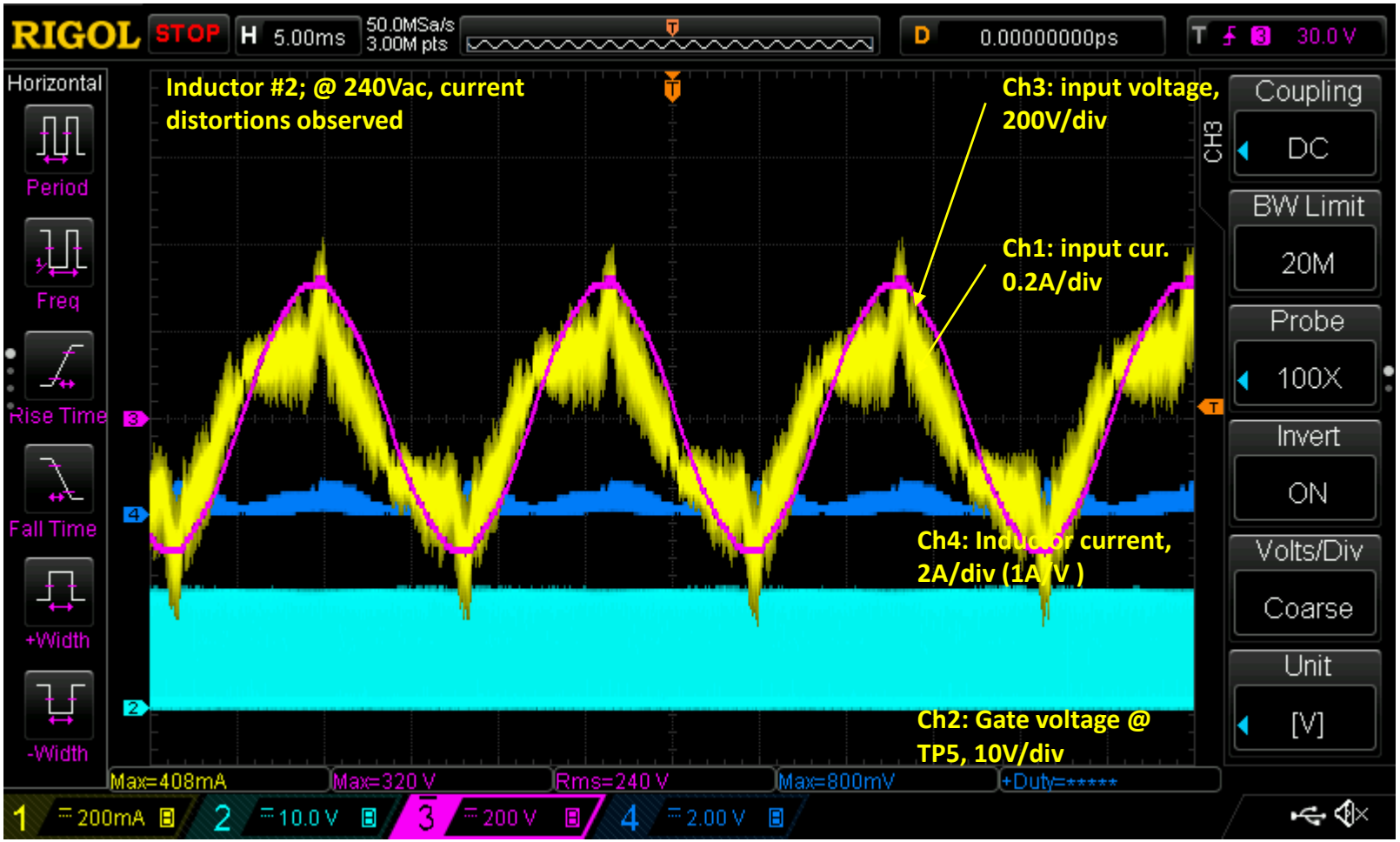
Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Measuring inductor current vs gate voltages, 1/15/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings

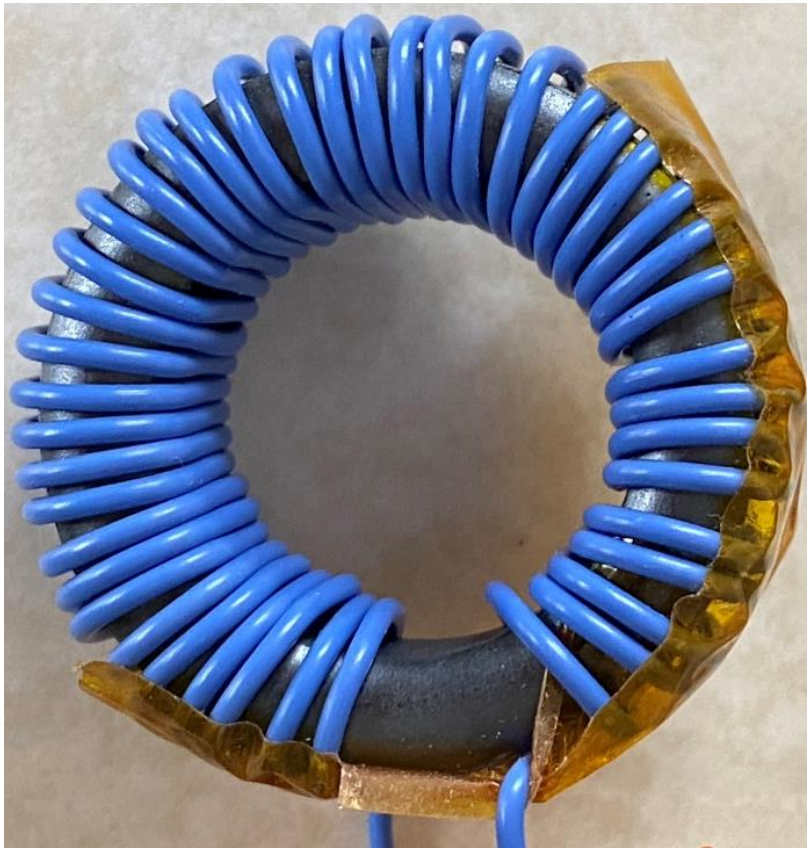
Conclusions on 1/15:

1) Two different inductors with no or minimal winding overlapping are tried out. Current distortions at high voltages were observe in both case.
2) Original inductor has overlapping windings and new ones do not. Even though the winding to winding capacitance is not measured, it is assumed that a single layer toroid inductor would result in lowest inter-winding capacitance.
3) Is there any practical way to measure the inter-winding capacitance?
4) Is there any rule of thumb as to how much inter-winding capacitance would be too much?

Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Inductor #2: Homemade inductor by using toroid core Wurth PN: 7427015 and 43 turns of single layer winding.
Inductance measured at 1.39mH @ 300kHz.

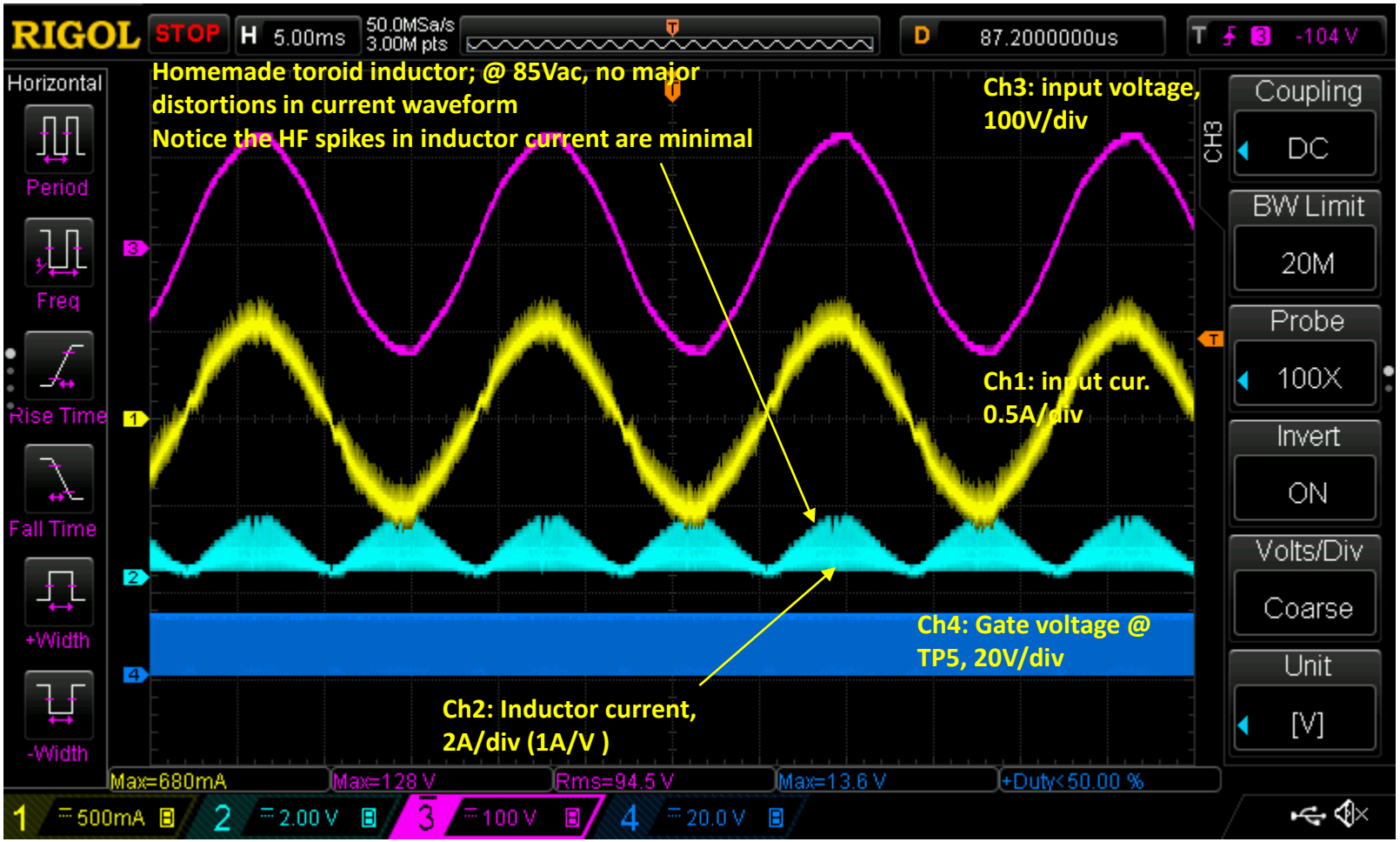
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



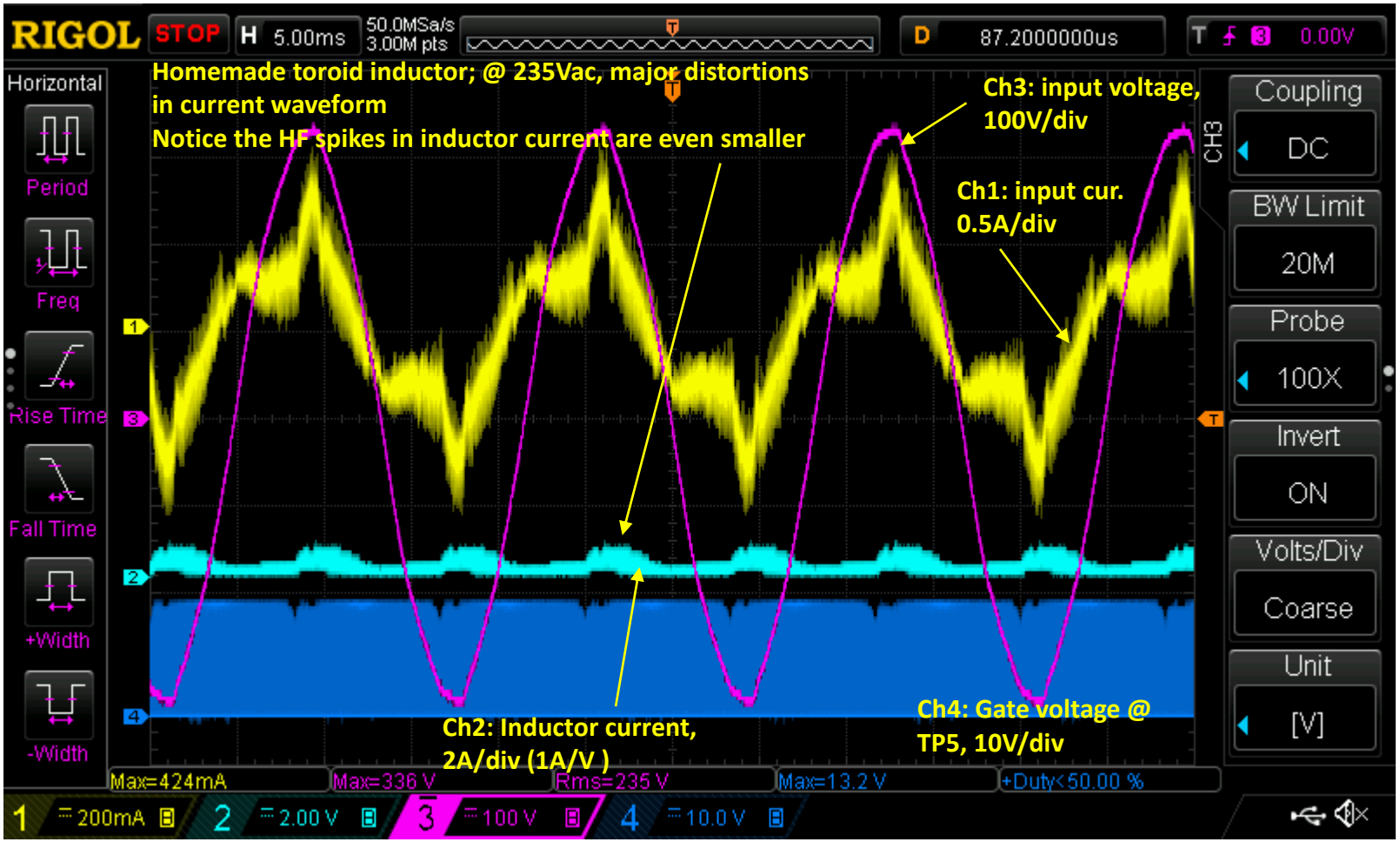
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



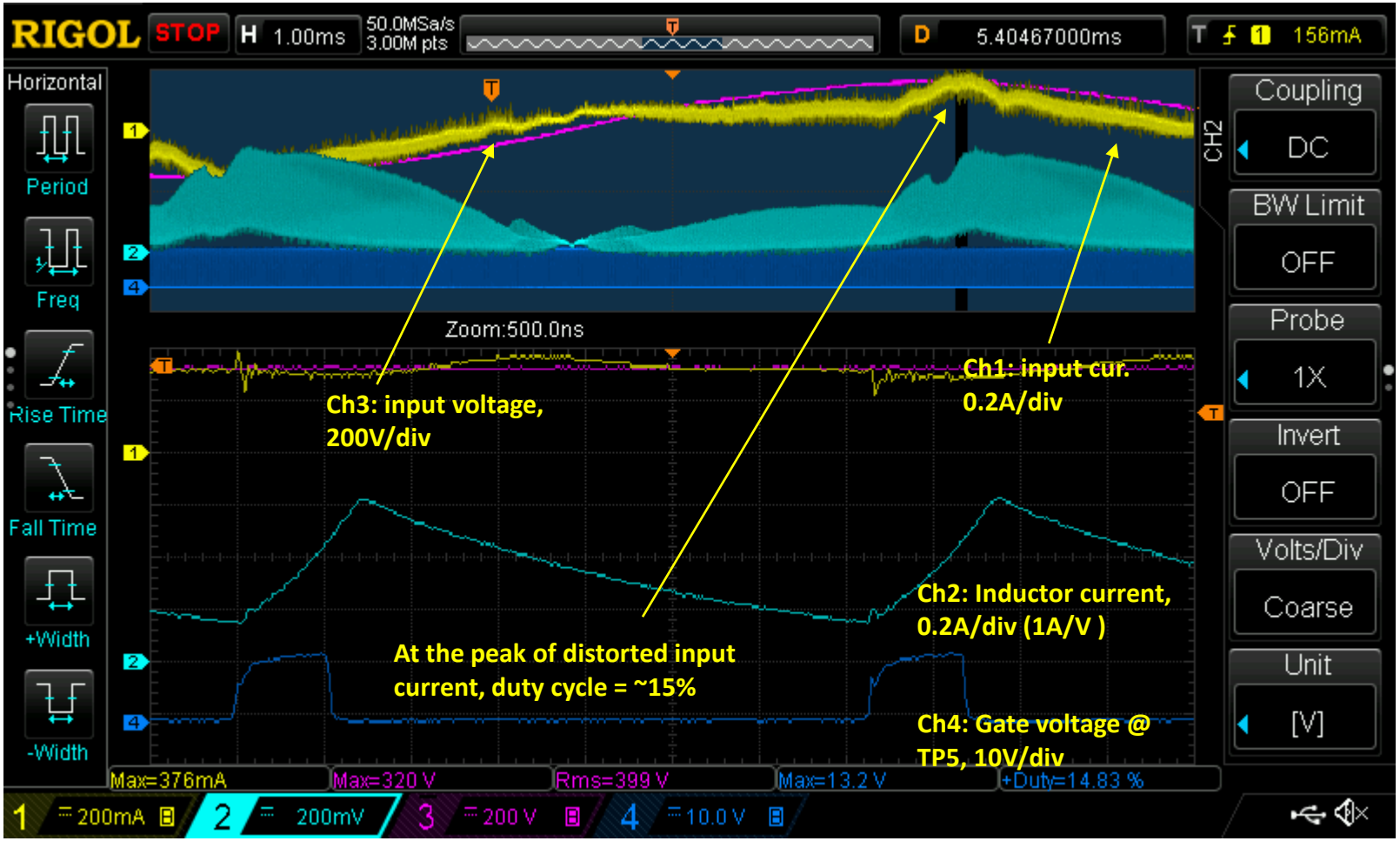
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Homemade toroid inductor; @ 235Vac, major distortions in current waveform. Notice that there are no turn-on spikes in inductor current waveform

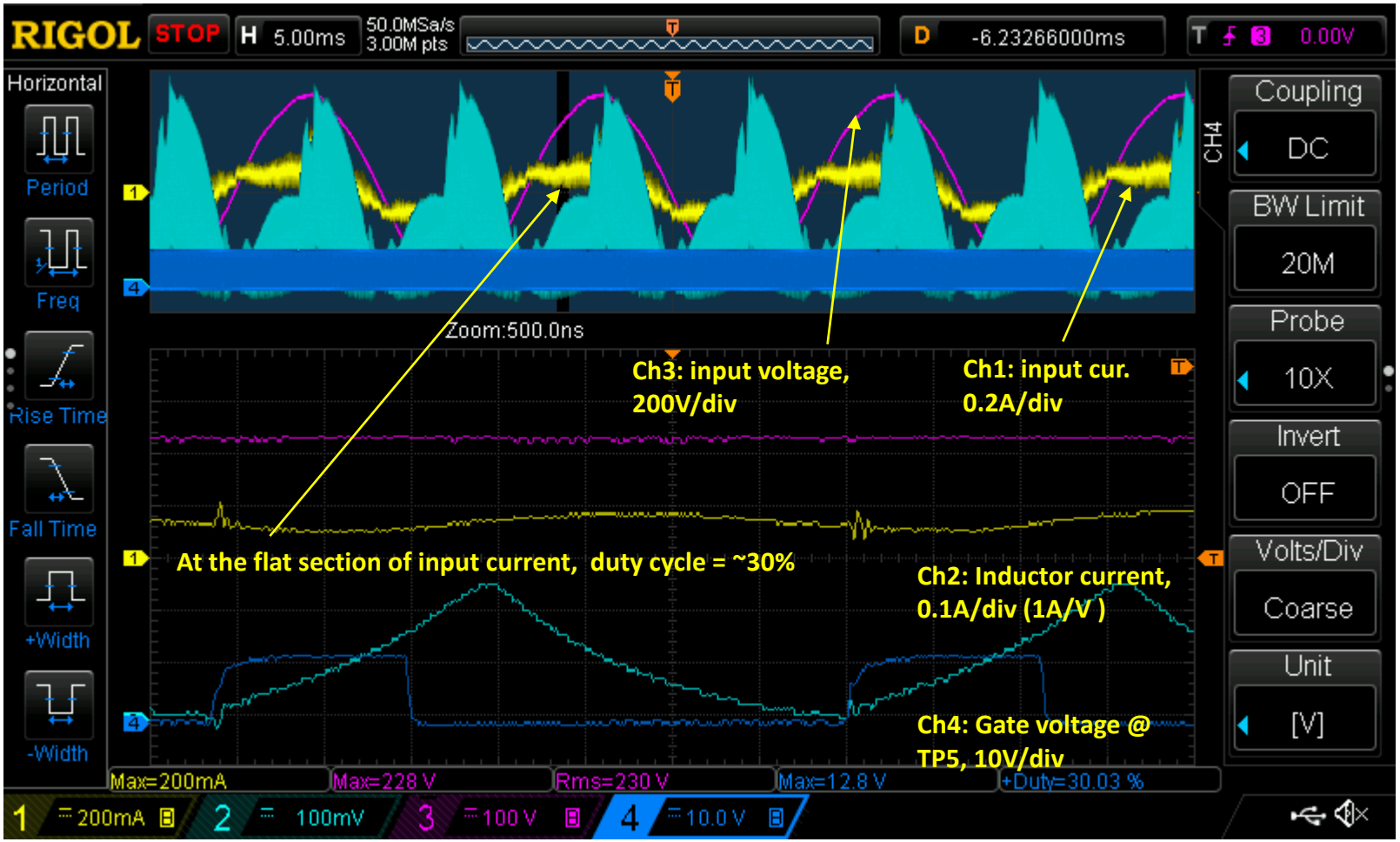
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



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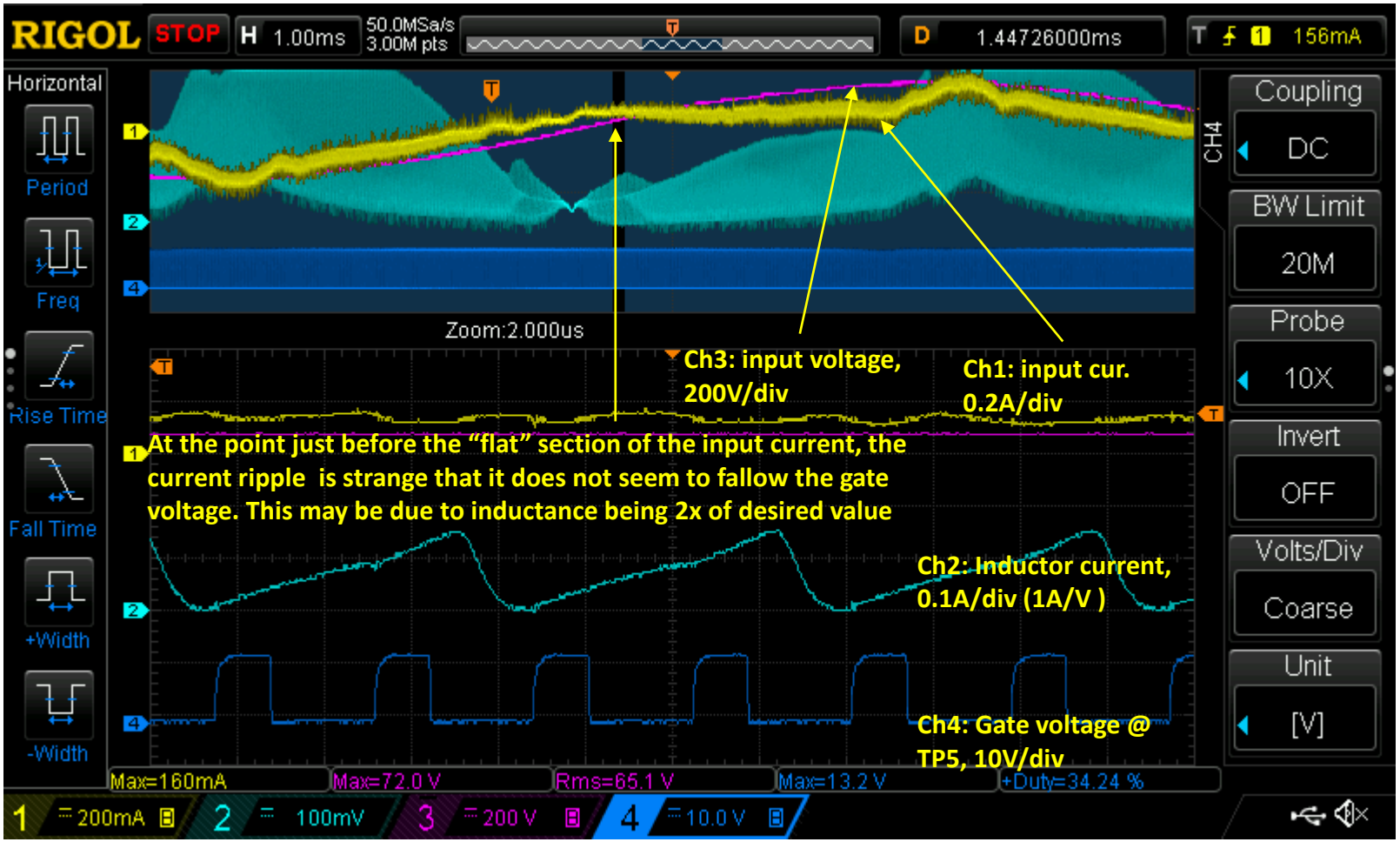
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Trying out with PFC boost inductors that are built by using toroid cores with no overlapping windings



Homemade toroid inductor; @ 235Vac, major distortions in current waveform. Notice that there are no turn-on spikes in inductor current waveform

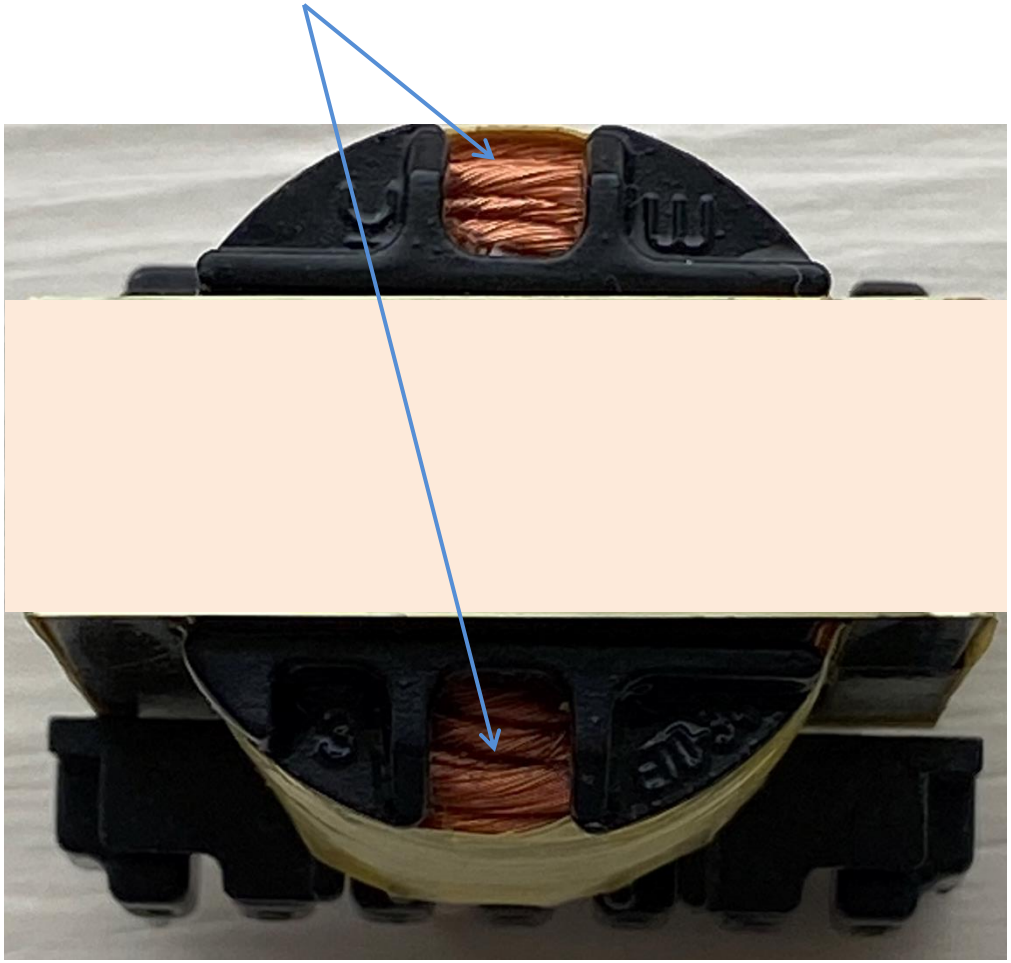
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Original PFC inductor (680uH) has overlapping layers of winding



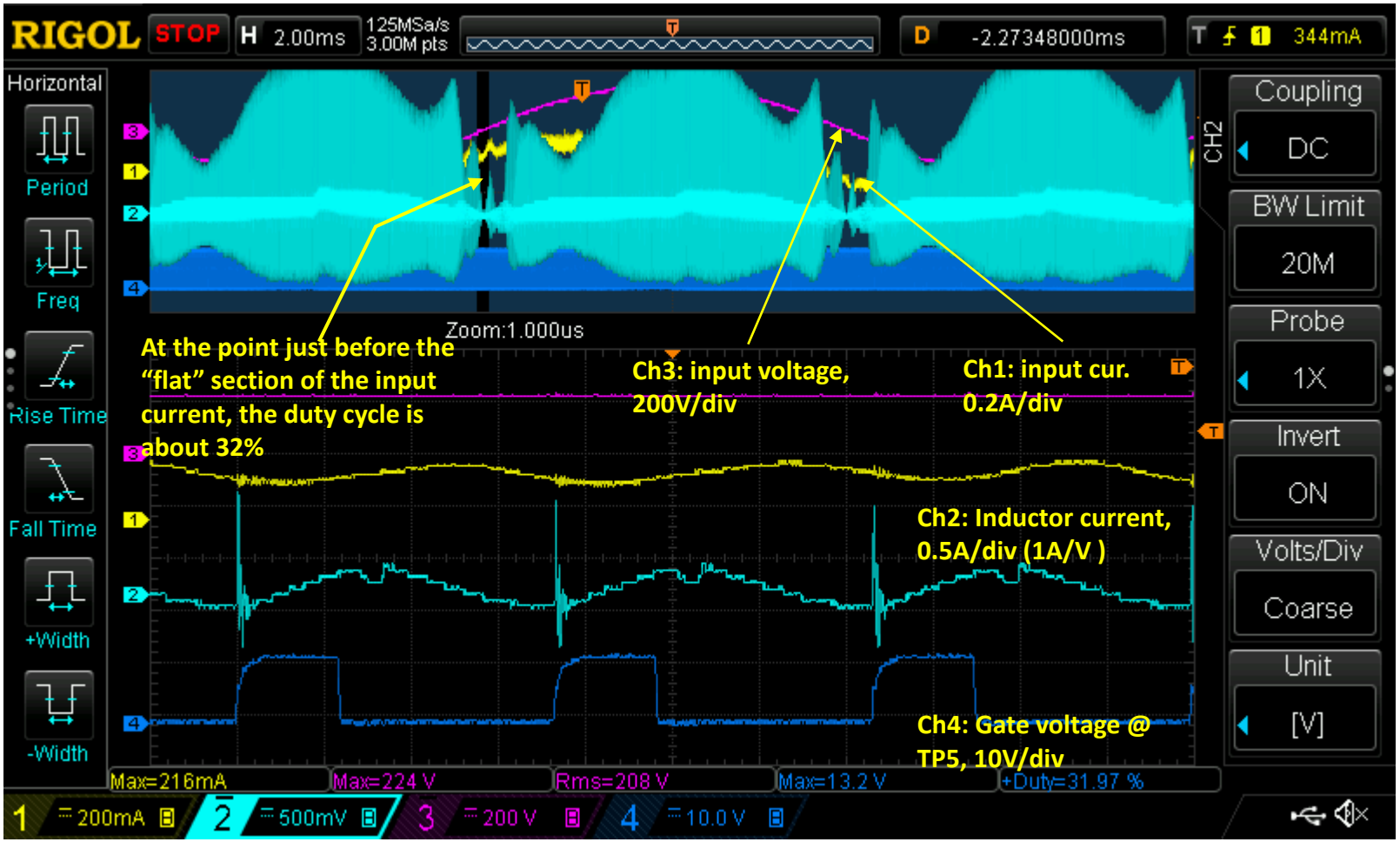
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Original inductor @ 235Vac, major distortions in current waveform. Notice that there are significant current spikes at the time when MOSFET turns on.



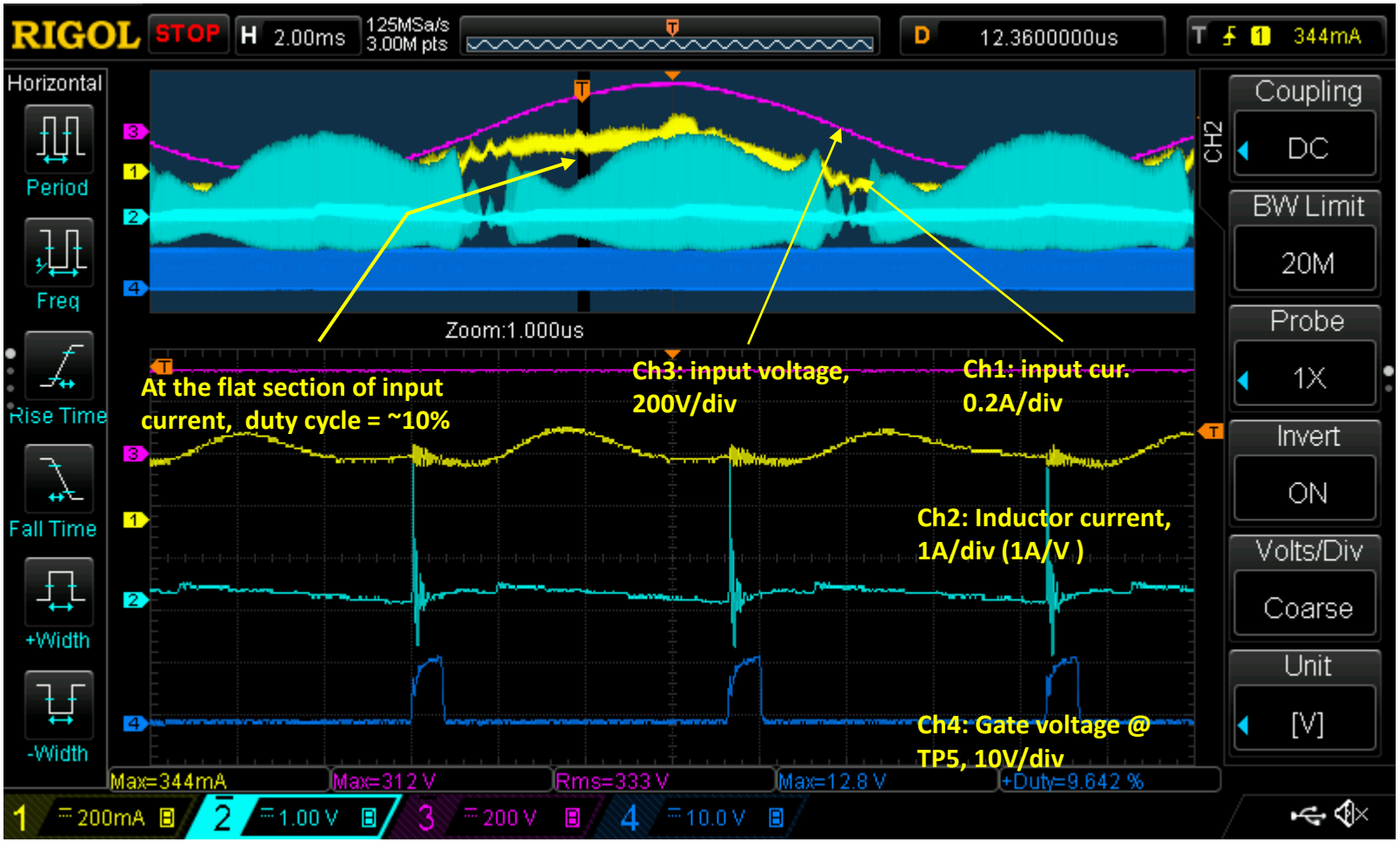
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Original inductor @ 235Vac, major distortions in current waveform. Notice that there are significant current spikes at the time when MOSFET turns on.



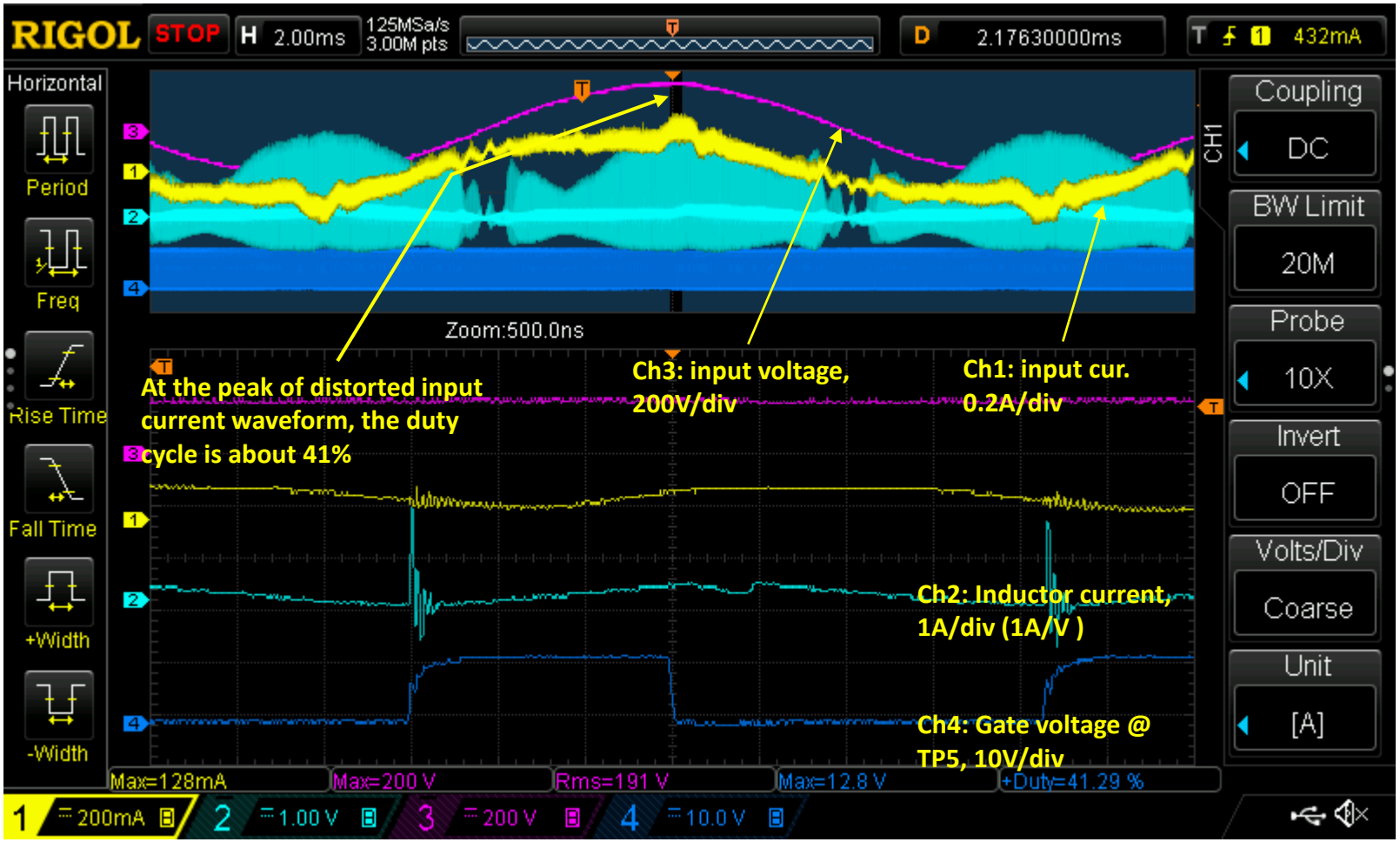
Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth

Ch4: Tek TCPA300 w/ TCP312 Current probe

Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Original inductor @ 235Vac, major distortions in current waveform. Notice that there are significant current spikes at the time when MOSFET turns on.



Measuring inductor current vs gate voltages, 1/22/2023

Ch1: Fluke 80i-110S, which has limited bandwidth
Ch4: Tek TCPA300 w/ TCP312 Current probe
Per changes listed on page 55, 100pF cap removed from R5, **10nF from UCC28513 pin14-pin11**

Conclusions on 1/22:

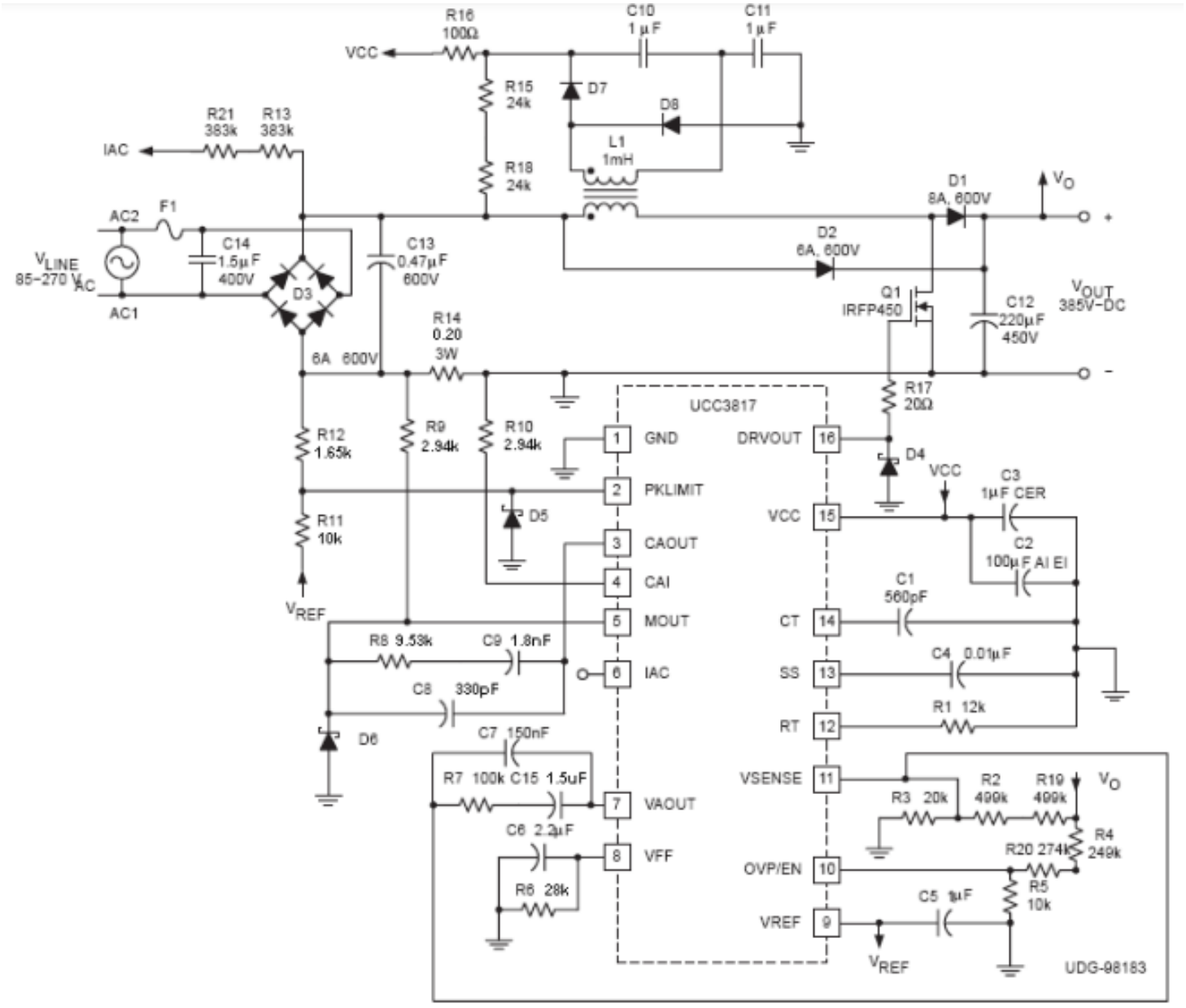
1. It seems like there is significant inter-winding capacitance in original inductor (TSD-3222, 680uH) which creates significant current spikes at the time when MOSFET turns on. Additional measurements conducted with 10nF cap on PKLMT pin14 to GND do not show any pulse droppings. However, the low frequency distortions in input current waveform are still visible.
2. The home-made toroid inductor (1.39mH @ 300kHz) was also tried out with 10nF on PKLMT pin. No pulse droppings observed. However, the low frequency distortions in input current waveforms were still visible. There was some unexpected results at the zero crossing of the voltage. This may be due to inductance being larger than the expected value. Repeat the same test with smaller toroid inductor with 680uH inductance.

Even though the original inductor has some inter-winding capacitance and even though it should be addressed, it seems that the current distortion may not be caused by the inter-winding capacitance since:

1. The current distortions are visible even when a toroid inductor with minimum inter-winding capacitance is used. There were no turn-on spikes and no pulse dropping observed with 10nF capacitance on PKLMT.
2. When the original inductor was used, there were significant current spikes at the turn on. Even though no pulse droppings observed with 10nF on PKLMT pin, the input current waveform was still distorted.

Measuring inductor current vs gate voltages, 2/5/2023

UCC3817 based design values



Measuring inductor current vs gate voltages, 2/5/2023

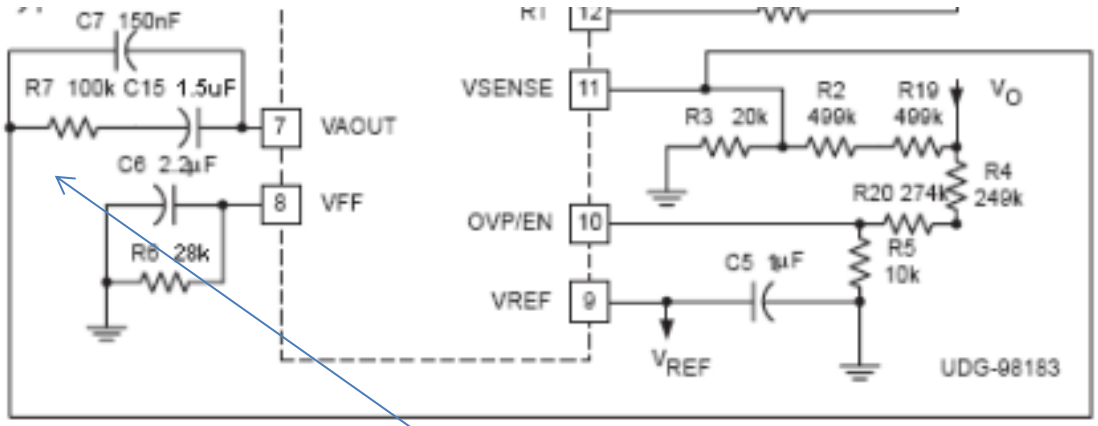
UCC3817 based design values

RefDes on UCC3817	RefDes on UCC28513	RefDes in Listen	PCB	Existing values	New values
R14=0.2	R2	R43	PSB-04	0.44	0.22
R3=20K	-	R60		22.1K	20K
R2/R19=499K	-	R44/R49		562K	499K
R21/R13	-	R47/R50		383K	No change
R11=10K	R14	R13	PFC-03	10K	No change
R12=1.65k	R7	R5		1.5K	1.62K
R9=2.94K	R12	R4		2.74K	2.94K (3.16k//39k)
C8=330p	C7	C8		150pF	330p
C9=1.8nF	C6	C6		3.3n	1.6nF
R8=9.53K	R13	R10		4.7K	9.53K (20k//18.2k)
R10=2.94K	R8	R9		2.74K	2.94K (3.16k//39k)
R6=28K	R15	R11		30.1K	28K (56k//56k)
C6=2.2uF	C8	C9		4.7uF	2uF (1uF//1uF)
C7=150n	C11	C2		150n	No change
C15=1.5uF	C10	C1		**1.5uF**	No change
R7=100k	R21	R1		48.7k	100k

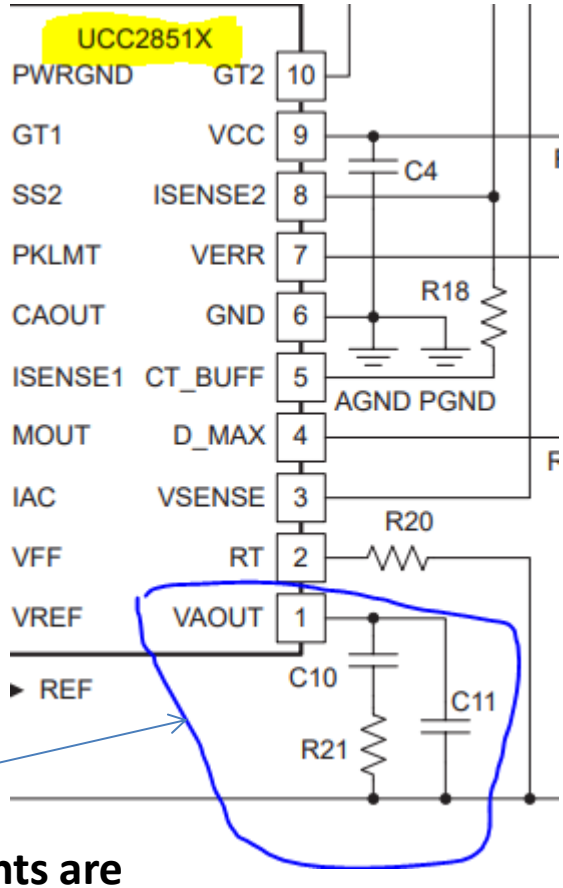
Measuring inductor current vs gate voltages, 2/5/2023

UCC3817 based design values

UCC3817 voltage error amp.



UCC28513 voltage error amp.



As part of this exercise, voltage error amp components are disconnected from GND and connected to pin3 (Vsense)

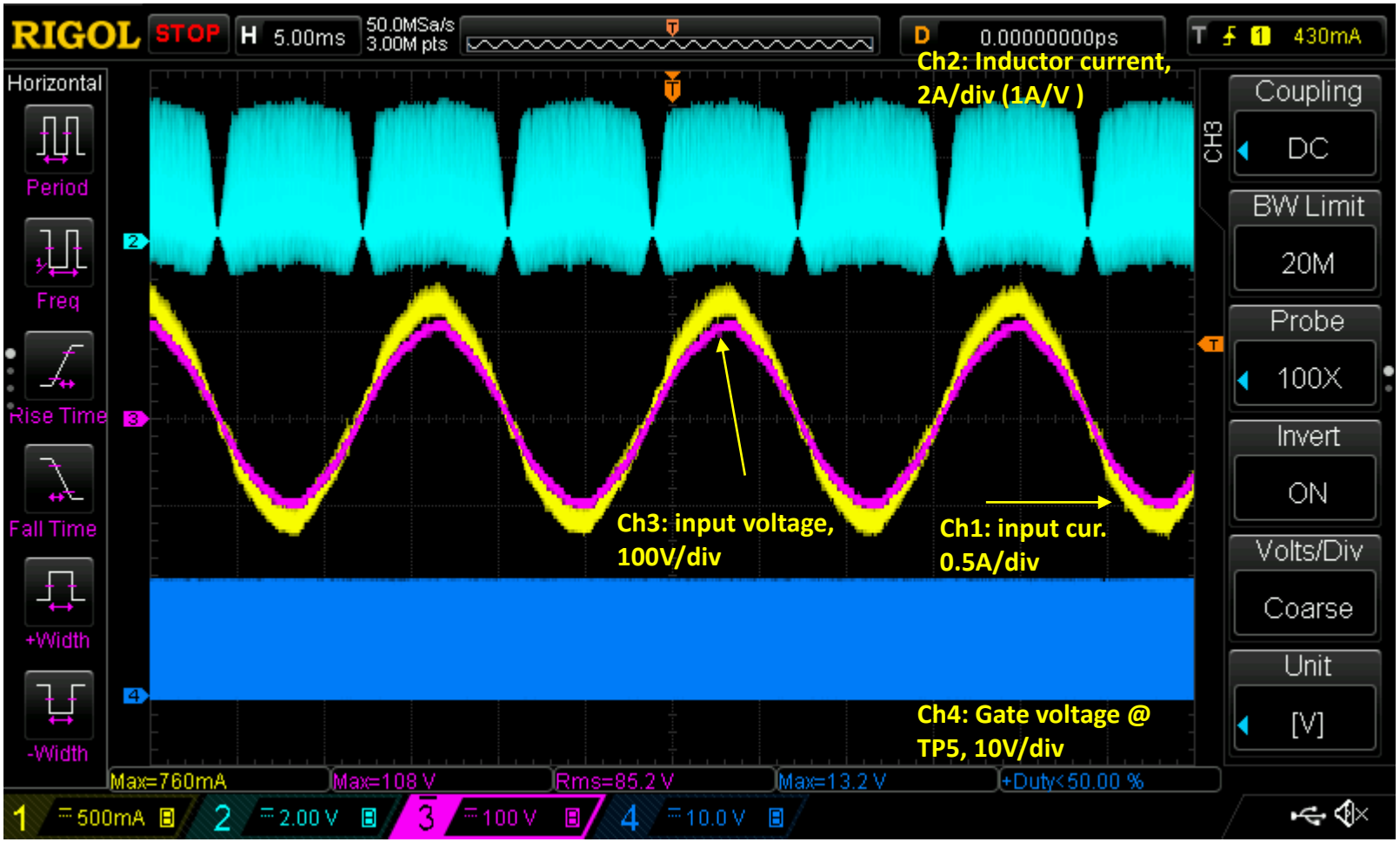
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

No major distortions at 85Vac input voltage



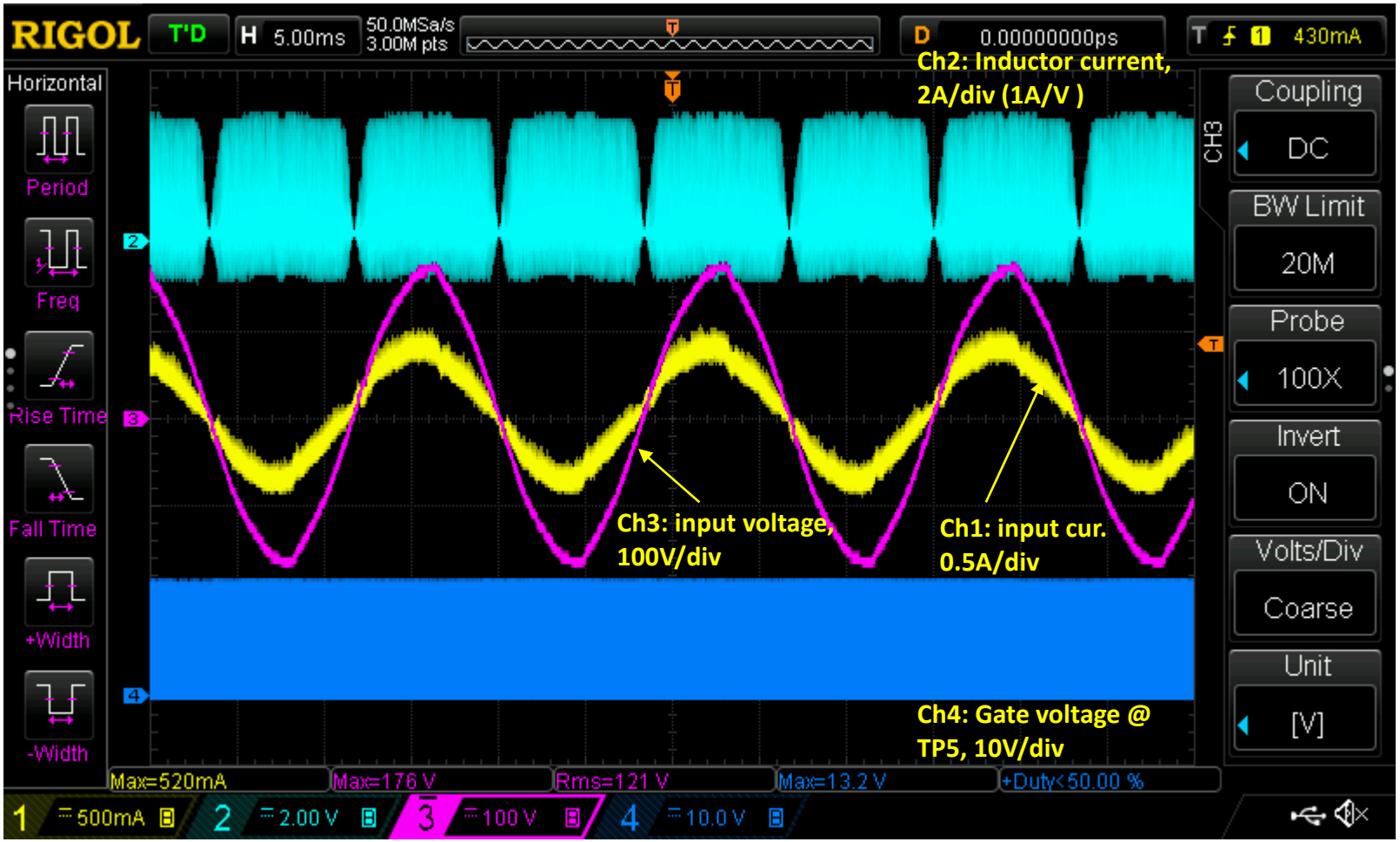
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

No major distortions at 120Vac input voltage



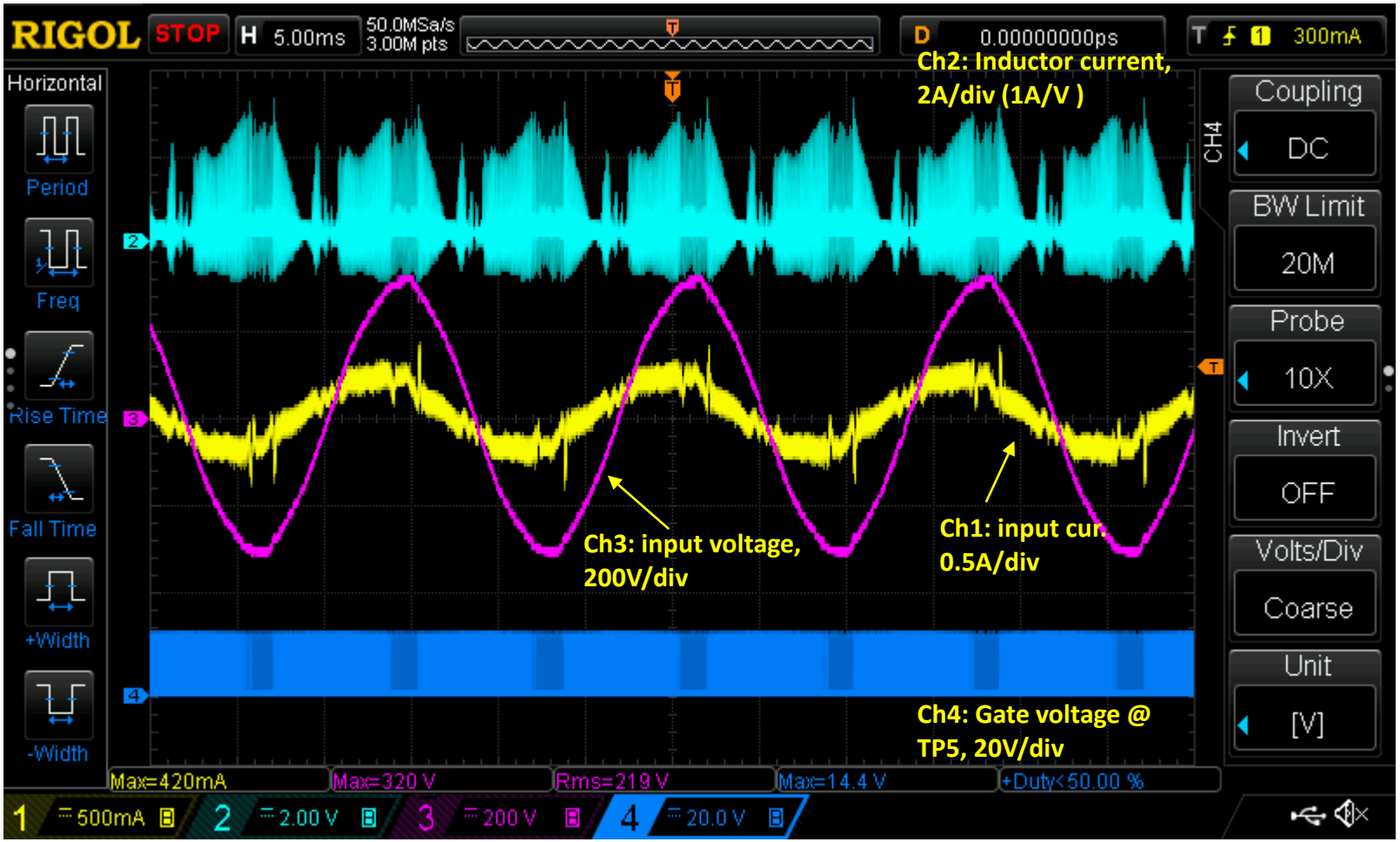
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac



Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; zooming into time just before input voltage reaches its peak region

Measuring inductor current vs gate voltages, 2/5/2023

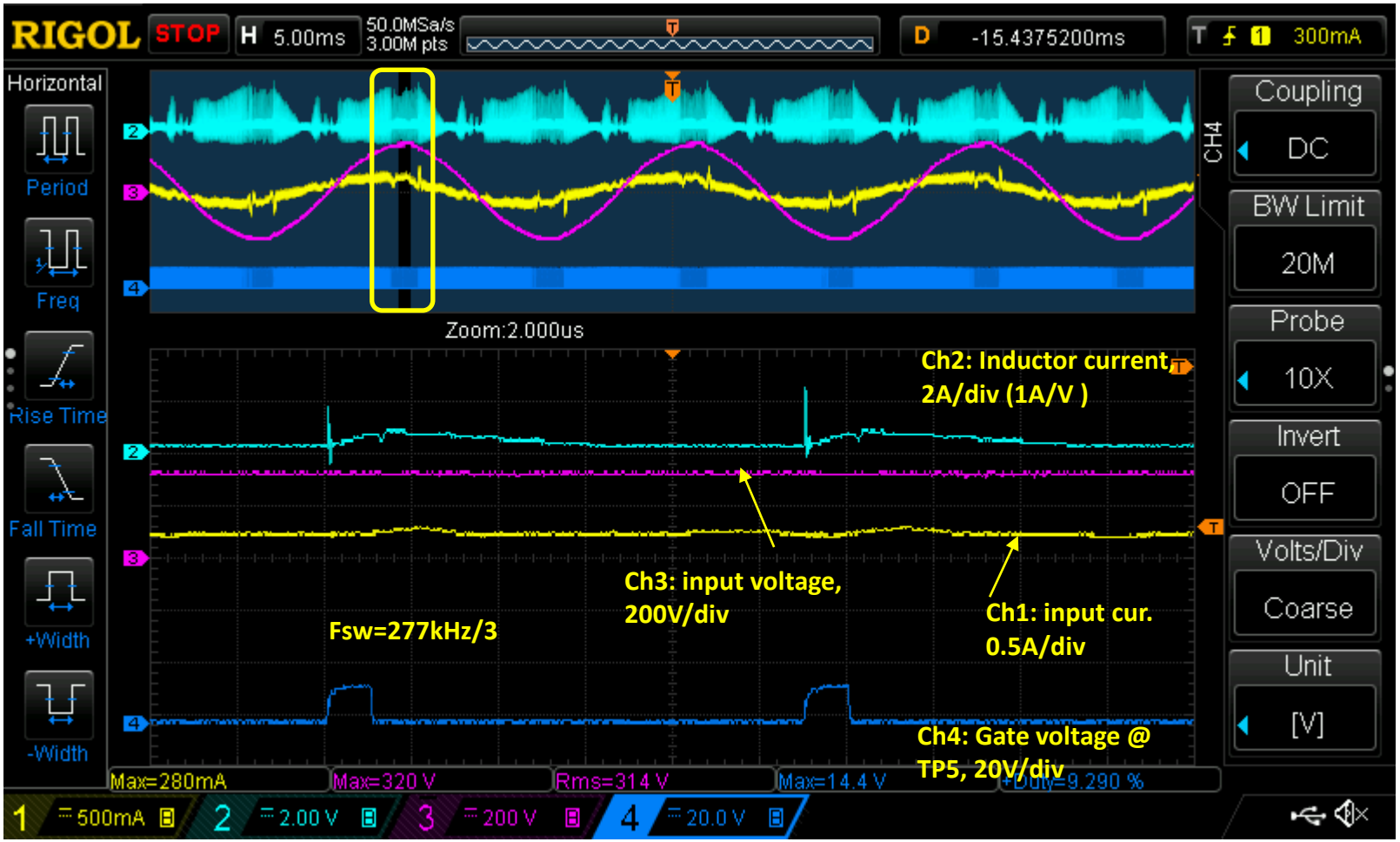
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; zooming into the region where input voltage is at its peak

Notice that the switching frequency is reduced to 1/3rd



Measuring inductor current vs gate voltages, 2/5/2023

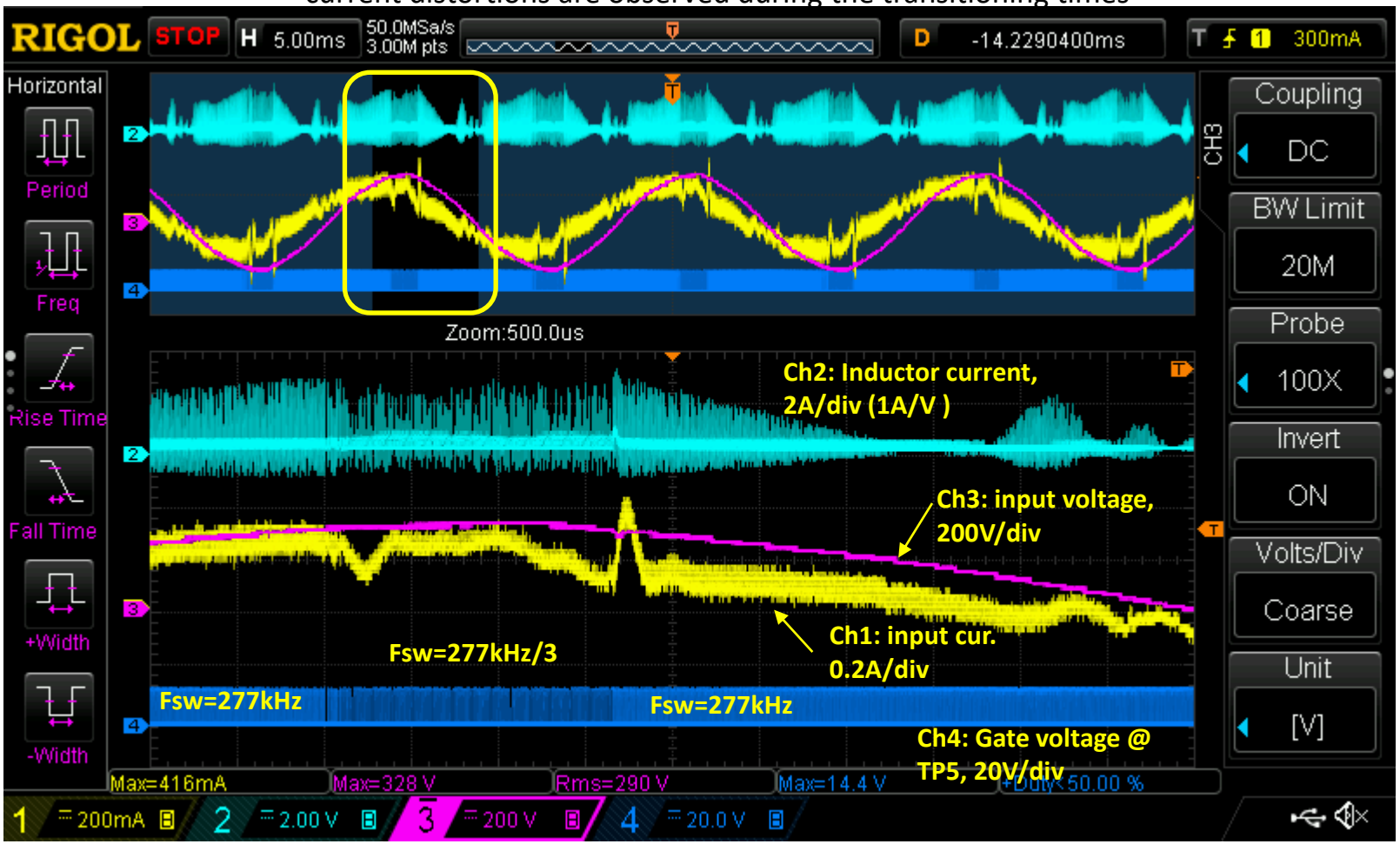
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; zooming into the region where input voltage is at its peak

Notice that the switching frequency is reduced to 1/3rd at the peak of input voltage and then changes back to Fsw and current distortions are observed during the transitioning times



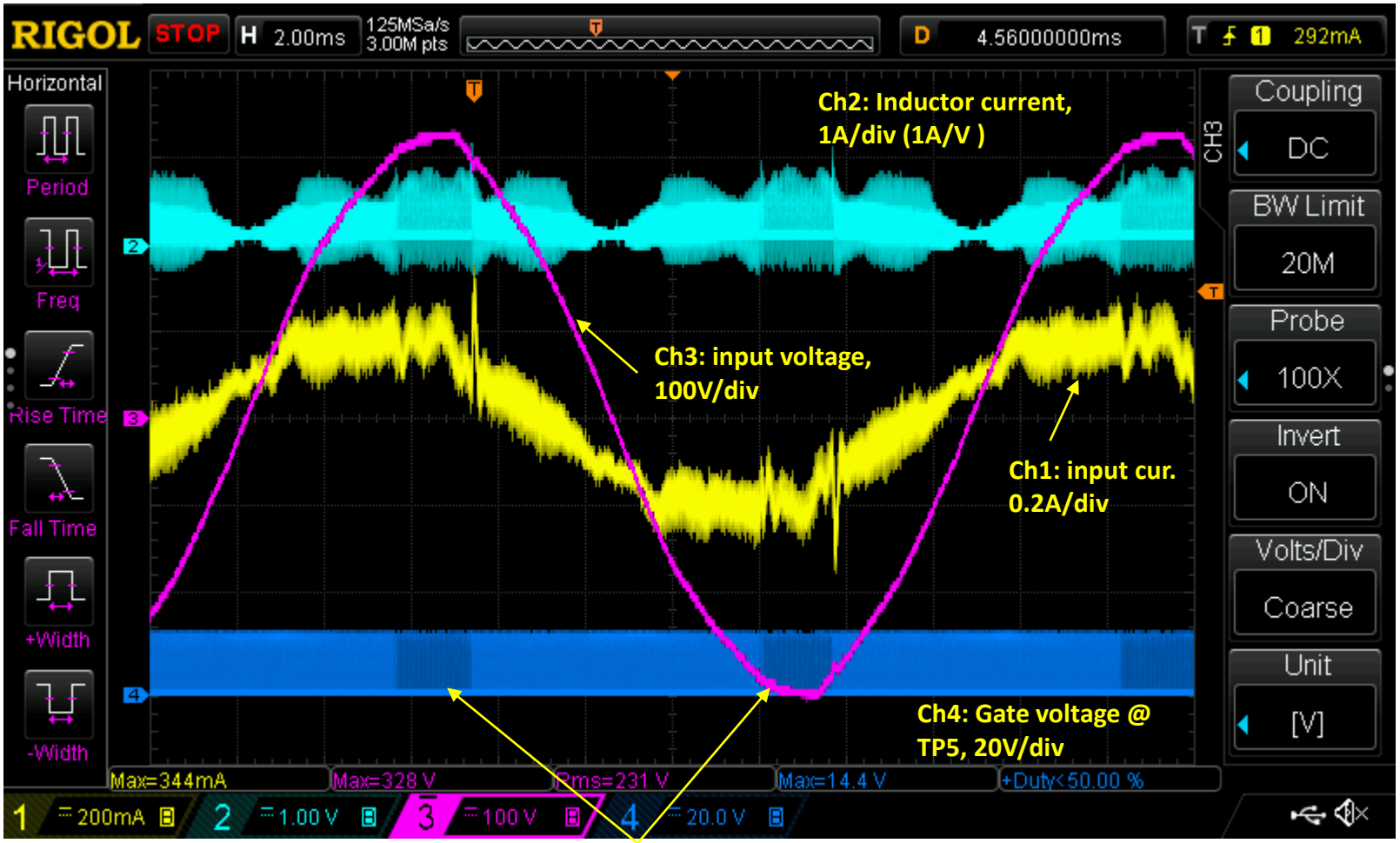
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; notice less HF cur. through inductor probably due to less inter-winding capacitance



Areas of interest

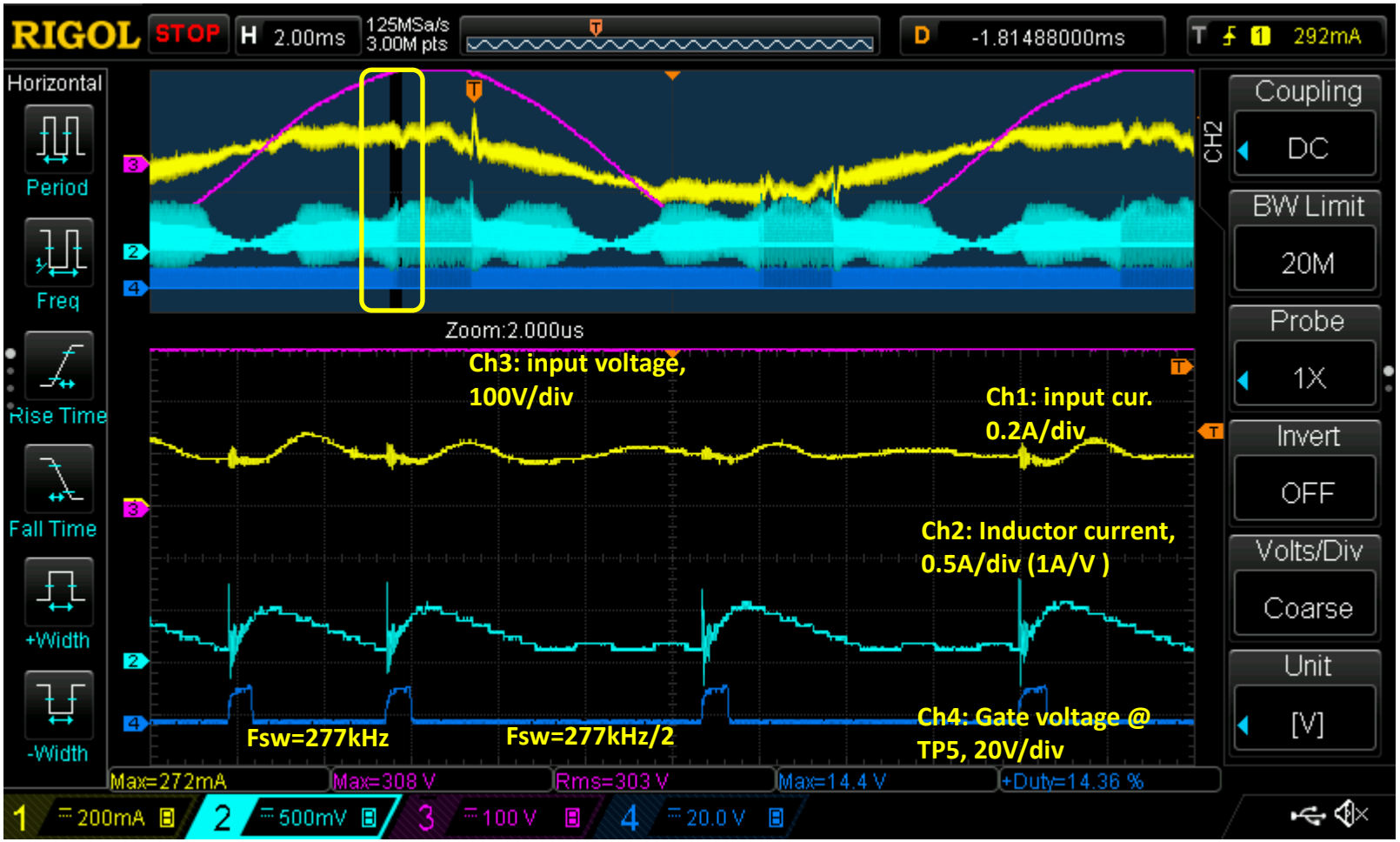
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; as input voltage reaches its peak, switching frequency is reduced by half



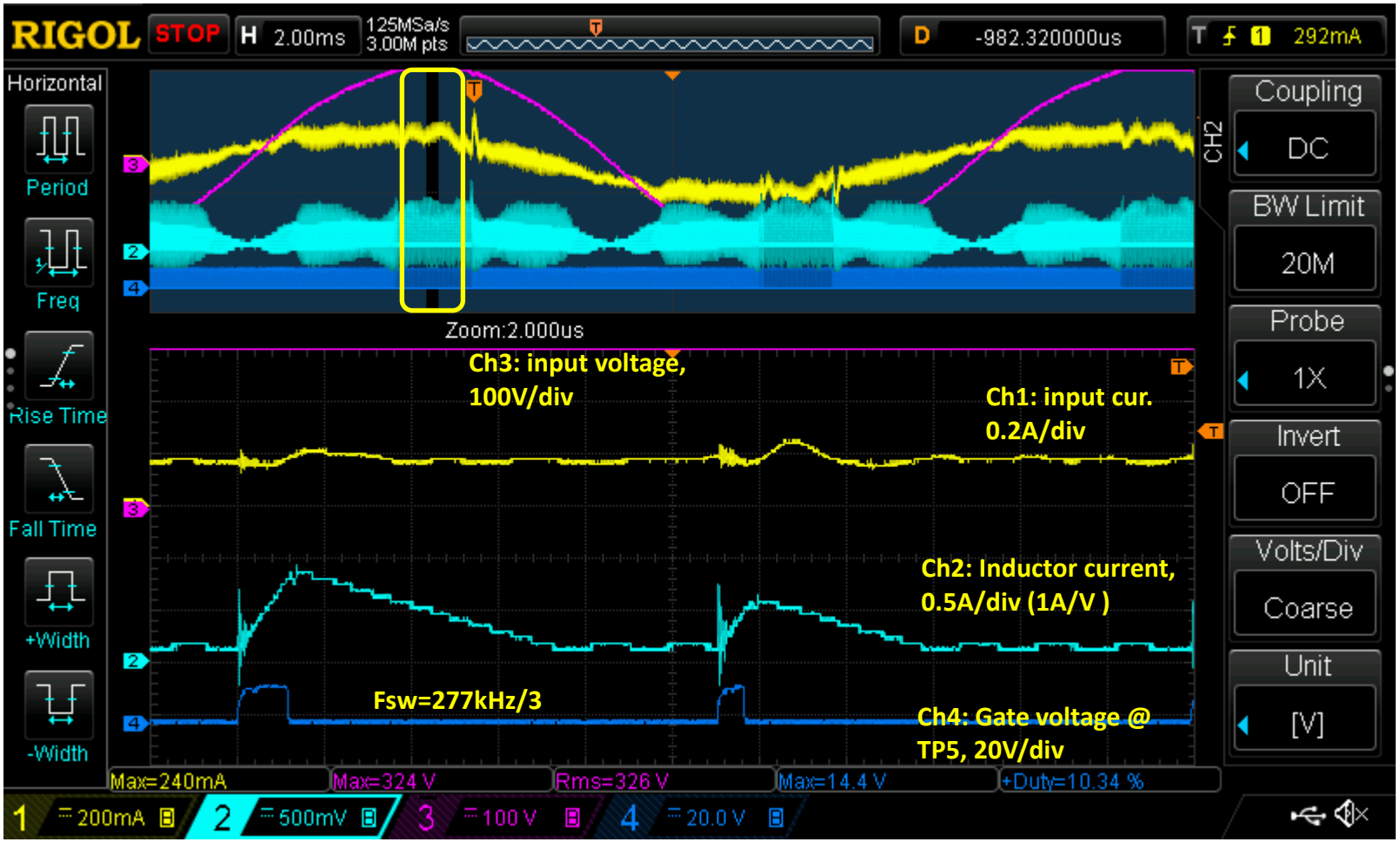
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; at the peak of input voltage , switching frequency is reduced to 1/3 rd



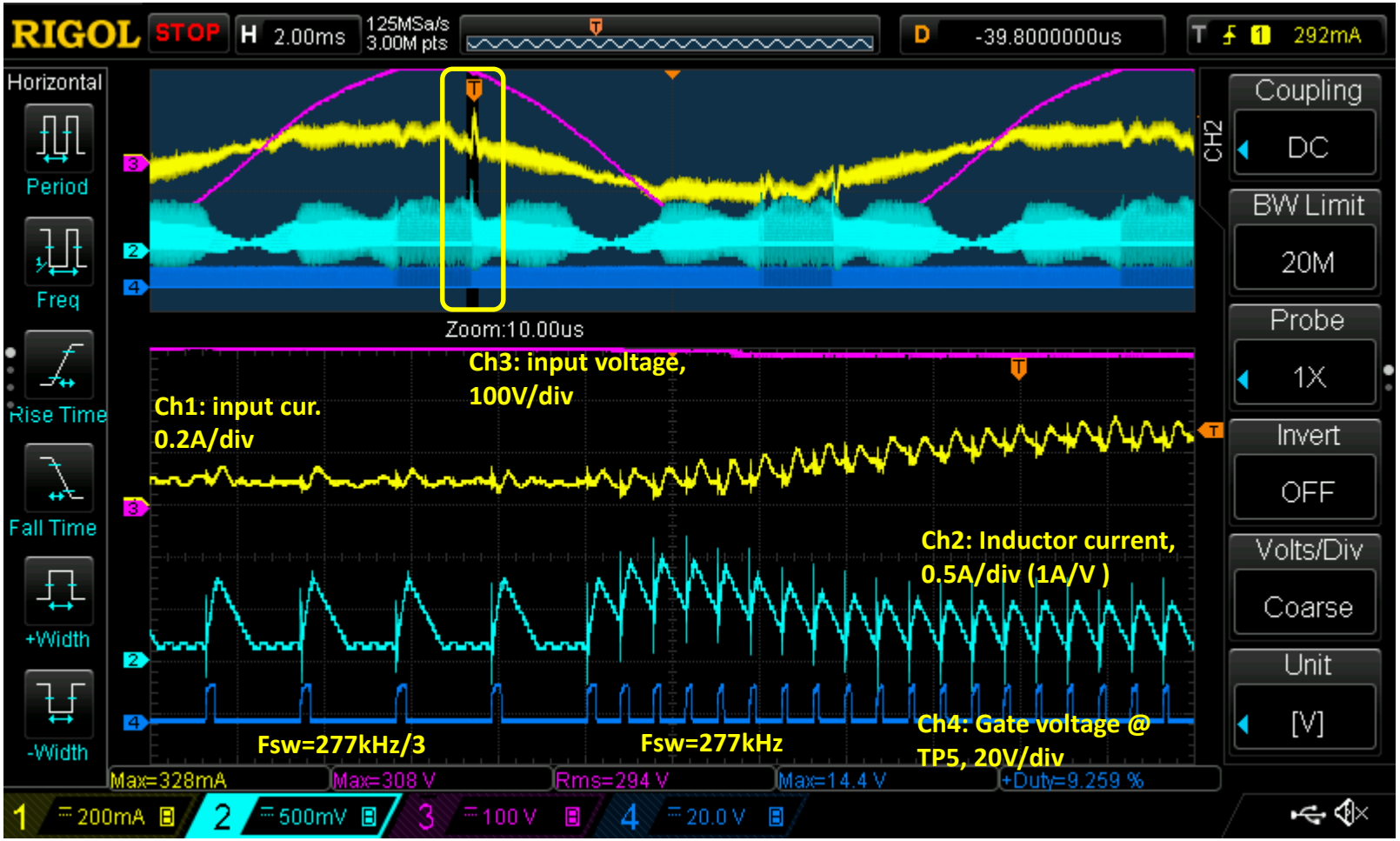
Measuring inductor current vs gate voltages, 2/5/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 25W external load across the DC-link, no capacitor across R5

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 94 for modifications

Distortions start at around 220Vac; current distortions observed as the switching frequency changes back to 277kHz



Measuring inductor current vs gate voltages, 2/5/2023

Conclusions:

- Referencing UCC3817 design, component values are updated
- Voltage feedback circuit is disconnected from GND and connected to pin3
- Two inductors were tried: original boost inductor (probably with some inter-winding capacitance) and an other toroid inductor, presumably with less inter-winding inductance. Both resulted in similar current distortions at high supply voltages.
- In both cases, the switching frequency was reduced at the time when supply voltage approached to its peak and switching frequency increased back as supply voltage starts to decrease. Current distortions were observed during the times when switching frequency changes were observed.
- There is no specific indication that PKLMT was initiated. All tests were conducted with 10nF cap from pin14 (PKLMT) to pin11 (GND) on UCC28513

Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND

RefDes on UCC28513	RefDes in Listen	PCB	Existing values	New values 2/5/23	New values 2/12/23
R2	R43	PSB-04	0.44	0.22	**0.44**
-	R60		22.1K	20K	No change
-	R44/R49		562K	499K	No change
-	R47/R50		383K	No change	No change
R14	R13	PFC-03	10K	No change	No change
R7	R5		1.5K	1.62K	No change
R12	R4		2.74K	2.94K (3.16k//39k)	**3k (3.16k//56k)**
C7	C8		150pF	330p	No change
C6	C6		3.3n	1.6nF	**4.9nF (1.6n+3.3n)**
R13	R10		4.7K	9.53K (20k//18.2k)	**3.23k (3.3k//150k)**
R8	R9		2.74K	2.94K (3.16k//39k)	**3k (3.16k//56k)**
R15	R11		30.1K	28K (56k//56k)	No change
C8	C9		4.7uF	2uF (1uF//1uF)	No change
C11	C2		150n	No change	No change
C10	C1		**1.5uF**	No change	No change
R21	R1		48.7k	100k	No change

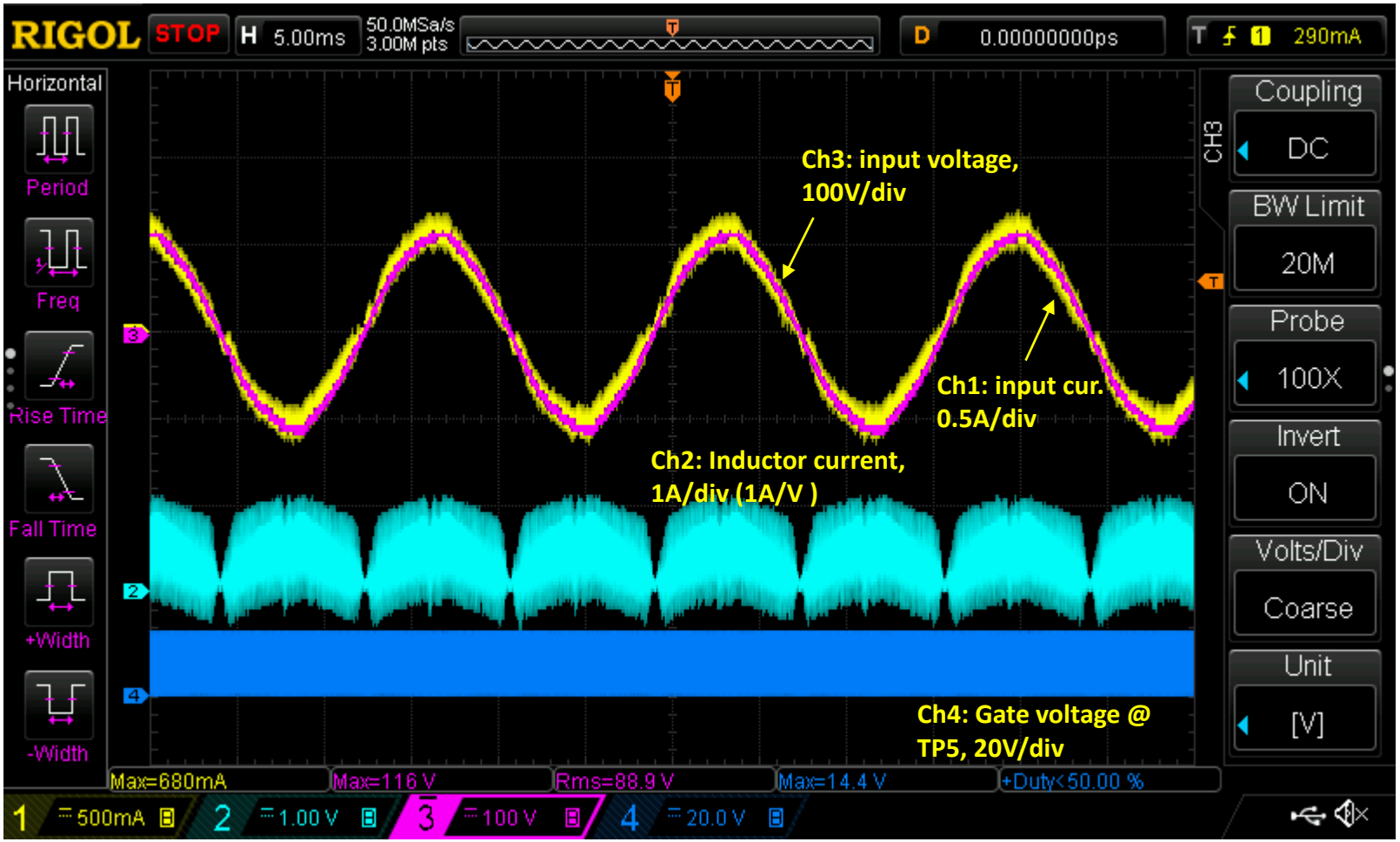
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

No major distortions at 85Vac



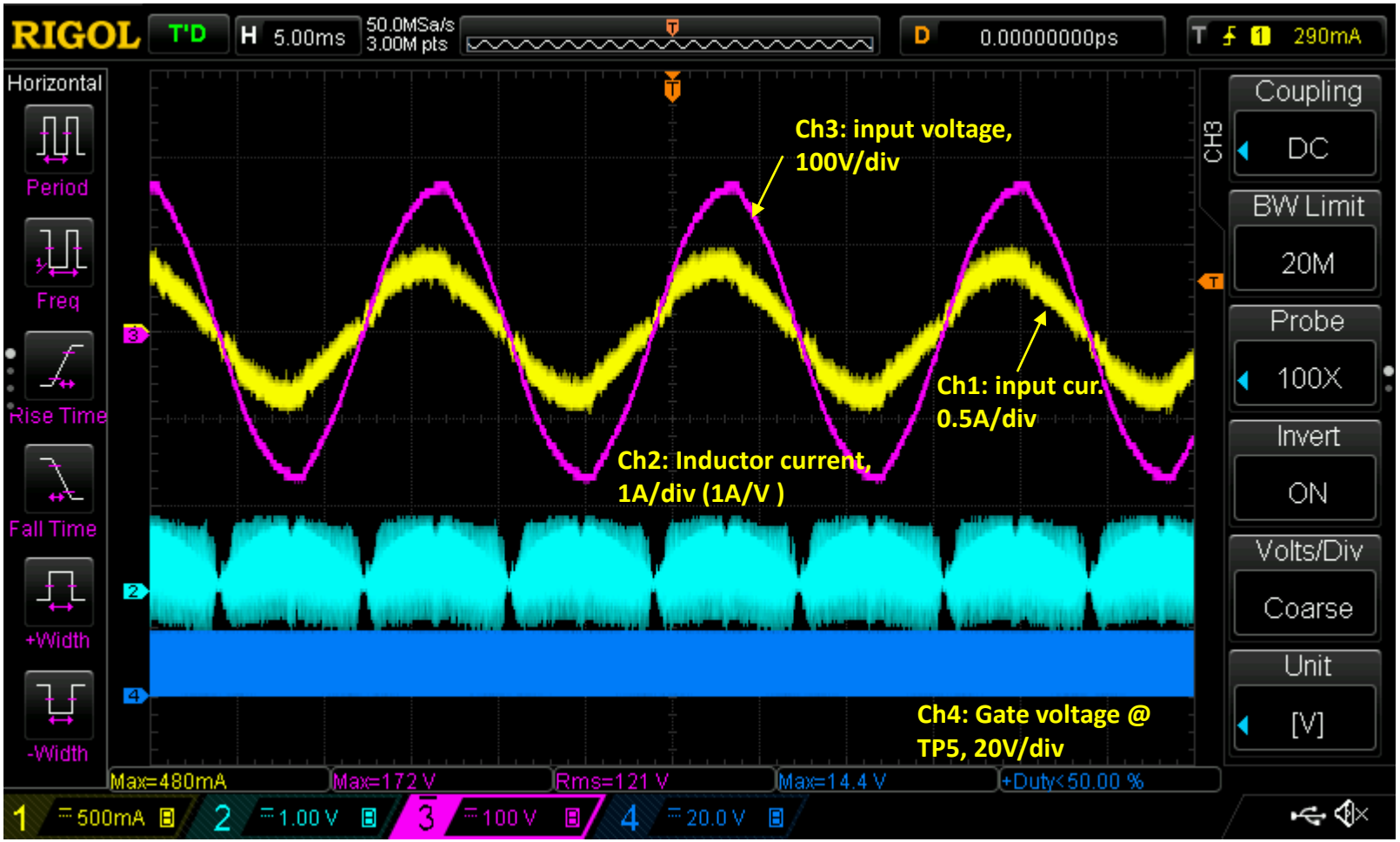
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

No major distortions at 120Vac



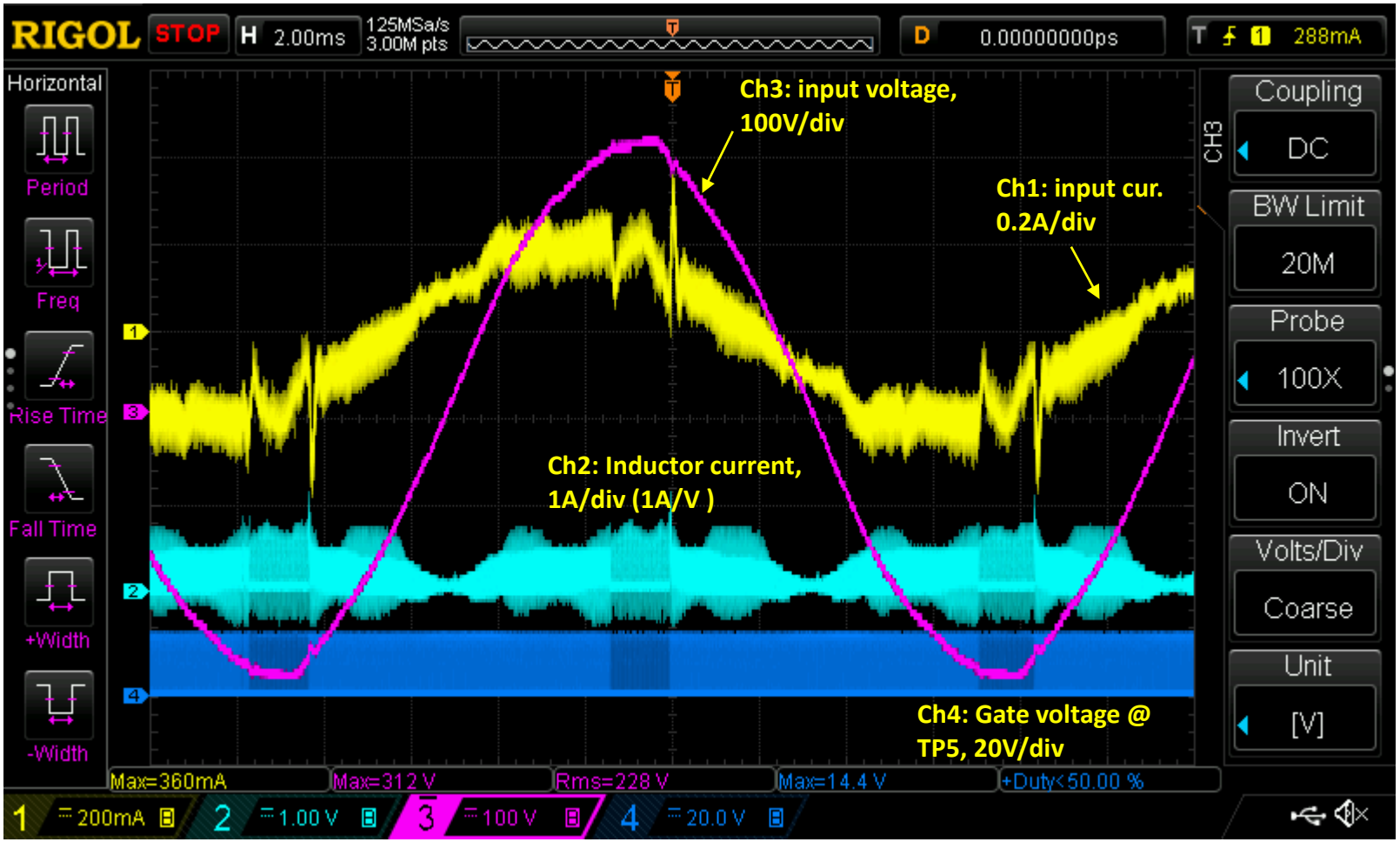
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

At around 230Vac, current distortions appear



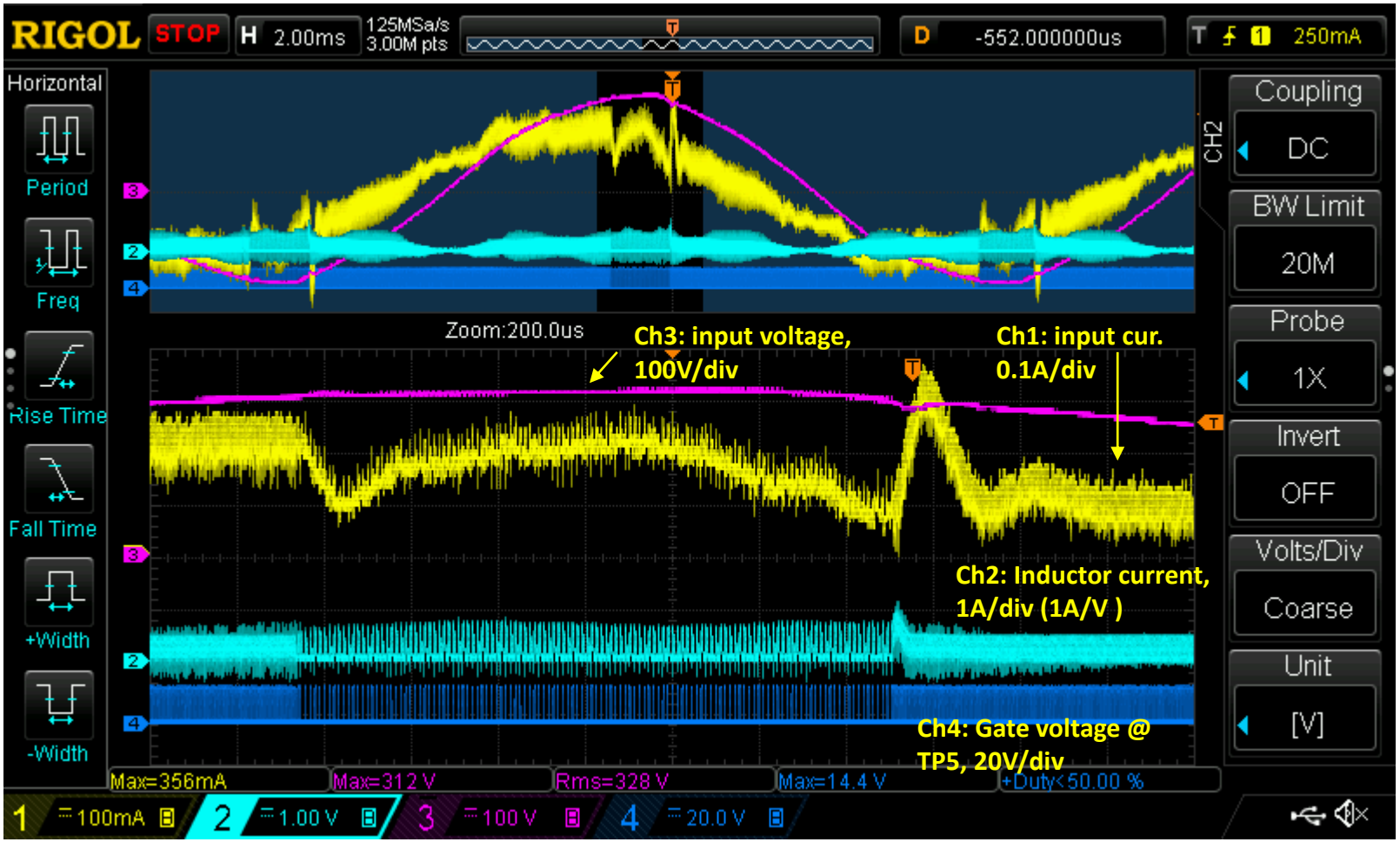
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

At around 230Vac, current distortions appear



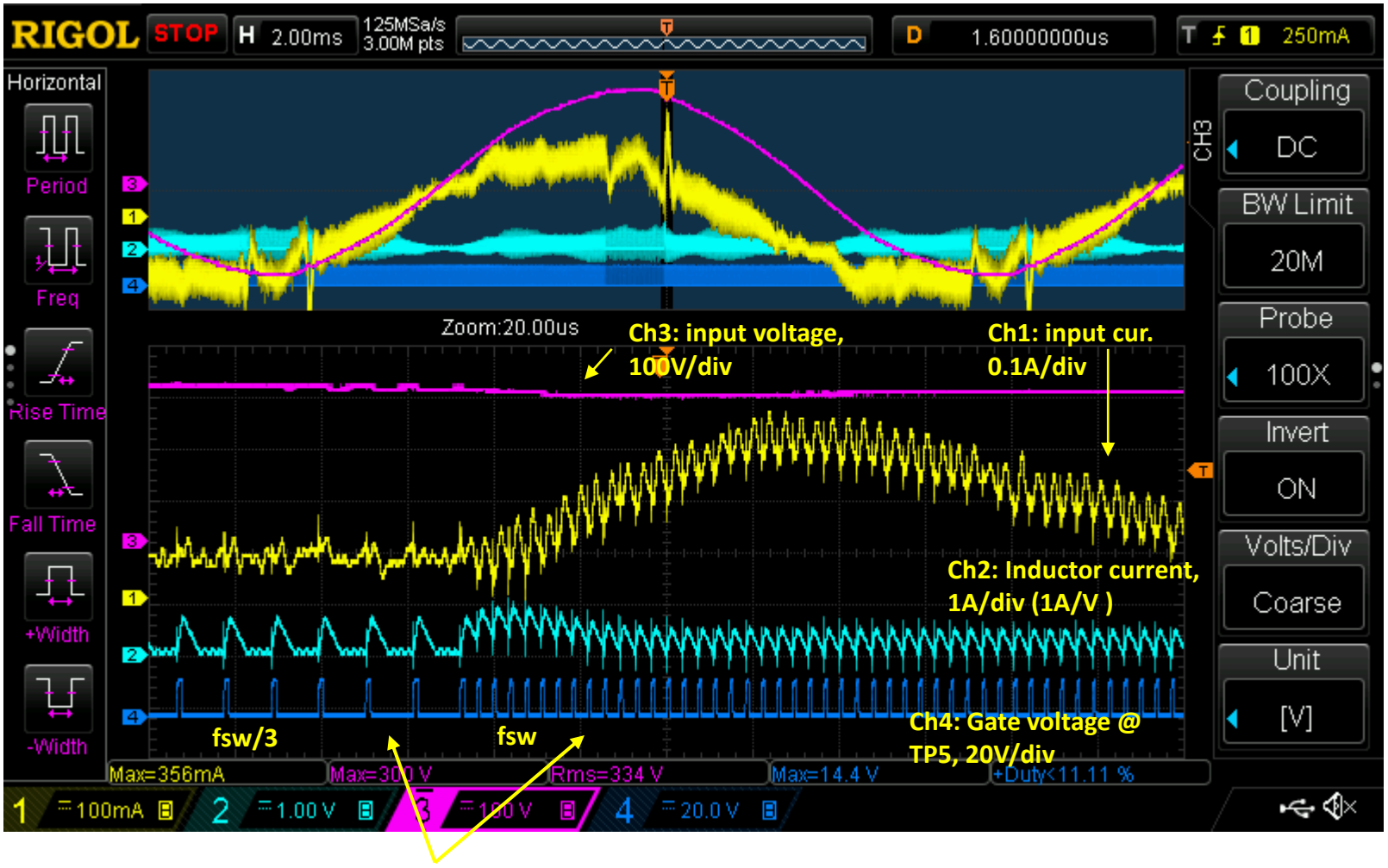
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

25W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

At around 230Vac, current distortions appear



Switching frequency was reduced to 1/3rd and then increased back; at which point current spike was observed

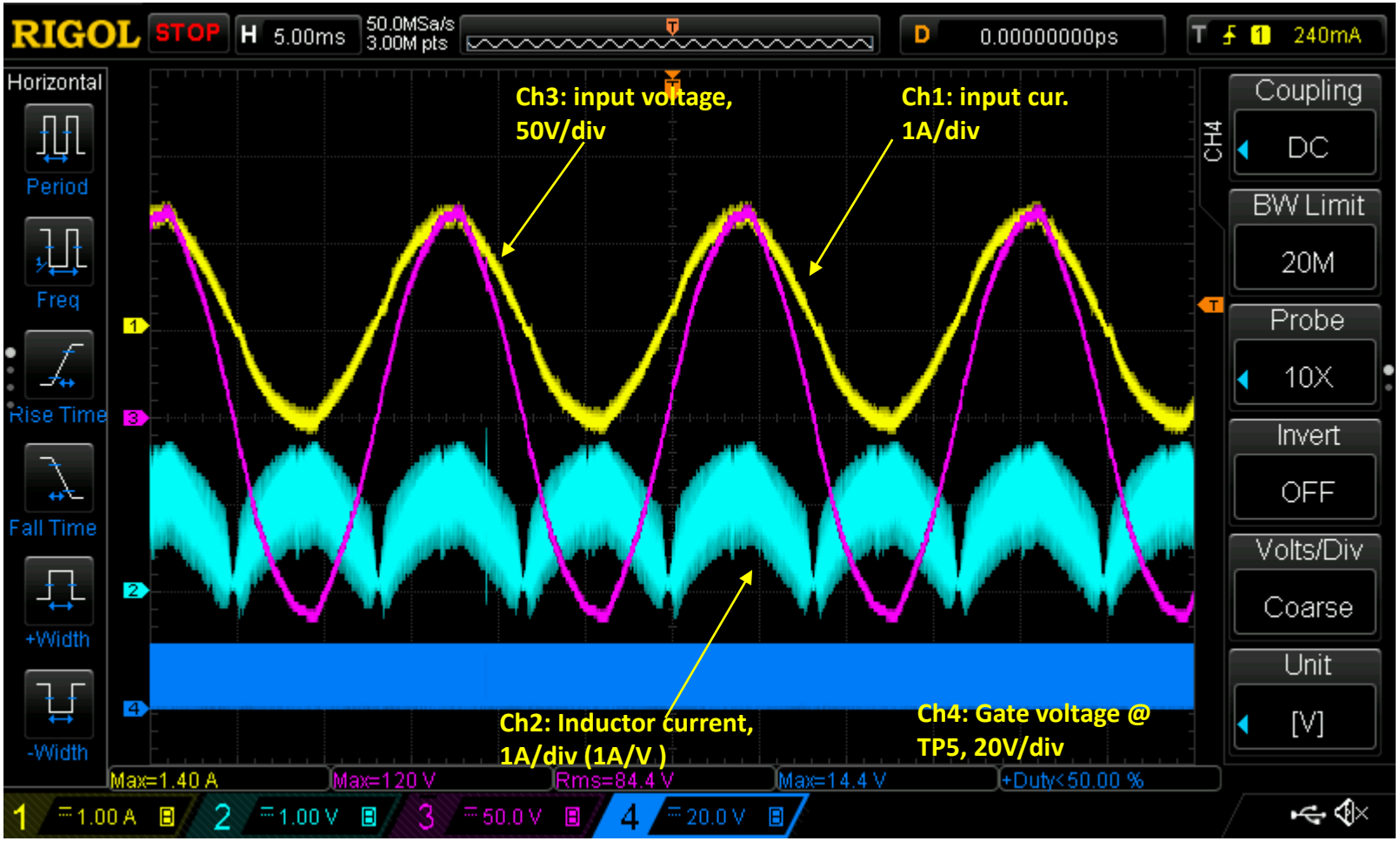
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 60W output power, no major distortions at 85Vac input



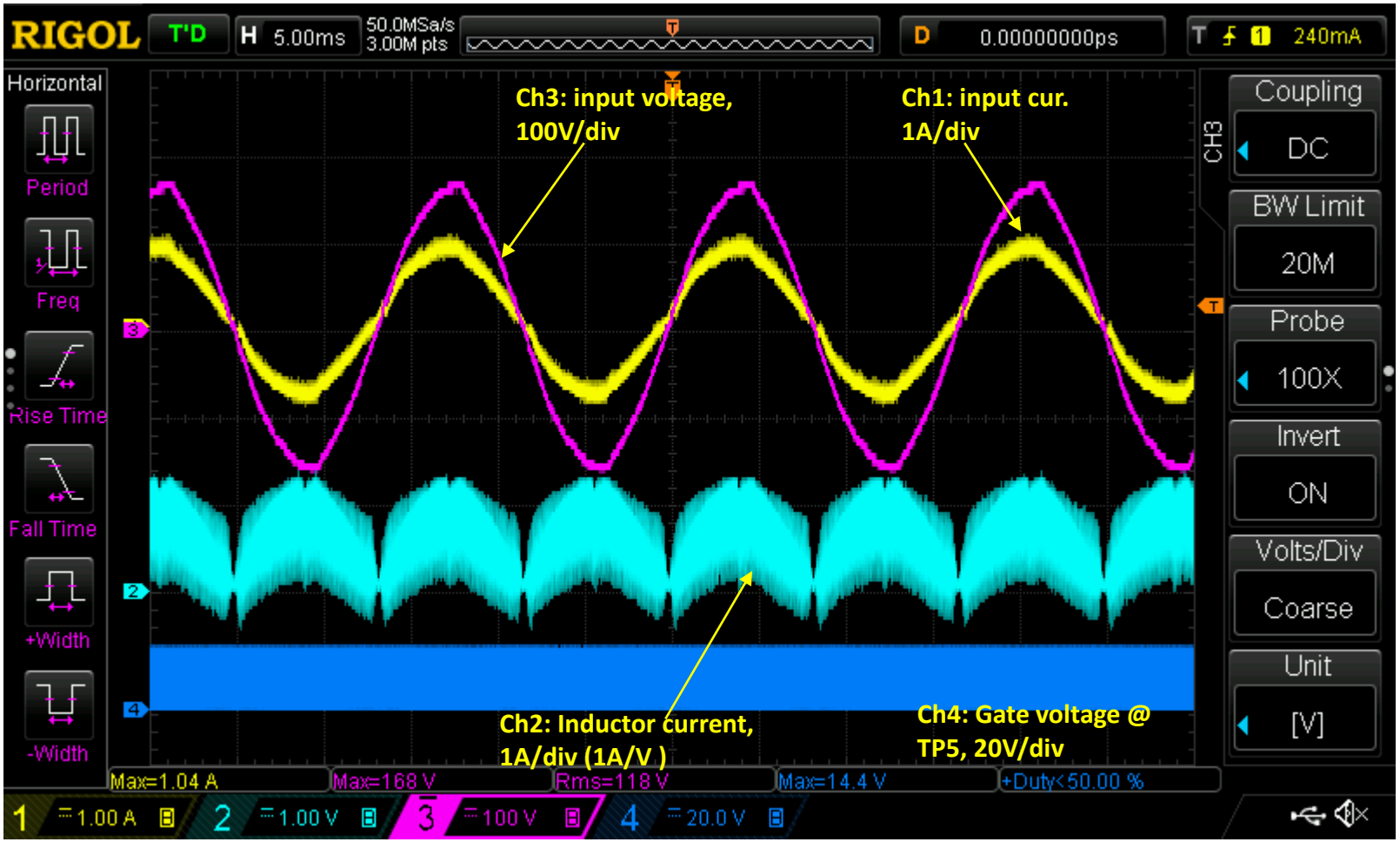
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 60W output power, no major distortions at 120Vac input



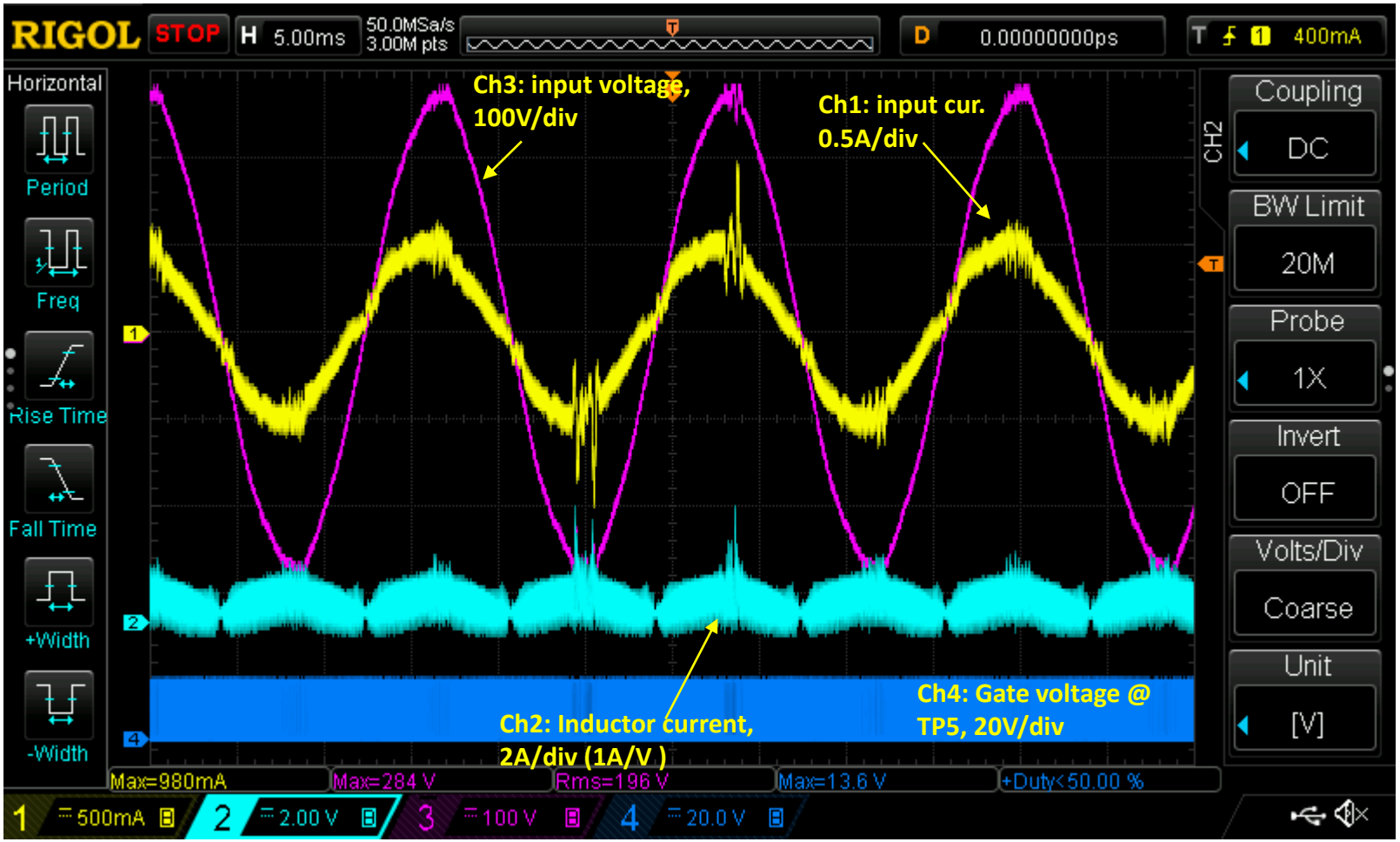
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 60W output power, major distortions at around 200Vac input (got worse)



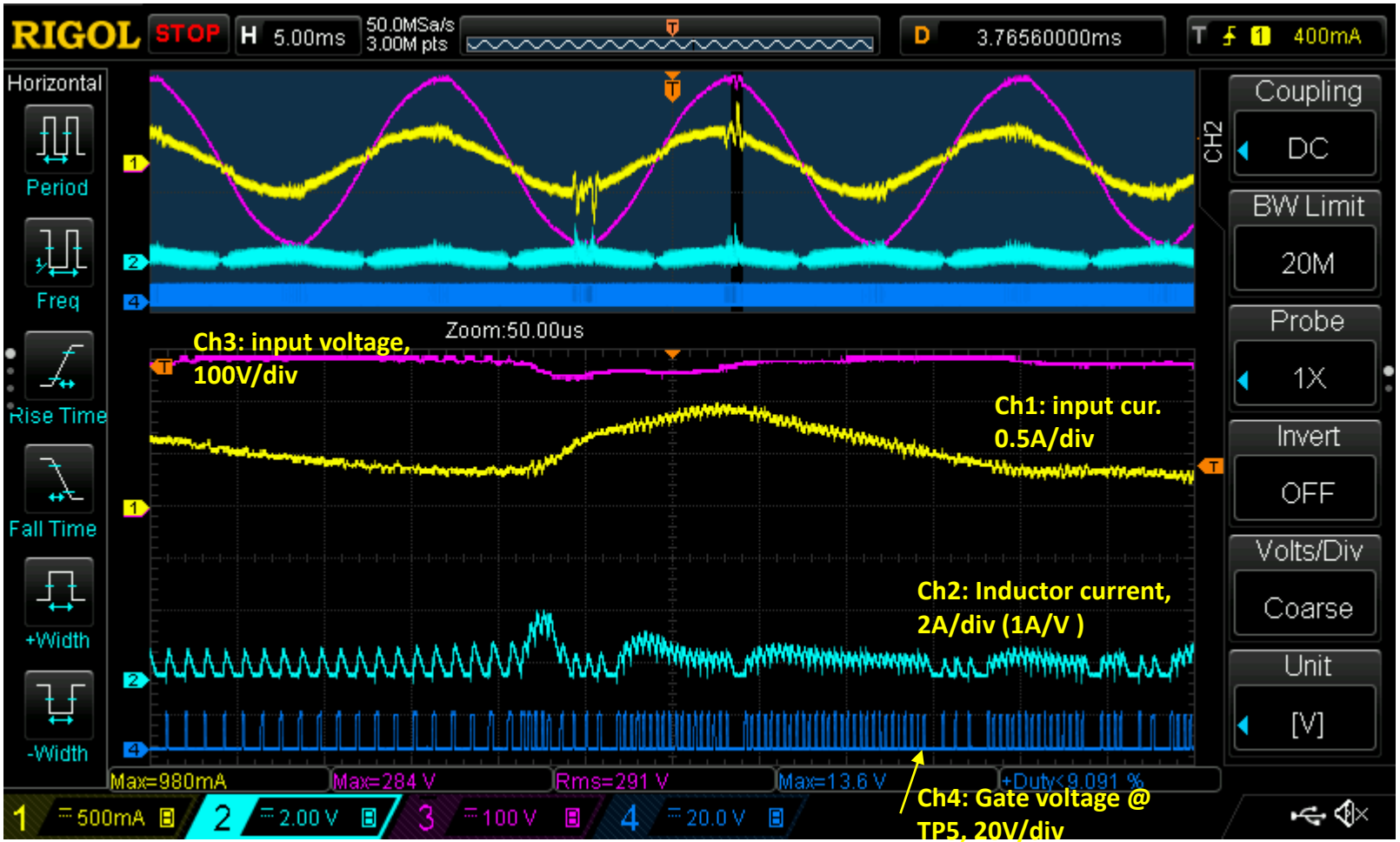
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

560uH toroid (2300LL-561-H-RC), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 60W output power, major distortions at around 200Vac input (got worse)



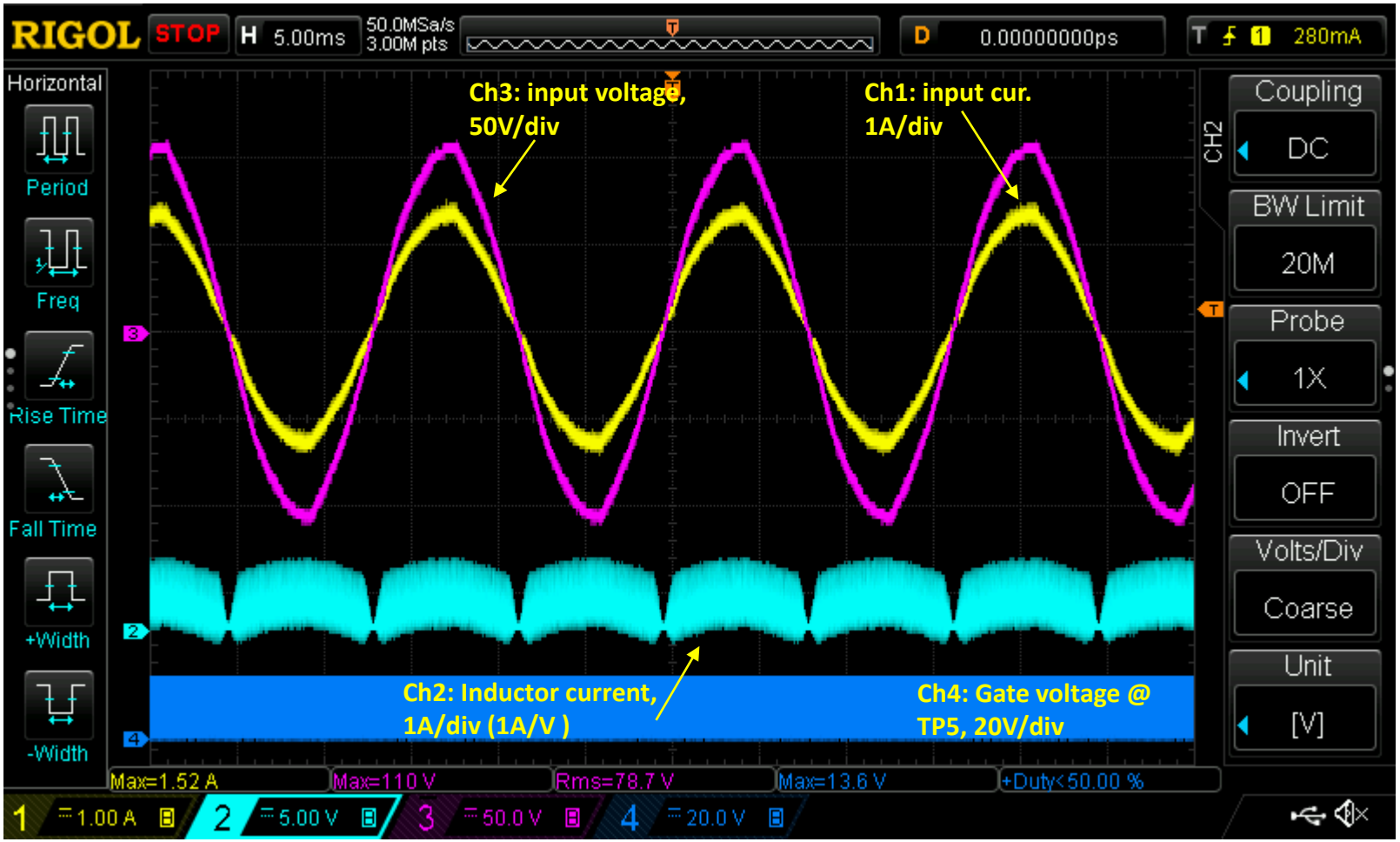
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor and 60W output power, no major distortions at 85Vac



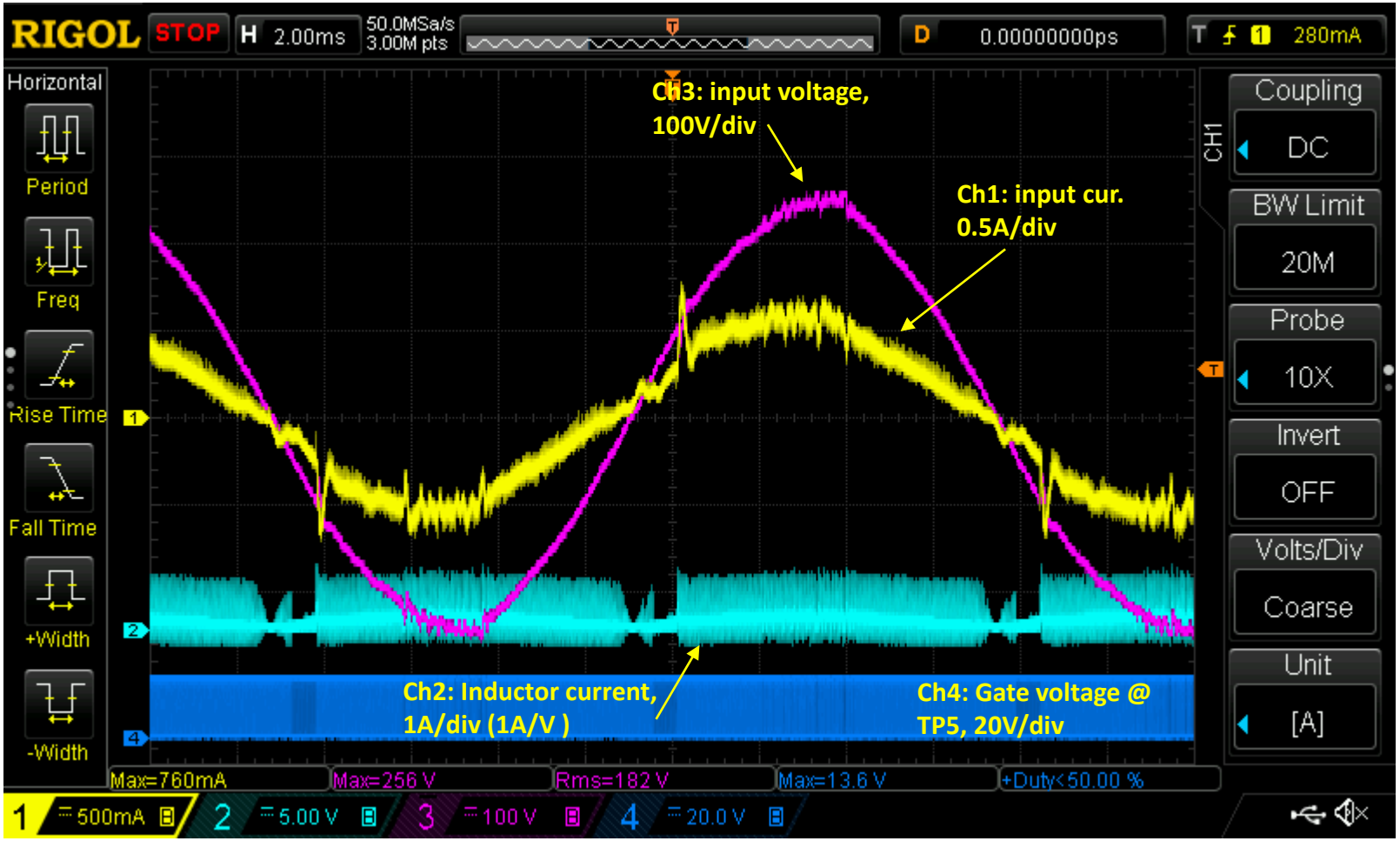
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor and 60W output power, distortions at slightly different locations started at even lower voltage, 180Vac



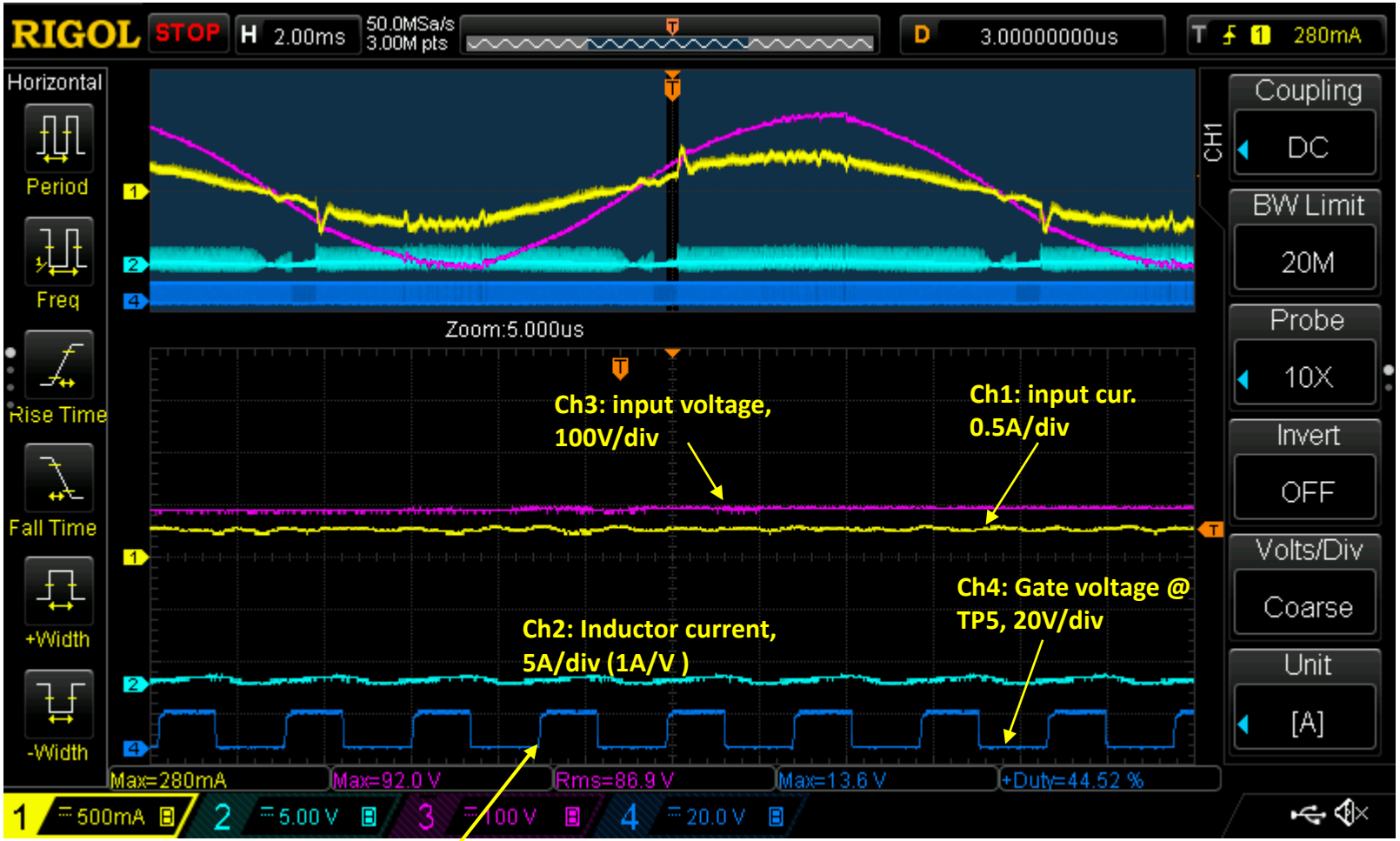
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor and 60W output power, distortions at slightly different locations started at even lower voltage, 180Vac



Switching frequency was reduced to fsw/s , duty cycle was ~50% prior to current spike

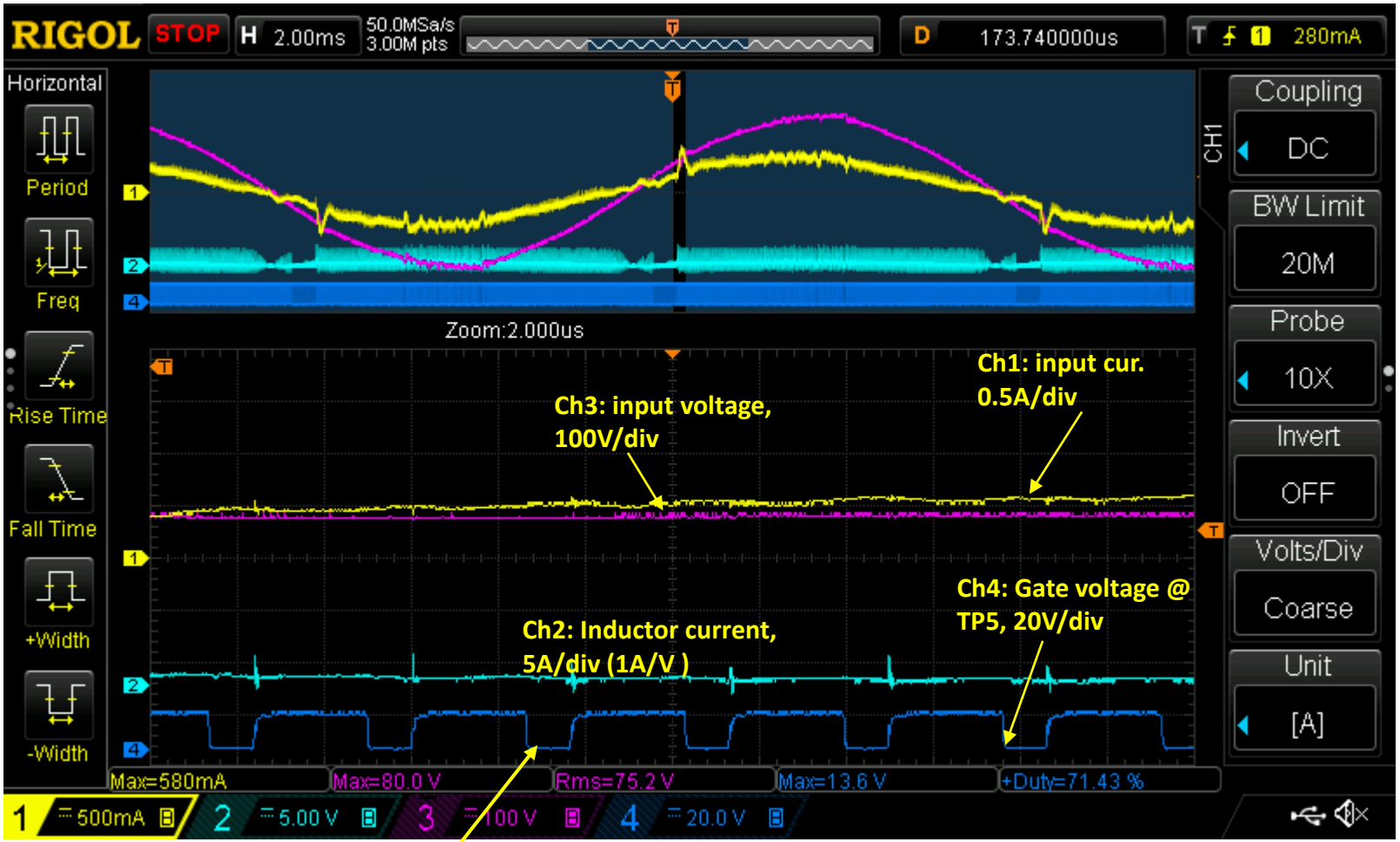
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor and 60W output power, distortions at slightly different locations started at even lower voltage, 180Vac



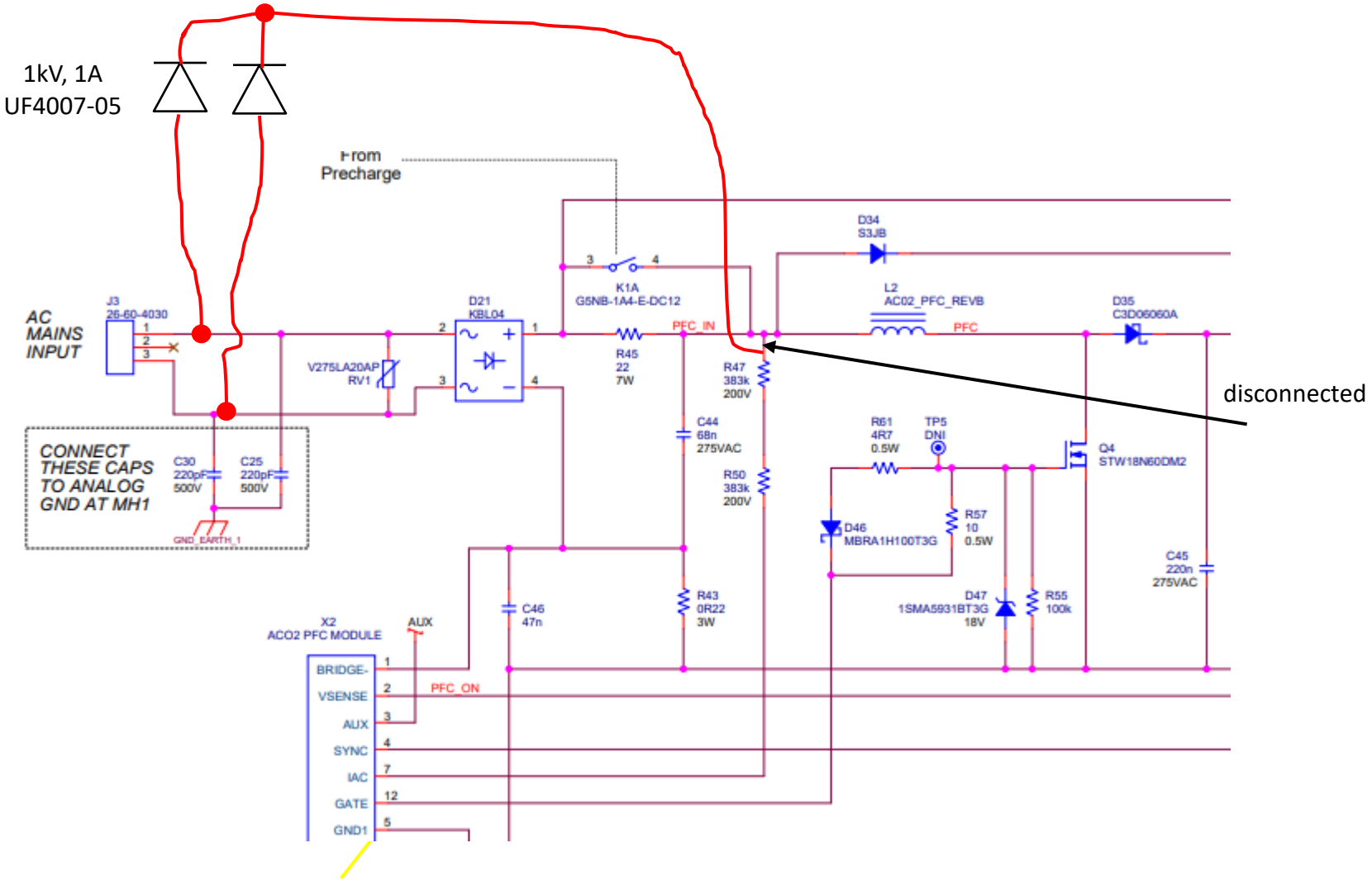
Switching frequency was increased back to fsw; at which point current spike was observed, duty cycle was about 70%

Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications



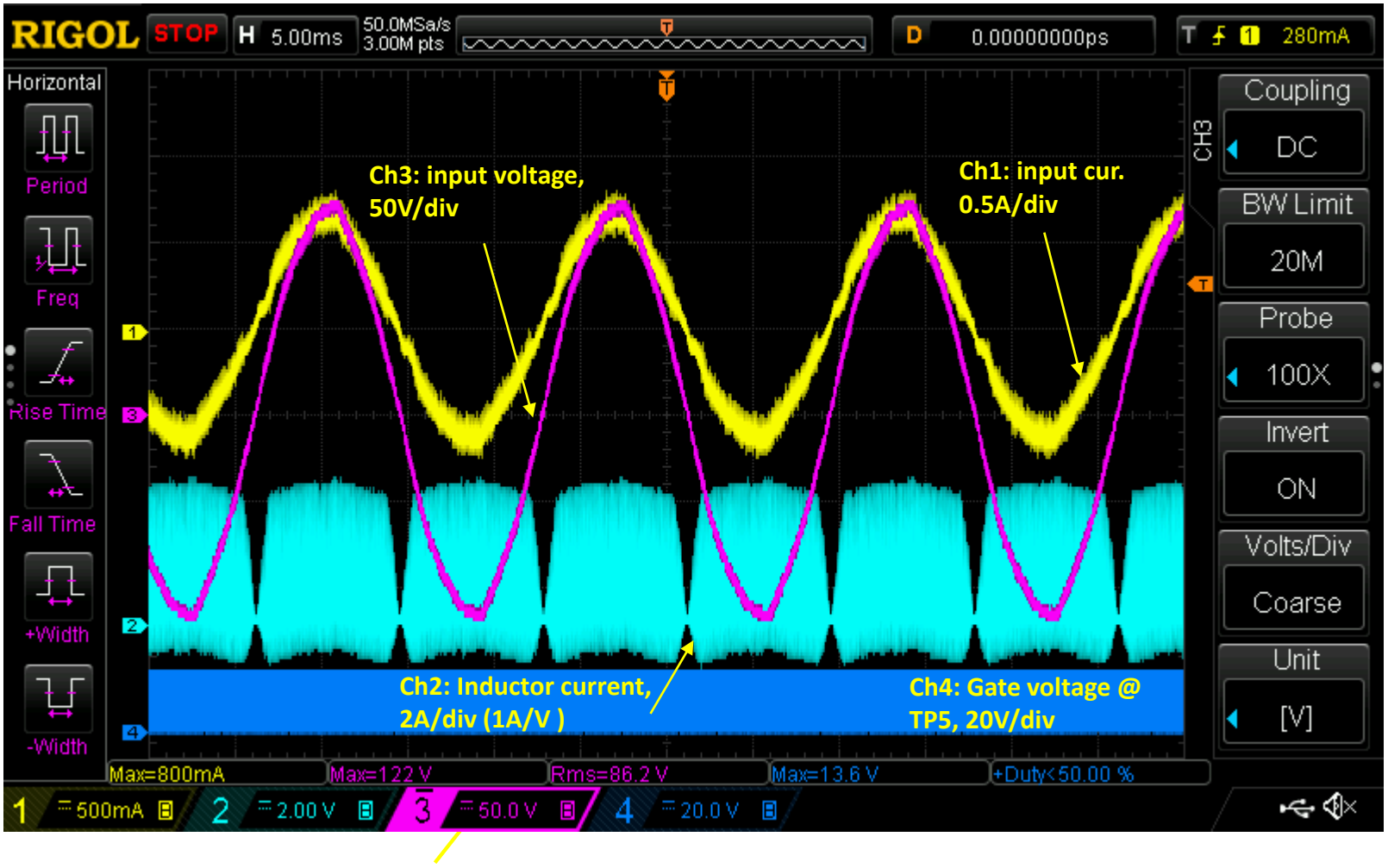
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, no major distortions at 85Vac



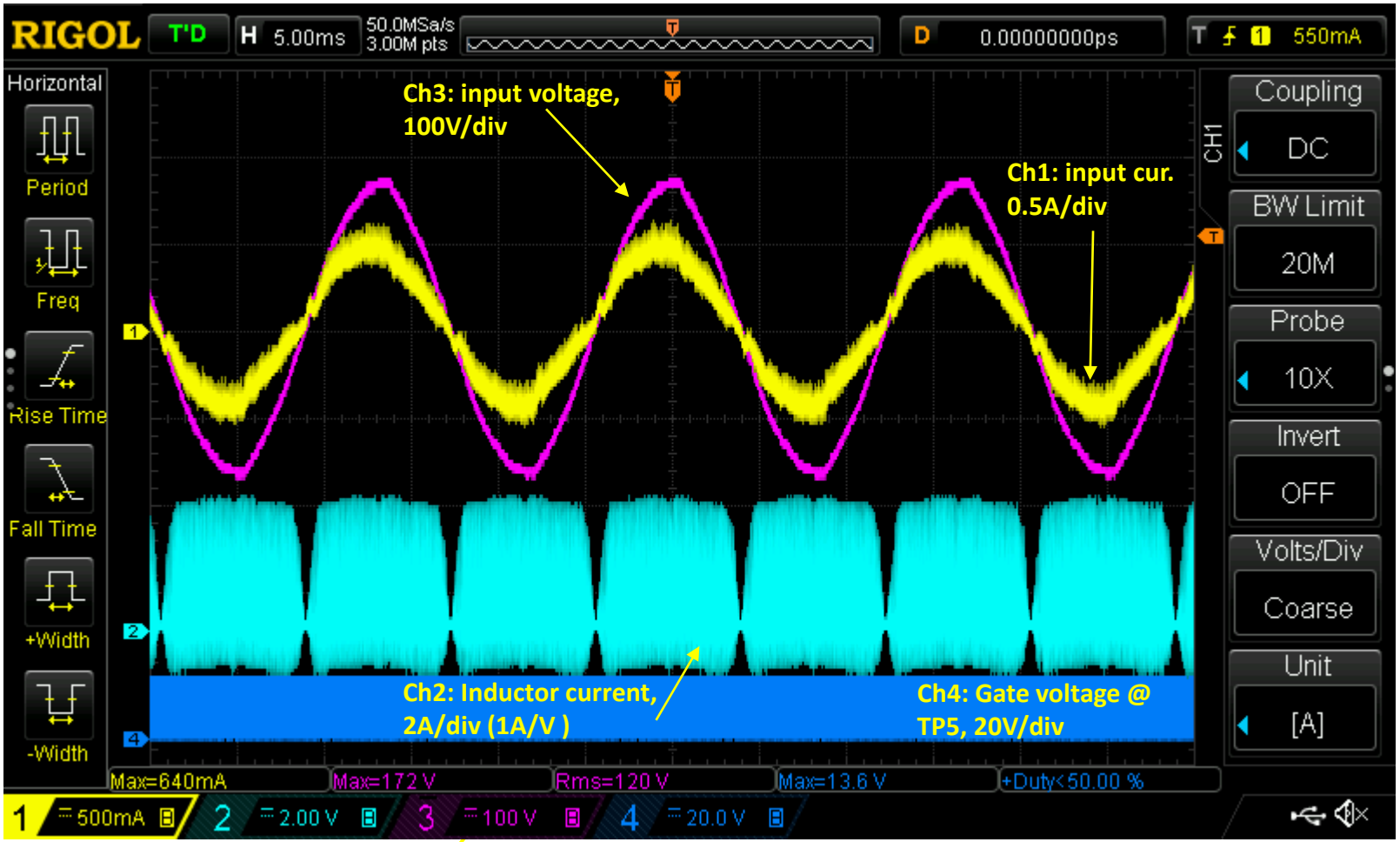
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, no major distortions at 120Vac



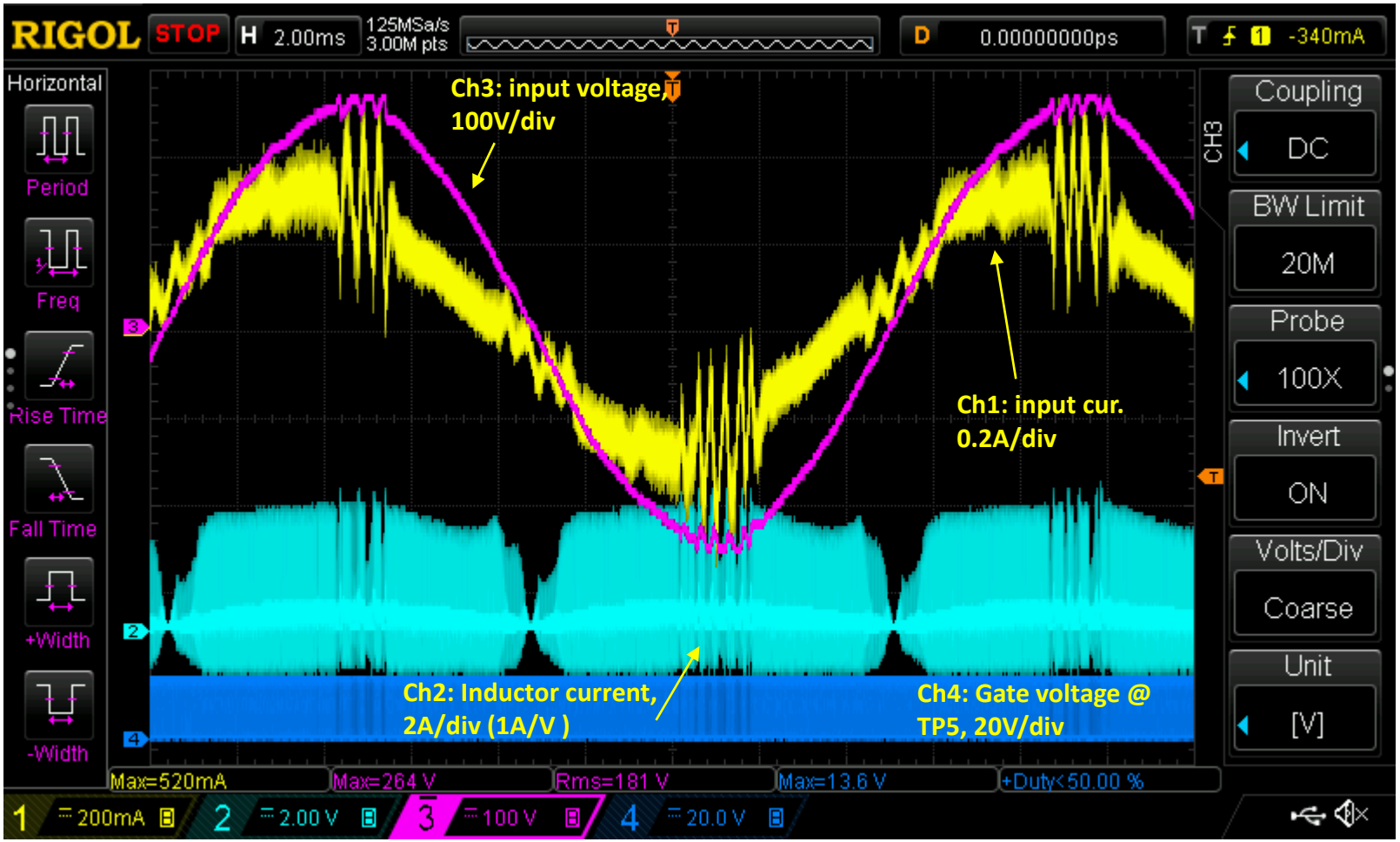
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, major distortions at 180Vac



Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, major distortions at 180Vac

Switching frequency was normal and duty cycle was about 32%
(notice that the on-time was constant)

Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, major distortions at 180Vac

Switching frequency was reduced to fsw/2 and duty cycle was about 16%
(notice that the on-time was constant)

Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

30W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power and Iac connection moved to input of rectifier, major distortions at 180Vac

About 3.3kHz current oscillations

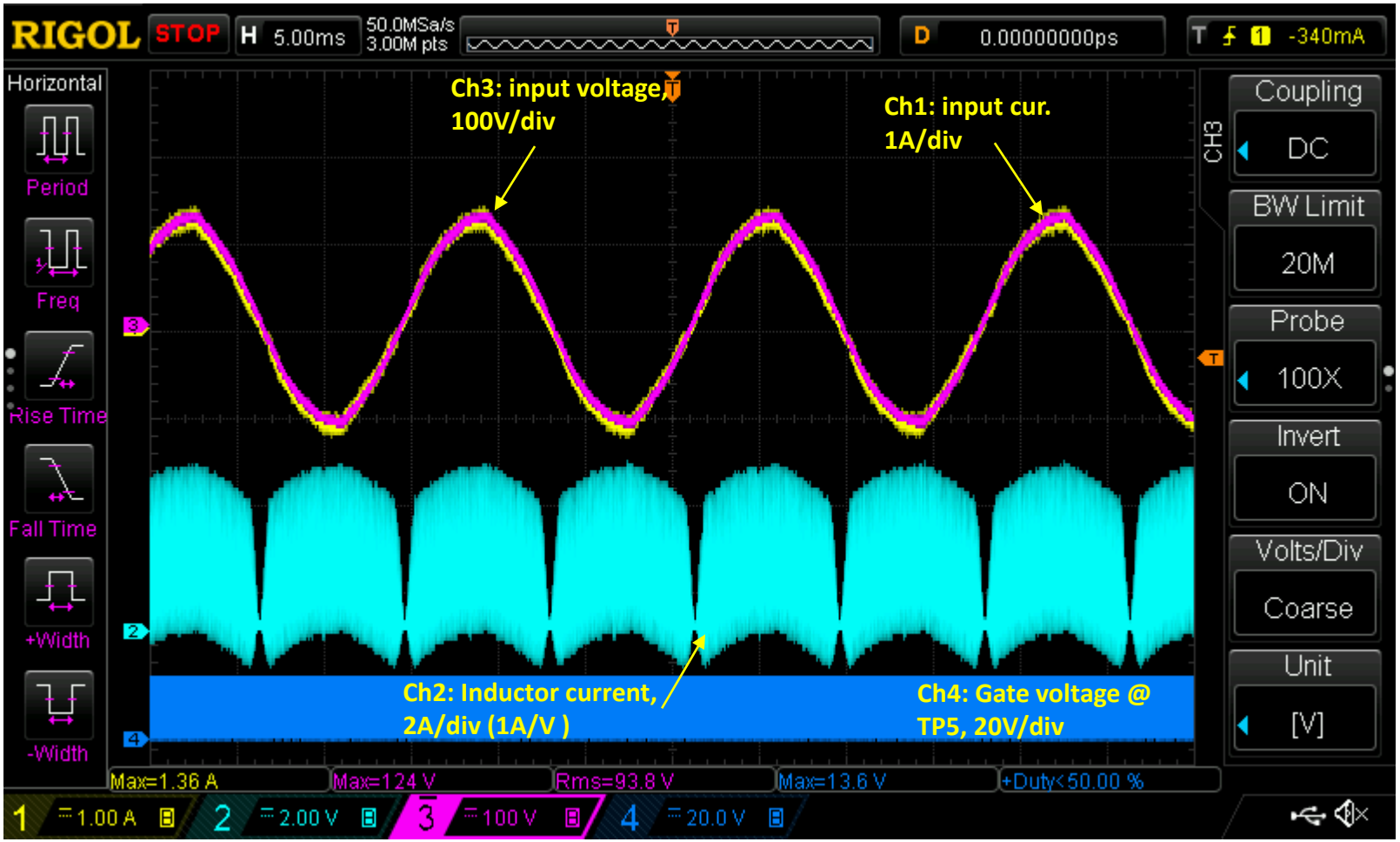
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 60W output power and Iac connection moved to input of rectifier, no major distortions at 85Vac



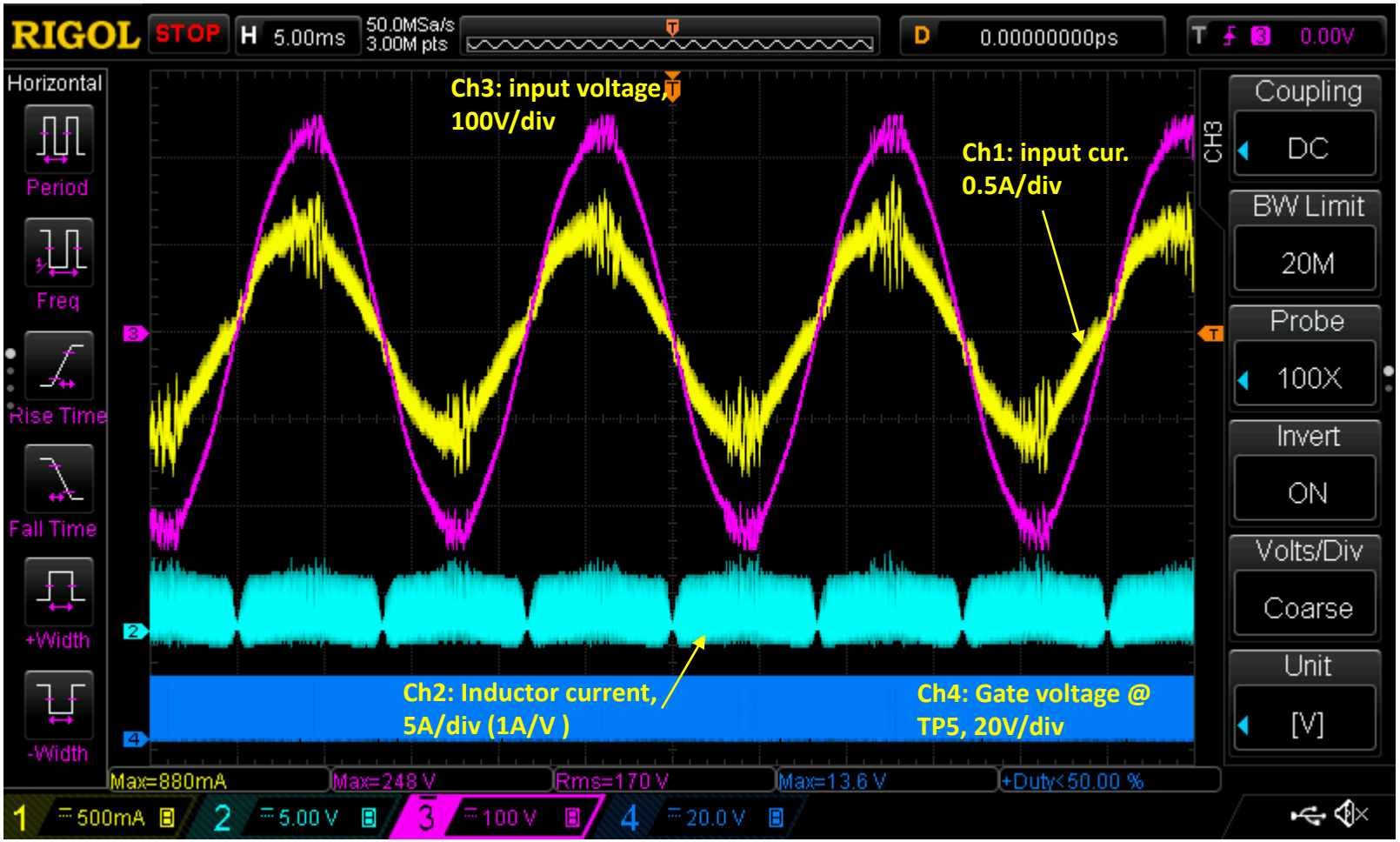
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 60W output power and Iac connection moved to input of rectifier, major distortions at ~180Vac



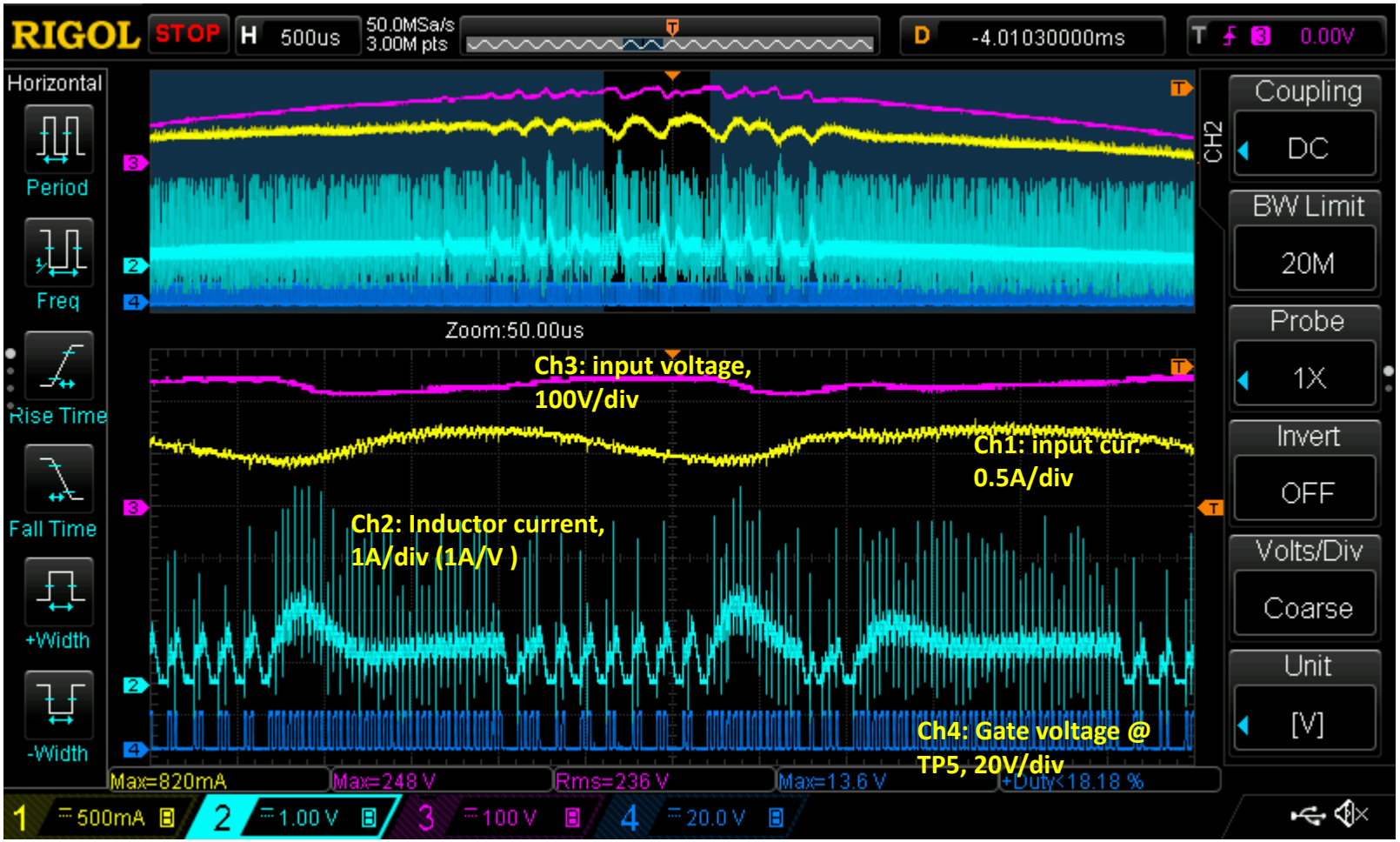
Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 60W output power and Iac connection moved to input of rectifier, major distortions at ~180Vac



Same phenomenon observed; switching frequency was reduced and then increased, at which time current spike was observed

Measuring inductor current vs gate voltages, 2/12/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

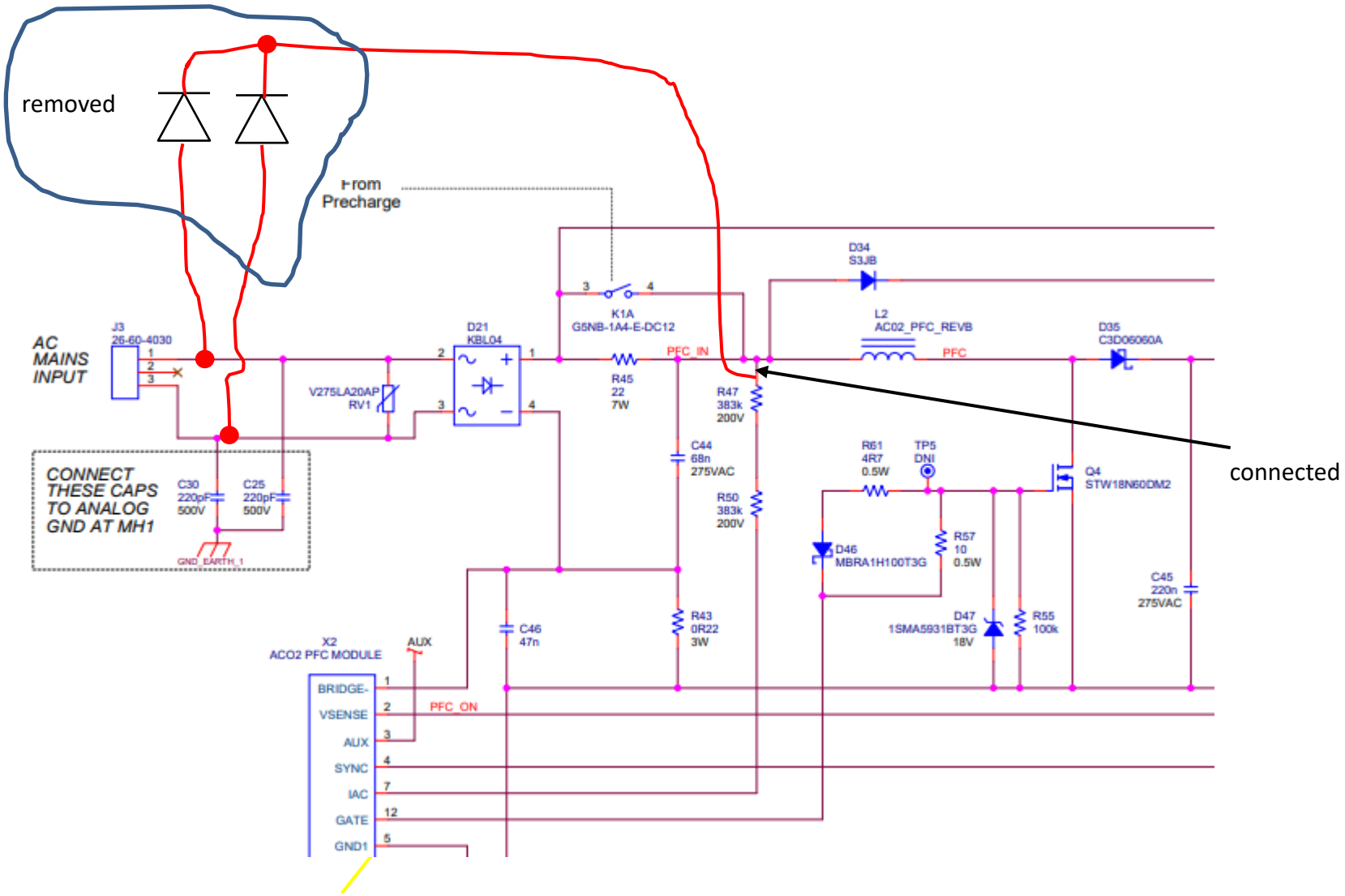
60W external load across the DC-link

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

Conclusions as of 2/12:

1) Changes on slide 107 were implemented; load was changed from 25W to 60W and inductance with lower inter-winding capacitance was tried out. No change
2) Iac sense point was moved to input of rectifier. Tried with different loads and inductors; the nature of distortion appears to change and the voltage at which distortions begins was lowered; so it got worse.

Measuring inductor current vs gate voltages, 2/19/2023



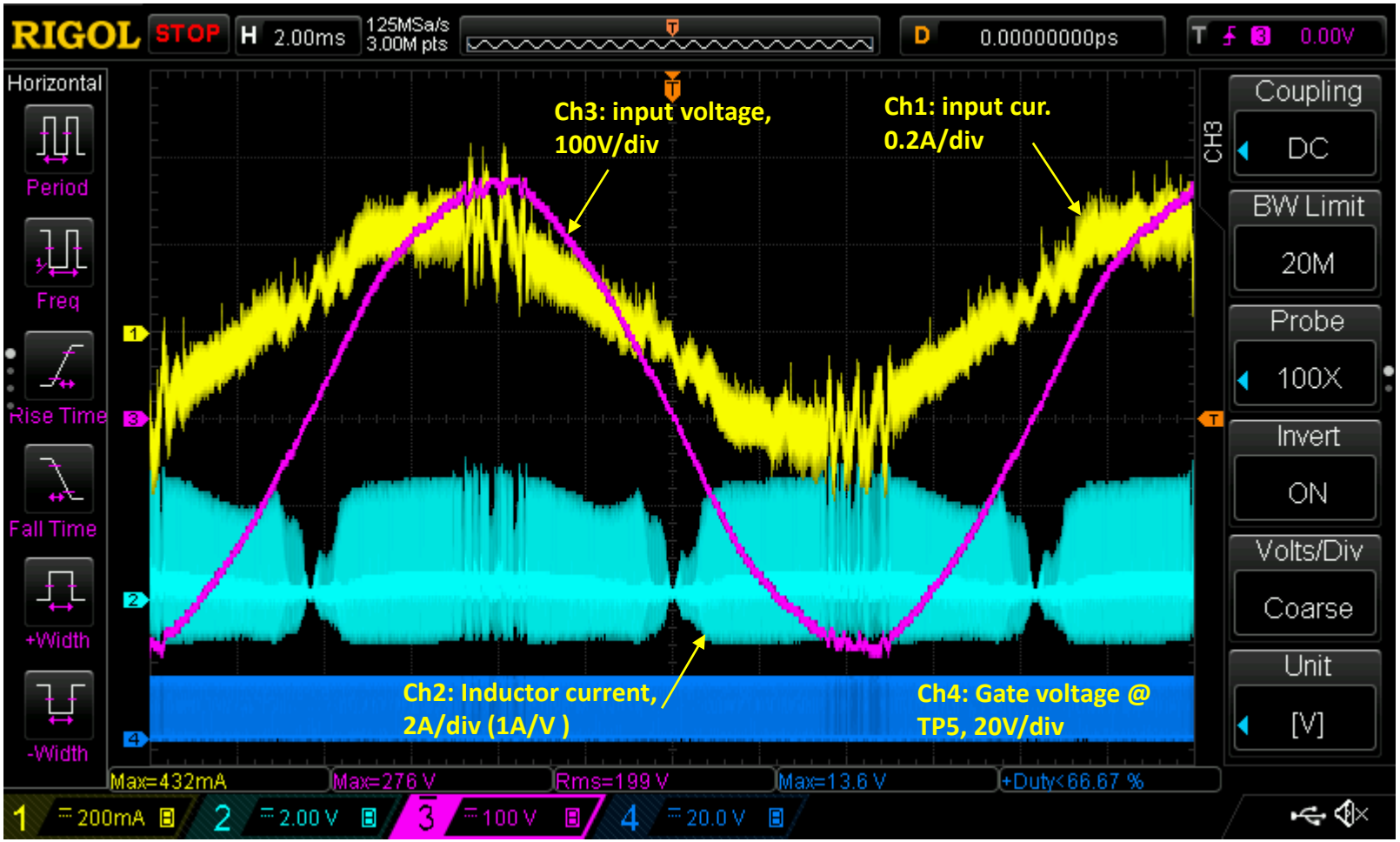
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

Original boost inductor (680uH), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With original inductor, 30W output power major distortions start above 200Vac



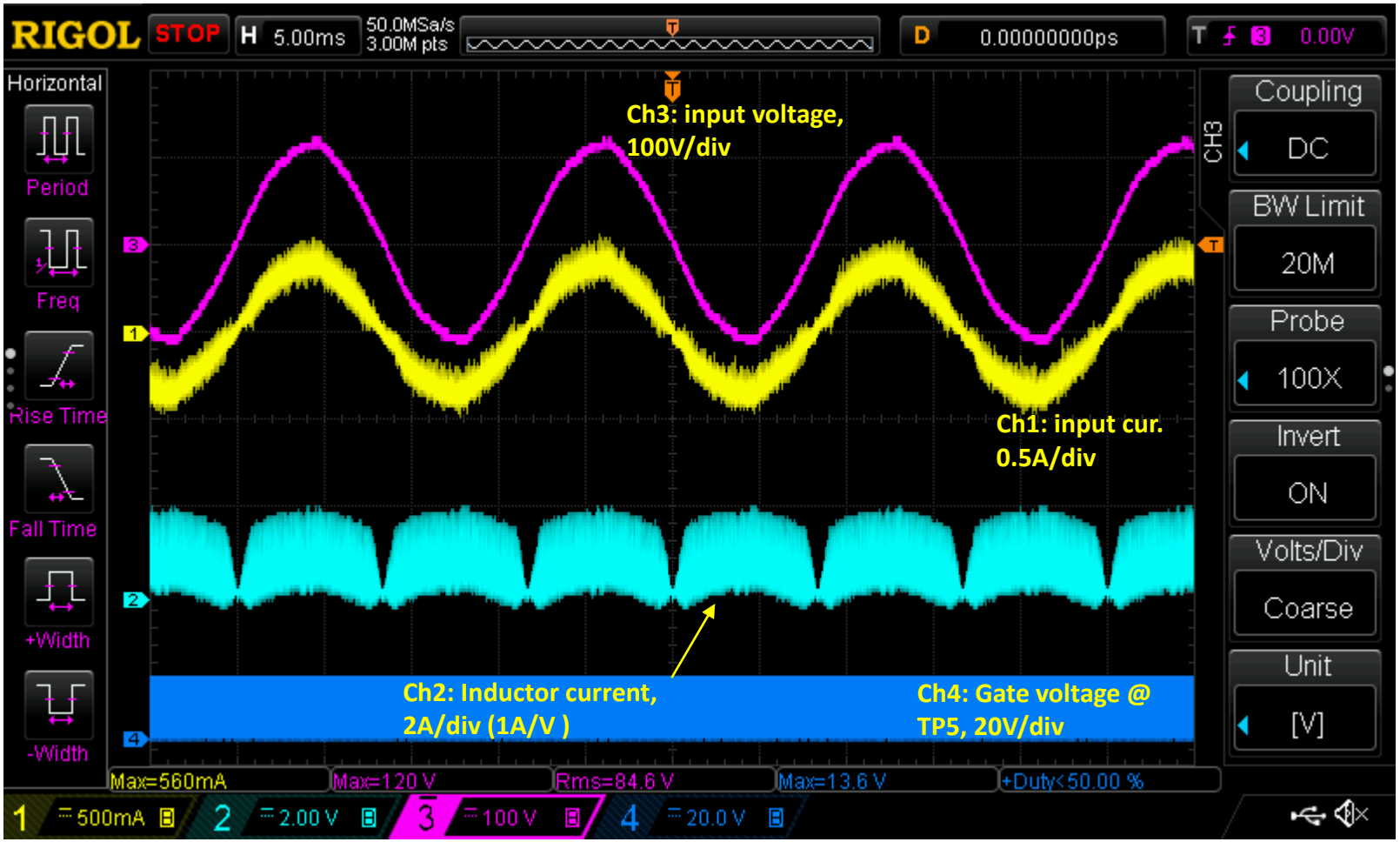
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, no distortions at 85Vac



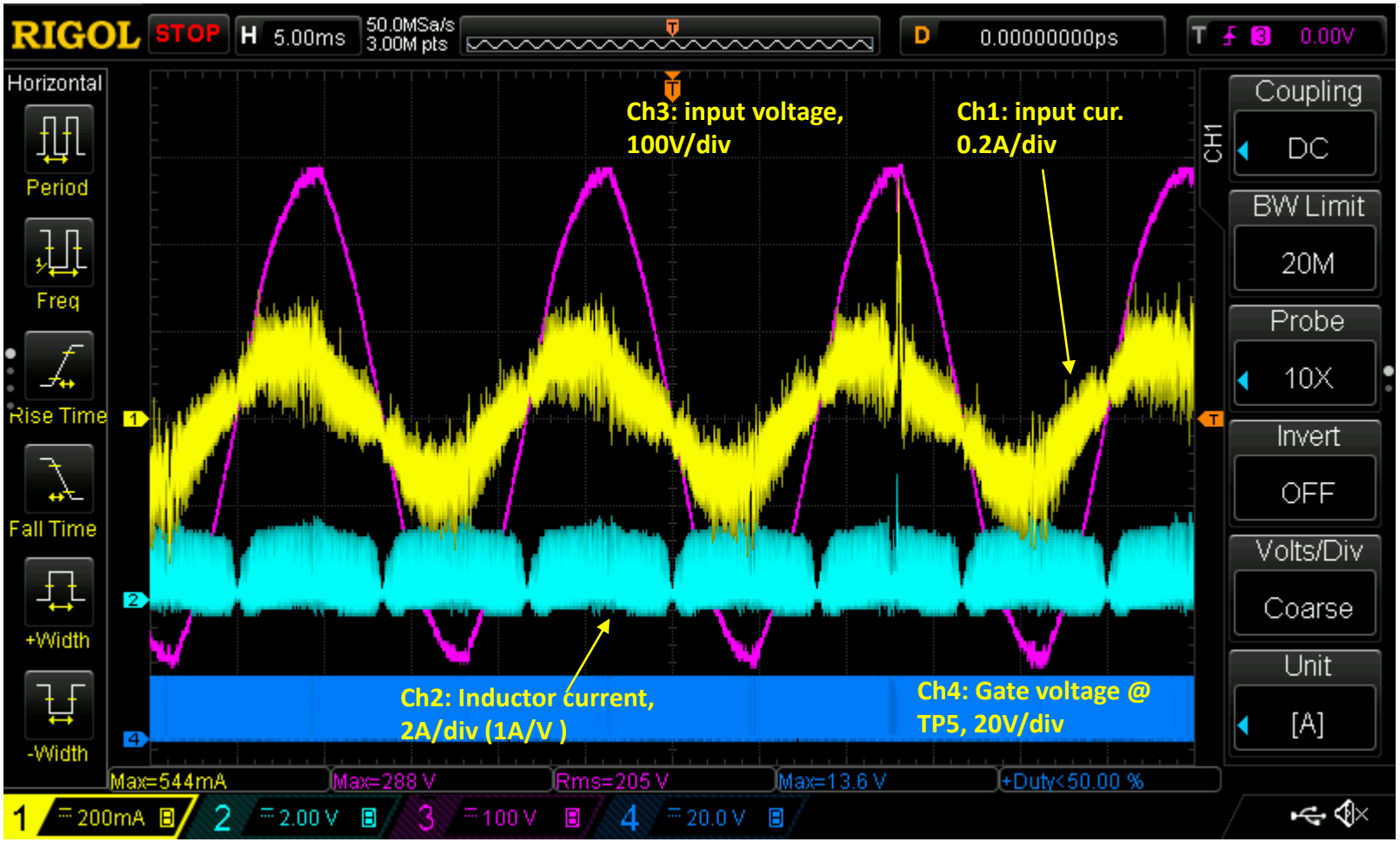
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, non-periodic distortions start to appear at 200Vac



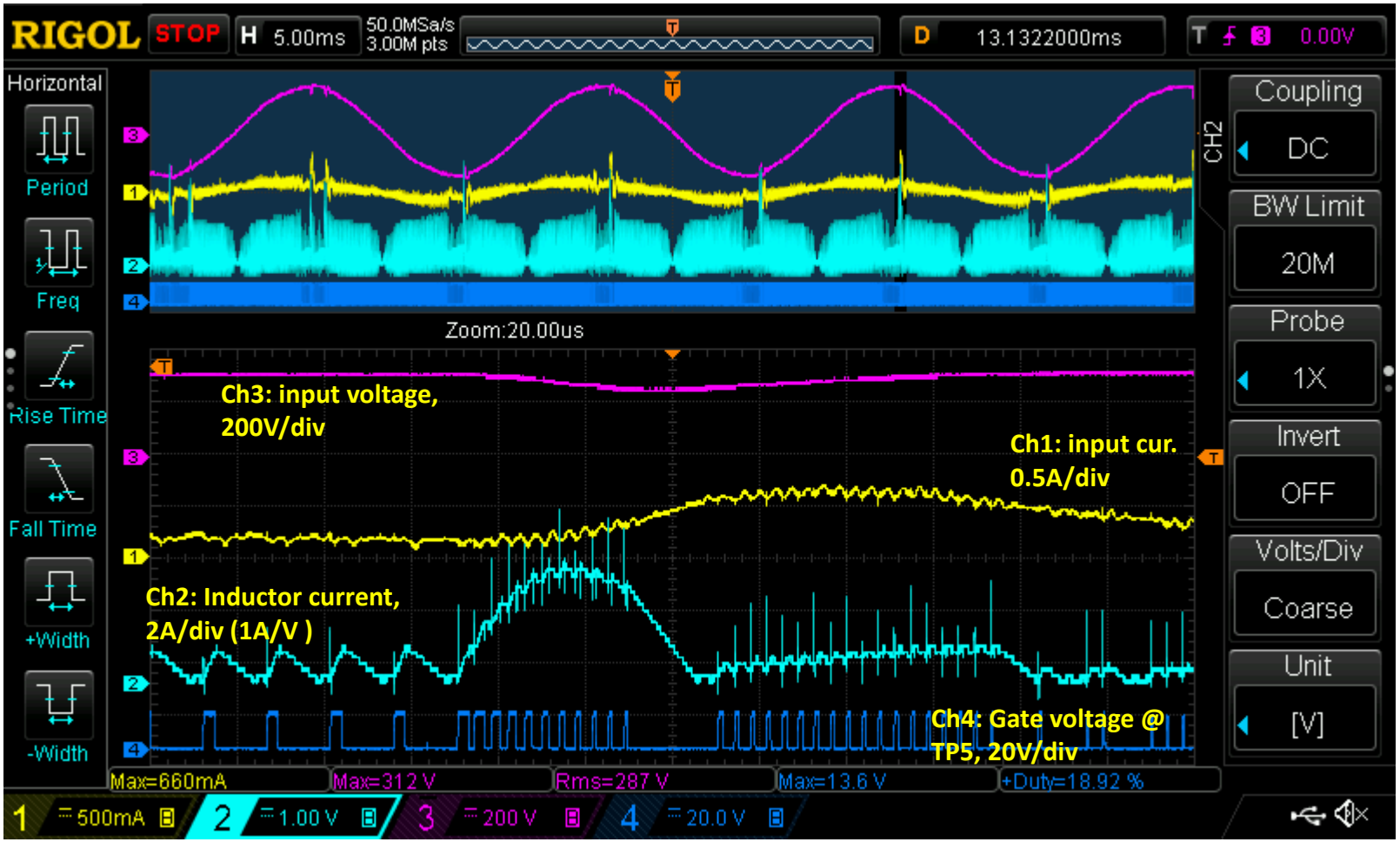
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, periodic distortions start to appear at 210Vac, note: Vdc_out=380V



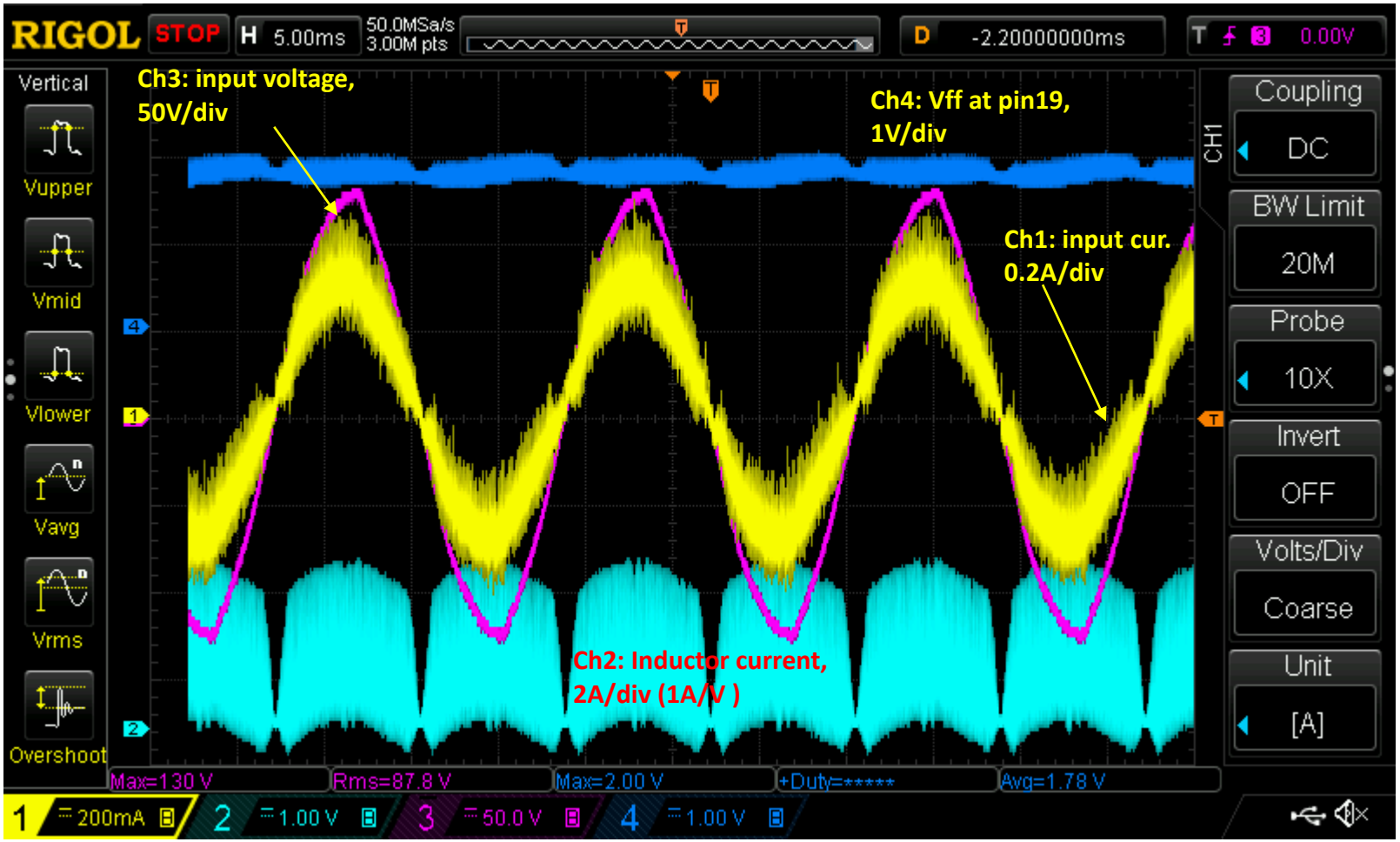
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, no distortions at 85Vac, Vff=1.78V w/ differential probe



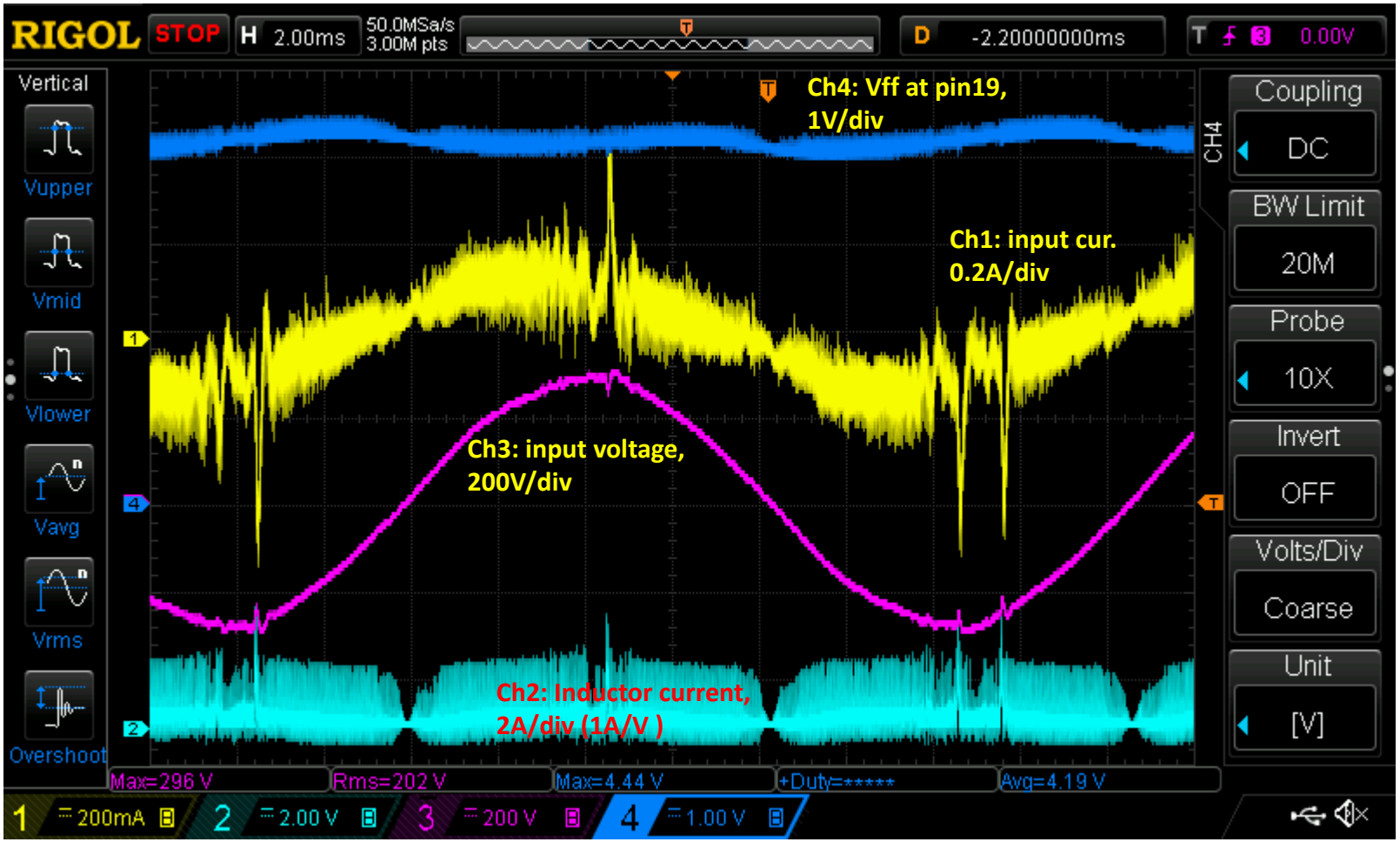
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, distortions at 200Vac, Vff=4.19V w/ differential probe



Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, distortions at 200Vac, Vff=4.19V w/ differential probe
It looks like differential probe has some DC offset at low voltages. Vff is also measured with a DVM, Fluke 179, by removing differential probe

Input voltage (Vrms)	Vff @ pin19 (Vdc) w/ differential probe	Vff @ pin19 (Vdc) w/ DVM
85	1.78	1.46
120		2.11
200	4.19	3.50
220		3.85

Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 30W output power, distortions at 220Vac, Vff=3.85V w/ DVM

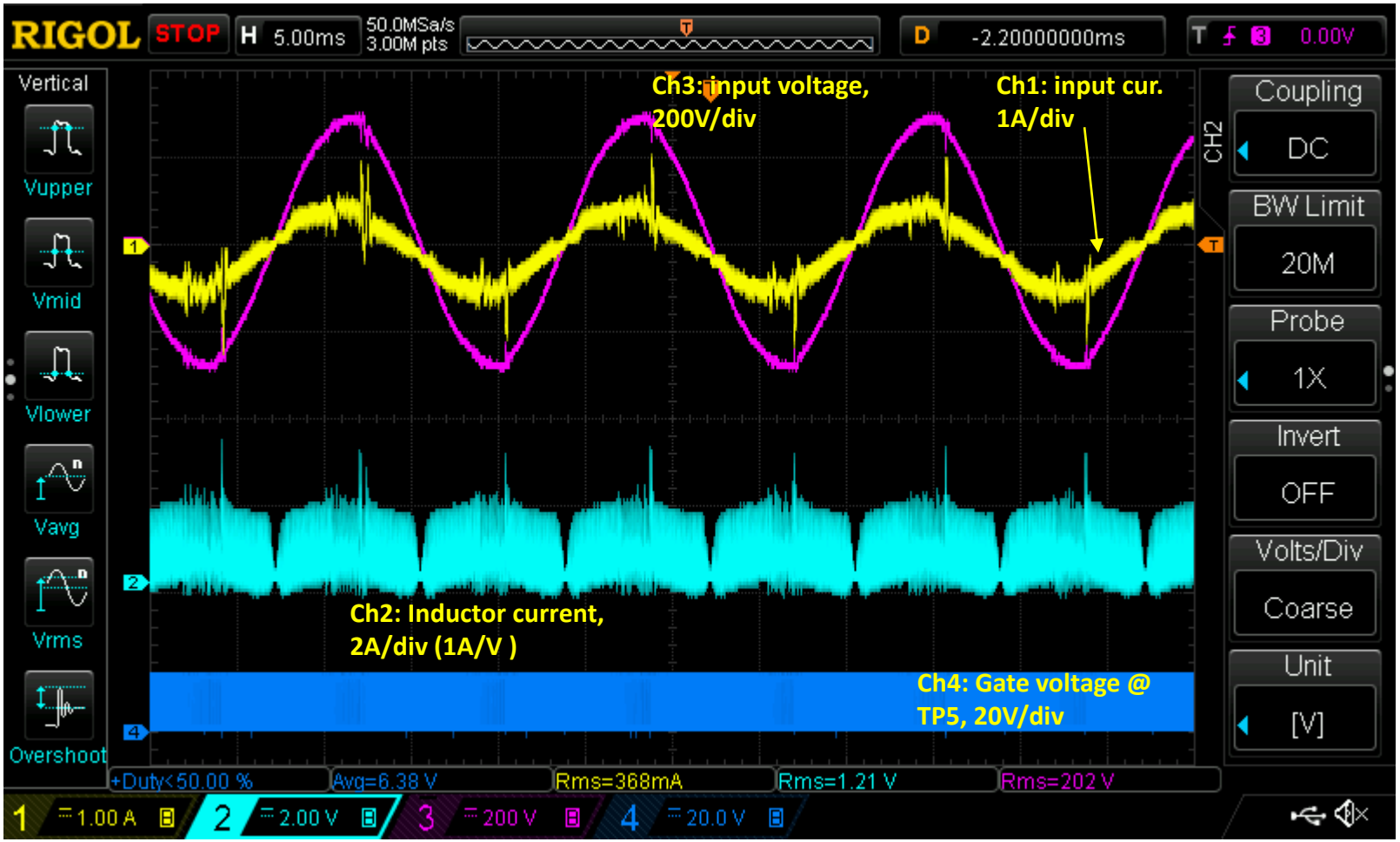
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **60W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 60W output power, distortions at 200Vac, Vff=3.45V w/ DVM



Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **60W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 60W output power, distortions at 200Vac, Vff=3.45V w/ DVM

Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **60W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 60W output power, distortions at 220Vac, Vff=3.79V w/ DVM

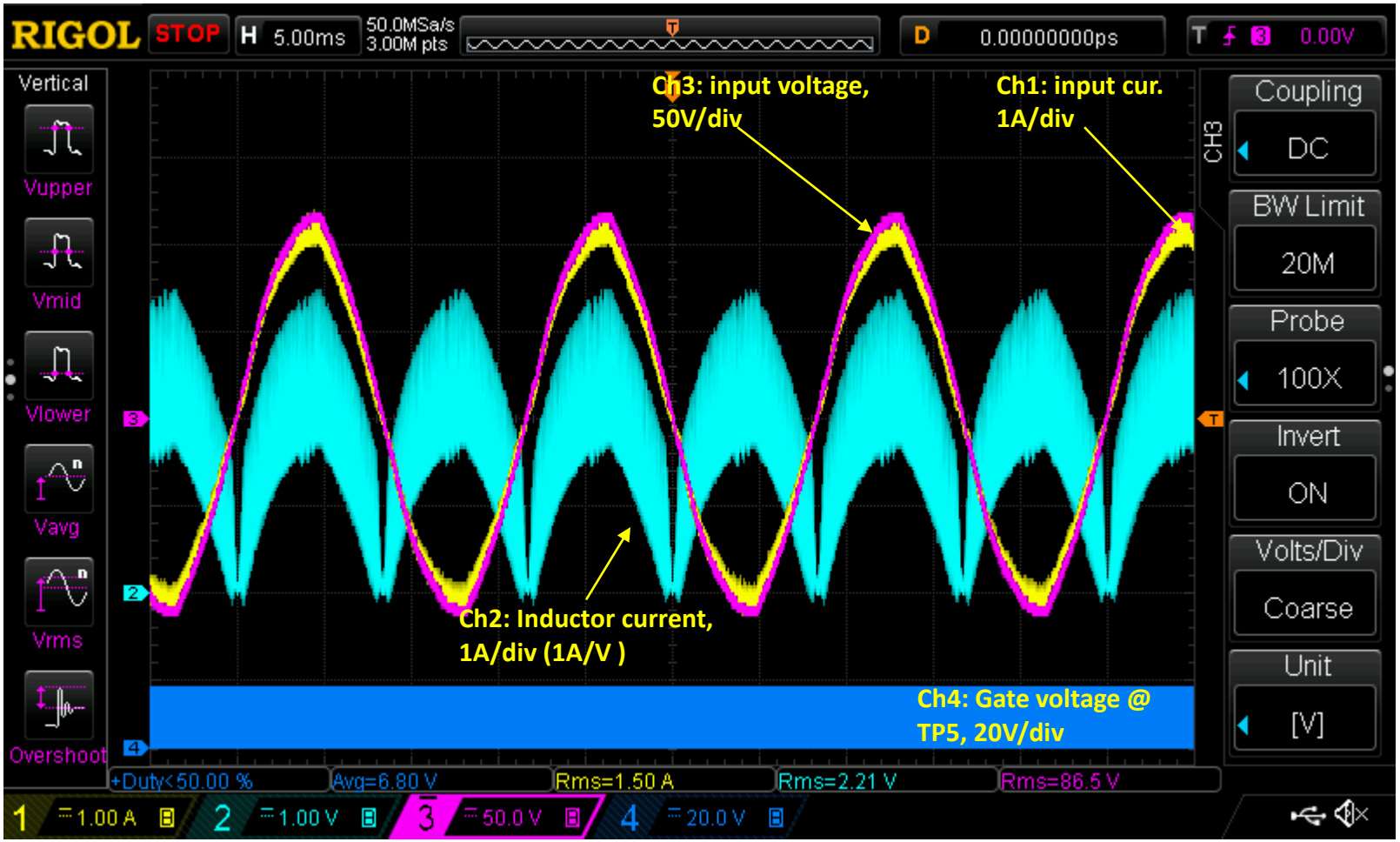
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 85Vac; (Vdc_out=355V maybe due to 2x input inductor and low input voltage)



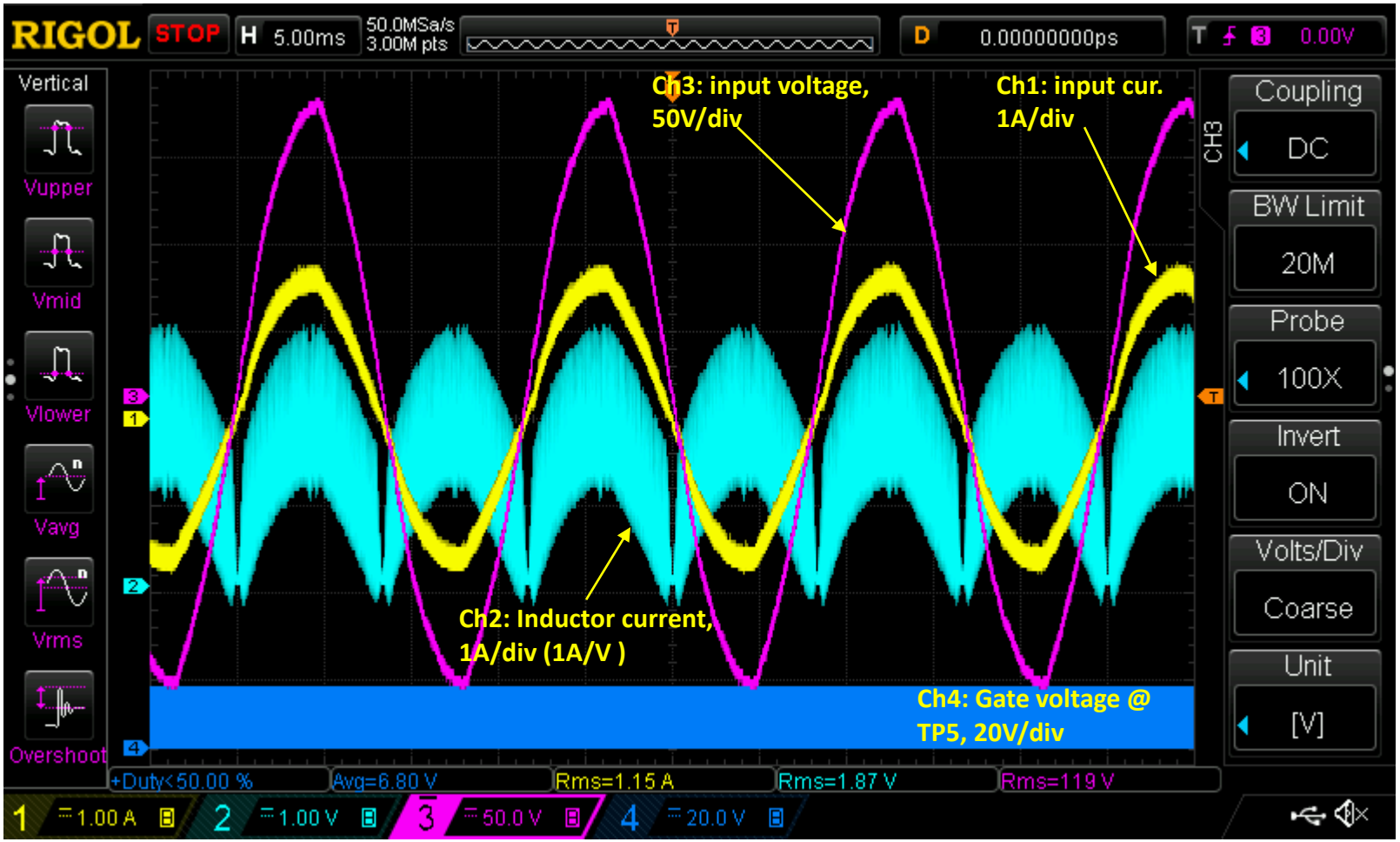
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 120Vac, Vdc_out=380V



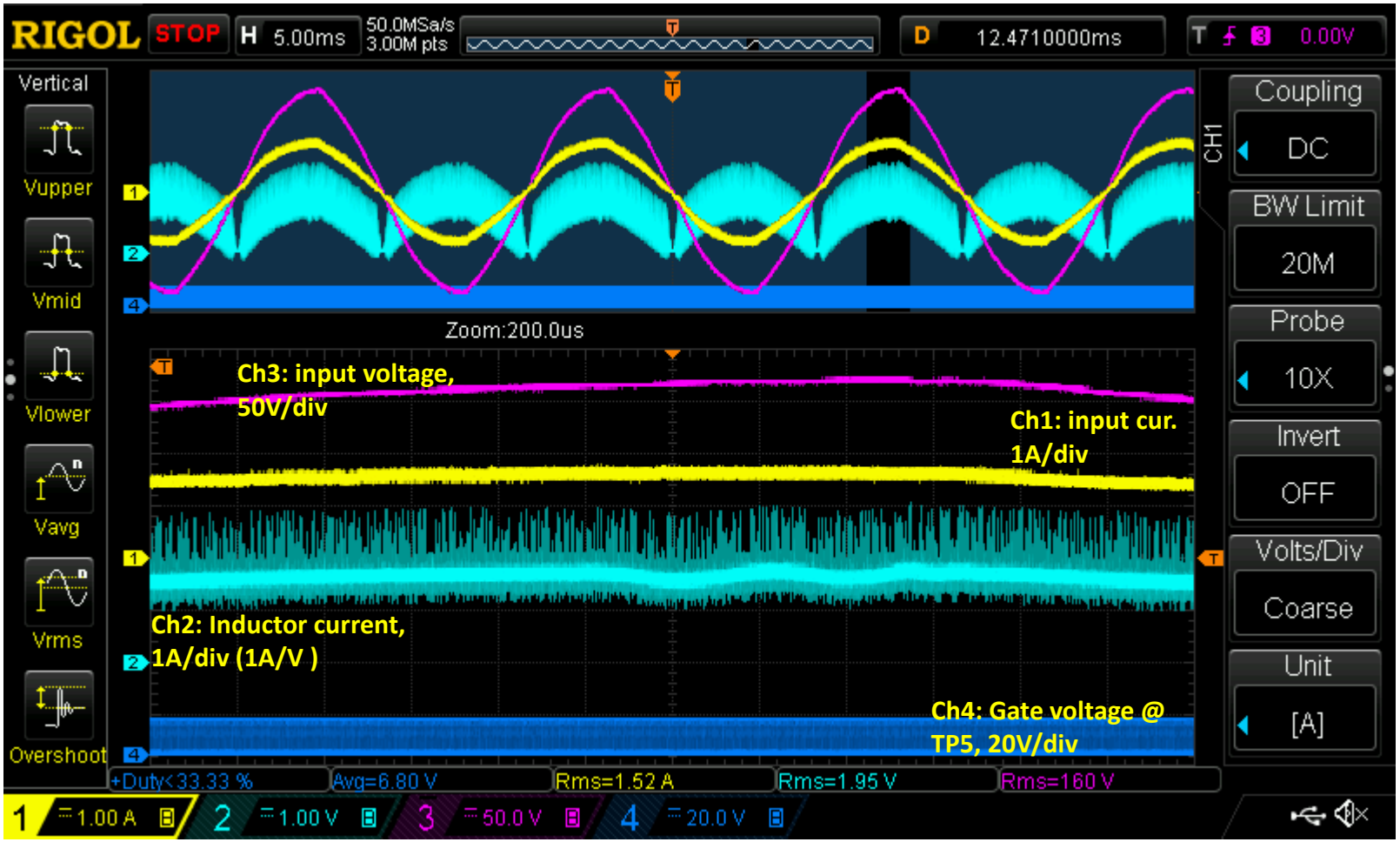
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 120Vac, Vdc_out=380V



Measuring inductor current vs gate voltages, 2/19/2023

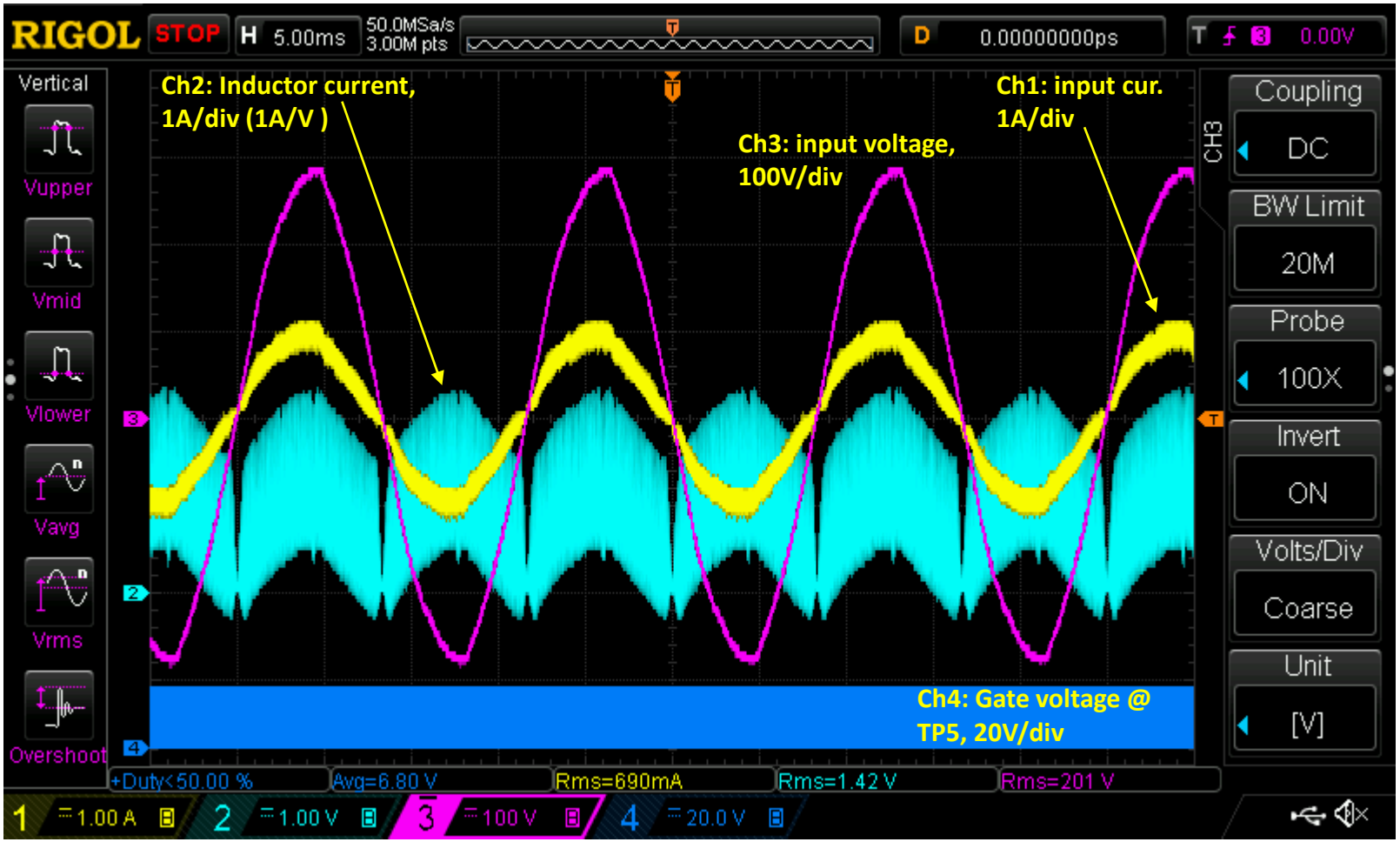
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 200Vac, Vdc_out=380V

Pin=0.69Arms*200Vrms=138W



Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 200Vac, no pulse dropping, Vdc_out=380V

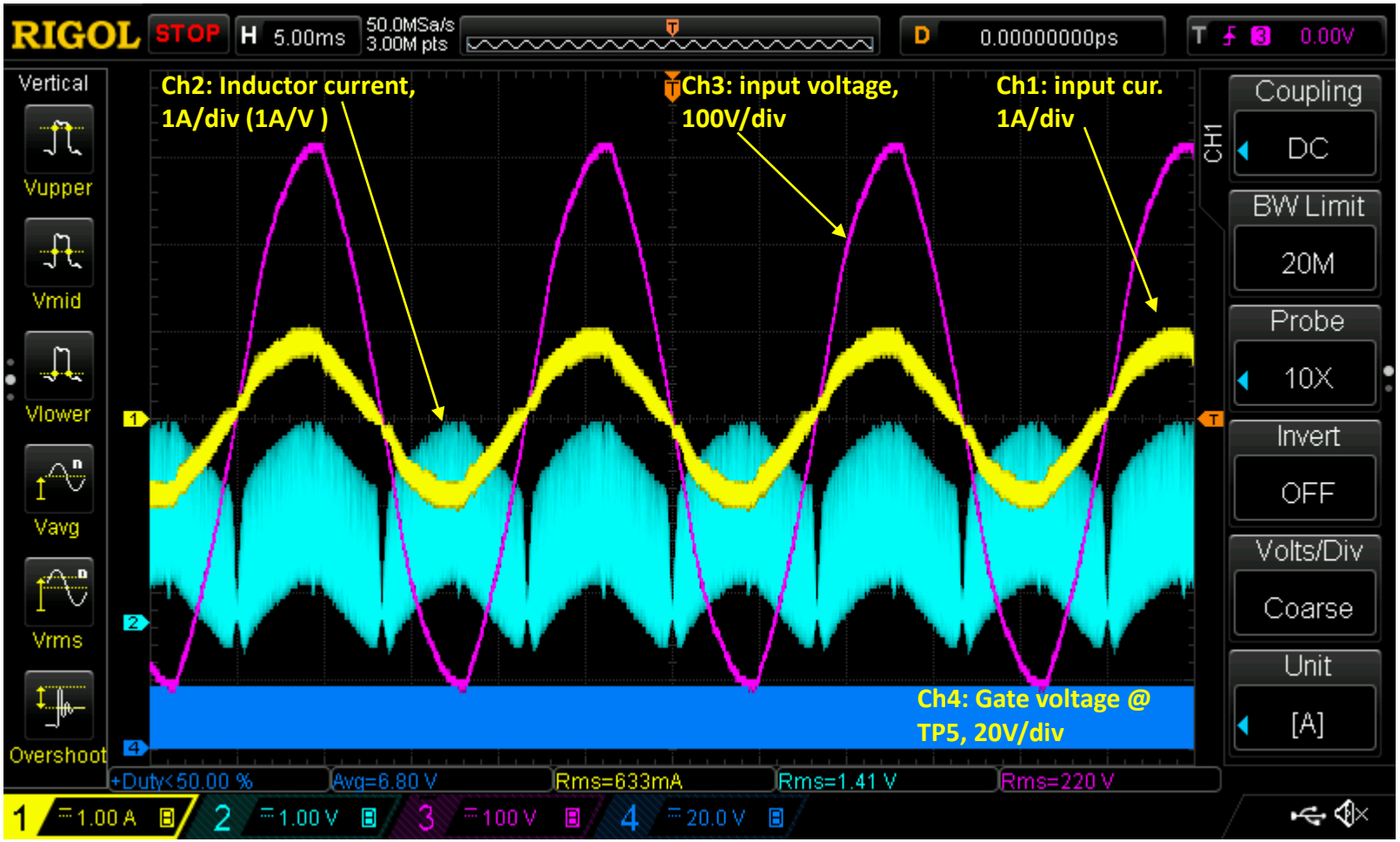
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 220Vac, no pulse dropping, Vdc_out=380V



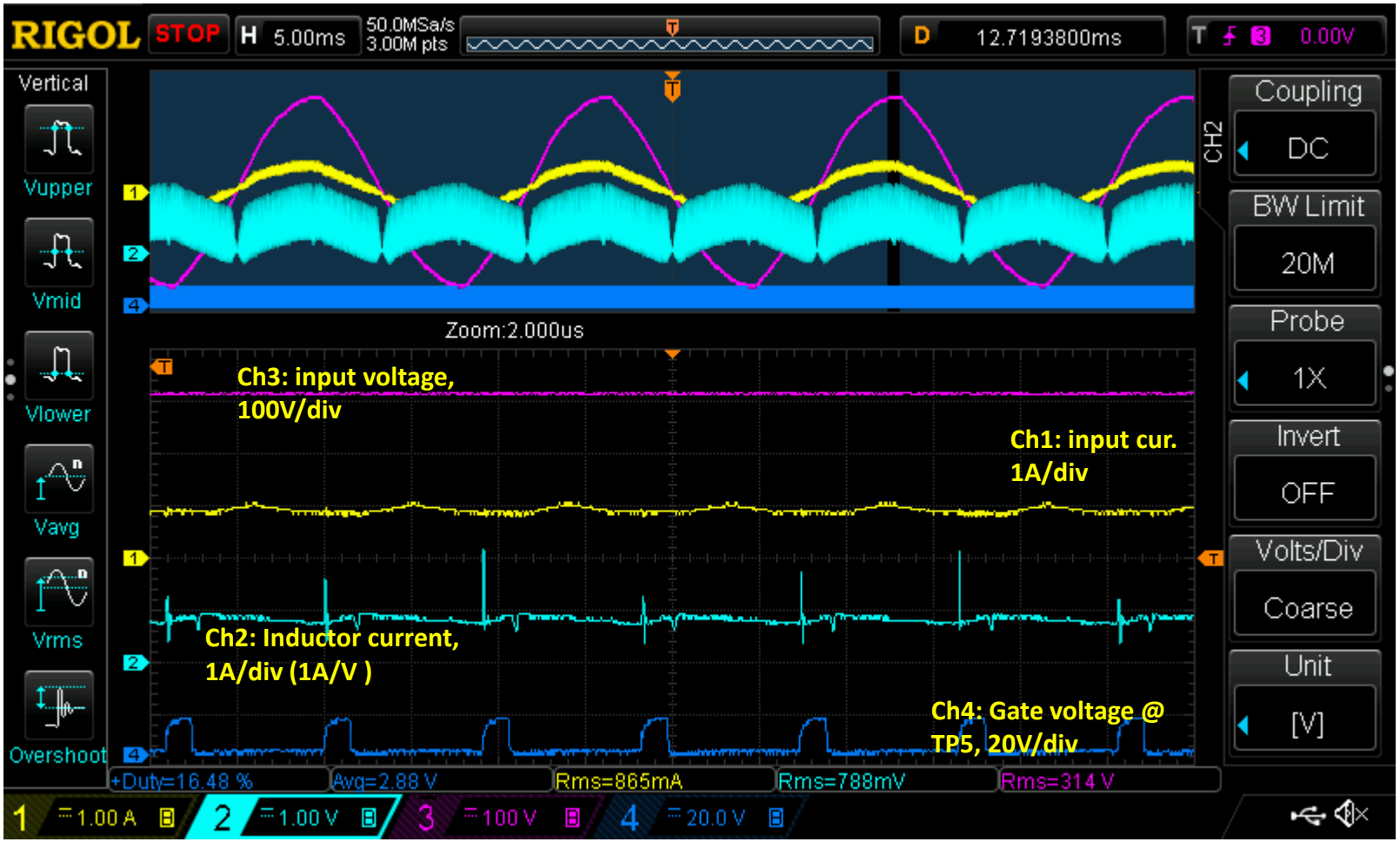
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no distortions at 220Vac, no pulse dropping, Vdc_out=380V



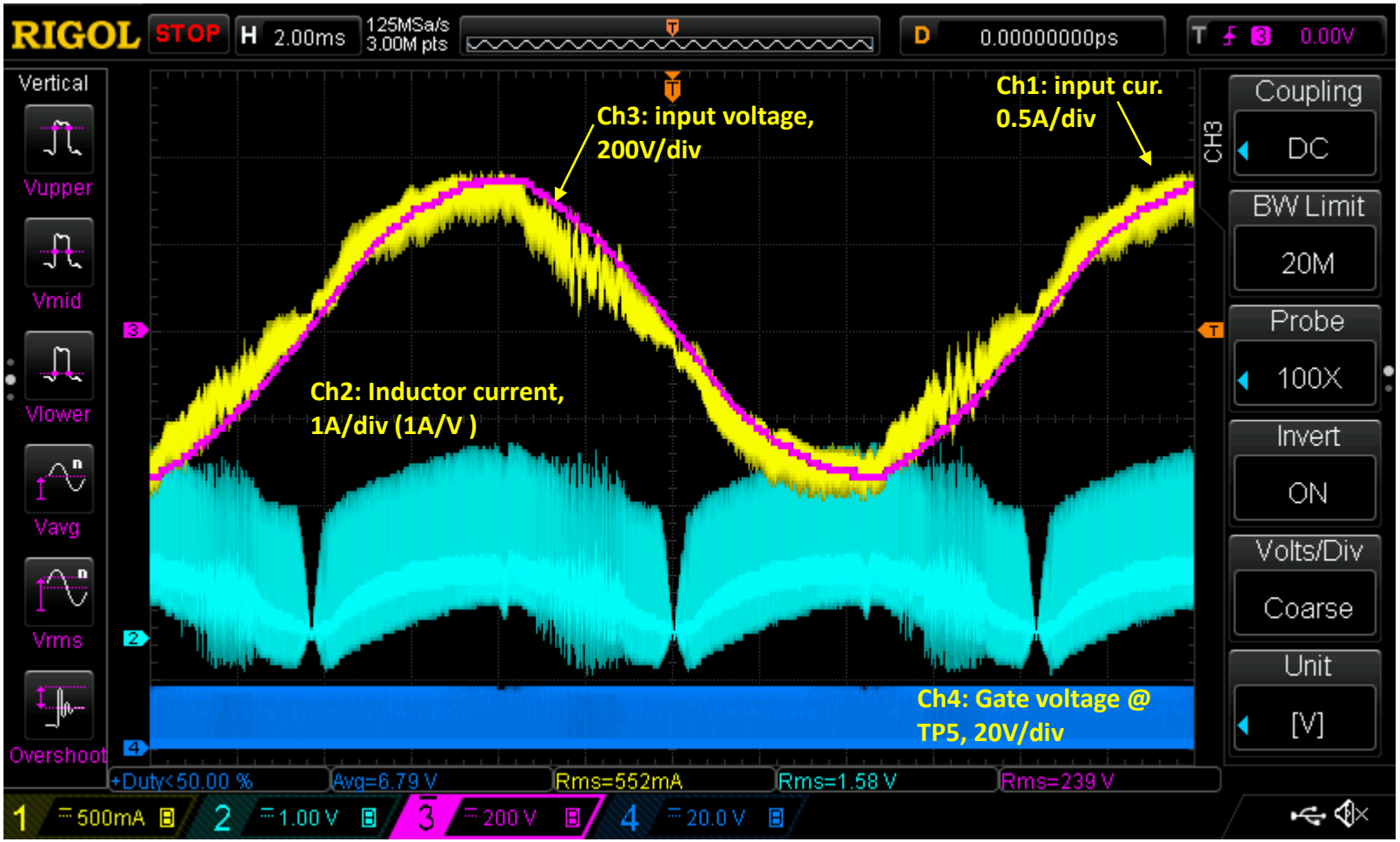
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no major distortions at 240Vac, however it appears like the distortions begin to start, Vdc_out=380V



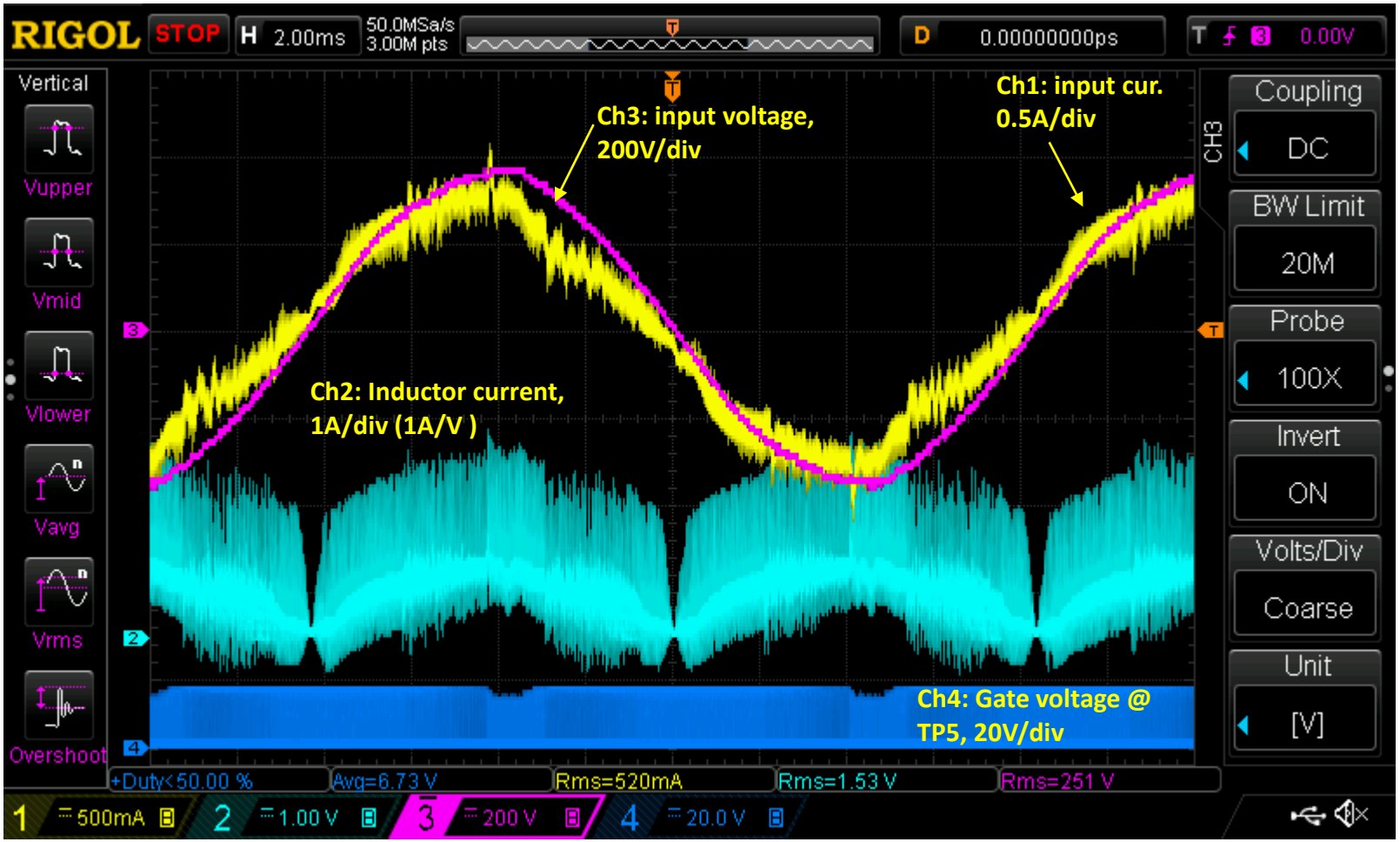
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no major distortions at 250Vac, however it appears like the distortions are a bit more than 240V case, Vdc_out=380V



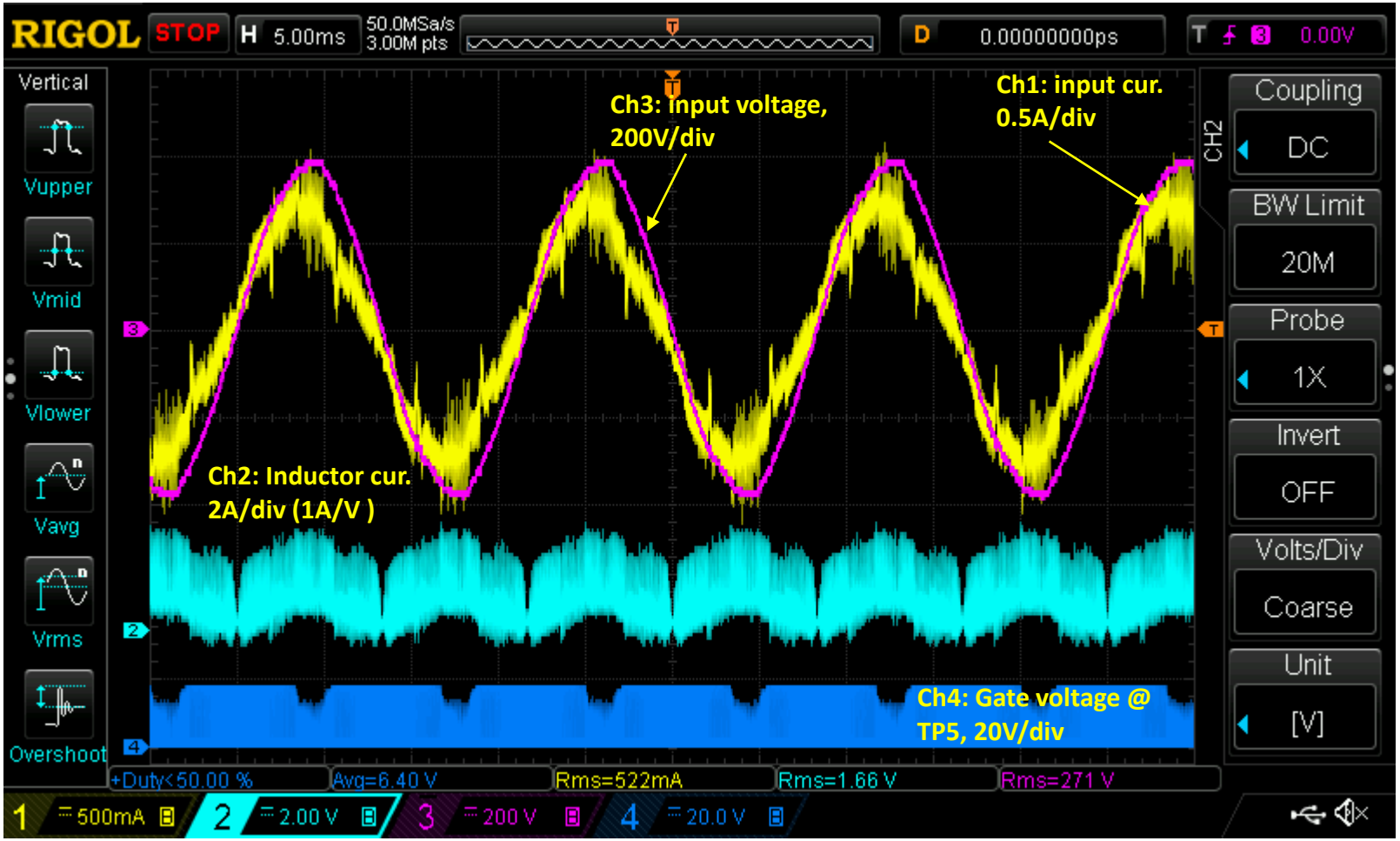
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no major distortions at 265Vac, however it appears like the distortions are a bit more than 250V case, Vdc_out=380V



Note: Input voltage is measured as 271Vac with differential probe and 265Vac with a DVM

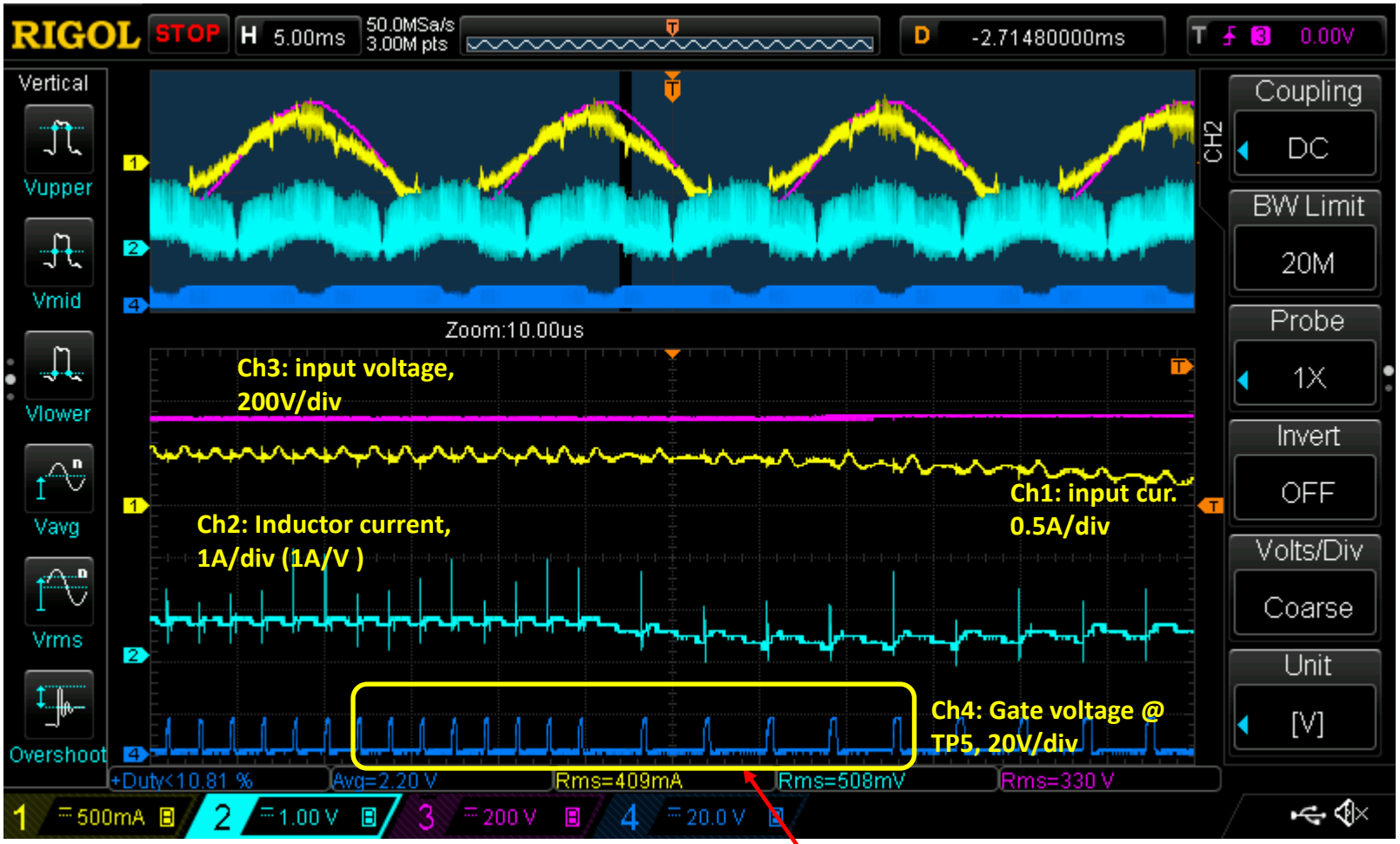
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no major distortions at 265Vac, pulse dropping observed, Vdc_out=380V



Pulse dropping observed

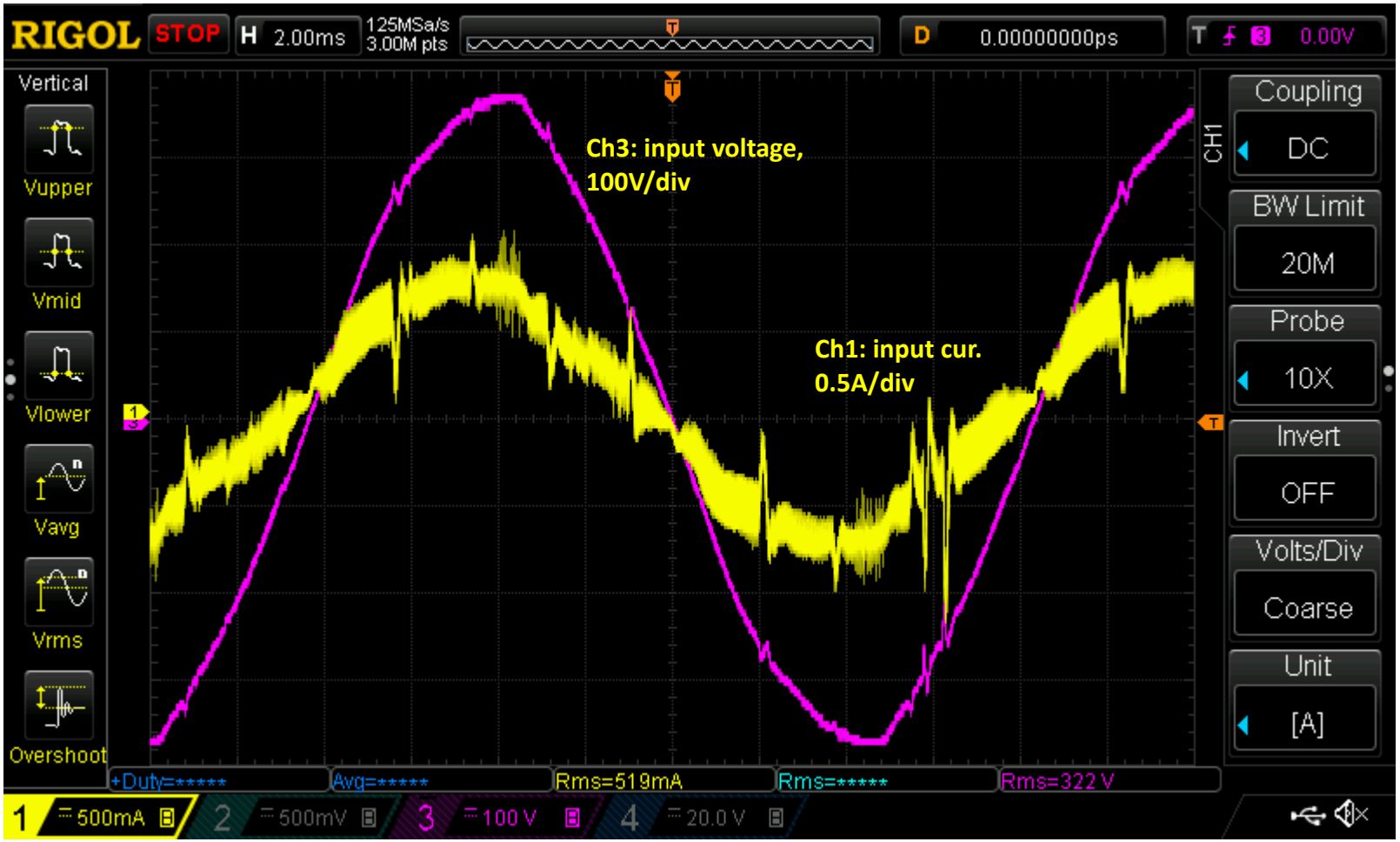
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, when DMM is connected to pin 19 for Vff, more distortions observed at 265Vac, Vdc_out=380V



Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

Input voltage (Vrms)	Vff @ pin19 (Vdc) w/ DVM
120	2.08
200	3.50
220	3.90
264	4.51

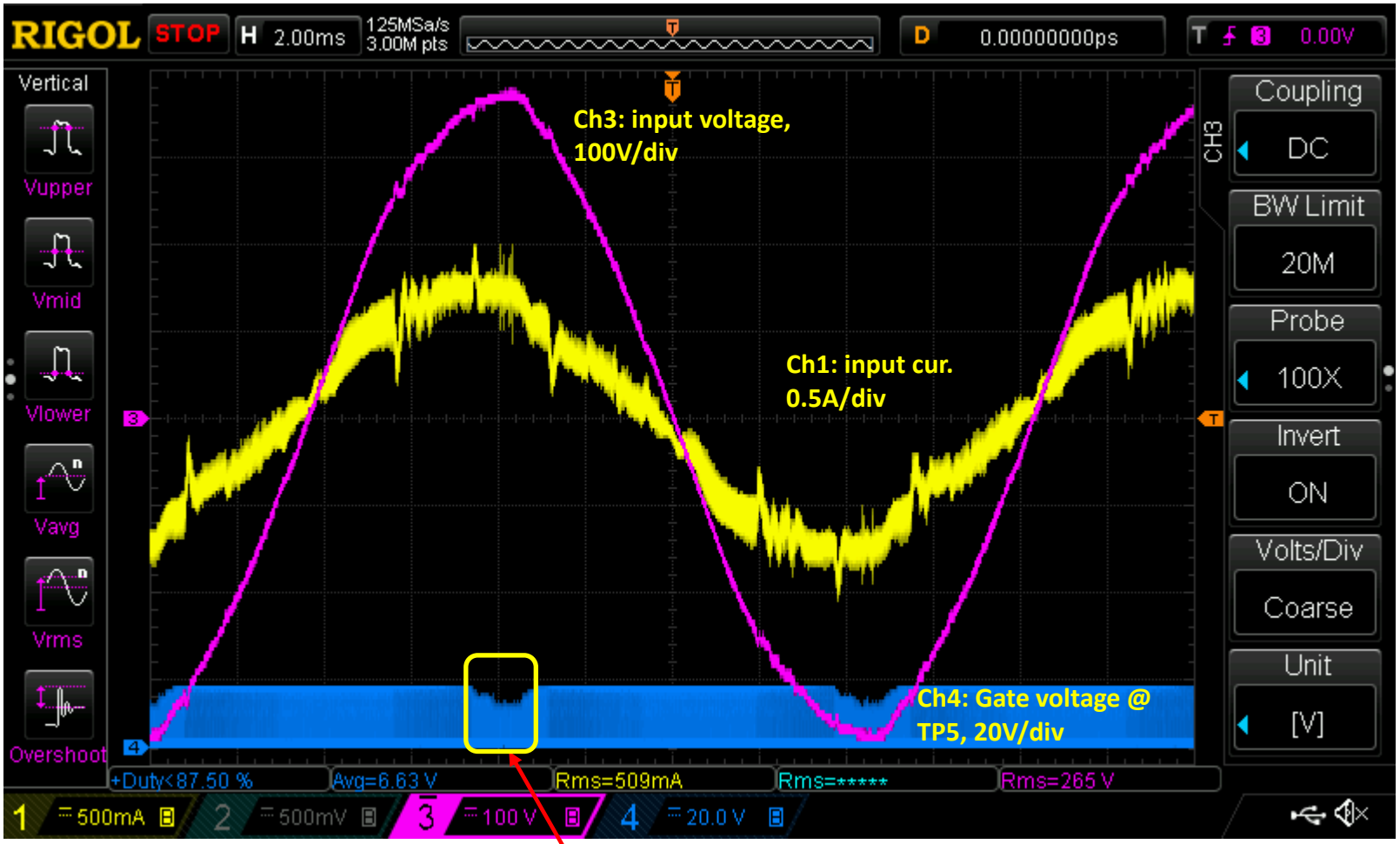
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no DMM on pin 19 for Vff, minor distortions observed at 265Vac, Vdc_out=380V



Pulse dropping observed

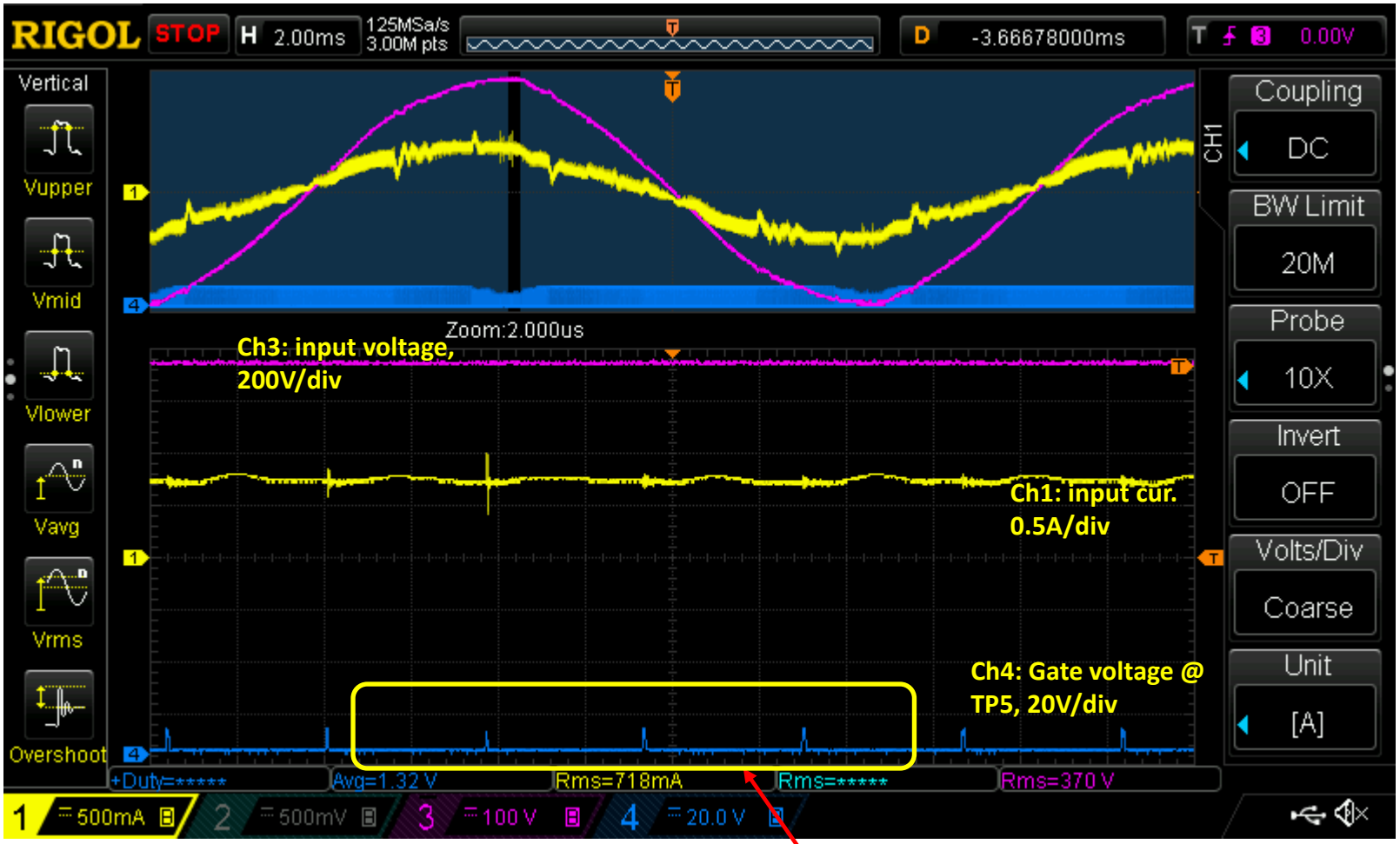
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, 12**0W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no DMM on pin 19 for Vff, minor distortions observed at 265Vac, Vdc_out=380V



Very small duty cycle however no pulse dropping at the peak of sine wave

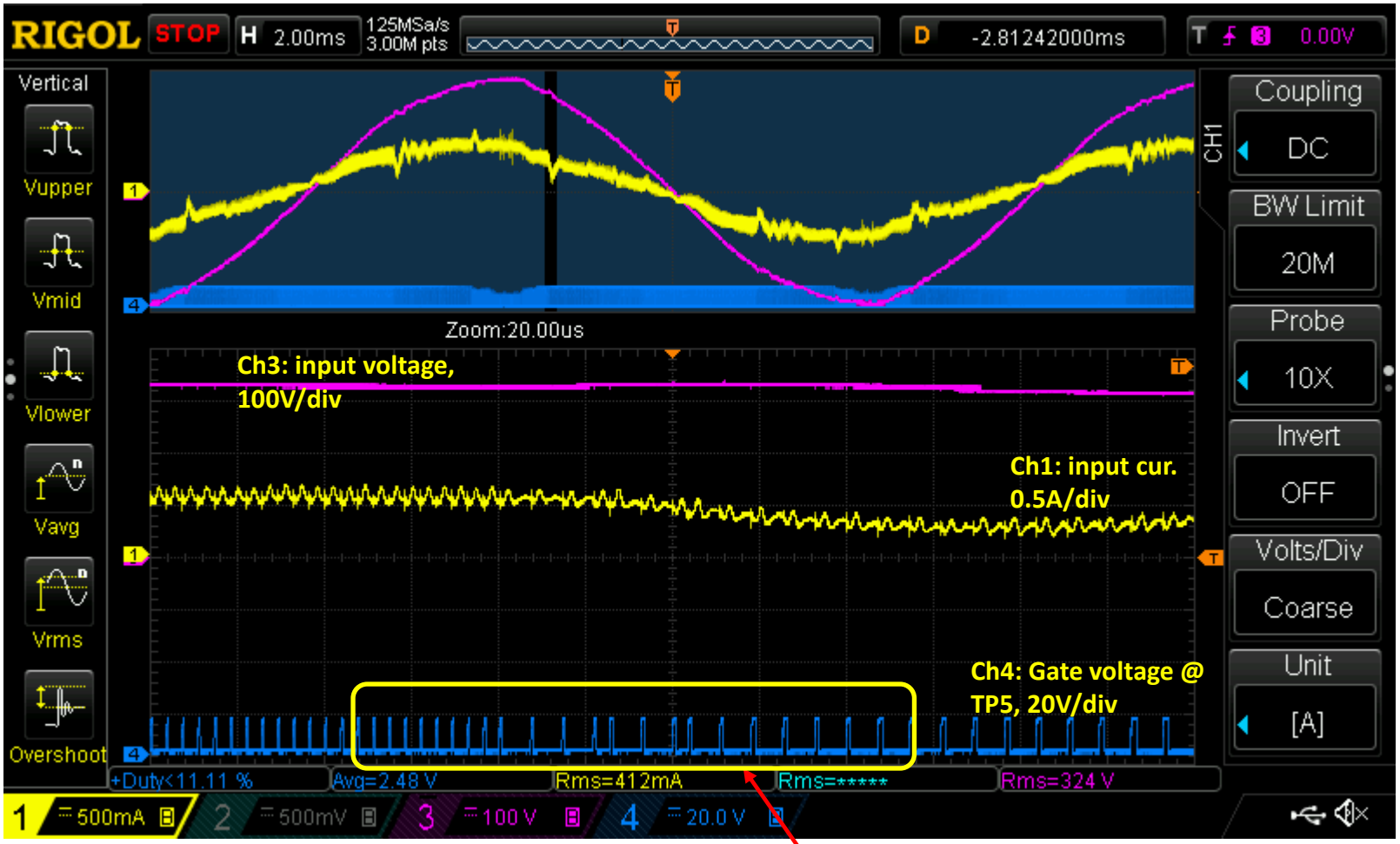
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no DMM on pin 19 for Vff, minor distortions observed at 265Vac, Vdc_out=380V



Pulse dropping observed

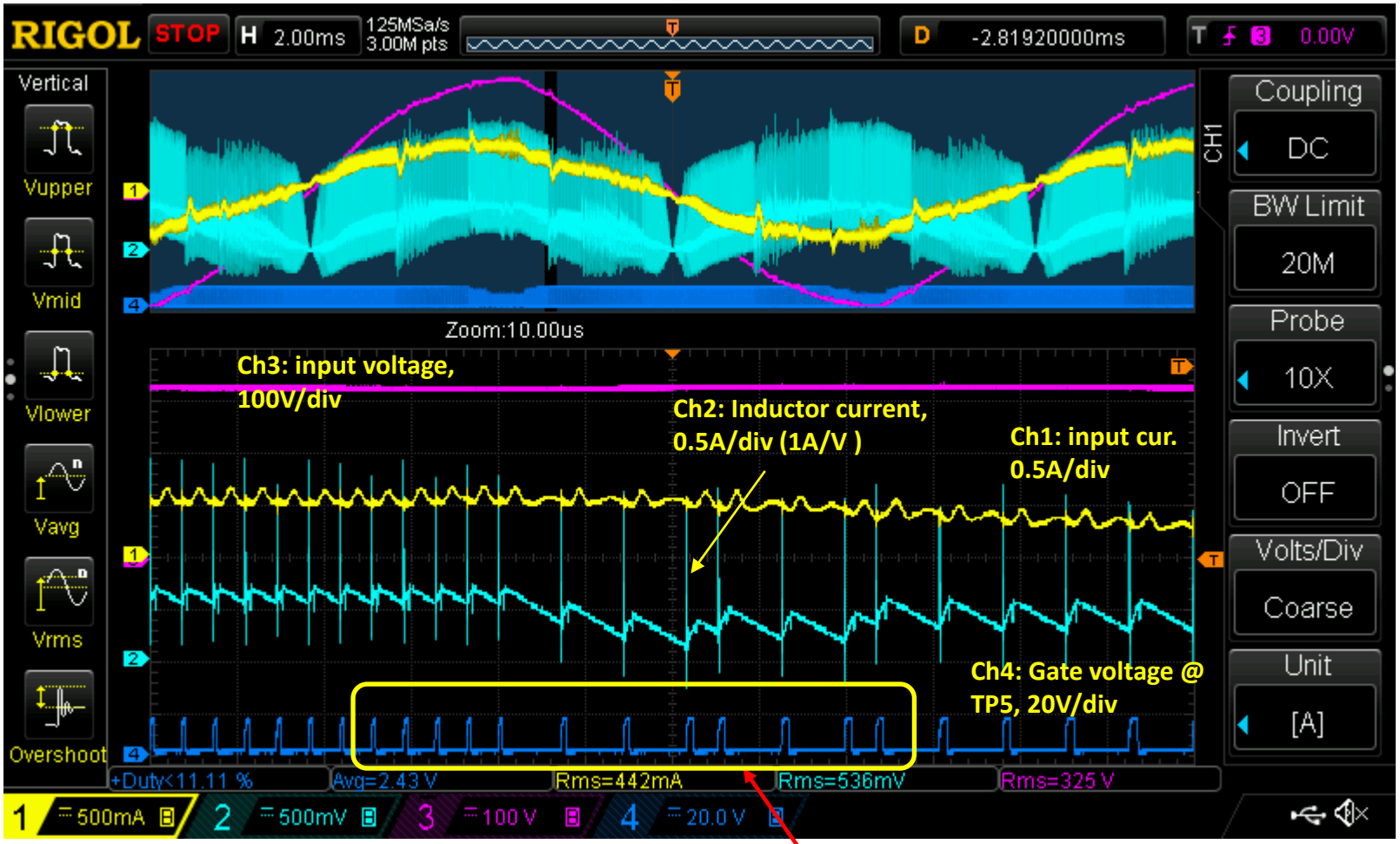
Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **120W external load across the DC-link**

2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

With 2x original inductor, 120W output power, no DMM on pin 19 for Vff, minor distortions observed at 265Vac, Vdc_out=380V



Pulse dropping observed

Measuring inductor current vs gate voltages, 2/19/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB removed, **30W external load across the DC-link**

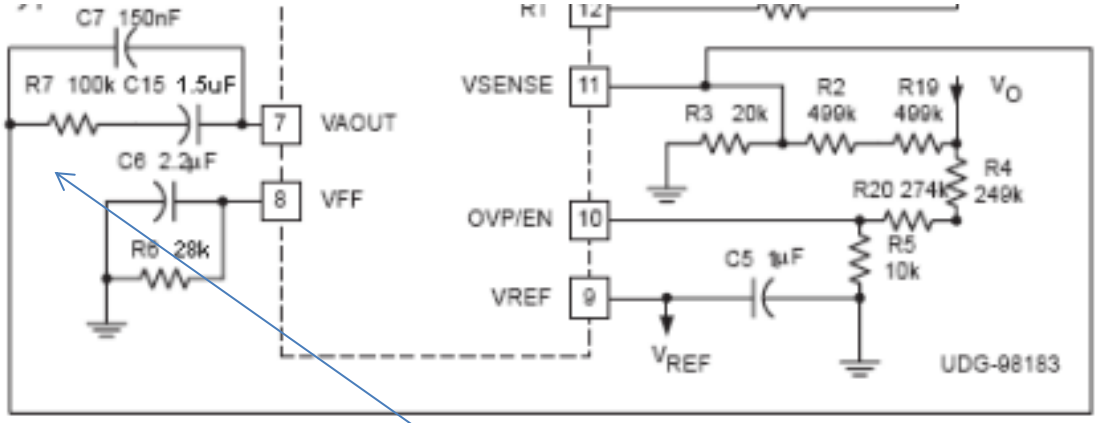
2pc of original boost inductors in series (1.36mH total), 10nF cap on PKLMT pin14 to GND, see slide 107 for modifications

Conclusions:

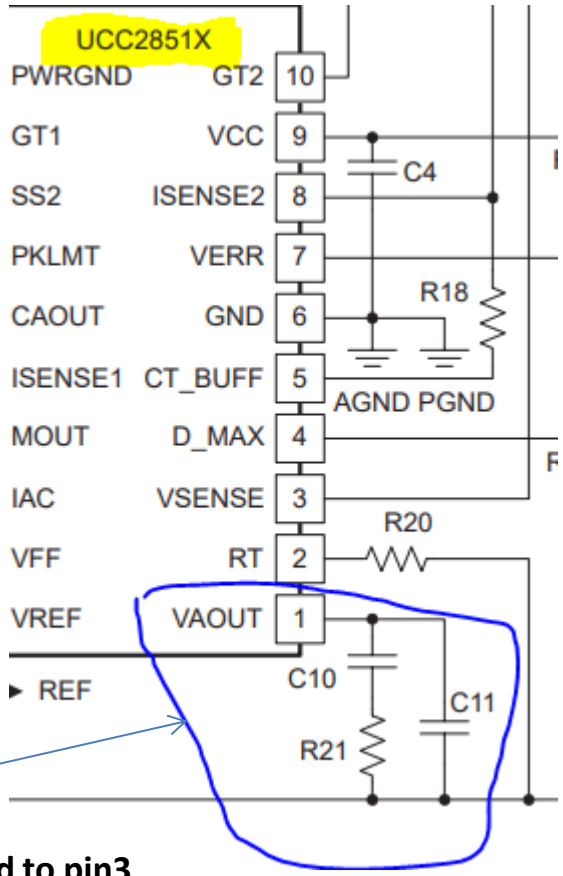
1) With 2x original inductors, current distortions were not observed up to 200Vac with 30W load on 380Vdc output. Periodic distortions started above ~210Vac
2) With 2x original inductors, current distortions were not observed up to 200Vac with 60W load on 380Vdc output. Periodic distortions started above ~220Vac
3) With 2x original inductors, current distortions were not observed up to 250Vac with 120W load on 380Vdc output. Periodic but a lot smaller distortions started above ~ 250Vac. Similar small distortions observed at 265Vac
4) Connecting DMM on pin19 resulted in a bit more distortions at high voltages in general. No DMM was connected to pin19 unless needed.
5) With 2x original inductors and 85Vac, output voltage was at 355V (instead of 380). Output was constant at 380V above ~100Vrms input.
6) It appears like the current distortions at high voltages are related with the performance of current regulator as unit transitions between DCM and CCM modes

Following pages describe the changes made to PFC stage in order to mitigate current distortions:

UCC3817 voltage error amp.



UCC28513 voltage error amp.



PFC board circuit diagram changes:

1) **UCC28513 is used in PFC design**
2) **Voltage error amp components are disconnected from GND and connected to pin3 (Vsense), similar to UCC3817 data sheet**
3) **Added 10nF cap on PKLMT pin14 to GND**

Measuring inductor current vs gate voltages, 8/6/2023

RefDes on UCC28513	RefDes in Listen	PCB	Values on 6/25/2023
R2	R43	PSB-04	0.47
-	R60		22.1K
-	R44/R49		562K
-	R47/R50		383K
R14	R13	PFC-03	10K
R7	R5		1.62K
R12	R4		3k (3.16k//56k)
C7	C8		330p
C6	C6		4.9nF (1.6n+3.3n)
R13	R10		3.23k (3.3k//150k)
R8	R9		3k (3.16k//56k)
R15	R11		28K (56k//56k)
C8	C9		2uF (1uF//1uF)
C11	C2		150n
C10	C1		1.5uF
R21	R1		100K

In addition:

- 10nF cap added from PKLMT pin14 to GND on PFC card.
- PFC inductor (L2) is replaced with TSD-5033 (w/o base)
- Sense resistor on PSB (R43) part number: MOSX5CR47J

Old PFC inductor (L2) w/ overlapping windings
625uH @ 4.8A

New toroidal PFC inductor (L2) w/o overlapping windings
750uH @ 8A

Measuring inductor current vs gate voltages, 8/6/2023

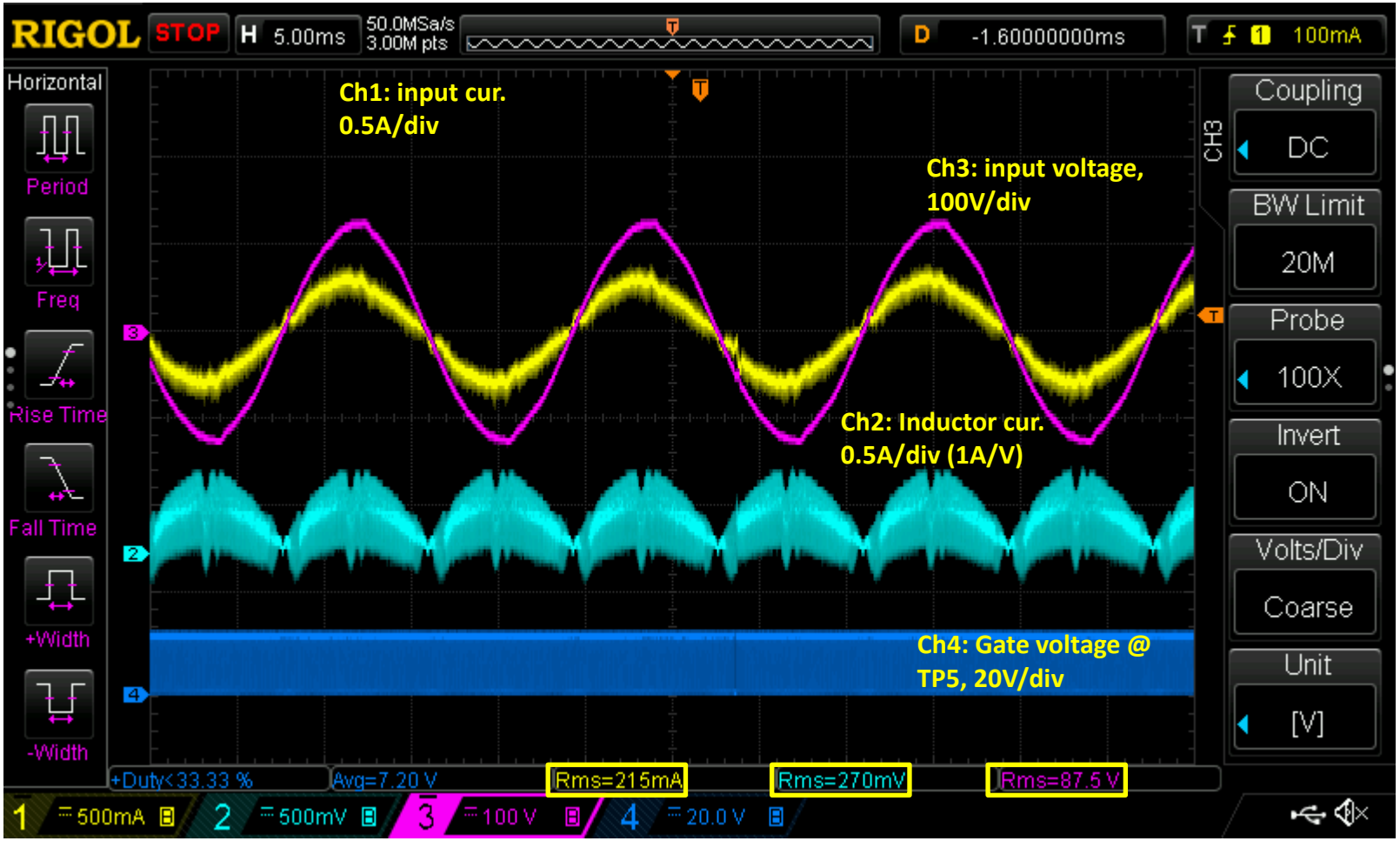
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 85Vac, 12.5K across DC-link:

output=387Vdc, input cur. = 0.215Arms, inductor cur. = 0.282Arms, Sin=18.27VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

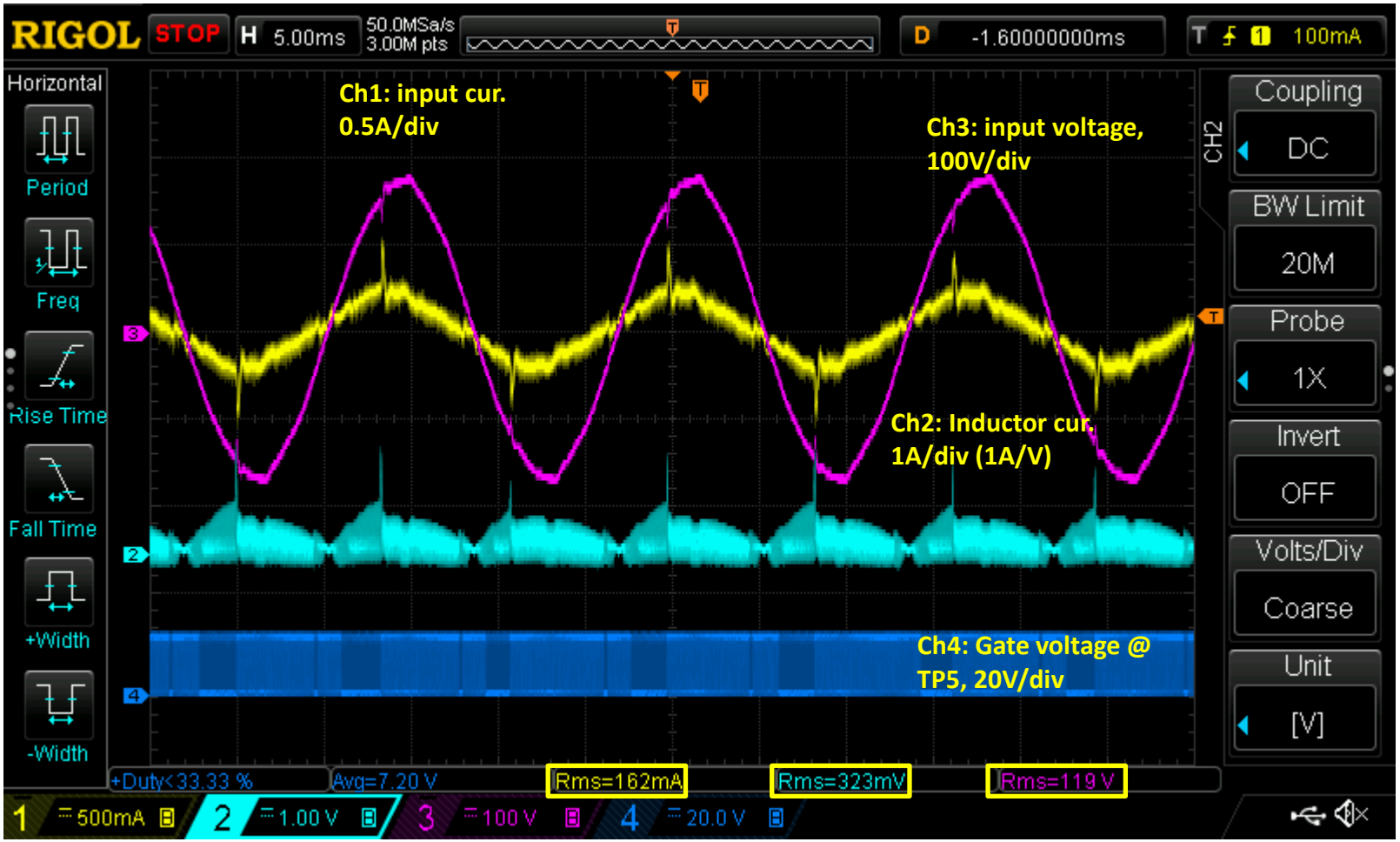
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 120Vac, 12.5K across DC-link:

output=389Vdc, input cur. = 0.162Arms, inductor cur. = 0.323Arms, Sin=19.4VA (OK PF)



Measuring inductor current vs gate voltages, 8/6/2023

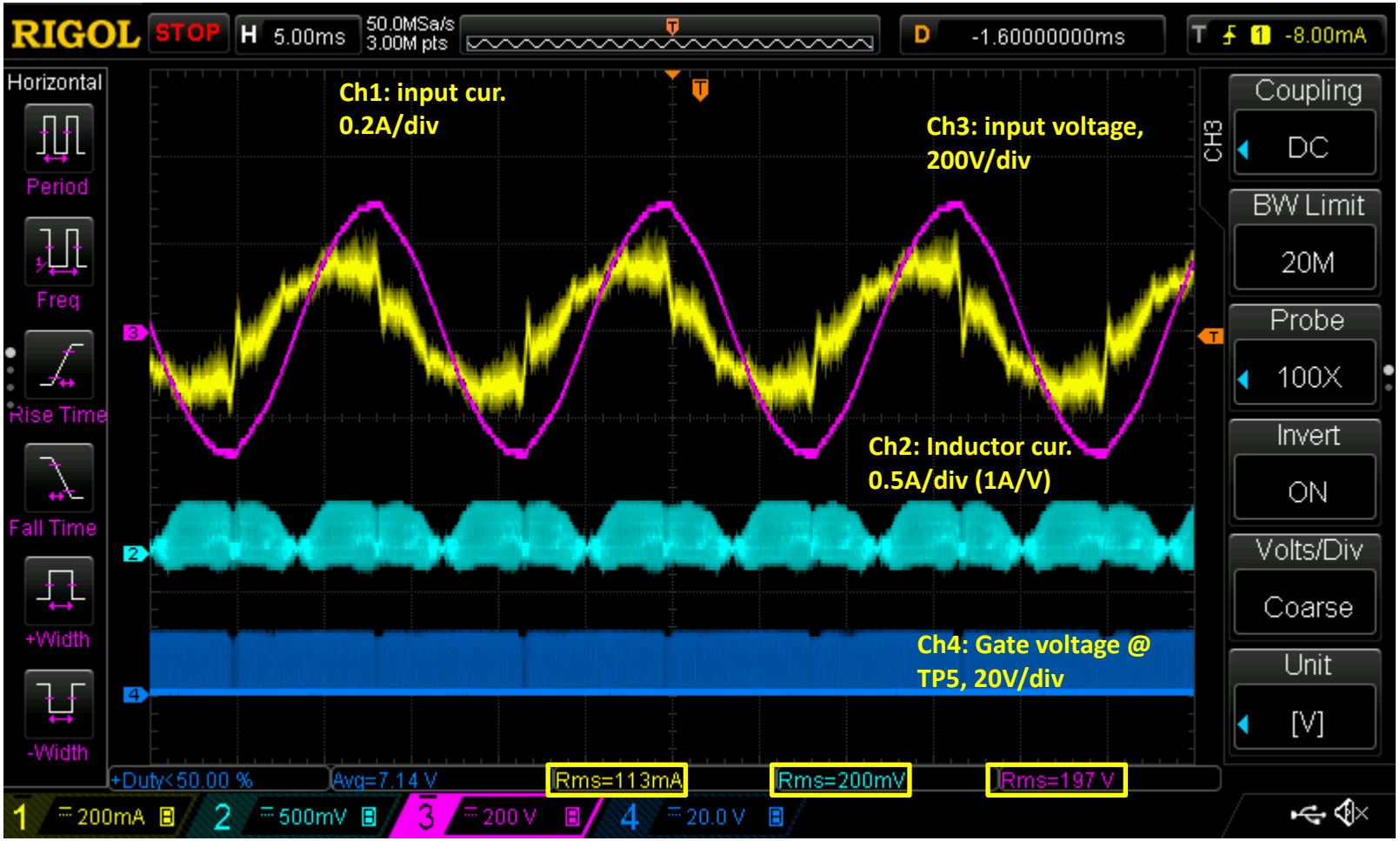
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 200Vac, 12.5K across DC-link:

output=388Vdc, input cur. = 0.113Arms, inductor cur. = 0.200Arms, Sin=22.6VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

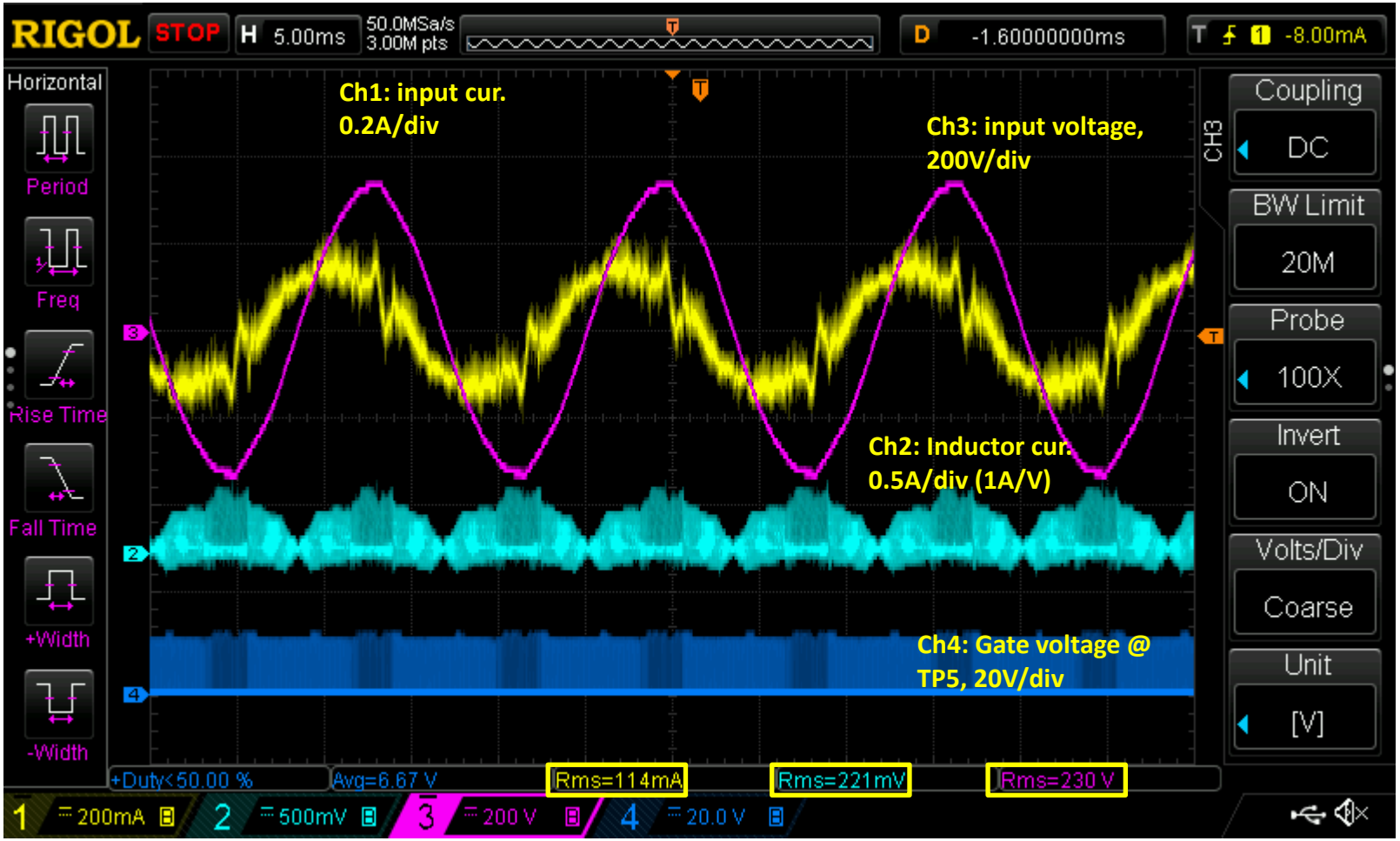
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 230Vac, 12.5K across DC-link:

output=388Vdc, input cur. = 0.114Arms, inductor cur. = 0.221Arms, Sin=26.2VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

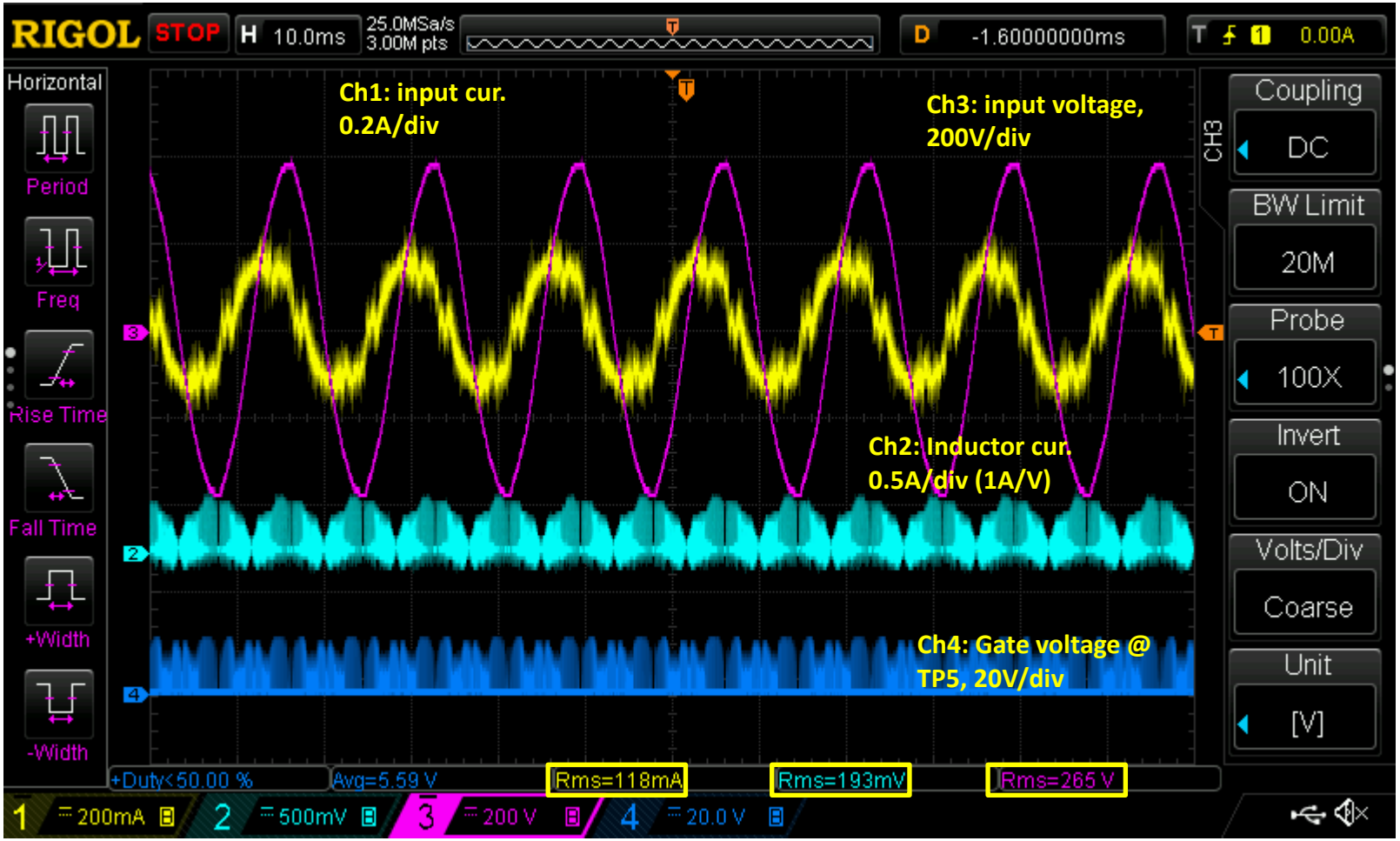
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 265Vac, 12.5K across DC-link:

output=388Vdc, input cur. = 0.118Arms, inductor cur. = 0.193Arms, Sin=31.2VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

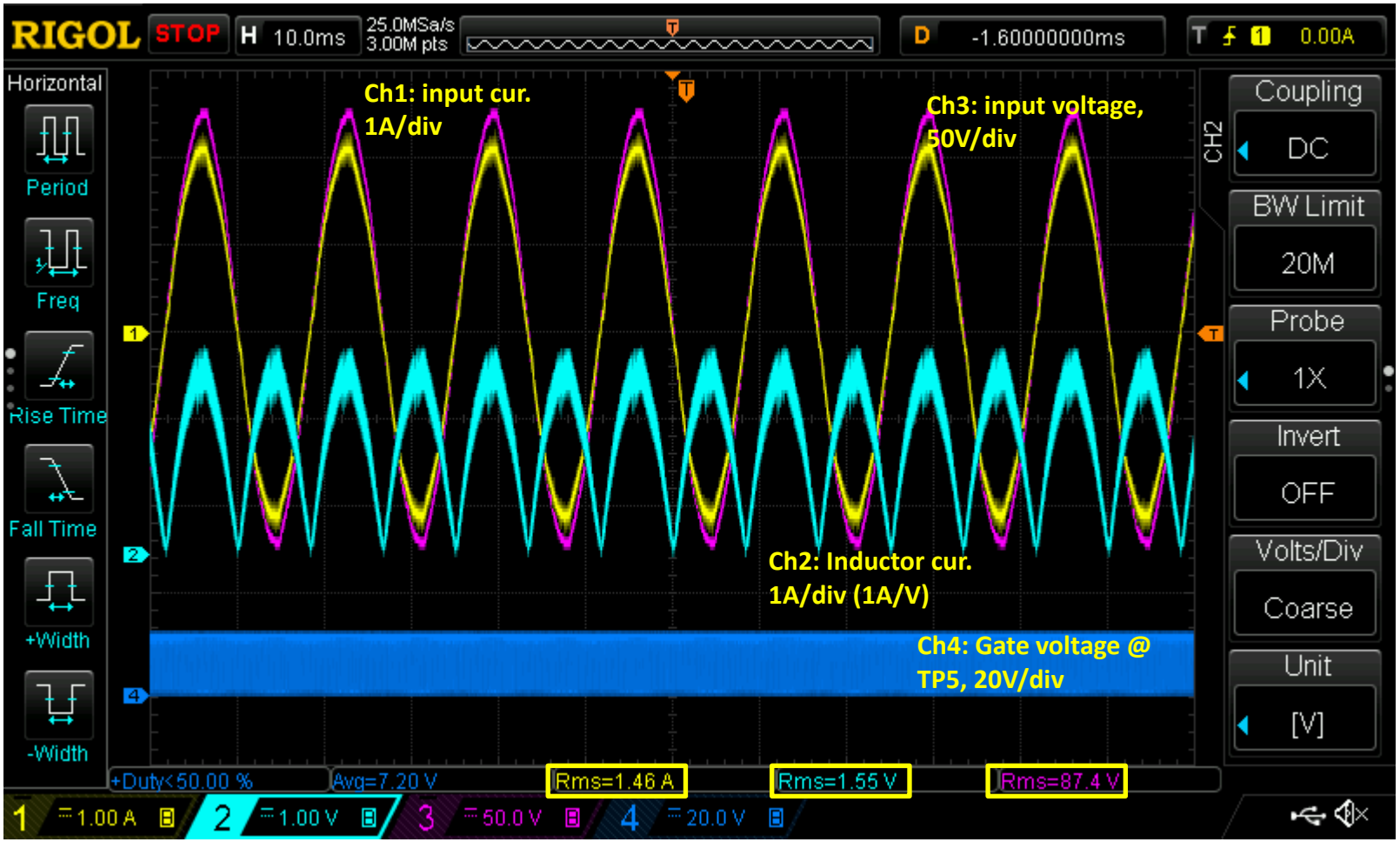
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 85Vac, 1.149K across DC-link:

output=360Vdc, input cur. = 1.46Arms, inductor cur. = 1.55Arms, Sin=124VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

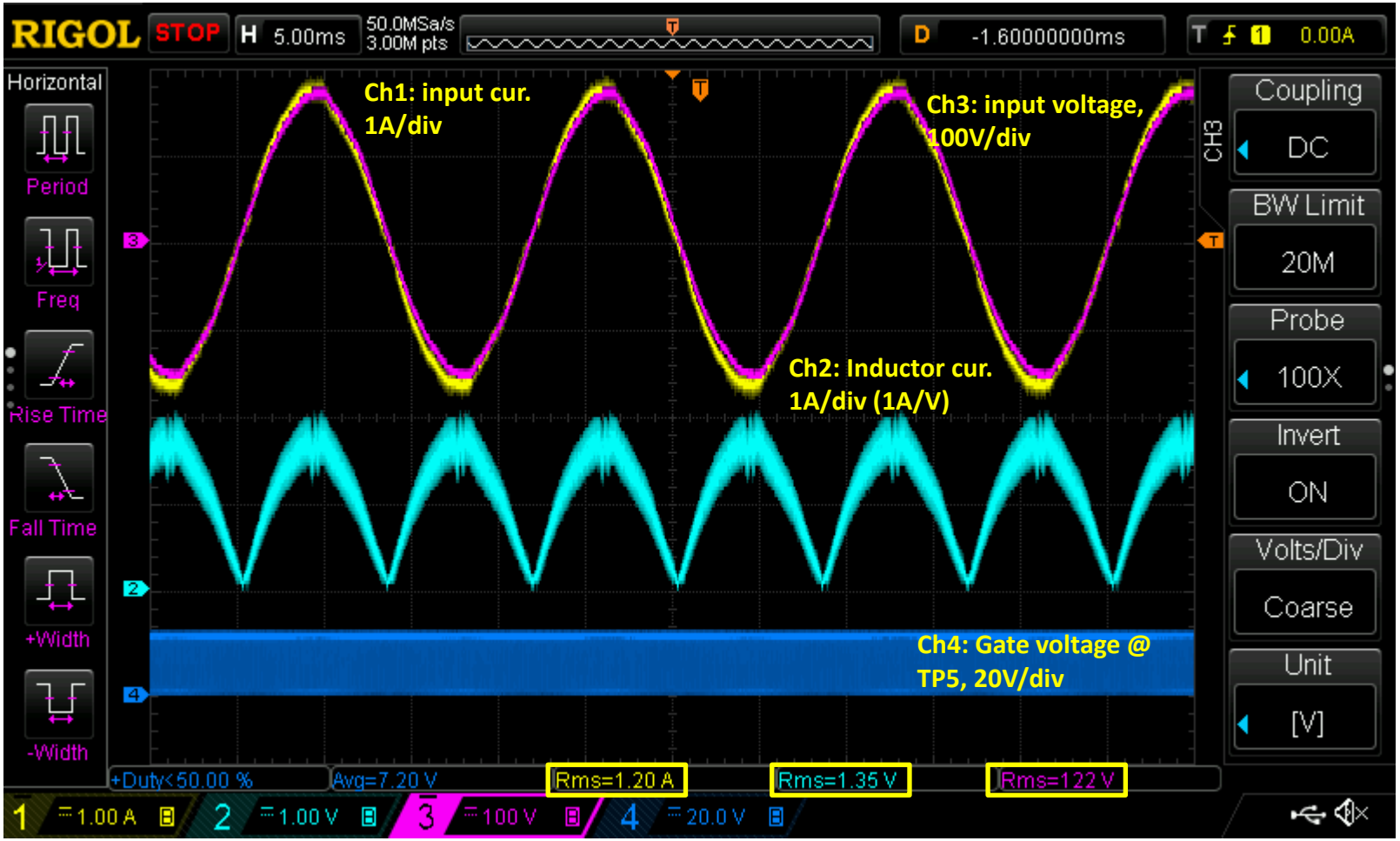
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 120Vac, 1.149K across DC-link:

output=373Vdc, input cur. = 1.20Arms, inductor cur. = 1.35Arms, Sin=144VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

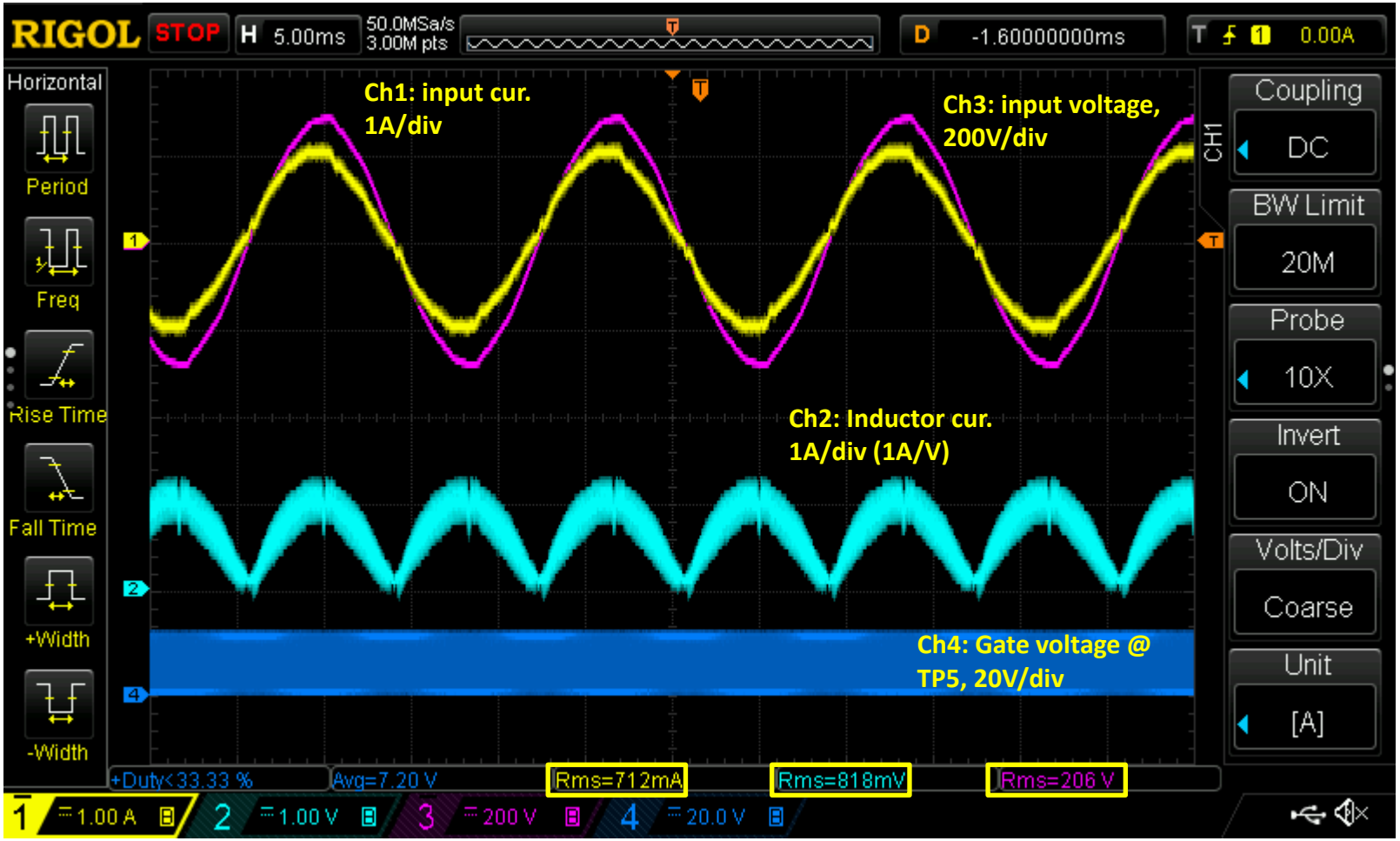
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 200Vac, 1.149K across DC-link:

output=381Vdc, input cur. = 0.712Arms, inductor cur. = 0.818Arms, Sin=142.4VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

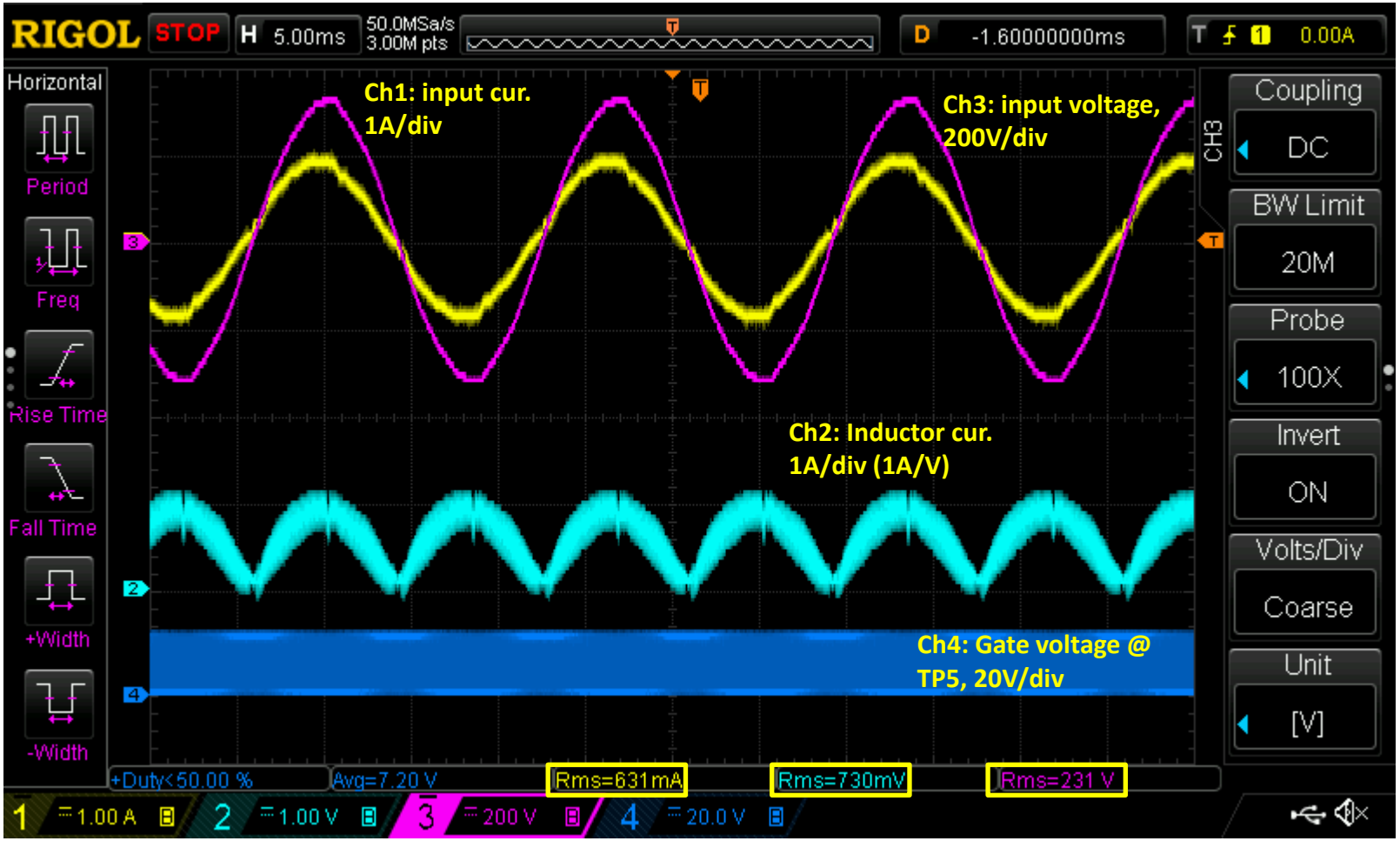
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 230Vac, 1.149K across DC-link:

output=382Vdc, input cur. = 0.631Arms, inductor cur. = 0.73Arms, Sin=145.1VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

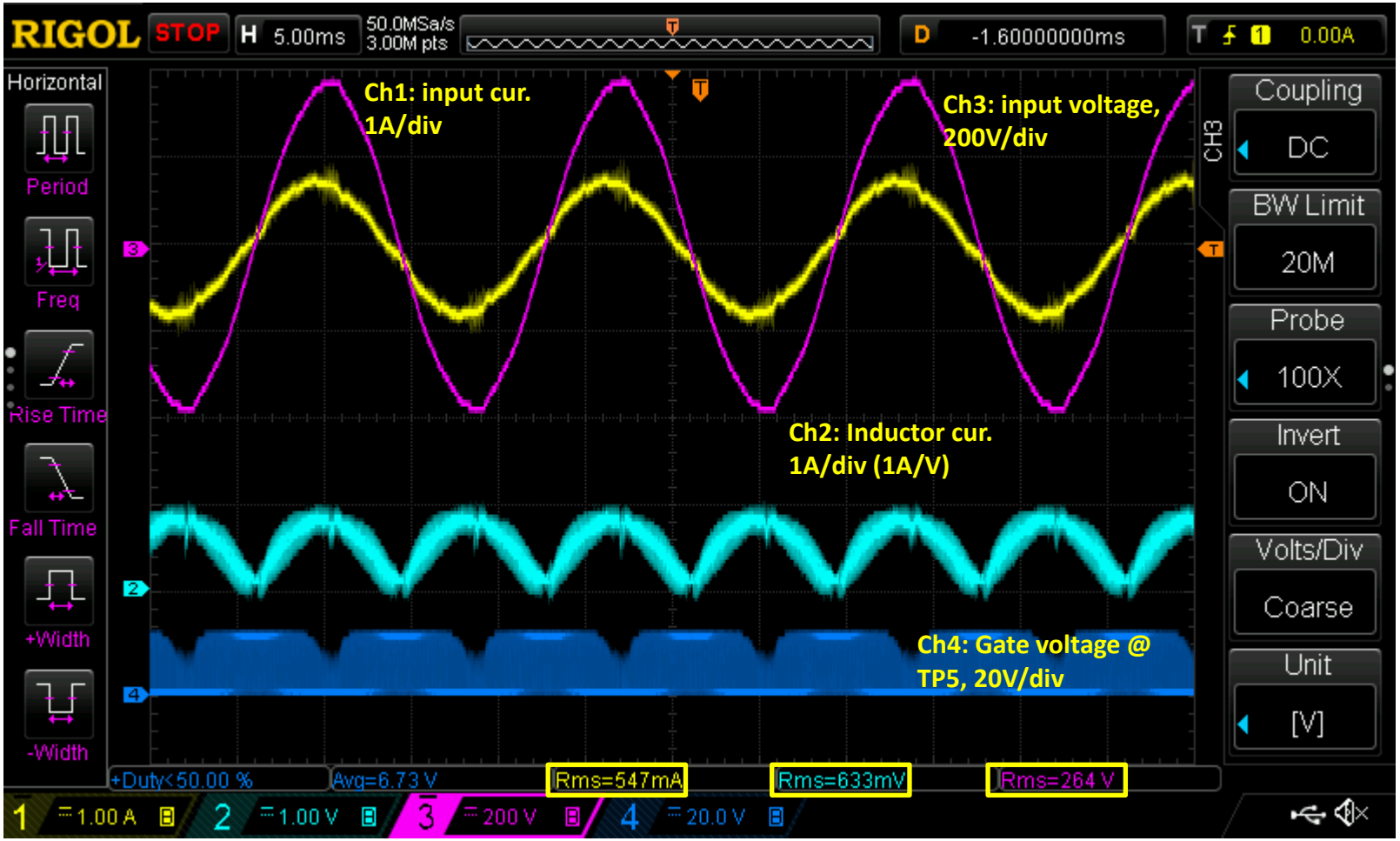
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

At 265Vac, 1.149K across DC-link:

output=380Vdc, input cur. = 0.547Arms, inductor cur. = 0.633Arms, Sin=144.9VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 on PSB are removed, R43 is 0.47Ω (PN: MOSX5CR47J), boost inductor is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

Summary of testing PFC stage input current distortions with min/max resistive loads across the DC-link

- By removing L1, Q5, Q6 on PSB, only the PFC stage was tested w/o secondary stage power supply board
- By using larger toroidal inductor, the current distortions observed earlier were mostly eliminated
- Turn-on current spikes were reduced, this is visible in inductor current measurements
- At min load from 85Vac-265Vac, good DC-link regulation was achieved
- At max output load and low AC voltage, the DC-link voltage was less than the set point of 390V

Dc-Link load (kΩ)	Input voltage (Vrms) By using Diff Probe	DC-link w/ DVM (Vdc)	Input current (Arms)	Inductor current (Arms)	Input power (VA)	Comments
12.5 Min load	85	387	0.215	0.282	18.27	OK PF, no major distortions
	120	389	0.162	0.323	19.40	OK PF, minor distortions
	200	388	0.113	0.200	22.60	Poor PF, no major distortions
	230	388	0.114	0.221	26.20	
	265	388	0.118	0.193	31.20	
1.149 Max load	85	371	1.57	1.65	124.0	Good PF, no distortions, lower DC-link
	120	382	1.12	1.25	144.0	Good PF, no distortions
	200	382	0.677	0.769	142.2	
	230	388	0.599	0.679	145.1	
	265	389	0.525	0.600	144.9	

Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6” away from PSB

See slides 162 and 163 for circuit configuration

Following slides show the test results by enabling the secondary stage DC/DC converter (L1, Q5, Q6 (PN: IRFPC50A) on PSB are installed**)**

Measuring inductor current vs gate voltages, 8/6/2023

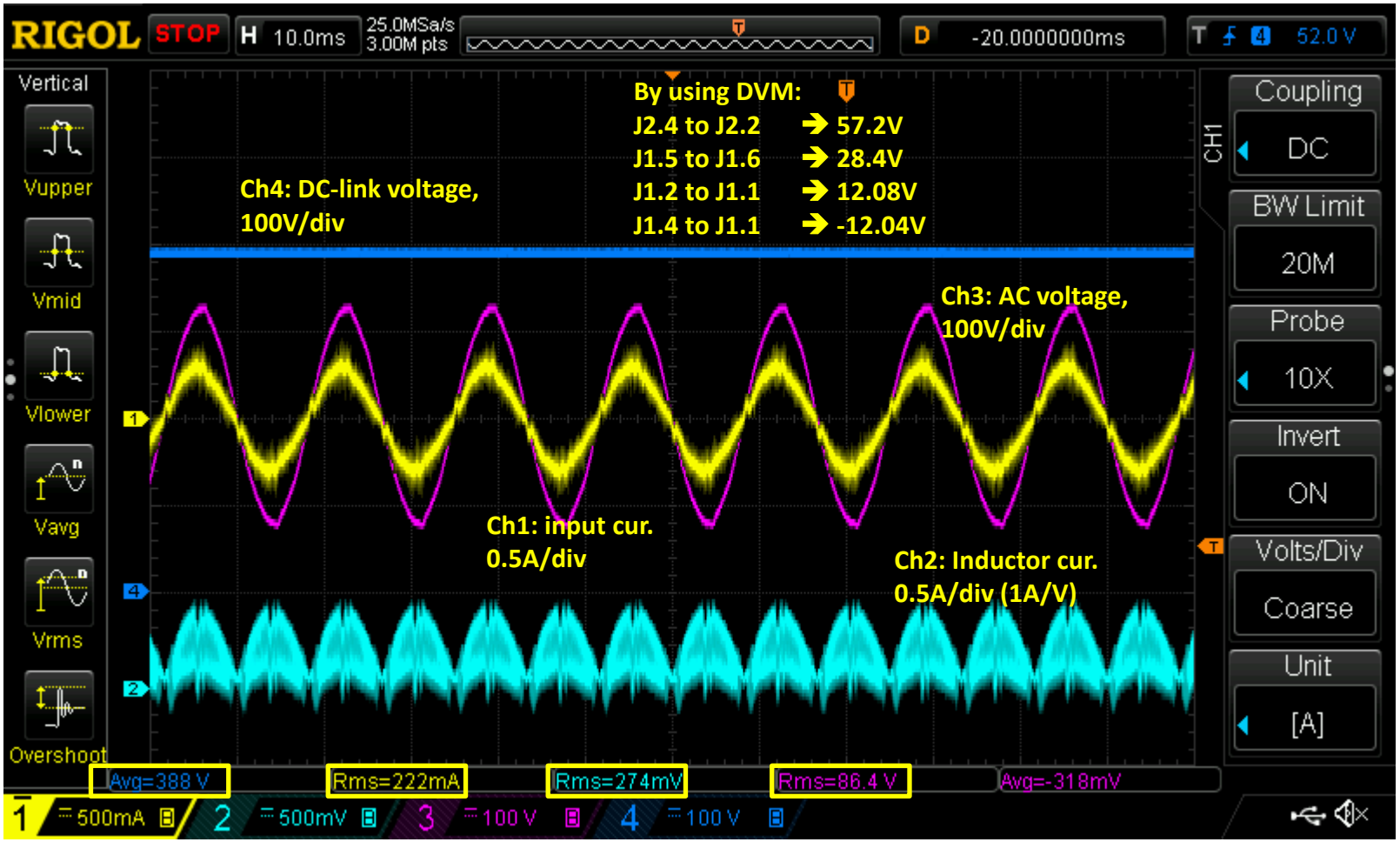
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At 85Vac, min loads on outputs at J1 and J2 connectors

output=388Vdc, input cur. = 0.222Arms, inductor cur. = 0.274Arms, Sin=18.8VA (good PF)



Measuring inductor current vs gate voltages, 8/6/2023

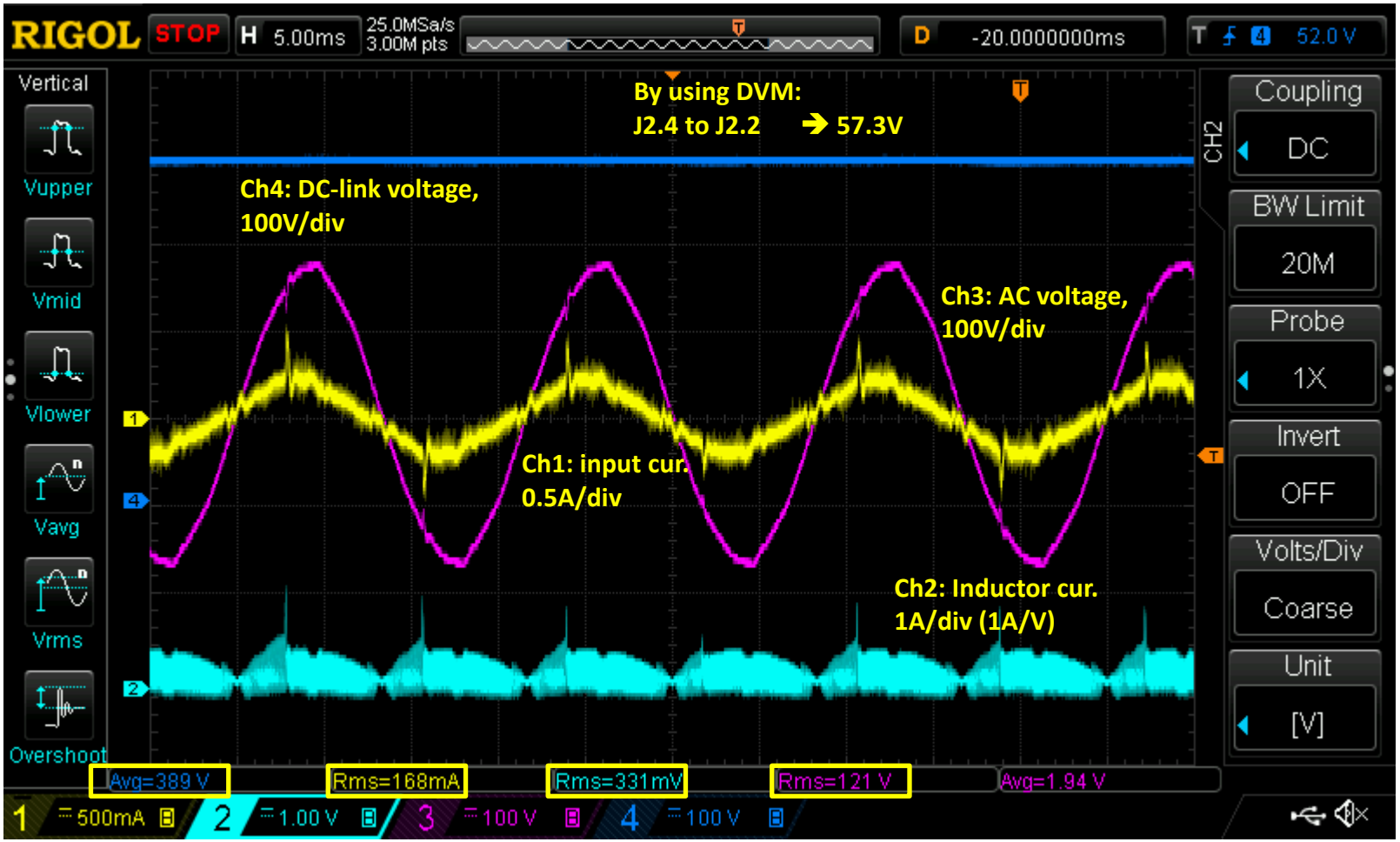
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At 120Vac, min loads on outputs at J1 and J2 connectors

output=389Vdc, input cur. = 0.168Arms, inductor cur. = 0.331Arms, Sin=20.1VA (OK PF)



Measuring inductor current vs gate voltages, 8/6/2023

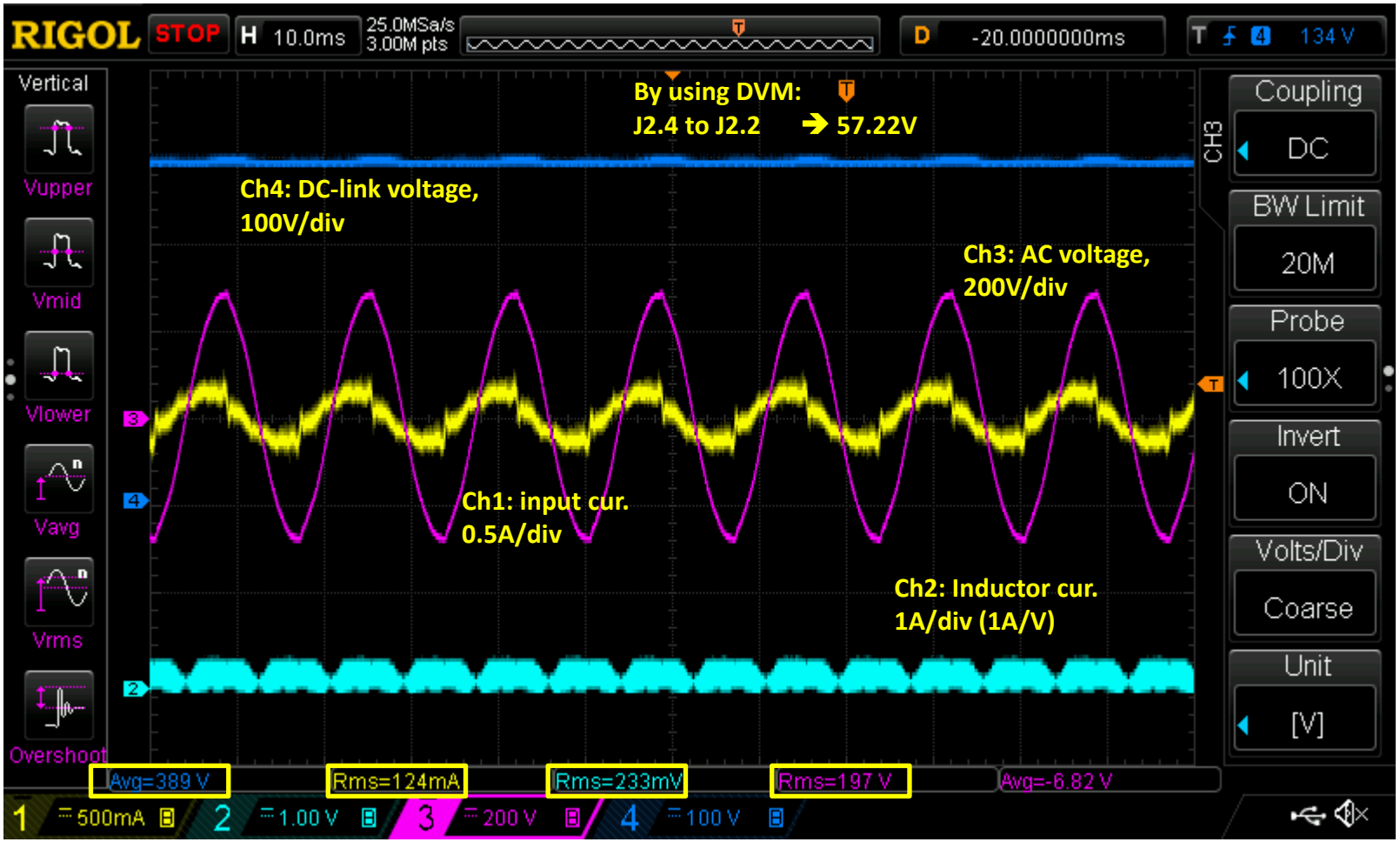
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At 200Vac, min loads on outputs at J1 and J2 connectors

output=389Vdc, input cur. = 0.124Arms, inductor cur. = 0.233Arms, Sin=24.8VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

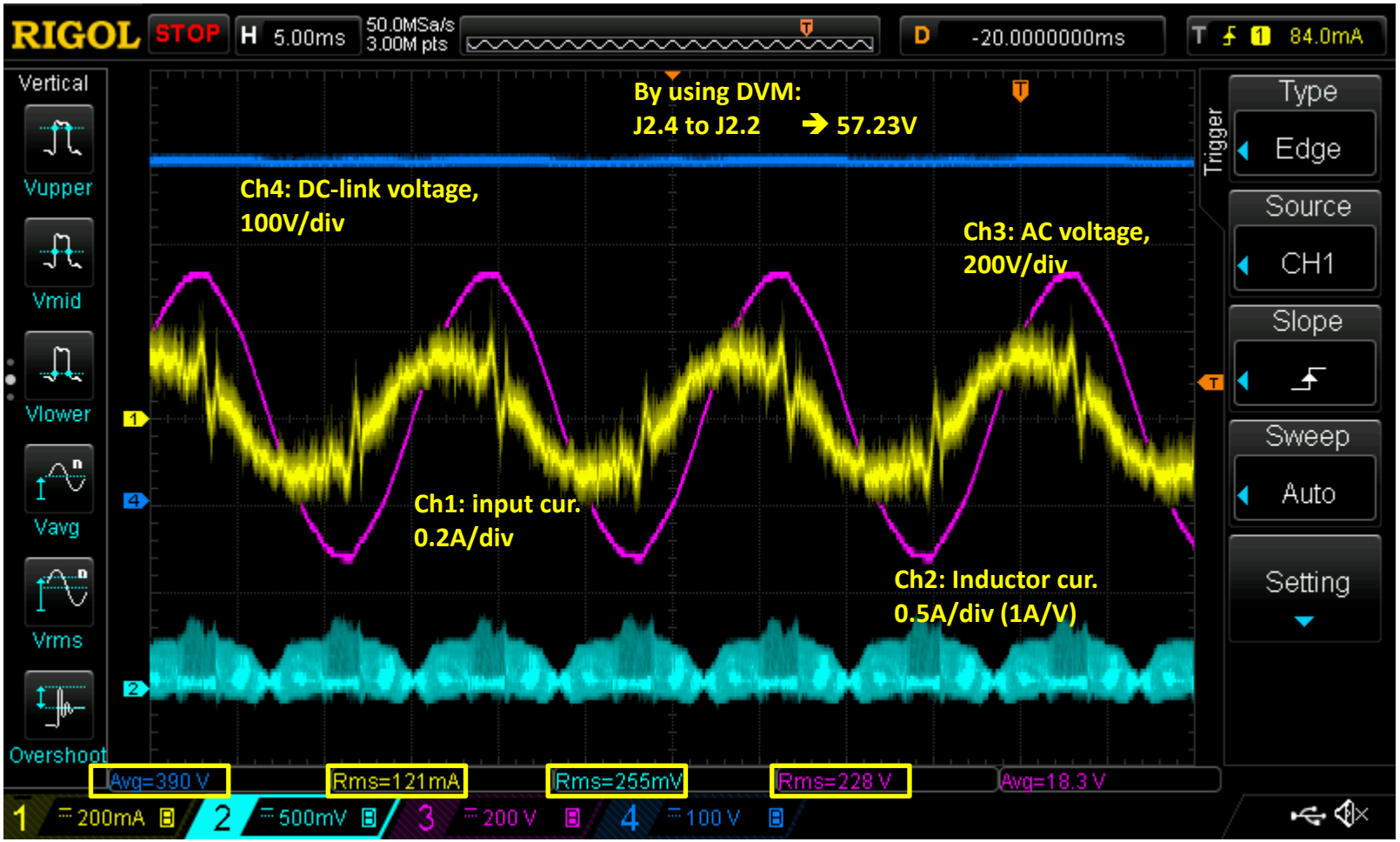
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At 230Vac, min loads on outputs at J1 and J2 connectors

output=390Vdc, input cur. = 0.121Arms, inductor cur. = 0.255Arms, Sin=27.8VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

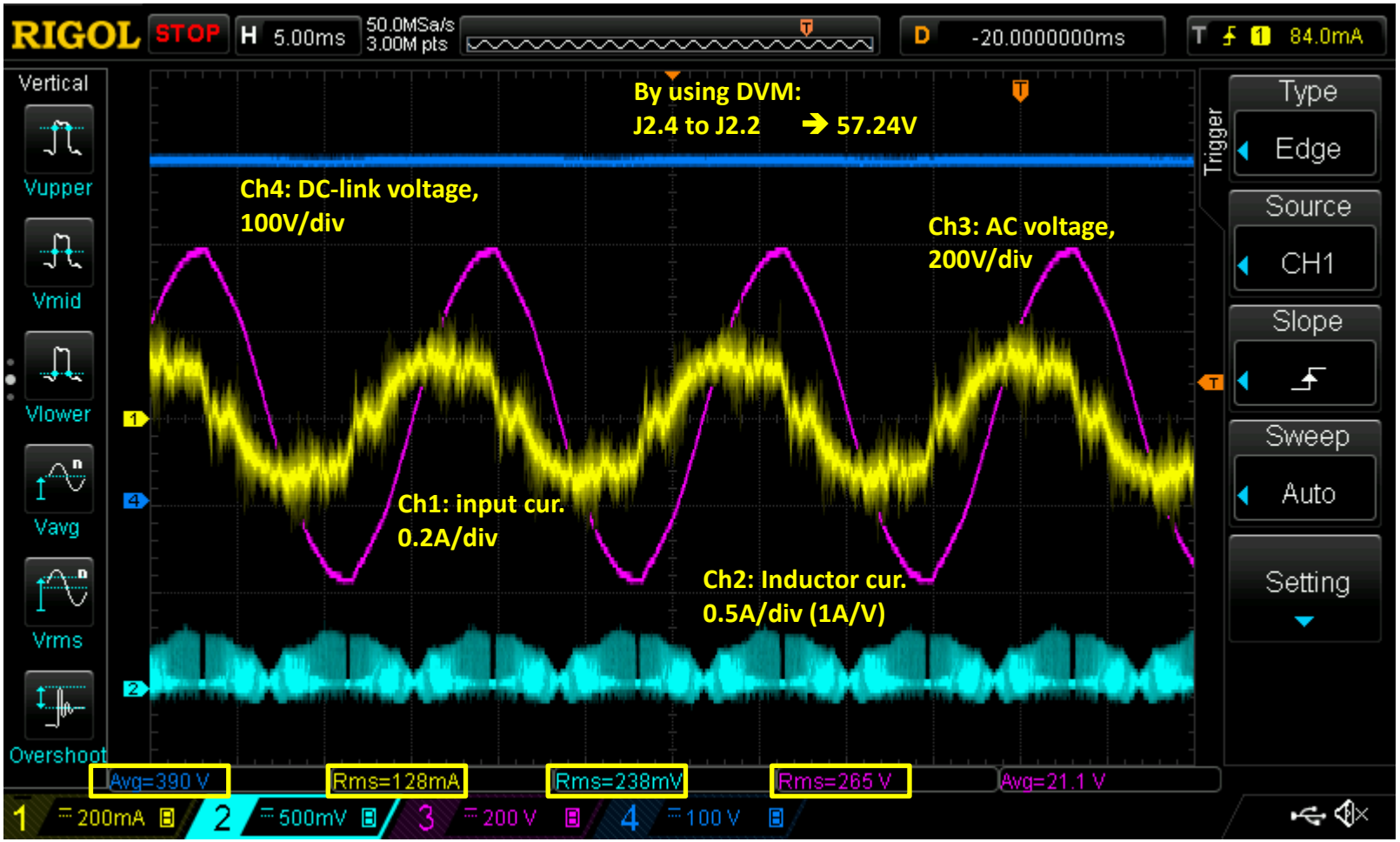
PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At 265Vac, min loads on outputs at J1 and J2 connectors

output=390Vdc, input cur. = 0.128Arms, inductor cur. = 0.238Arms, Sin=33.9VA (poor PF)



Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

With minimum resistive load on secondary stage DC/DC converter, from 85Vac to 265Vac input voltage, stable DC-link voltage regulation and distortion free PFC stage input currents are obtained

Dc-Link load (kΩ)	Input voltage (Vrms) By using Diff Probe	DC-link w/ DVM (Vdc)	Input current (Arms)	Inductor current (Arms)	Input power (VA)	Comments
12.5	85	388	0.220	0.274	18.70	OK PF, no major distortions
	120	389	0.171	0.316	20.52	OK PF, minor distortions
	200	389	0.124	0.233	24.80	Poor PF, no major distortions
	230	390	0.121	0.255	27.83	
	265	390	0.128	0.238	33.92	

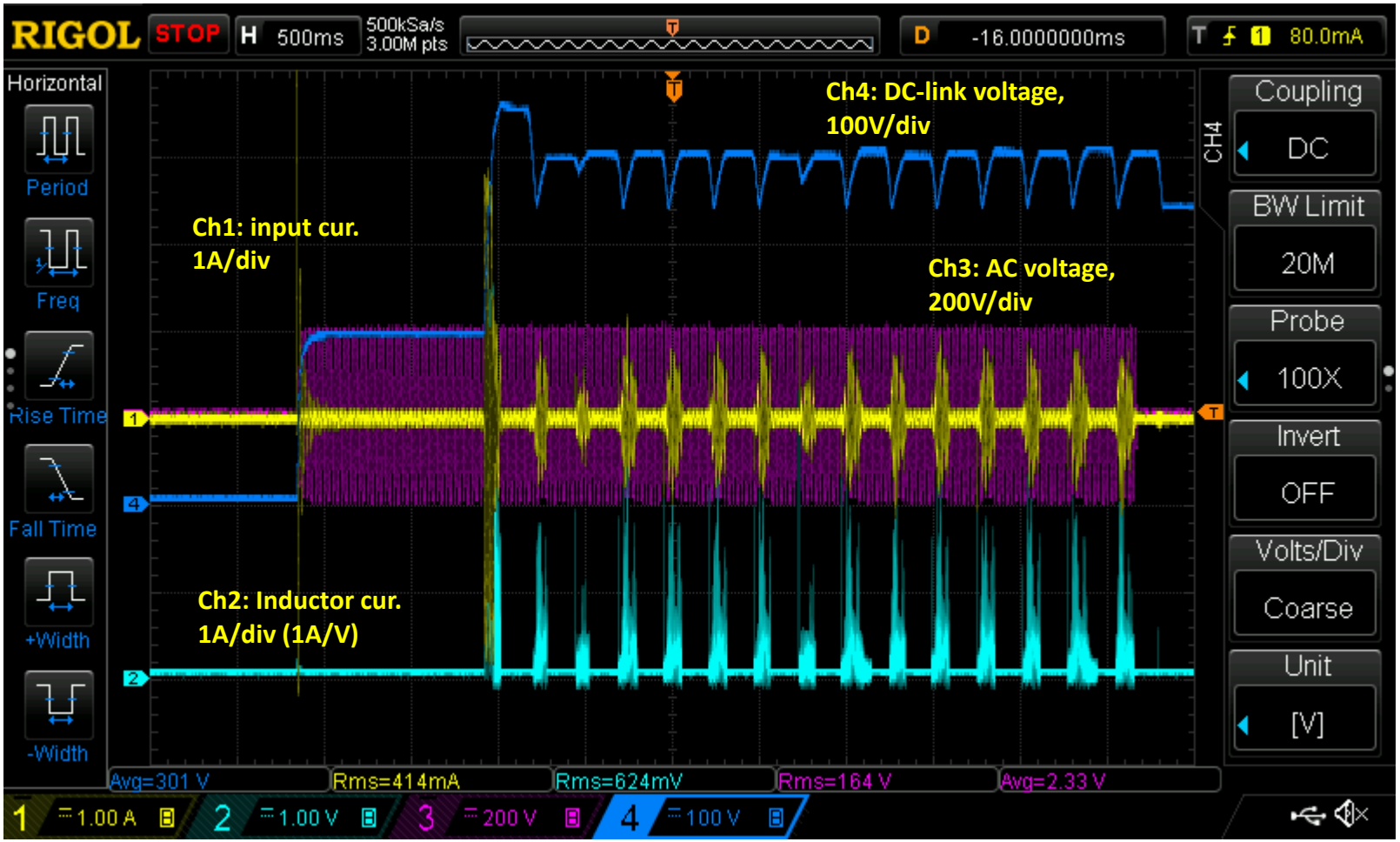
Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At ~120Vac, max loads on outputs at J1 and J2 connectors



DC-link voltage regulation does not work with max output power

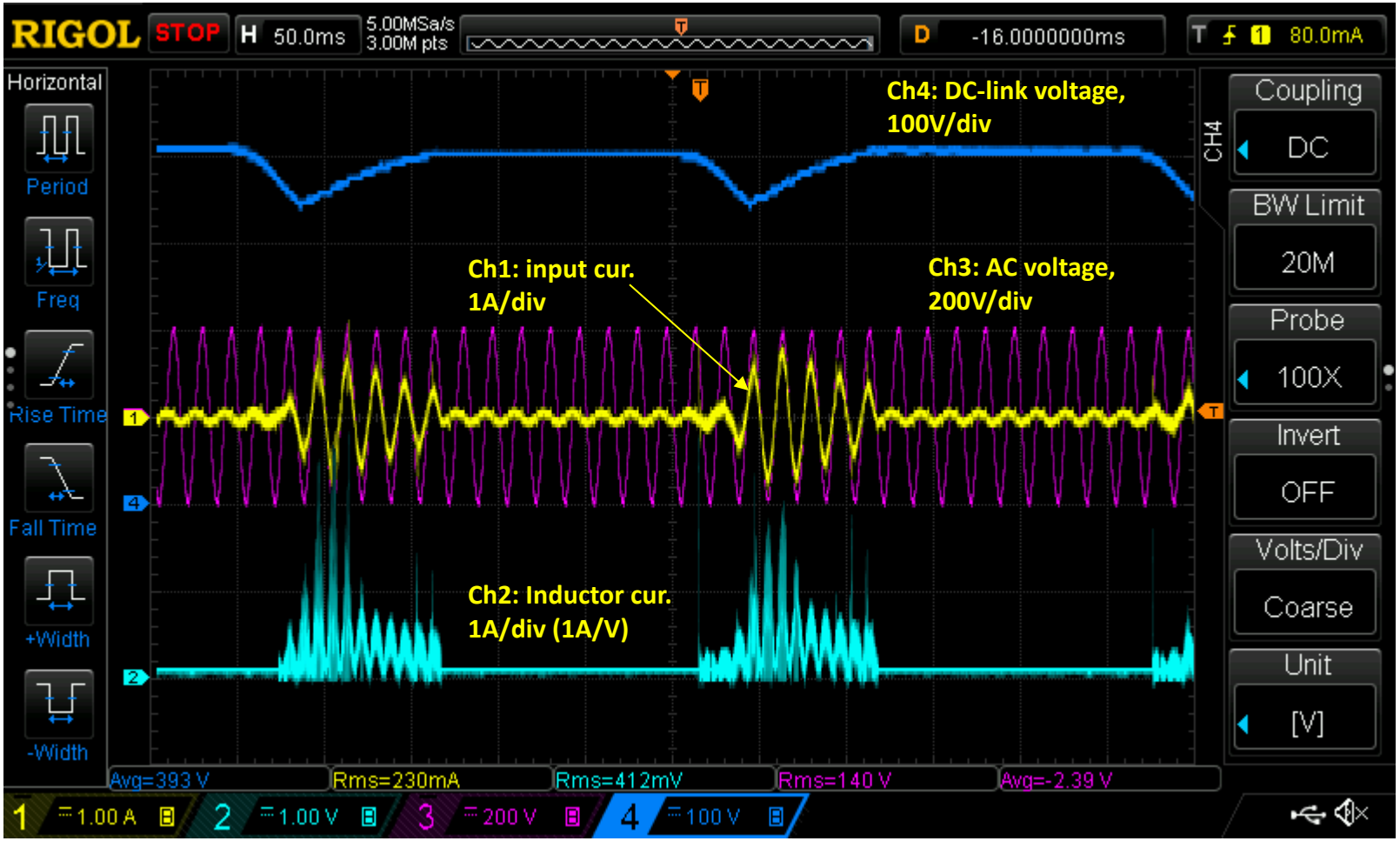
Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

At ~140Vac, max loads on outputs at J1 and J2 connectors



With output dc/dc converter and max load is connected on J1/J2 connectors, the DC-link voltage regulation is not stable.

Measuring inductor current vs gate voltages, 8/6/2023

PSB-04, PFC-03, CONT A w/ PFC board ,SN: AG155544221261437

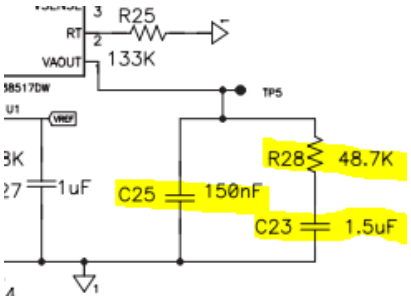
L1, Q5, Q6 (PN: IRFPC50A) on PSB **are installed**, R43=0.47Ω (PN:MOSX5CR47J), boost ind. is TSD-5033 and 6" away from PSB

See slides 162 and 163 for circuit configuration

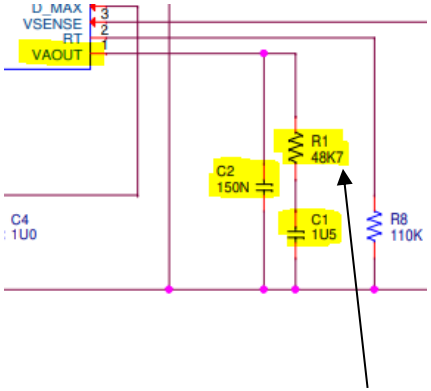
Conclusions:

- With PFC stage only, without secondary stage DC/DC converter, at min AC voltage and max load on DC-link, the DC-link voltage was lower than the set point (360V vs 390V)
- With PFC stage followed by secondary stage DC/DC converter, at low AC voltages and max load on dc/dc converter, the DC-link voltage was not stable and had oscillations.
- Below are the voltage feedback circuit used in the design:

Voltage feedback compensator from UCC28513 data sheet



Voltage feedback compensator used in PFC board (prior to modifications shown on slides 162/163)



Changed to 100K per slides 162/163

UCC3817 voltage feedback circuit shown for reference