LM(2)5190(-Q1) CCCV Buck Converter Design Tool

WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems
PHOENIX DESIGN CENTER | TEXAS INSTRUMENTS

Wide Input Voltage

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Step 1: Operating Specifications

Input Voltage – Min, $V_{SUPPLY(min)}$	**23.0**	**V**
Input Voltage – Typ, $V_{SUPPLY(typ)}$	**24.0**	**V**
Input Voltage – Max, $V_{SUPPLY(max)}$	**24.0**	**V**
Regulation Target in CV, V_{LOAD}	**23.5**	**V**
Regulation Target in CC / Full load current in CV, I_{LOAD}	**10.0**	**A**
Switching Frequency, f_{SW}	**470.0**	**kHz**
Switching Mode	**FPWM**	
Device P/N	**LM5190(-Q1)**	
Frequency Set Resistor, R_{RT}	49.9	kΩ

Step 2: Current Sense Resistor

Required Peak Inductor C/L Setpoint at $V_{SUPPLY(MAX)}$, I_{PEAKCL}	**12.0**	**Apk**
Recommended Maximum Sense Resistance	4.5	mΩ
Selected Sense Resistance, R_S	**4.0**	**mΩ**
Power Loss at C/L, P_{RS}	0.58	W

Step 3: Buck Inductor

Recommended Inductance for 40% Pk-Pk Ripple Current at $V_{SUPPLY(typ)}$	0.26	µH
Minimum Inductance	-0.16	µH
Selected Buck Inductance, L_{OUT}	**3.30**	**µH**
Peak Inductor Current at $V_{SUPPLY(max)}$ and Full Load (CV mode)	10.2	Apk
Peak Inductor Current Limit$_{(max)}$ at $V_{SUPPLY(max)}$	16.5	Apk
Switching Skip at $V_{SUPPLY(max)}$	doesn't happen	
Dropout Mode Operation at $V_{SUPPLY(min)}$	can happen	

Step 4: C_{VCC}, C_{BOOT}, C_{VIN}, R_{PGOOD}, T_{SSCV}

VCC Capacitor, C_{VCC}	2.2	µF
Boot Capacitor, C_{BOOT}	100	nF
VIN pin Capacitor, C_{VIN}	220	nF
Power Good Pull-up Resistor, R_{PGOOD}	100	kΩ
Internal Soft-start Time in CV mode, T_{SSCV}	2.75	ms

Step 5: Enable, UVLO

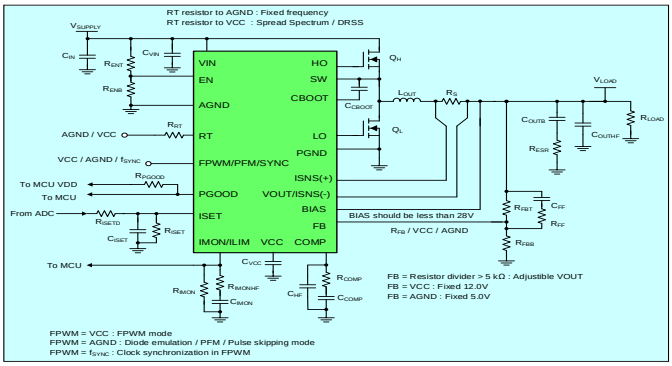
Desired Start-up Voltage	**4.0**	**V**
Upper Enable Resistor for UVLO, R_{ENT}	**100.0**	**kΩ**
Lower Enable Resistor for UVLO, R_{ENB}	35.59	kΩ
Estimated Shutdown Voltage	3.6	V

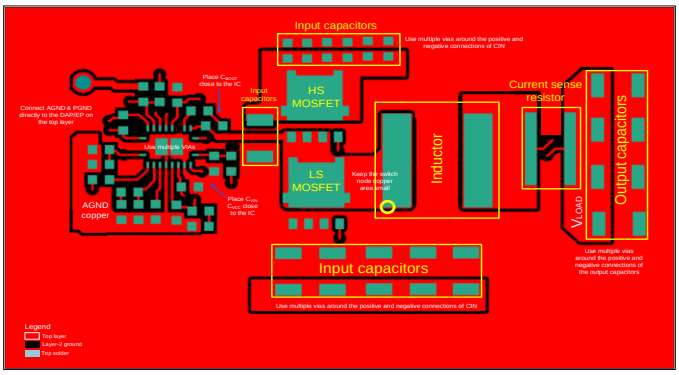
Step 6: Output Capacitors

Desired Undershoot during 50% Load Transient in FPWM (CV mode)	**6.0**	**%**
Desired Crossover Frequency, $f_{CROSS(desired)}$ (CV mode)	**28.0**	**kHz**
Minimum Derated Output Capacitance	20.2	µF
Rated Output Capacitance (Bulk/SuperCap), C_{OUTB}	**424**	**µF**
Derating Factor (Bulk/SuperCap)	**0.5**	
Derated Output Capacitance (Bulk/SuperCap)	212.0	µF
Effective Capacitor ESR (Bulk/SuperCap), R_{ESRB}	**5**	**mΩ**
Rated Output Capacitance (Ceramic Capacitor/Local C_{OUT}), C_{OUTHF}	**0.1**	**µF**
Derating Factor (Ceramic Capacitor)	**0.7**	
Derated Output Capacitance (Ceramic Capacitor)	0.1	µF
Effective Capacitor ESR (Ceramic Capacitor), R_{ESRHF}	**1**	**mΩ**
Derated Output Capacitance (Total)	212.1	µF
Estimated Output Voltage Ripple at $V_{SUPPLUY(max)}$ (CV mode)	0.1	mVpk-pk
Estimated Overshoot (when switching stops at full-load to no-load) (CV mode)	0.1	%
Estimated Undershoot (during no-load to full-load transition in FPWM) (CV mode)	7.5	%

Step 7: Feedback Resistors (CV mode)

Upper Feedback Resistance, R_{FBT}	**150.0**	**kΩ**
Lower Standard Feedback Resistance, R_{FBB}	5.29	kΩ





Step 8: Loop Compensation Design (CV mode)

Load Pole Frequency, f_{LP}	0.4	kHz
ESR Zero Frequency, f_{ESRZ}	149	kHz
Desired Maximum R_{COMP}	43.84	kΩ
Desired Minimum C_{COMP}	1.3	nF
Desired C_{HF}	24	pF
Desired Compensation Zero Frequency	2.80	kHz
Desired Compensation Pole Frequency	153	kHz
Selected R_{COMP}	**5.90**	**kΩ**
Selected C_{COMP}	**12.00**	**nF**
Selected C_{HF}	**47**	**pF**
Selected Compensation Zero Frequency, f_{COMPZ}	2.25	kHz
Selected Compensation Pole Frequency, f_{COMPP}	576	kHz
Selected Feedforward Capacitance, C_{FF}	**1**	**pF**
Selected Feedforward Resistance, R_{FF}	**1000**	**kΩ**
Selected C_{FF} Zero Frequency, f_{CFFZ}	1061	kHz

Step 9: ISET Components (CC mode)

Desired ISET Voltage, V_{ISET}	**1.80**	**V**
ISET Resistor, R_{ISET}	OPEN or 120	kΩ
Selected ISET Capacitor, C_{ISET}	**100**	**nF**
Current Regulation Soft-start Time, T_{SSCC}	10.0	ms

Step 10: Loop Compensation Design (CC mode)

Desired R_{IMON}	17.14	kΩ
Desired Minimum C_{IMON}	29.07	nF
Desired R_{IMONHF}	36.46	Ω
Desired IMON Pole Frequency	0.3	kHz
Desired IMON Zero Frequency	150	kHz
Selected R_{IMON}	**26.10**	**kΩ**
Selected C_{IMON}	**10.00**	**nF**
Selected R_{IMONHF}	**0.000**	**Ω**
Selected IMON Pole Frequency, f_{IMONP}	0.6	kHz
Selected IMON Zero Frequency, f_{IMONZ}	>2000	kHz

Step 11: Efficiency

Inductor			
Inductor DCR at 25°C, R_{DCR}		**3.9**	**mΩ**
Estimated Inductor Core Loss at $V_{SUPPLY(typ)}$		**1.6**	**W**
MOSFETs	**High-side**	**Low-side**	
On-State Resistance at 25°C, $R_{DS(on)}$	**0.5**	**0.5**	**mΩ**
Total Gate Charge, Q_G	**11**	**11**	**nC**
Gate-Drain Charge, Q_{GD}	**3**	**3**	**nC**
Gate-Source Charge, Q_{GS}	**5**	**5**	**nC**
Output Charge, Q_{OSS}		**7**	**nC**
Output Capacitance, C_{OSS}	**150**	**150**	**pF**
Gate Resistance, R_G	**1.0**	**1.0**	**Ω**
Transconductance, g_{FS}	**52**	**52**	**S**
Gate-Source Threshold Voltage, V_{TH}	**3.1**	**3.1**	**V**
Body Diode Forward Voltage, V_{BD}	**0.8**	**0.8**	**V**
Body Diode Rev Recovery Charge, Q_{RR}		**41**	**nC**
Thermal Resistance, θ_{JA}	**62**	**62**	**°C/W**
External Schottky Diode (if applicable)		**Low-side**	
Schottky Fwd Voltage, V_{FWDsch}		**0.0**	**V**
Schottky Rev Recovery Charge, Q_{RRsch}		**0**	**nC**

Step 12: IC Power Loss

External BIAS from V_{LOAD}	**Yes**	
Ambient Temperature (T_A)	**100**	°C
Estimated IC Power Dissipation, P_{IC}	0.25	W
Estimated Junction Temperature (eT_J)	111.0	°C
MOSFET driving current	10.34	mA

Step 13: Input Capacitors

Input Voltage Ripple Spec	**50**	**mVpk-pk**
Minimum Derated Input Capacitance, C_{IN}	106.4	µF
Maximum Input Capacitor RMS Current	5.0	A(rms)
Maximum Input Capacitor ESR	5	mΩ