Optimal Design for the Damping Resistor in RCD-R Snubber to Suppress Common-mode Noise

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***Abstract*—The RCD snubber is usually used in flyback converter, in order to limit the voltage spikes caused by leakage inductance of the transformer. But after the clamping diode in the RCD snubber turns off, the high frequency oscillations caused by the leakage inductance and intrinsic capacitance of the transistor is still serious due to the residual energy that can't be entirely absorbed by the clamping capacitor. These oscillations will generate unexpected CM noises at some particular frequencies. In practical applications, a damping resistor in series with the RCD circuit which is called RCD-R snubber in this paper can be used to suppress the CM noises. The goal of this paper is to analyze the RCD-R snubber circuit operations and to develop design guideline to optimal choose the value of the damping resistor. Both the theoretical analysis and experimental results verify that the RCD-R snubber circuit can suppress CM noise effectively and have no cost on the efficiency of the converter.**

I. INTRODUCTION

Dissipative RCD snubber is widely used in low power DC-DC applications for its simplicity and low cost. It can suppress voltage transient spikes effectively with some acceptable losses [1]-[4]. But due to the physical limitations, the energy stored in the leakage inductance of the transformer can't be entirely absorbed by the RCD snubber, which will cause high frequency oscillations between the leakage inductance and the intrinsic capacitance of the transistor. These oscillations not only can cause extra losses [5], but also will generate unexpected CM noises at some particular frequencies. Choosing smaller dissipative resistor in the RCD snubber can lower the clamping voltage of the capacitor and reduce the residual energy left in the circuit. But the efficiency of the converter will suffer from it.

The RCD-R snubber shown in Fig. 1 can decrease the residual energy left in the circuit. If the damping resistor R_d is well chosen, there won't be any residual energy left in the circuit after the clamping diode D_c turns off. So no oscillation between the leakage inductance and the intrinsic capacitance of the transistor can take place after D_c turns off and the CM noise caused by these oscillations can be suppressed. If R_d continues increasing, it will make no help to EMI performance, but the voltage spikes of the transistor Q_1 will increase.

In this paper, the working principle of the RCD-R snubber is studied in detail. A helpful method to optimal design the damping resistor is proposed. Both the theoretical analysis and experimental results verify that damping resistor can suppress CM noise effectively and have no cost on the efficiency of the converter.

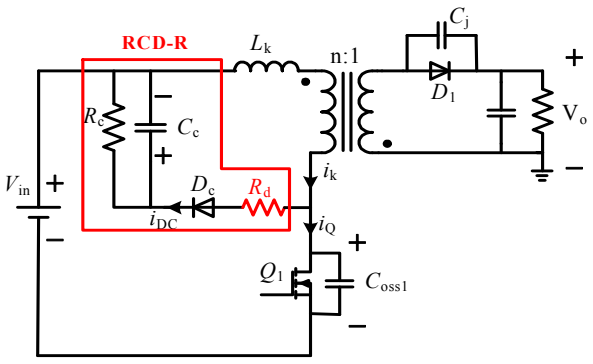

Figure 1. Flyback converter with RCD-R snubber.

II. OPERATION PRINCIPLES OF RCD-R SNUBBER

Fig. 2 shows the key operation waveforms of the flyback converter with RCD-R snubber shown in Fig. 1. i_{DC} is the current in the clamping diode D_c, V_{ds} and V_c are the voltage across the main transistor Q_1 and the capacitor C_c respectively. When Q_1 turns off, the transformer begins to transfer the energy stored during the on-time to the output. The voltage across the transformer is clamped to nV_o by the output voltage. But the energy stored in the leakage inductance can't transfer to the secondary-side, which will charge the intrinsic capacitance of the transistor C_{oss1} until t_0 when V_{ds} is charged to $V_{in} + V_{cp}$, V_{cp} is the clamping voltage of C_c. Then the diode D_c turns on. During the interval $t_0 - t_1$, the current is transferred from the transistor Q_1 to the RCD circuit.

Stage 1 (t_1-t_2): At t_1 the current in the transistor reaches the peak value I_F. The equivalent circuit of this stage is shown in Fig. 3. R_{trans_ac} is the ac resistance of the transformer. Because the RCD circuit is operating in high frequency, so R_{trans_ac} can't be ignored.

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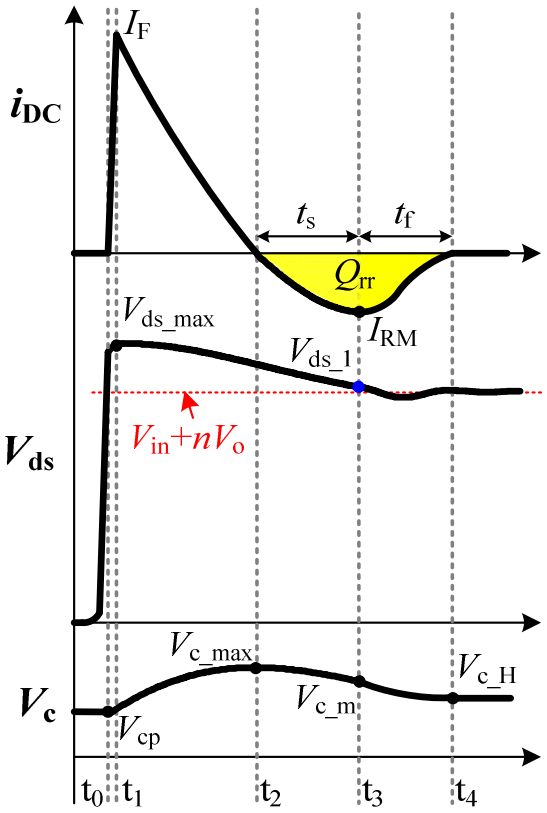

Figure 2. Operating waveforms

To evaluate the voltage of the clamping capacitor $v_c(t)$, apply Kirchoff's voltage law (KVL) around the loop in Fig. 3 gives

$$\frac{\partial^2 v_c}{\partial t^2}+\left(\frac{R_{eq}}{L_k}+\frac{1}{R_c C_c}\right)\cdot\frac{\partial v_c}{\partial t}+\frac{R_{eq}+R_c}{R_c L_k C_c}\cdot v_c=\frac{nV_o}{L_k C_c} \quad (1)$$

In which, $R_{eq}=R_d+R_{trans\_ac}$.

Assume that $v_c(t_1)\approx v_c(t_0)=V_{cp}$. V_{cp} is the clamping voltage of capacitor C_c, the initial voltage $v_c(t_1)$ and its derivative can be derived

$$v_c(t_1)=V_{cp} \quad (2)$$

$$\frac{dv_c(t_1)}{dt}=\frac{I_F}{C_c}-\frac{V_{cp}}{R_c C_c} \quad (3)$$

Then voltage $v_c(t)$ can be obtained as

$$v_c(t)=\frac{R_c\cdot nV_o}{R_{eq}+R_c}+e^{-b(t-t_1)}\left[A_1\cos(\omega_d(t-t_1))+A_2\sin(\omega_d(t-t_1))\right] \quad (4)$$

In which,

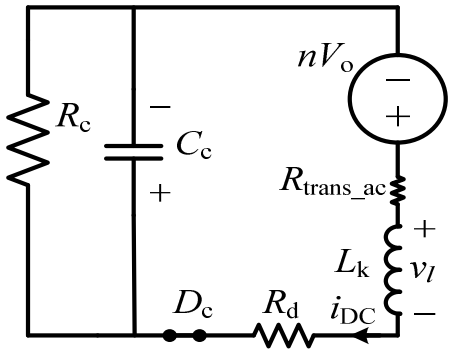

Figure 3. Equivalent circuit of Stage 1 and Stage 2

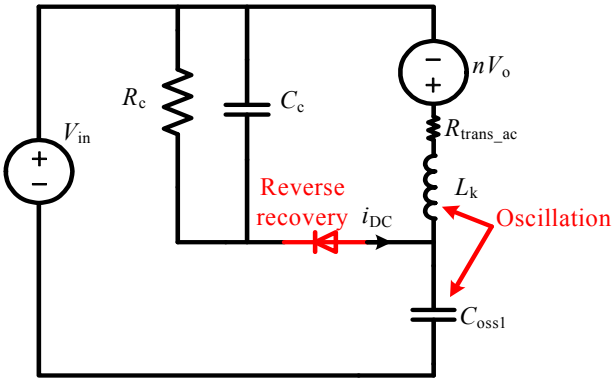

Figure 4. Equivalent circuit of Stage 3

$$b=\frac{R_{eq}R_c C_c+L_k}{2R_c L_k C_c} \quad (5)$$

$$\omega_d=\sqrt{\frac{2R_{eq}R_c C_c L_k+4R_c^2 L_k C_c-R_{eq}^2 R_c^2 C_c^2-L_k^2}{4R_c^2 L_k^2 C_c^2}} \quad (6)$$

$$A_1=\frac{V_{cp}(R_{eq}+R_c)+nV_o R_c}{R_{eq}+R_c}\quad A_2=\frac{bA_1 R_c C_c+I_F R_c-V_{cp}}{\omega_d R_c C_c} \quad (7)$$

From Equation (4), the maximal value of $v_c(t)$ at t_2 can be evaluated

$$V_{c\_max}=\frac{R_c\cdot nV_o}{R_{eq}+R_c}+e^{-\frac{\pi b}{2\omega_d}}\sqrt{A_1^2+A_2^2}=f(V_{cp}) \quad (8)$$

The voltage spike of the main transistor Q_1 can be evaluated approximately by

$$V_{ds\_max}\approx V_{in}+V_{cp}+I_F\cdot R_d \quad (9)$$

The current in the diode D_c can be evaluated similarly

$$i_{DC}(t)=\frac{nV_o}{R_{eq}+R_c}+e^{-b(t-t_1)}\left[B_1\cos(\omega_d(t-t_1))+B_2\sin(\omega_d(t-t_1))\right] \quad (10)$$

In which,

$$B_1 = \frac{I_F(R_{eq}+R_c)-nV_o}{R_{eq}+R_c} \quad B_2 = \frac{bB_1L_k + nV_o - V_{cp} - I_F R_{eq}}{\omega_d L_k} \quad (11)$$

In Equation (4), (8), (9) and (10), only V_{cp} is the unknown variable that related with the RCD-R snubber, all the other parameters are constants for a particular converter.

Stage 2 (t_2-t_3): Although i_{DC} reaches zero at t_2, the diode continues to conduct until t_3 at which point all the stored charge has been removed from the diode. So this stage could also be modeled by the equivalent circuit shown in Fig. 3. Equations (4) and (10) are also valid for this stage.

Stage 3 (t_3-t_4): At t_3 the charges stored have been removed from the diode, and then the diode starts blocking. Reverse recovery losses occur during this stage since negative current is present while the blocking voltage across the diode increases. The equivalent circuit of this stage is shown in Fig. 4. The reverse recovery of the diode and the ringing between L_k and C_{oss1} takes place at the same time.

It can be found that, the reason that caused oscillation between L_k and C_{oss1} is the residual energy left in the circuit when D_c starts blocking. This residual energy is mainly stored in C_{oss1}.at t_3. The voltage of V_{ds} at t_3, marked as $V_{ds\text{-}1}$, can be evalusted by

$$V_{ds\_1} = V_{in} + V_{c\_m} - I_{RM} \cdot R_d \quad (12)$$

In which, $V_{c\text{-}m}$ is the voltage of V_c at t_3, I_{RM} is the peak reverse recovery current D_c at t_3.

So, if $V_{ds\text{-}1}$ is equal to $V_{in} + nV_o$, there will be almost no residual energy left in the circuit and little oscillation can take place any more.

Stage 4 [t_4-(t_0+T)]: After t_4 the energy stored in C_c will be dissipated by R_c until Q_1 turns on again.

The reference directions are shown in Fig. 5, so

$$i_c(t) = C_c \cdot \frac{dv_c(t)}{dt} = -\frac{v_c(t)}{R_c} \Rightarrow \frac{1}{v_c(t)} \cdot dv_c(t) = -\frac{1}{C_c R_c} \cdot dt \quad (13)$$

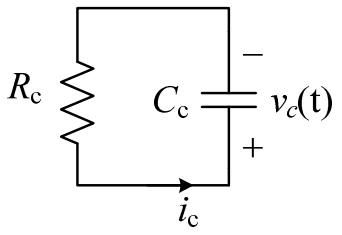

Figure 5. Equivalent circuit of Stage 4

Apply integration to (13) in one period T yields:

$$\begin{aligned} &\int_{t_4}^{t_4+T} \frac{1}{v_c(t)} \cdot dv_c(t) = \int_{t_4}^{t_4+T} -\frac{1}{C_c R_c} \cdot dt \\ &\Rightarrow \ln v_c(t_4+T) - \ln v_c(t_4) = -\frac{T}{C_c R_c} \end{aligned} \quad (14)$$

According to the capacitor charging balance, there has $v_c(t_4+T) = V_{cp}$. Substitute this equation into (14) yields

$$\ln V_{cp} - \ln V_{c\_H} = -\frac{T}{C_c R_c} \quad (15)$$

In which, $V_{c\text{-}H}$ is the voltage of V_c at t_4, T is the working period of the converter.

III. Optimal Design for RCD-R Snubber and Power Losses Analyse

A. Diode reverse recovery modeling

The reverse recovery of the diode is an important issue. Only the reverse recovery of the diode is precisely modeled, can the RCD-R snubber be well designed. [6] indicates that the reverse recovery charge is a function of the diode's forward current at the initiation of the turn-off process and the *di*/*dt* when forward current decreases. In this circuit the current in the diode oscillates to zero when the diode turns off. So the reverse recovery charge Q_{rr} can be fitted to di_{DC}/dt by using a high order polynomial which provides a good fit of the original data, so

$$Q_{rr} = f(x) = a_n x^n + a_{n-1} x^{n-1} \cdots a_1 x + a_0 \quad (16)$$

x refers to the value of di_{DC}/dt at t_2, which can be evaluated from

$$\left.\frac{di_{DC}}{dt}\right|_{t=t_2} = \frac{v_{l_k}(t_2)}{L_k} = \frac{nV_o - V_{c\_\max}}{L_k} \quad (17)$$

In which $V_{c\text{-}max}$ is the value of $v_c(t)$ at t_2. During the period t_2-t_4 when reverse recovery of the diode takes place, it can be derived that

$$C_c \cdot (V_{c\_\max} - V_{c\_H}) = Q_{rr} \quad (18)$$

In which, V_{c_H} is the voltage of V_c at t_4.

Combine (16) and (18) gives

$$V_{c\_\max} - V_{c\_H} = \frac{Q_{rr}}{C_c} = g(y) = b_n y^n + b_{n-1} y^{n-1} \cdots b_1 y + b_0 \quad (19)$$

In which, $y = nV_o - V_{c\_max}$, $b_i = a_i / C_c L_k$

To apply polynomial regression to (19), data points must first be selected to adequately describe the Q_{rr} surface. Solving (19) then produces a surface which provides a best fit by minimizing the squared error between the surface and the original data.

Then the time interval t_s when the stored charge is extracted from the diode, as shown in Fig. 2, can also be modeled by a high order polynomial similarly

$$t_s = h(y) = c_n y^n + c_{n-1} y^{n-1} \cdots c_1 y + c_0 \tag{20}$$

B. *Solving the variables related with the RCD-R snubber*

Combine the equations (8), (15) and (19) can solve the three unknown variables V_{cp}, V_{c_max} and V_{c_H}.

Substitute equation (20) into equations (4) and (10) can solve the values of v_c and i_{DC} at t_3, respectively.

$$V_{c\_m} = v_c(t_2 + t_s) \tag{21}$$

$$I_{RM} = i_{DC}(t_2 + t_s) \tag{22}$$

Up till now, all the variables related with the RCD-R snubber have been evaluated. It's important to notice that, Different from the conventional analysis that assume the voltage of the clamping capacitor keeps invariant when the clamping diode is on, in this paper the charging procedure of the clamping capacitor is modeled precisely. Moreover, the reverse recovery of the clamping diode is also taken into consideration. So the calculating result in this paper is much closer with the reality.

C. *Design procedure for R_d*

It has been mentioned in section II that, if $V_{ds\text{-}1}$ is equal to $V_{in} + nV_o$, there will be almost no residual energy left in the circuit and little oscillation can take place any more. Thus, let Equation (12) equal to $V_{in} + nV_o$ yields

$$V_{c\_m} - I_{RM} \cdot R_d = nV_o \tag{23}$$

Substitute (21) and (22) into (23) yields

$$v_c(t_2 + t_s) - R_d \cdot i_{DC}(t_2 + t_s) = nV_o \tag{24}$$

Solving Equation (24) can evaluate the optimal designed value of R_d as

$$R_d = \frac{v_c(t_2 + t_s) - nV_o}{i_{DC}(t_2 + t_s)} \tag{25}$$

D. *Calculating the power losses in the RCD circuit*

The losses in the RCD circuit can be divided into two parts: the losses caused during t_0-t_4 when the diode is on, and the losses caused during t_4-(t_0+T) when the energy in C_c is dissipated by R_c. The former losses W_1 can be determined from the energy balance requirement [1]:

Loss = energy from source – increase in energy stored in capacitor – increase in energy stored in inductor. So,

$$\begin{aligned} W_1 &= nV_o \int_{t_0}^{t_4} i\,dt - C_c \int_{v(t_0)}^{v(t_4)} v\,dv - L_k \int_{i(t_0)}^{i(t_4)} i\,di \\ &= nV_o \cdot C_c(V_{c\_H} - V_{cp}) - \frac{1}{2} C_c(V_{c\_H}^2 - V_{cp}^2) + \frac{1}{2} L_k I_Q^2 \end{aligned} \tag{26}$$

The losses dissipated by R_c is

$$W_2 = \frac{1}{2} C_c(V_{c\_H}^2 - V_{cp}^2) \tag{27}$$

Then the total power losses dissipated in the RCD circuit is

$$P_{loss} = f \cdot (W_1 + W_2) = f \cdot \left[nV_o \cdot C_c(V_{c\_H} - V_{cp}) + \frac{1}{2} L_k I_Q^2 \right] \tag{28}$$

IV. Experimental Verification

A 24 Watts, 100kHz, 170V input, 16V output flyback converter is built up to illustrate the design procedure for R_d in the RCD-R circuit and verify the analysis given above. The key components and parameters are shown in table I.

TABLE I. KEY COMPONENTS AND PARAMETERS

Q_1	D_1	Transformer	n	D_c
SPA11N60C	STPS20S100	PQ26/20/TP4	24:4	FR107

R_c	L_k	C_c	V_o	f
47kΩ	5.7uH	2.2nF	16V	100kHz

$V_{ds\text{-}1}$ and P_{loss} can be evaluated by Equations (12) and (28), respectively. They are plotted in Fig. 6 as a function of the damping resistor R_d. If V_{ds_1} equals to $V_{in} + nV_o$, there will be almost no residual energy left in the circuit and little oscillation can take place any more. Fig. 6 indicates the optimal design point R_d = 62Ω that can eliminate almost all the oscillations caused by the leakage inductance and intrinsic capacitance of the transistor.

The calculated power losses in the RCD circuit P_{loss} is also plotted in Fig. 6, which indicates that as R_d increases, the power losses in the RCD circuit will decrease slightly. But the decrement is too small that the measured efficiency remains almost the same with different R_d as shown in Fig. 7, which indicates that the RCD-R snubber won't cause extra power losses compare with the RCD snubber with the same parameters.

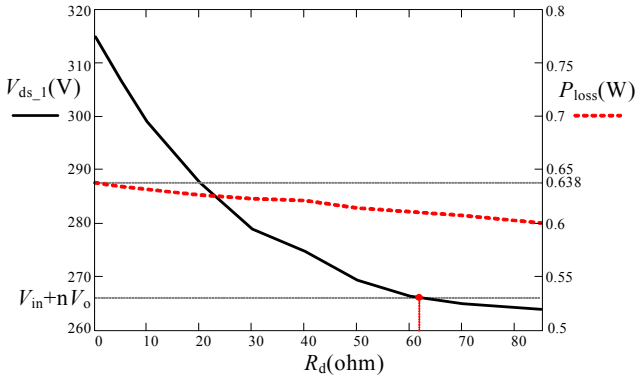

Figure 6. Optimal design for R_d and the calculated power losses in the RCD-R snubber

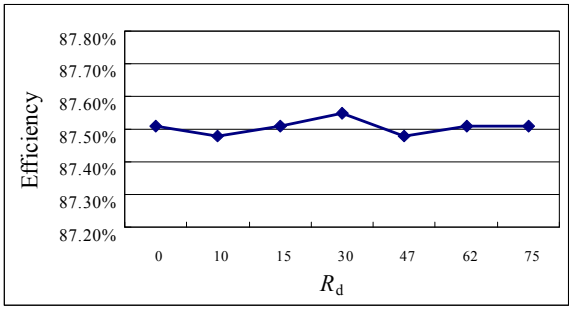

Figure 7. Measured efficiency with different R_d

Fig. 8 (a) and (b) shows the experimental waveforms of this flyback converter with optimal designed R_d = 62Ω and without R_d respectively. V_{ds} is voltage across the main transistor, i_{DC} is the current in the clamping diode. In Fig. 8 (a) no oscillation takes place in the waveform of V_{ds} any more. On the contrary, in Fig. 8 (b) there are serious high frequency oscillations appear in the waveform of V_{ds} after the clamping diode turns off. The frequency of these oscillations is determined by the leakage inductance and intrinsic capacitance of the transistor at around 8.6MHz, which is measured in Fig. 8 (b).

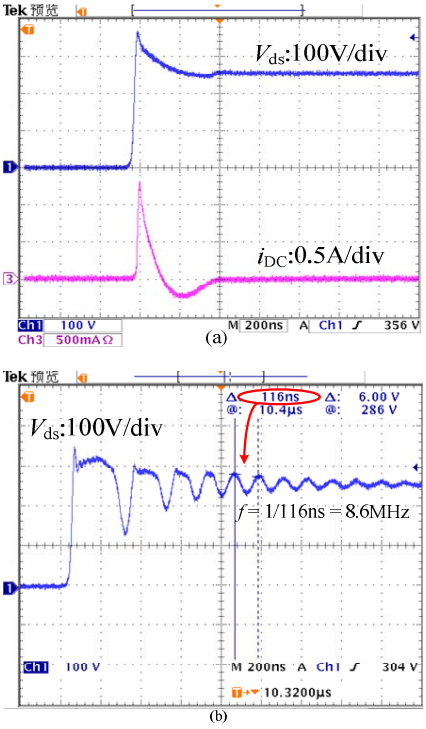

Figure 8. (a) Experimental waveforms of V_{ds} and i_{DC} when R_c=47kΩ, R_d=62Ω (b) Experimental waveform of V_{ds} when R_c=47kΩ, R_d =0

The CM noises of this topology when the converter is with and without damping resistor R_d are both tested. The curves of the tested EMI noise are shown in Fig. 9, in which curve ***A*** is tested without R_d and curve ***B*** is tested with R_d=62Ω. Please be aware that all the CM noises are tested without any EMI filter. Curve ***A*** has CM noise spikes at around 8.6 MHz, which is consistent with the oscillation frequency between the leakage inductance and intrinsic capacitance of the transistor as shown in Fig. 8 (b). The CM noise spikes around this frequency point are suppressed in curve ***B***, because with well designed R_d no oscillation between the leakage inductance and intrinsic capacitance of the transistor can take place any more.

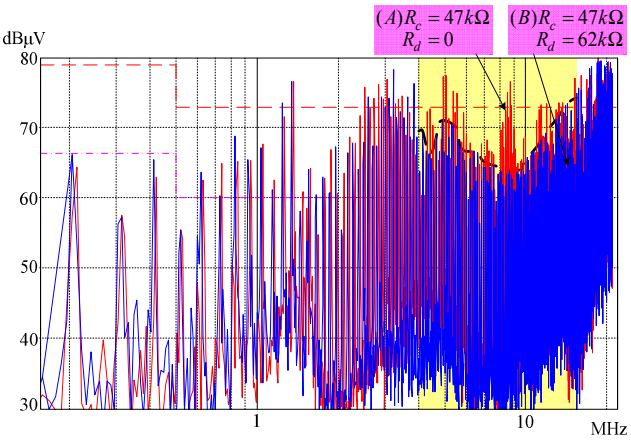

Figure 9. Comparison the effect of CM noise reduction with damping resistor R_d

V. CONCLUSION

RCD-R snubber can suppress the CM noise caused by the high frequency oscillation between the leakage inductance and intrinsic capacitance of the transistor. Different from the general concept that the improvement on EMI performance always at the cost of efficiency. The power loss in the RCD-R snubber is almost the same as in the RCD snubber with the same parameters, but the CM noise can benefits much from the RCD-R snubber. The working principle of RCD-R snubber is studied in detail. A novel design procedure is obtained to choose the value of the damping resistor.

ACKNOWLEDGMENT

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