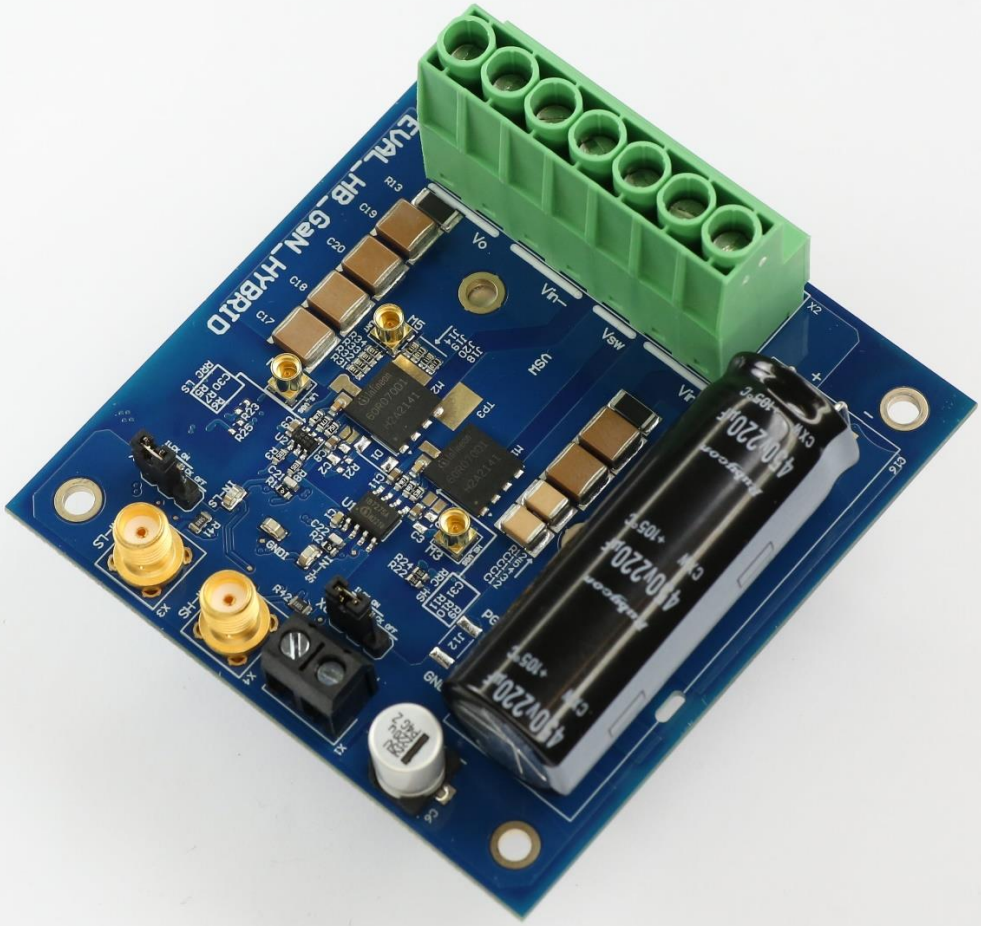


WHITEPAPER

# Gate drive configurations for GaN power transistors

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# Table of contents

# 1 Introduction

A proper gate control is crucial for system performance. This is valid for all power switches, and it is valid for gallium nitride (GaN) switches, too. Among the different GaN technologies available on the market, Infineon's portfolio comprises both common enhancement-mode (normally-off) concepts. They utilize a p-doped gate to shift the threshold voltage from the inherently negative value (normally-on) to a positive value. Depending on the realization of the gate contact, the resulting devices are either referred to as "gate injection transistor" (GIT) with an ohmic gate contact or as "Schottky gate transistor" (SGT) with an isolated gate structure similar to that of MOSFETs. While GITs are exclusively used in high-voltage applications (up to 700 V), SGTs cover a broader voltage range from 100 to 700 V. Essentially, the gate drive considerations discussed in this document are valid for all voltage classes.

All GaN switches are characterized by low terminal capacitances, and this results in a gate charge that is almost an order of magnitude lower than that of their silicon counterparts. Thus the driving capability of standard MOSFET drivers is usually more than sufficient for driving GaN transistors. However, there is a parameter typical for enhancement-mode (e-GaN) switches that significantly influences gate drive concepts. It is the low threshold voltage of the p-GaN gate, typically only slightly above +1 V. This has severe consequences:

– a relatively small gate current for switch-off at zero gate voltage
– an increased sensitivity with respect to cross-conduction in half-bridge applications

Both these effects can be mitigated by using a negative gate drive voltage. But there are also drawbacks associated with this measure, as a negative gate drive causes an increased voltage-drop in reverse (third quadrant) operation and thus higher conduction losses during dead-time. The optimum gate drive thus always depends on basic application conditions (hard/soft-switching, power class, switching voltage, frequency, etc.).

This whitepaper gives a compact overview of the recommended gate drive concepts for both GIT and SGT product families. A versatile standard drive (RC interface) can be easily adapted to both technologies. The document also provides basic gate drive dimensioning guidelines and some typical application examples.

# 2 Overview of standard GaN gate drive solutions

These solutions are characterized by utilizing standard gate drivers, acting as low impedance voltage sources to drive the GaN gate. In general, a passive interface then adapts the gate driver to specific GaN requirements.

## 2.1 RC interface

Although the RC interface is a natural solution for driving a GIT, it can also be adapted to drive an SGT. The main advantage in both cases is the generation of a well-defined negative gate drive voltage.

### 2.1.1 RC interface for GIT

The GIT is characterized by a non-isolated gate with a diode-like input characteristic. In the equivalent circuit of **Figure 1** this is indicated by the diode located between the gate and source, with a forward voltage drop $V_F$ of about 3.5 V.

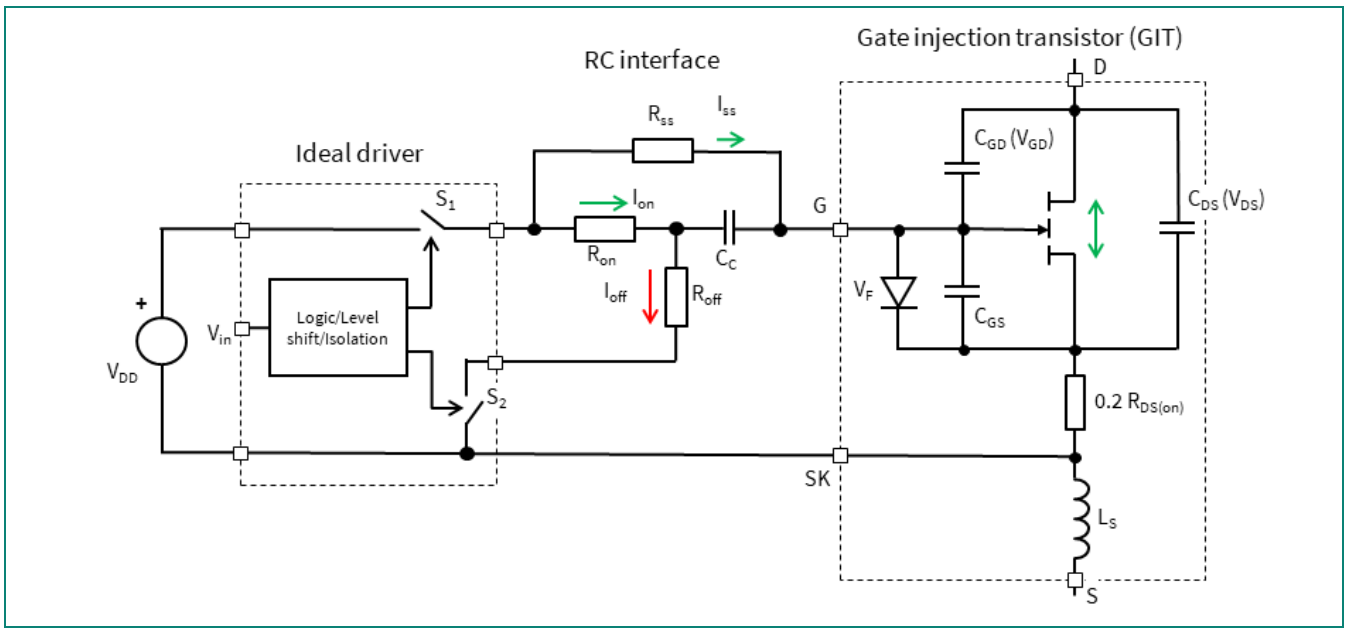


Figure 1 Equivalent circuit of CoolGaN™ GIT and a standard gate drive with RC interface

It is evident that the GIT gate structure is not compatible with standard MOSFET driving schemes, because a low-impedance voltage drive would cause unacceptably high current through the gate diode. But the standard way to drive a GIT is nevertheless simple. As shown in **Figure 1**, an interface consisting of a coupling capacitance $C_C$ and resistors $R_{on}$, $R_{off}$, and $R_{SS}$ is added to a standard gate driver supplied with voltage $V_{DD}$. A gate driver from Infineon's EiceDRIVER™ product family **[6]** or a comparable one can in most applications be regarded as "quasi-ideal", i.e., it has only a small or even negligible influence on the switching behavior which is mainly controlled by the external components. The ideal driver is characterized by:

- low-impedance outputs with high current capability
- true rail-to-rail operation
- a low input-to-output delay with very small random variations
- a galvanic input-to-output isolation (up to 8 kV)

In the steady "on"-state, the best way to drive a GIT's gate is by a small, constant gate current Iss. This ensures stable operating conditions, independent of temperature, load current, or parameter variations. $I_{SS}$ is defined by the driver-supply $V_{DD}$ and the relatively high $R_{SS}$. A low-impedance path in parallel, formed by $R_{on}/C_C$ for turn-on and $R_{off}/C_C$ for turn-off, provides the higher current needed during fast-switching transitions. **Figure 2**, left, shows the resulting current waveform.

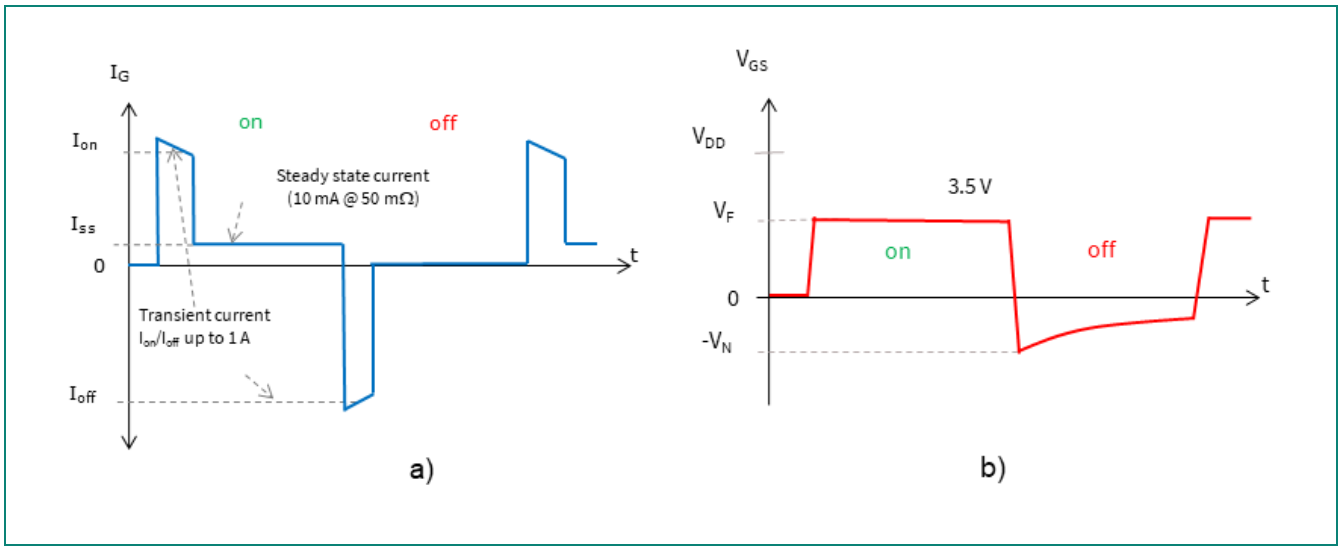


Figure 2 Typical gate current and gate voltage waveforms for GIT

As a very valuable feature of this approach, the coupling capacitance $C_C$ not only provides the high-current path, but also generates a negative gate drive voltage VN in the "off"-state. This is possible because during the preceding "on"-state (S1 closed), $C_C$ is charged to the difference of the driver supply $V_{DD}$ and gate diode clamping voltage $V_F$. By switching to the "off"-state (closing S2), $C_C$ acts as a charge pump, driving the gate to a negative voltage with an initial value of $-V_N$ that is defined by the total gate charge $Q_{Gtot}$ (corresponds to $Q_G$ in the datasheet), gate driver supply voltage $V_{DD}$, and coupling capacitance $C_C$, according to the relation

$$-V_N = -\frac{C_C \cdot (V_{DD} - V_F) - Q_{Gtot}}{C_C + C_{GS}} \quad (1)$$

While for soft-switching systems, usually a $-V_N$ value of –2 V to –3 V is sufficient, a value of –3 V to –5 V is a good choice in most hard-switching applications. After the "off"-transition $-V_N$ decays at a time constant given by $C_C$ and $R_{SS}$ (Figure 2b). This time constant is typically in the range of a few microseconds; it is essentially defined by the switch parameters (gate charge and steady-state gate current).

A negative gate drive voltage not only enables the usually intended fast switching "off", but it is also beneficial during hard commutations in a half-bridge to protect the passive device from turning "on" and causing cross-conduction. Details of this very important mechanism, sometimes also referred to as "spurious turn-on" or "shoot-through", are explained in the Appendix.

In many cases the hard commutation occurs soon after switching "off" the passive device. In other words, the dead-time with both switches in the "off"-state is short (complementary switching). The initial VN is sufficiently large to prevent cross-conduction, and the following decay of VN is even beneficial, as any negative gate drive increases the voltage drop in diode operation. The tradeoff of reduced cross-conduction versus increased dead-time losses is inevitably associated with negative gate drive.

In certain applications, however, both switches in a half-bridge can be in the "off"-state for a longer period (non-complementary switching). Then, due to the discharging of $C_C$ (decay of $V_N$), the RC interface may no longer guarantee sufficient suppression of cross-conduction. In this case the use of a bipolar supply voltage can be an option (Section 2.2).

Figure 1 also shows a separate source connection SK (Kelvin source) as the reference for the gate driver IC. Using the SK pin, any influence from the source inductance $L_S$ on the gate loop is avoided. All discrete switches in Infineon's GIT portfolio offer such a Kelvin source connection. It is not available in integrated power stages (IPS) that combine two GaN switches in half-bridge configuration with dedicated gate drivers in a common package.

### 2.1.2 RC interface for SGT

A GaN switch with a Schottky gate contact lacks the internal gate diode. Thus the equivalent circuit looks very similar to that of a MOSFET, and basically can be driven like a MOSFET, by applying a driving voltage to the gate via a low-impedance driver plus a gate resistor. Nevertheless, specific GaN aspects have to be considered. For a Schottky gate GaN switch, the optimum gate voltage range in the "on"-state is relatively small (typically 5 V to 6 V). And again, due to the low threshold, a negative gate drive can be beneficial to allow fast switching "off" and to avoid cross-conduction, particularly in hard-switched applications at higher voltage and power levels.

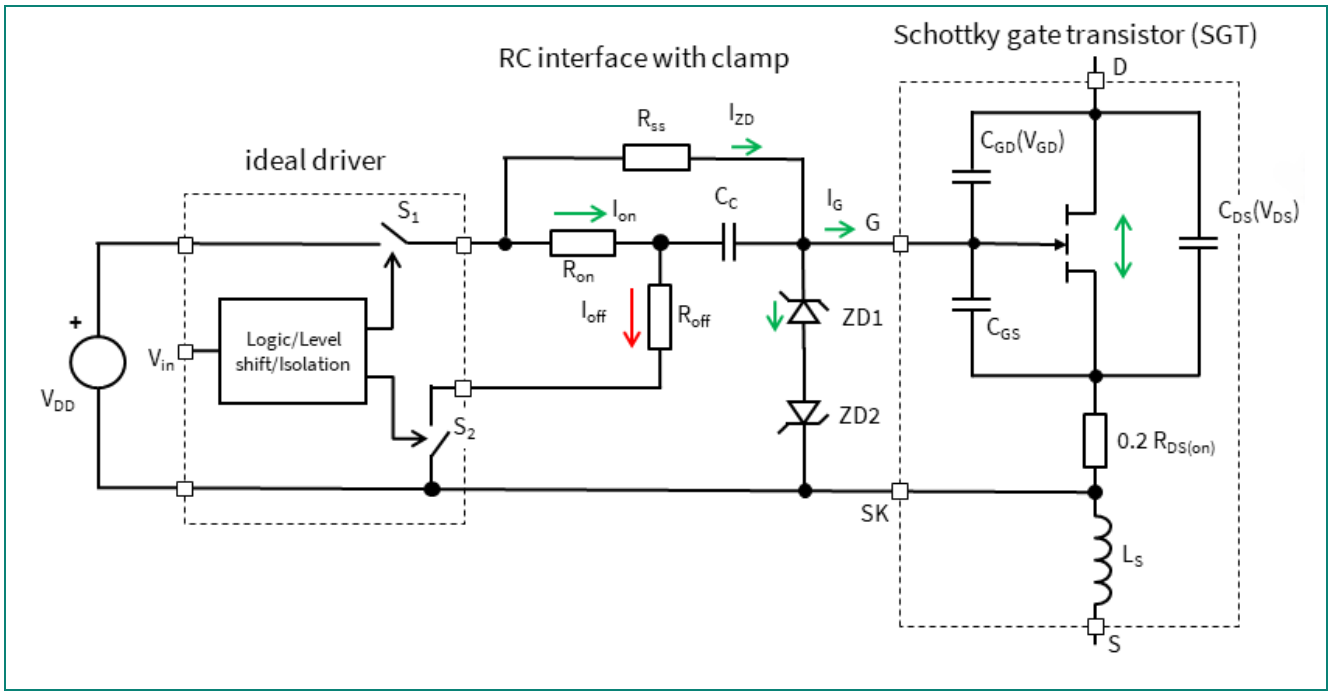


Figure 3 Equivalent circuit of CoolGaN™ SGT and gate drive with RC interface and clamping diodes

Figure 3 shows a gate drive concept for a Schottky gate GaN transistor, similar to the RC drive described in Section 2.1.1. The gate voltage clamping function inherent to a GIT is taken over here by external components. Thus two Zener diodes ZD1 and ZD2 are added to the RC interface, clamping the gate voltage for both polarities (for ZD2 a standard diode also can be used. ZD1 typically is a 5.3 V Zener diode, resulting in a gate drive voltage of ~6 V. If VDD is chosen sufficiently high (e.g., VDD = 9 V), a negative gate drive voltage $-V_N$, according to equation 1, will be generated in the "off"-state. This is illustrated in the respective gate voltage and current waveforms of Figure 4.

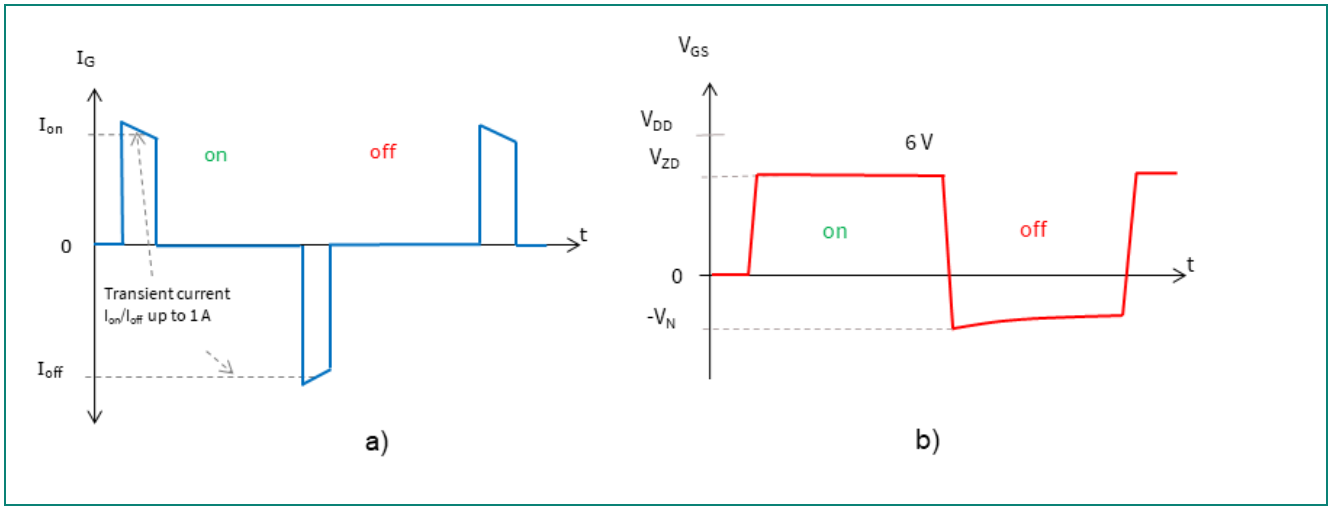


Figure 4 Typical gate current and gate voltage waveforms for SGT

Obviously, there is no current into the gate in the steady “on”-state; the current through the Zener diodes can be lower than the steady-state gate current for a GIT. This is why the time constant associated with the discharging of $C_C$ is not restricted to a few microseconds as with a GIT, but can be chosen to be significantly longer, up to some hundreds of microseconds. Due to the wide possible range for the discharging time constant, the concept is applicable in systems with non-complementary switching, too.

With the proposed circuitry, the gate is driven at an approximately constant voltage close to 6 V. However, the effective gate drive varies not only with temperature, but also with the load current; this is caused by the fact that for a lateral transistor like GaN, a part of the channel resistance $R_{DS(on)}$ is situated within the gate drive loop (**Figure 3**). The voltage drop across this resistor obviously reduces the effective driving voltage.

## 2.2 Bipolar driver supply voltage

In general, the coupling capacitance of the RC interface generates a negative gate voltage in the “off”-state with a starting value $-V_N$ that then decays at a time constant $R_{SS} * C_C$. The negative gate voltage is required in hard switched half-bridges to avoid significant cross-conduction. Most applications use complementary control signals, with the switching transient happening within a short dead-time (typically < 100 ns) after having switched “off” the passive transistor. The generated negative voltage thus remains nearly unchanged and no further measures are needed to avoid cross-conduction.

Whenever hard commutation is possible at fully discharged $C_C$, e.g., at system start-up or with non-complementary switching signals, the use of a bipolar gate-driver supply voltage can be an option. As an additional benefit for SGT, the gate drive voltage can be controlled more accurately.

**Figure 5** shows the solutions for both an SGT and a GIT. While for an SGT a simple resistive interface is sufficient (**Figure 5a**), the GIT still needs the RC interface to provide the required two gate current paths (**Figure 5b**).

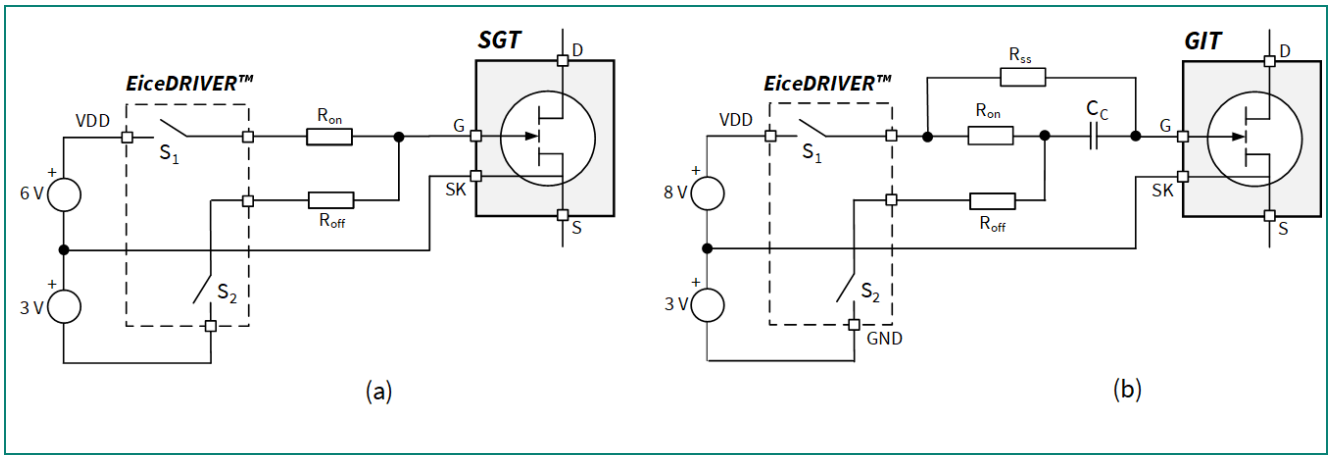


Figure 5 Gate drive with bipolar supply voltage for SGT (a) and GIT switches (b)

The main benefit of a bipolar driver supply is that the negative gate drive is always available, independent of the control scheme. And the main drawback is also clear – it is basically impossible to utilize bootstrapping for generating the high-side driver supply voltage.

## 2.3 Direct drive

An SGT, in essence, behaves like a MOSFET. The most important difference results from the low threshold voltage. For fast switching and safely keeping off the SGT without a negative gate drive voltage, the gate impedance must be extremely low. It is the parasitic inductance in the gate loop that contributes mainly to this impedance. For reliable hard-switching operation without a negative gate drive, a total gate loop inductance as low as 1 nH to 2 nH is required. This is not achievable with common bond-wire package technology, as used in Infineon's high-voltage (HV) GaN products [7], with a VDS capability up to 700 V.

A different approach is chosen in some of the medium-voltage (MV, 100 V) switches [7]. A "source down" packaging technology avoids bond wires and results in very low source and gate inductance values. With this concept, it is possible to realize a total gate loop inductance in the range required to allow the use of a unipolar driver supply.

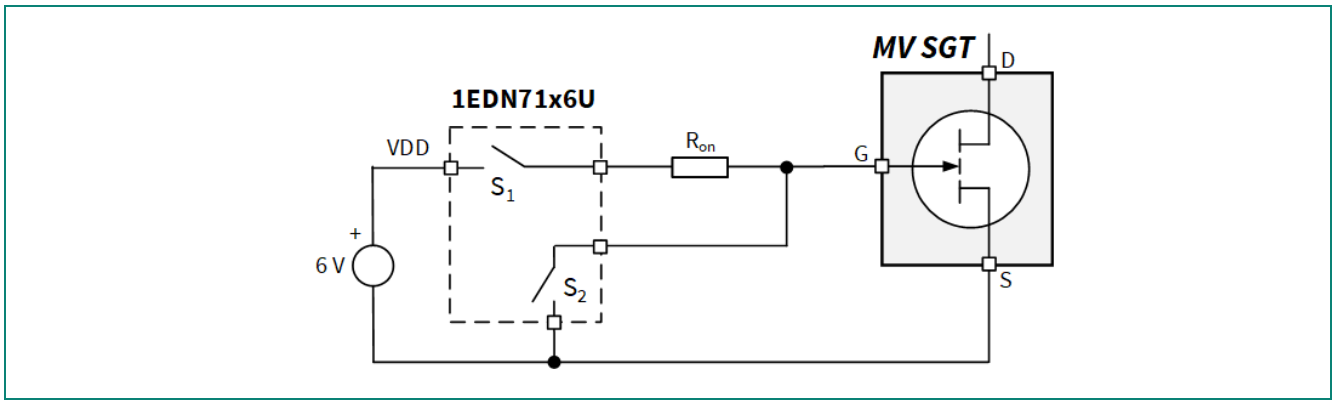


Figure 6 Direct-driven medium-voltage SGT

Figure 6 shows the resulting simple, "direct-driven" configuration. Here, no external resistor is used in the "off" path. This helps to realize a very low impedance "off"-loop. Even for zero "off"-voltage, the gate current is sufficiently high to guarantee fast switching "off". In this particular case, of course, the "ideal driver" concept is no longer applicable, as it is the pull-down resistance of the driver together with the loop inductance and the switch input capacitance that controls the behavior of this loop. The proposed gate driver IC offers different pull-down resistance values (0.8 Ω to 1.5 Ω) to adapt to various switches and gate loops, and to allow a sufficient damping factor even without external resistors. For suppression of hard-switching induced cross conduction, an additional pull-down path with very low on-resistance (0.3 Ω) is available.

As is also evident from Figure 6, there is no need for Kelvin source pins due to the extremely low source inductance.

# 3 General dimensioning guidelines

The dimensioning of the RC interface is relatively uncritical if a few basic relations are fulfilled. Further restrictions may result from specific application requirements.

## 3.1 Supply voltage $V_{DD}$

For a GIT, the intended high-impedance gate driver requires a supply voltage that is significantly larger than the gate diode clamping voltage VF. The recommended driving voltage ranges between 8 V and 12 V (higher voltages are possible, but at the expense of increased third quadrant and driving losses.

For an SGT, the optimum gate voltage range is relatively small (typically 5 V to 6 V) to avoid reliability issues. Thus, an SGT driver is typically supplied with 9 V, if one of the recommended options with negative gate drive is chosen; a direct-driven SGT ideally utilizes a 6 V supply.

Generally, the negative gate drive voltage $V_N$ calculated from Equation (1) should never be higher than needed, as this would only increase losses in third quadrant operation without providing any benefit.

## 3.2 Coupling capacitance $C_C$

Equation (1) is the key relation for dimensioning the RC interface. It is evident that the gate drive voltage in "off"-state must never become positive. According to Equation (1) this is fulfilled if the charge in the coupling capacitor in the "on"-state is larger than the total gate charge. To safely guarantee this under all possible conditions, the steady-state charge in $C_C$ under nominal conditions should be two to three times the total gate charge, resulting in a simple relation for $C_C$,

$$C_C \geq (2 \dots 3) \cdot Q_{Gtot}/(V_{DD} - V_F) \quad \text{(unipolar supply)} \tag{2a}$$

Although this slightly increases the dynamic gate drive power dissipation, the overall effect on losses is usually negligible.

With the use of a bipolar supply voltage, a reduction of $C_C$ is recommended to avoid a high negative gate drive. As a rule of thumb,

$$C_C = Q_{Gtot}/(V_{DD} - V_F) \quad \text{(bipolar supply)} \tag{2b}$$

If SGTs are used with the RC interface, the possible range for the coupling capacitor is larger, because the difference between the supply and clamping voltages can be lower. This also increases the range for the discharging time constant.

## 3.3 Resistor $R_{SS}$

For GITs, the required steady-state gate current $I_{SS}$ is directly set by $R_{SS}$ according to the relation:

$$I_{ss} = (V_{DD} - V_F)/R_{ss} \tag{3}$$

A steady-state current of typically 10 mA is recommended for the 55 mΩ GIT. For different $R_{DS(on)}$ values, $I_{SS}$ should be scaled inversely proportionally (e.g., half the $I_{SS}$ for double the $R_{DS(on)}$).

With $V_{DD}$ = 8 V, an $I_{SS}$ of 10 mA causes an additional 40 mW of gate drive power (assuming a 50% duty-cycle). In many applications, this will be negligible. If it is of concern, $I_{SS}$ can be further reduced. However, a minor increase in $R_{DS(on)}$ will be the consequence. Respective characterization data are given in the switch datasheets.
The average current through the Zener diodes in the RC drive for an SGT can be even smaller (< 1 mA) as the effect on the dissipated power is definitely negligible.

## 3.4 Resistors $R_{on}$, $R_{off}$

In general, a decrease in $R_{on}$ causes a faster voltage transient and reduced switching losses (shorter voltage/current overlap period). A lower limit of $R_{on}$ is usually given by the fact that faster switching leads to higher inductive overvoltages. The resulting drain-source voltage stress for the switch, however, has to be limited due to reliability reasons.

In soft-switching systems, $R_{on}$ is rather uncritical and a larger value can be chosen without significant impact. Switching "off" should normally happen as fast as possible. However, there exists another lower limit on the gate resistors, which arises from the fact that the gate loop is essentially a series RLC circuit. It can be shown that a damping resistor with a minimum value

$$R_{min} = 1.5 \cdot \sqrt{L_G / C_G} \tag{4}$$

results in adequate gate voltage waveforms. Assuming, for example, a total gate loop inductance $L_G$ of 10 nH (discrete HV switch), an effective capacitance $C_G$ of around 0.5 nF ($C_{ISS}$ in series with $C_C$) and considering the gate driver output resistance and internal gate resistance, we can conclude that a minimum external gate resistor of a few ohms is required for $R_{off}$ (usually the $R_{on}$ value resulting from switching speed limitations is anyway higher).

Table 1 summarizes typical component values for the 55 mΩ GIT, taking into account these guidelines.

Table 1 Typical RC interface component values for 55/140 mΩ CoolGaN™ GIT

| $V_{DDO}$ [V] | $C_{C,soft}$ [nF] | $C_{C,hard}$ [nF] | $R_{SS}$ [kΩ] | $R_{on}$ [Ω] | $R_{off}$ [Ω] |
|---|---|---|---|---|---|
| 8 | 2.2/1.5 | 3.9/3.3 | 0.41/1.2 | 4.7–22/10–47 | 2.2/4.7 |
| 10 | 1.5/1.2 | 2.2/1.8 | 0.68/1.8 | 6.8–27/12–56 | 2.2/4.7 |
| 12 | 1/0.8 | 1.8/1 | 0.82/2.2 | 10–33/22–68 | 2.2/4.7 |

It should be noted that different $C_C$ values are proposed for hard-switching and soft-switching topologies. This is because in hard-switched half-bridges, a higher negative gate drive is required to optimize the tradeoff between cross-conduction effects and increased reverse conduction losses. The minimum $R_{on}$ depends on the total power loop inductance due to a further fundamental tradeoff between switching speed and voltage stress. The low $R_{on}$ values require a total power loop inductance of a few nH only; the higher this inductance, the higher the $R_{on}$ value should be. Similar considerations are valid for the typical values/ranges of the RC interface components for an SG switch as given in Table 2; for ZD1 a 5.3 V Zener diode is chosen.

Table 2 Typical RC interface component values for 50/150 mΩ CoolGaN™ SGT

| $V_{DD}$ [V] | $C_C$ [nF] | $R_{SS}$ [kΩ] | $R_{on}$ [Ω] | $R_{off}$ [Ω] |
|---|---|---|---|---|
| 9 | 3.3–4.7 | 10 | 4.7–22/10–47 | 2.2/4.7 |
| 12 | 1.2–4.7 | 20 | 6.8–33/15–68 | 2.2/4.7 |

With the high $C_C$ values of **Table 2**, $V_N$ stays nearly constant and is equal to the difference of supply voltage and Zener clamp voltage. The variation of $V_{DD}$ then allows an easy control of $V_N$.

# 4 Application examples

## 4.1 Universal gate driving circuit for GIT and SGT half-bridge with unipolar supply voltage and dual-channel gate driver IC

Figure 7 shows a standard solution for a universal GaN half-bridge gate drive circuit. The two isolated output stages of the dual-channel EiceDRIVER™ 2EDB7259Y drive the respective switch via the RC interface, as described in sections 2.1 and 2.2. In case of an SGT, two Zener diodes are added to the RC interface, clamping the gate voltage for both polarities. The component values for the RC interface should be dimensioned following the guidelines in Section 3. As the dual-channel gate driver ICs do not provide separate source and sink outputs, a diode must be added to the standard interface if different values for $R_{on}$ and $R_{off}$ are required (in many applications, particularly soft-switching ones, a single resistor is sufficient). The circuit in Figure 7 is typical for hard-switched topologies, with the driver connected to the Kelvin source SK. Two separate power supplies generate the driver output supplies (e.g., 8 V).

The dual-channel isolated EiceDRIVER™ 2EDB7259Y [7] is offered in a DSO-14 150 mil package with 3.3 mm channel-to-channel creepage and features a 3 $kV_{rms}$ single protection isolation rating according to the UL 1577 standard. Furthermore, it ensures a minimum of 150 V/ns common-mode transient immunity (CMTI) robustness, which exceeds the requirements for even very fast switching GaN applications. With a stable propagation delay (–5/+9 ns) over both temperature and production variations, EiceDRIVER™ 2EDB7259Y ensures accurate timing and reliable operation over the full temperature range. More detailed information including measurement data is available in [1] and [2].

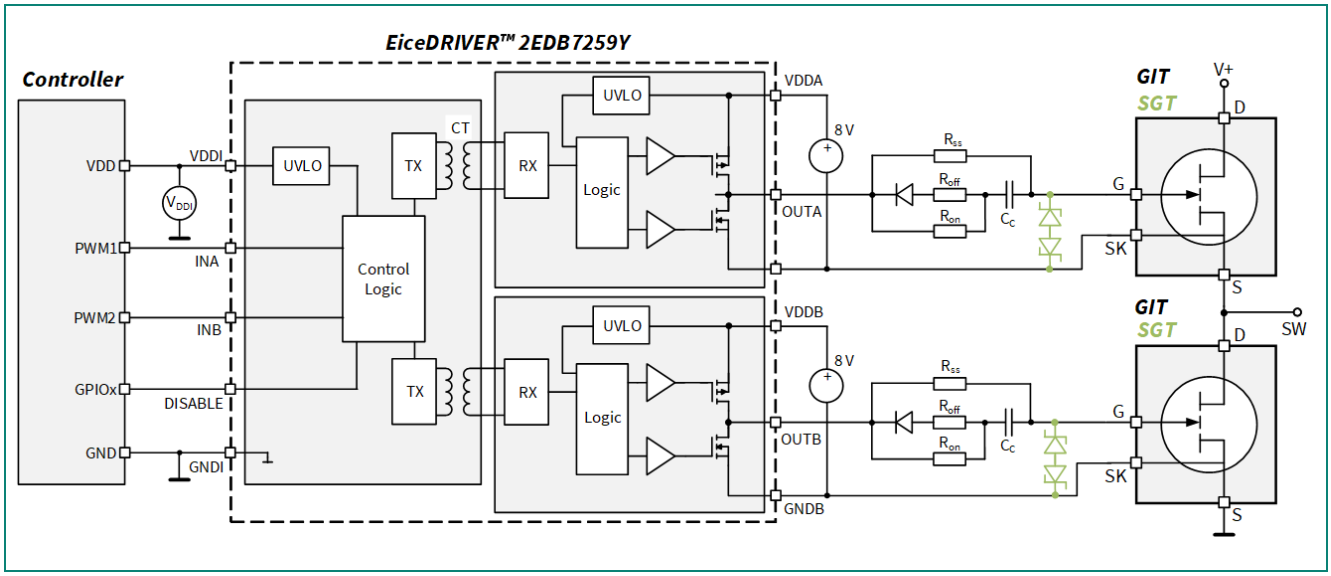


Figure 7 Universal gate driving circuit for GIT and SGT based on RC interface

## 4.2 Universal gate driving circuit for GIT and SGT half-bridge with bipolar supply voltage and single-channel gate driver ICs

Figure 8 shows a similar universal GaN half-bridge configuration utilizing a bipolar gate drive supply voltage. Instead of a dual-channel, it implements two single-channel EiceDRIVER™ 1EDB7275F with separate source and sink outputs. This can be beneficial in achieving a more compact PCB layout.

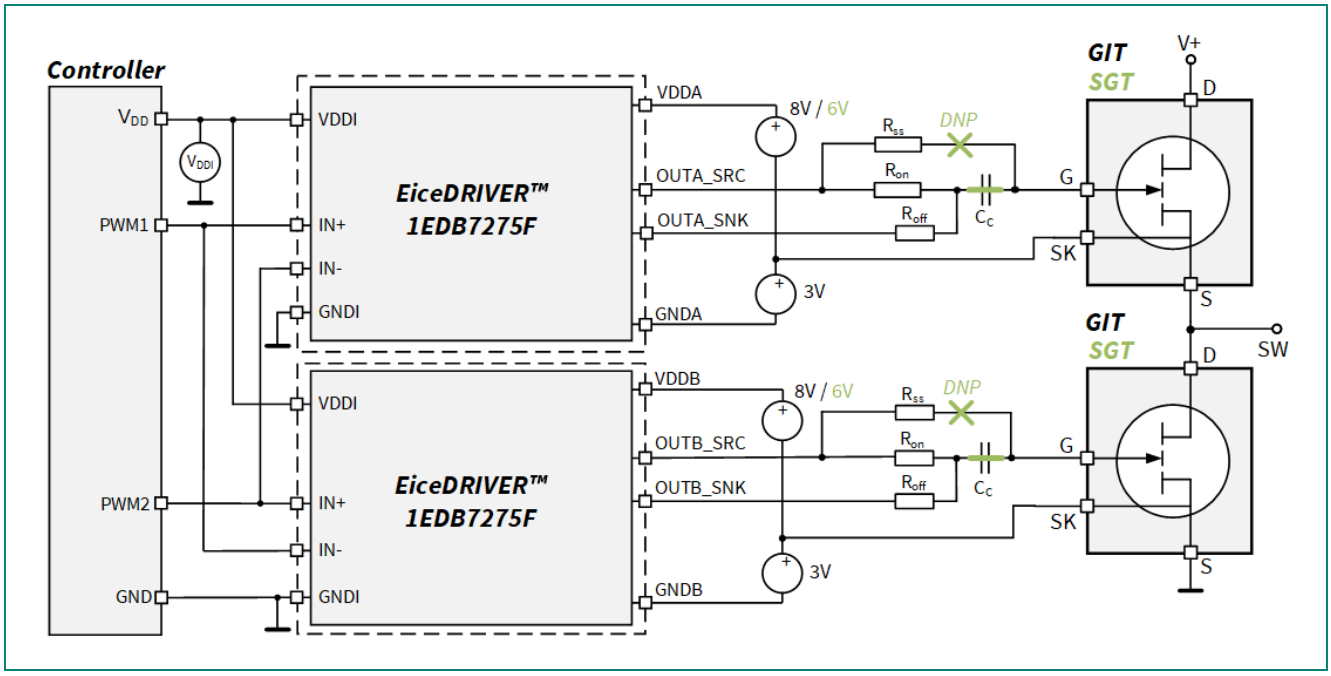


Figure 8 Universal gate driving circuit for GIT and SGT with bipolar driver supply

As indicated in Figure 8, again the same PCB can easily be adapted to drive either an SGT with an interface consisting of two gate resistors only, or to drive a GIT with the appropriately dimensioned RC interface.

The gate driver ICs have non-inverting and inverting inputs (IN+ and IN-) that can be connected as shown in Figure 8 to implement shoot-through protection. This feature provides an additional safety layer and therefore significantly improves system robustness. More detailed information including measurement data is available in [3]–[5].

# 5 Summary

Table 3 and Table 4 summarize the discussed gate drive configurations for a GIT and an SGT. As shown in Section 4, a "universal" gate driving circuit compatible with both GaN technologies can be designed using the standard RC interface and populating accordingly the components on the PCB [1].

Table 3 Gate drive configurations for GIT

| Driving voltage | Gate driver | Interface | Pros | Cons | Application |
|---|---|---|---|---|---|
| unipolar<br>+8 V to +12 V | standard | RC | negative gate drive | larger gate loop | soft-switching<br>hard-switching<br>(complementary) |
| bipolar<br>+9 V/–3 V<br>(typical) | standard<br>isolated | RC<br>(reduced $C_C$) | negative gate drive | no bootstrapping | hard-switching<br>(non-complementary) |

Table 4 Gate drive configurations for SGT

| Driving voltage | Gate driver | Interface | Pros | Cons | Application |
|---|---|---|---|---|---|
| unipolar<br>+5 V to +6 V | standard | $R_{on}$ only<br>"direct" drive | like MOSFET | requires very low gate loop inductance (<1 nH) | medium voltage (100 V) |
| unipolar<br>+8 V to +12 V | standard | RC plus clamping diode | similar to standard GIT drive<br>large discharging time-constant range | additional components (Zener diodes) | soft-switching<br>hard-switching |
| bipolar<br>+6 V/–3 V<br>(typical) | standard<br>isolated | $R_{on}$, $R_{off}$ | negative gate drive | no bootstrapping | soft-switching<br>hard-switching |

In these tables, the "standard" driver refers to fast low-impedance gate driver ICs with a current capability above 1 A. Input-to-output isolation is always required with bipolar supply and for high-side operation [3]. For low-side operation, differential-input drivers are available; see [4] and [5]. More information about the recommended EiceDRIVER™ gate driver ICs for driving GaN switches is available in [6].

# Appendix

## GaN half-bridge switching dynamics

Stacking two GaN/driver combinations and applying a (high) voltage $V_+$ results in the most important building block of a majority of power topologies: the half-bridge, consisting of a high-side (hs) and a low-side (ls) switch. The connection point is the switching node SW that is either connected to $V_+$ (hs "on") or to ground (ls "on"), or exhibits high impedance (both switches "off"). It is evident that the two switches must never be in "on" state at the same time. If, except for a short dead-time, high- and low-side switches are always in opposite states, we talk about complementary switching. Such a situation is shown in **Figure 9** (the equivalent circuit here has been reduced to comprise only the most important elements; power and gate loop inductance components have been lumped into $L_L$ and $L_{GG}$, respectively.)

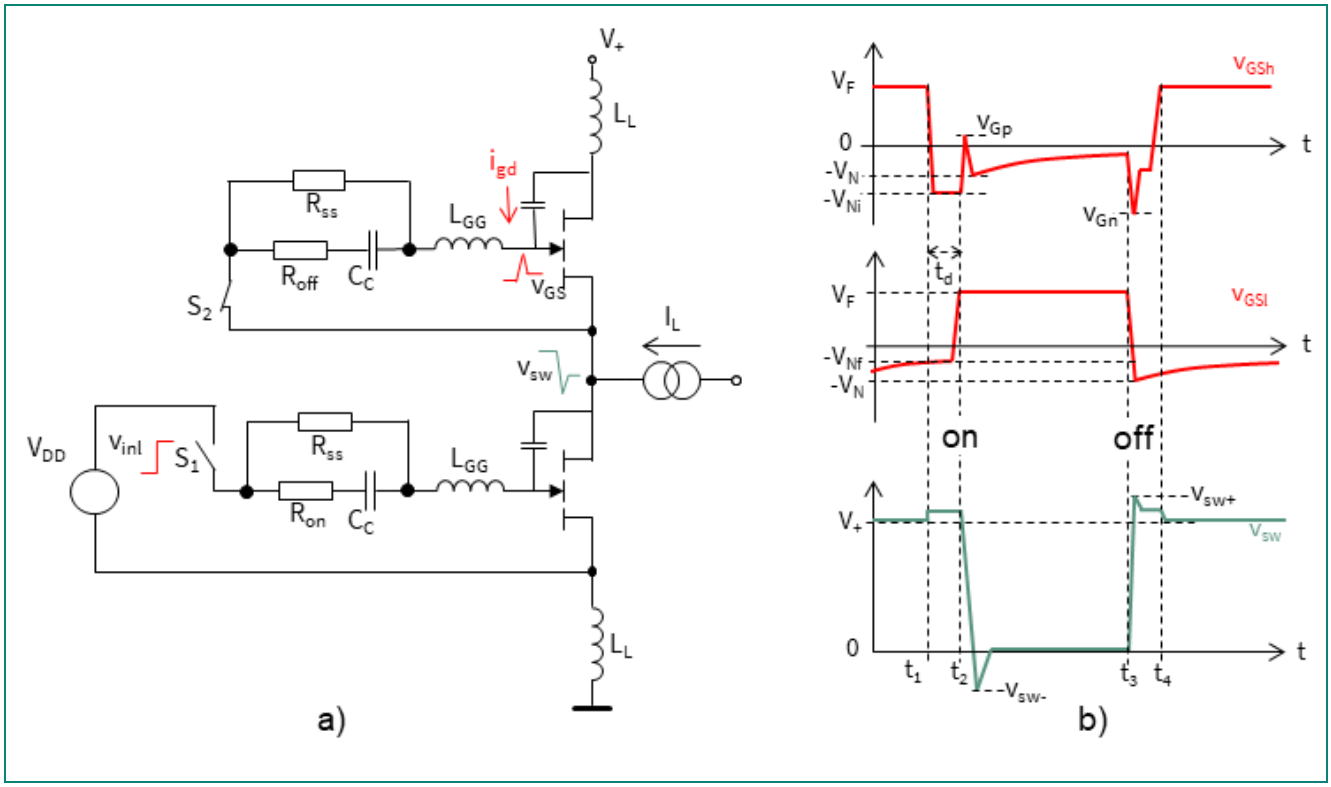


Figure 9 Hard-switched GaN half-bridge in boost configuration: equivalent circuit for hard switching transition (a) and symbolic voltage waveforms (b)

The constant load current $I_L$ flowing into the switching node SW defines the role of the switches: if the low-side switch is "off", $V_{SW}$ is high and $I_L$ flows through the upper switch in the reverse direction. Switching "on" the ls switch at time $t_2$ then causes the high-to-low transition of $V_{SW}$ ("hard switching"). The opposite transition starts when switching "off" the low-side ($t_3$), as then the switching node is pulled up by the load current, and the high-side can be switched "on" at zero $V_{DS}$ ("soft switching"). Thus, in the chosen "boost" configuration, the low-side is the active switch, whereas the high-side acts as the free-wheeling diode.

The qualitative (not to scale) waveforms in **Figure 9b** illustrate a few important effects associated with half-bridges. We start with the ls switch in the "off" state and $V_{SW}$ at a level slightly higher than the supply voltage $V_+$, as the hs switch is operated in reverse mode with a small negative $V_{DS}$ ($R_{DS(on)} * I_L$). At time $t_1$ the hs switch is switched "off" ($S_2$ closed), and the charge in $C_C$ causes a negative $V_{GS}$ with an initial value of $-V_{Ni}$. To further allow current flow in reverse direction, $V_{SW}$ has to exceed $V_+$ by $V_{Ni}$ plus the GaN threshold $V_{th}$. This explains the small step in the $V_{SW}$ waveform at time $t_1$. After a short dead-time $t_d$, the ls switch is switched "on" at time $t_2$, causing the "hard" negative transition of $V_{SW}$. Due to the associated $Q_{GD}$, this transition finally leads to a hs gate voltage increase from $-V_{Ni}$ to $-V_N$ according to

$$V_{Ni} - V_N = Q_{GD}/(C_C + C_{GS}) \tag{5}$$

$V_N$ then slowly decays during the "off"-phase at a typical time constant $R_{SS} * C_C$, reaching a final value $-V_{Nf}$ at the end of the "off"-phase. It is evident that this $Q_{GD}$-induced gate voltage step has to be carefully considered for switching transitions occurring when $C_C$ is uncharged (e.g., for non-complementary signals, during start-up or in burst mode operation).

The indicated undershoot of the switch node voltage after the switch-"on" event ($V_{SW-}$) is equivalent to a $V_{DS}$ peak for the hs switch. It is caused by the power loop inductance $L_L$ and depends on the switching speed that is essentially controlled by $R_{on}$. After the "on"-phase, the low-side is switched "off" at $t_3$, and $I_L$ again pulls $V_{SW}$ up. The high-side has to conduct in reverse direction, and the required gate current causes the negative $V_{GS}$ peak ($V_{Gn}$, **Figure 9b**) at time $t_3$. Usually, the switching "off" process is sufficiently fast, and the overshoot of $V_{SW}$ caused by $L_L$ ($V_{SW+}$) then mainly depends on $I_L$. In most applications $V_{SW+}$ is lower than $V_{SW-}$. After another dead-time the hs switch is switched "on" at $t_4$, reducing $V_{DS}$ again to its $R_{DS(on)}$-defined value.

The most important effect associated with hard-switching, however, is caused by the switches' gate-to drain capacitance $C_{GD}$. This is one of the components causing an interaction between the gate and the power loop (the other one being the common source inductance). As indicated in **Figure 9a**, the falling $V_{SW}$ is equivalent to an increase in the drain-to-gate voltage for the passive (hs) switch; this causes a current $I_{GD}$ flowing into $C_{GD}$. Obviously $I_{GD}$ has to be sunk by the gate driver, and the non-zero gate loop impedance leads to a peak in $V_{GS}$ ($V_{Gp}$). If $V_{Gp}$ exceeds the threshold voltage, both transistors are conducting simultaneously (cross-conduction or "spurious turn-on" (STO)). As the threshold concept is of course a simplification and approximation of real switch characteristics, STO effects also are not digital in nature, but may vary from "negligible" over "increased switching power" to even "destructive". For GaN switches, a reduction through the negative $V_{GS}$ is usually required in high-voltage applications with hard-switching voltage transitions. However, the trade-off with the increased reverse voltage drop during dead-time ($t_1$ - $t_2$ and $t_3$ - $t_4$) has to be taken into account.

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