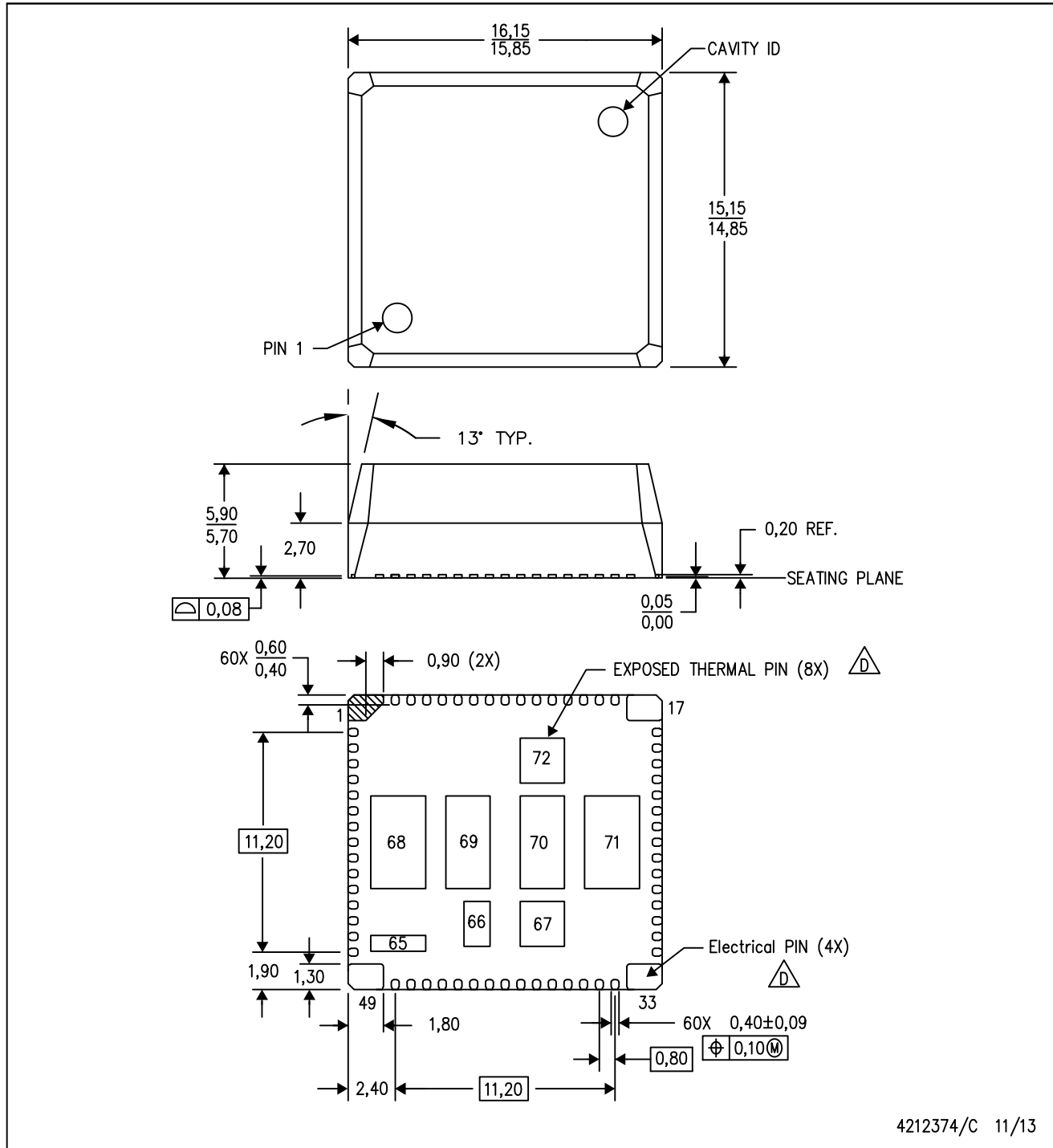




RLG (R-PB4QFN-N72)

PLASTIC QUAD FLATPACK NO-LEAD



4212374/C 11/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.

-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
-  The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane..

THERMAL PAD MECHANICAL DATA

RLG (R-PB4QFN-N72)

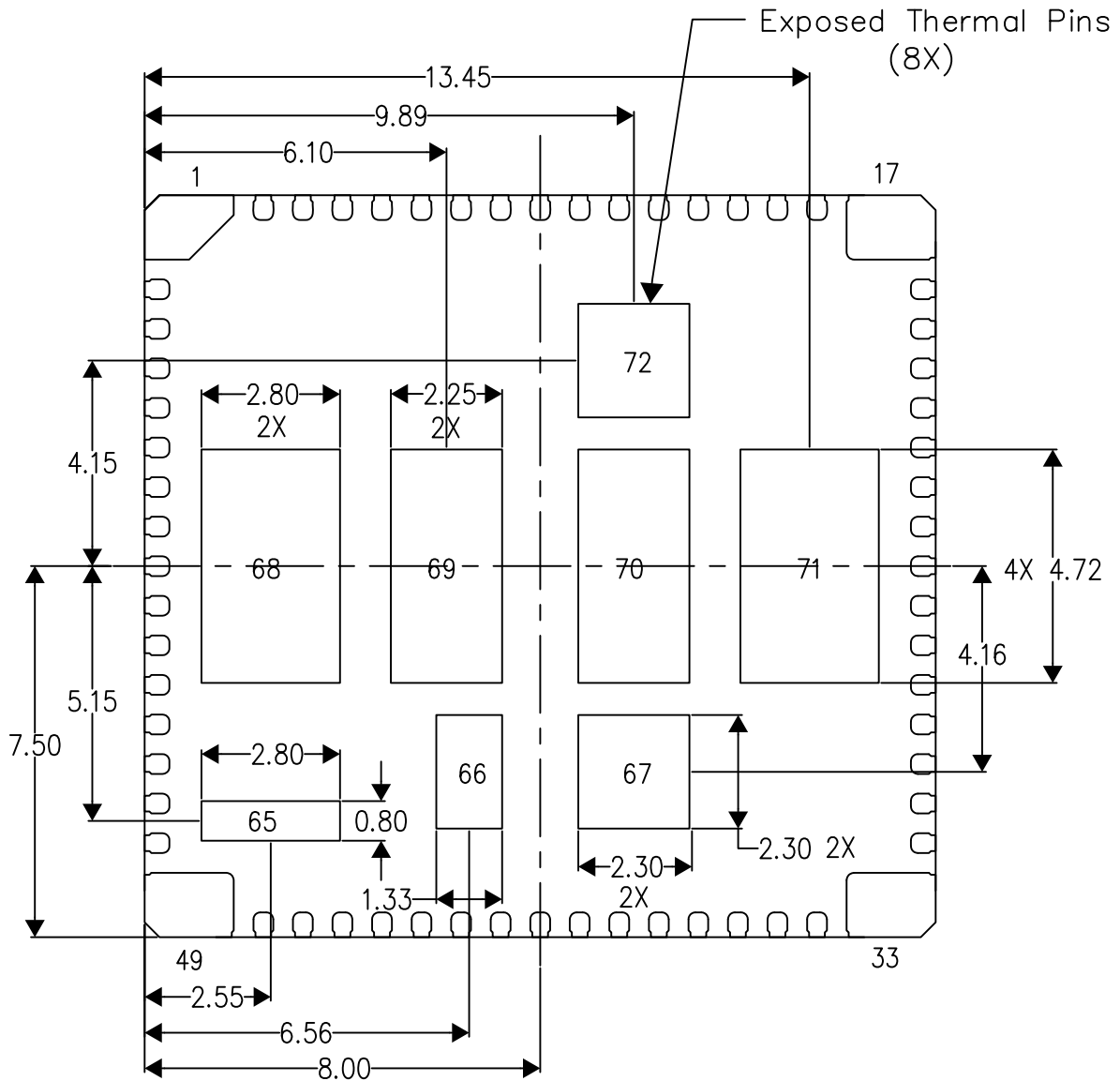
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



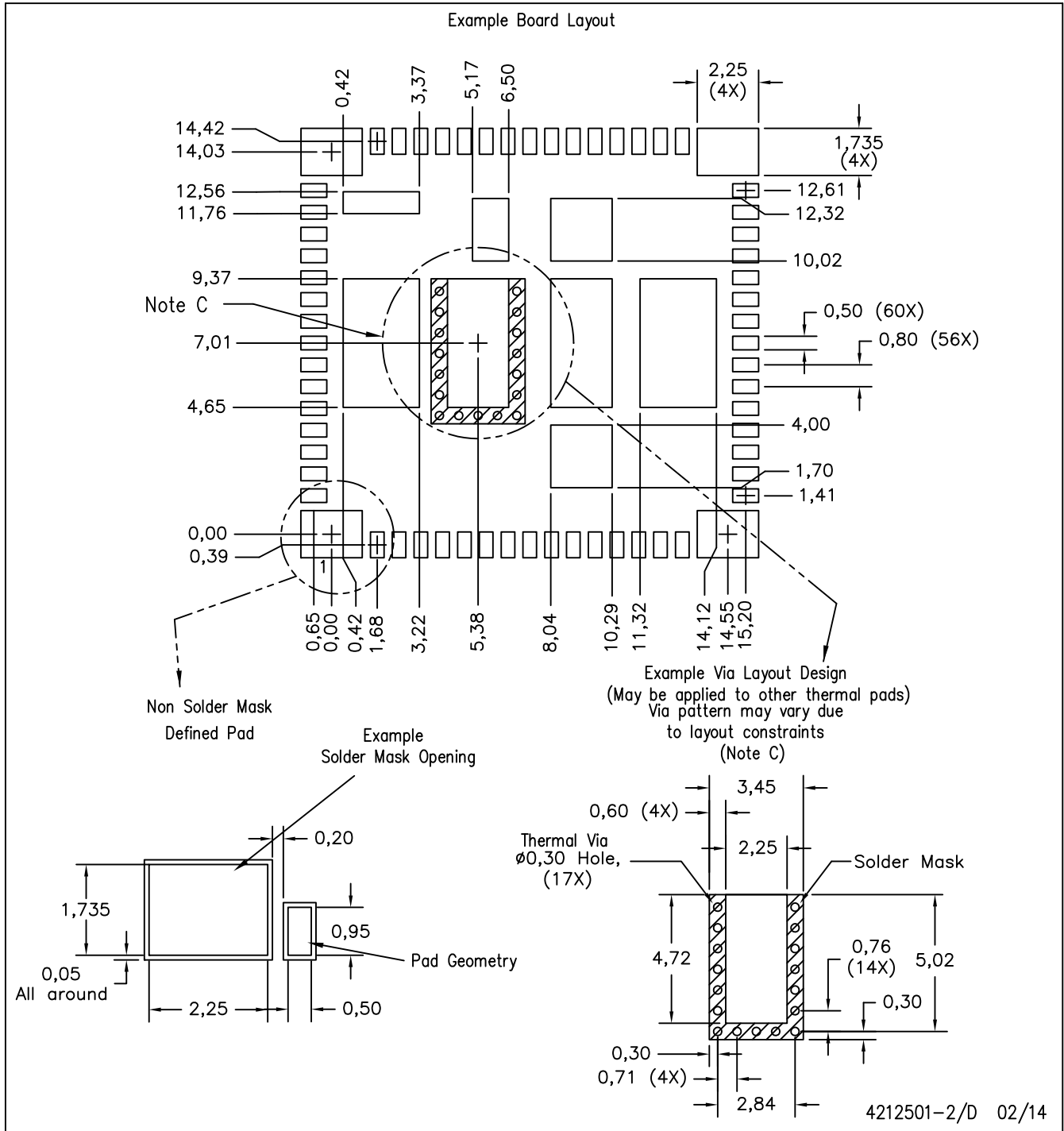
Bottom View
Exposed Thermal Pad Dimensions
Thermal Pad Tolerance: $\pm 0.10\text{mm}$

4215300/C 10/14

NOTE: All linear dimensions are in millimeters

RLG (R-PB4QFN-N72)

PLASTIC QUAD FLATPACK NO-LEAD

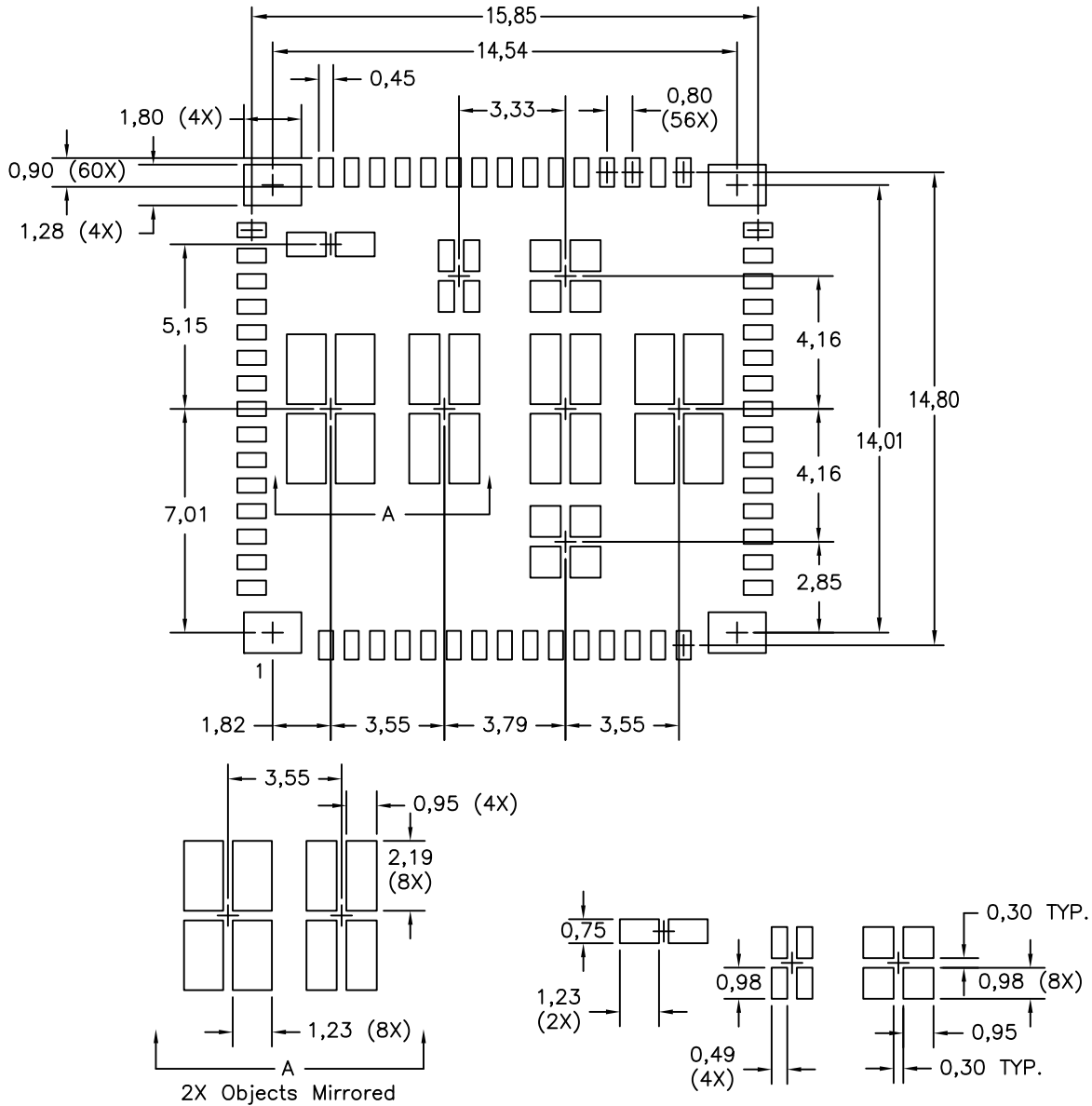


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is designed to be soldered to thermal pads on the board. Refer to Application Note, Quad Flat-Pack Package, Texas Instruments Literature No. SCBA017, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - D. See sheet 3 for stencil design recommendation.

RLG (R-PB4QFN-N72)

PLASTIC QUAD FLATPACK NO-LEAD

Example Stencil Design (Note E)
Stencil Thickness = 0,125mm



4212501-3/D 02/14

NOTES:

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customer should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

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