

DATA BOOK
PACKAGE OUTLINE

PREVIEW

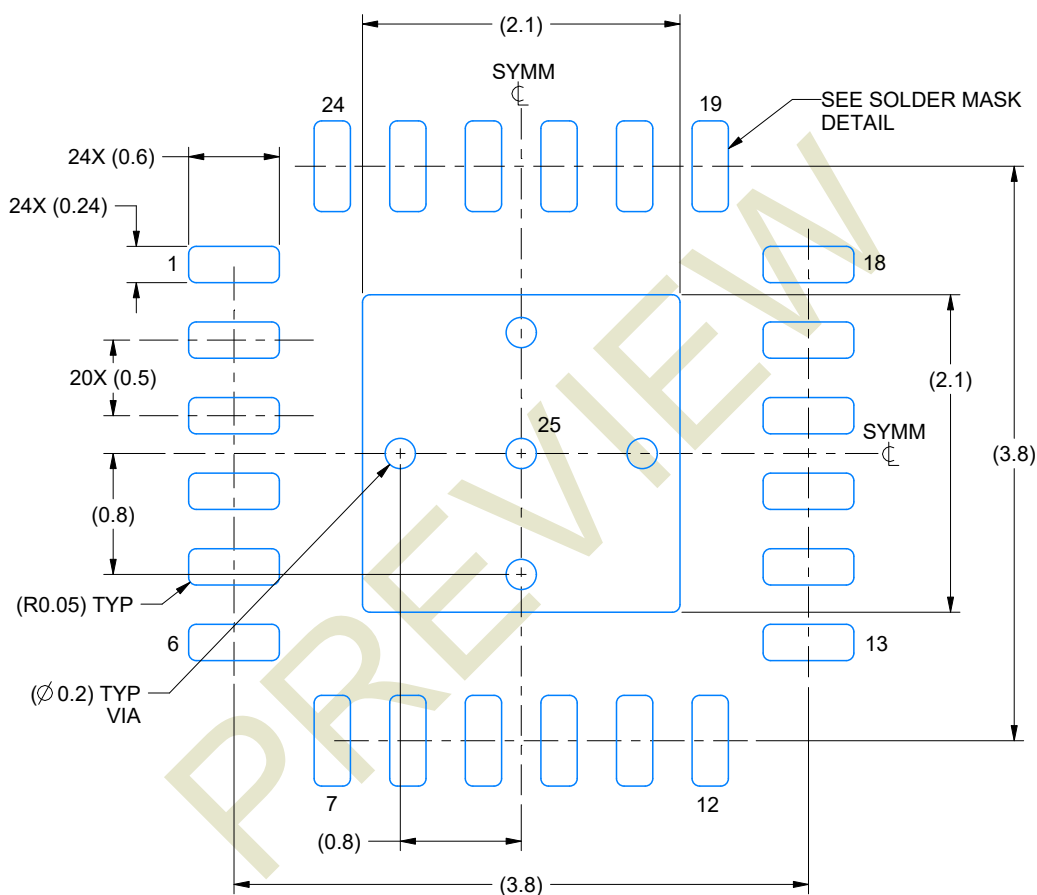
DRAFTER:	K. SINCERBOX	DATE:	2024	DIMENSIONS IN MILLIMETERS	
DESIGNER:		DATE:		 TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS ePOD, RTW0024C / WQFN, 24 PIN, 0.5 MM PITCH	CODE IDENTITY NUMBER 01295
CHECKER:	K. SINCERBOX	DATE:	2024		
ENGINEER:	M. ZHANG	DATE:	2024		
APPROVED:	K. SINCERBOX	DATE:	2024		
RELEASED:	K. SINCERBOX	DATE:	2024		
TEMPLATE INFO:	EDGE# 4218519	DATE:	04/07/2016	SCALE NTS	SIZE A
				4214981	REV A
					PAGE 1 OF 5

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

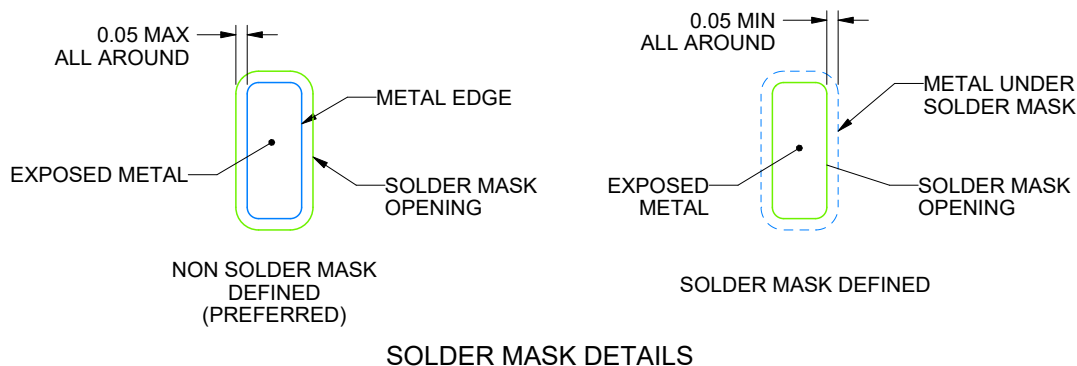
RTW0024C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



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NOTES: (continued)

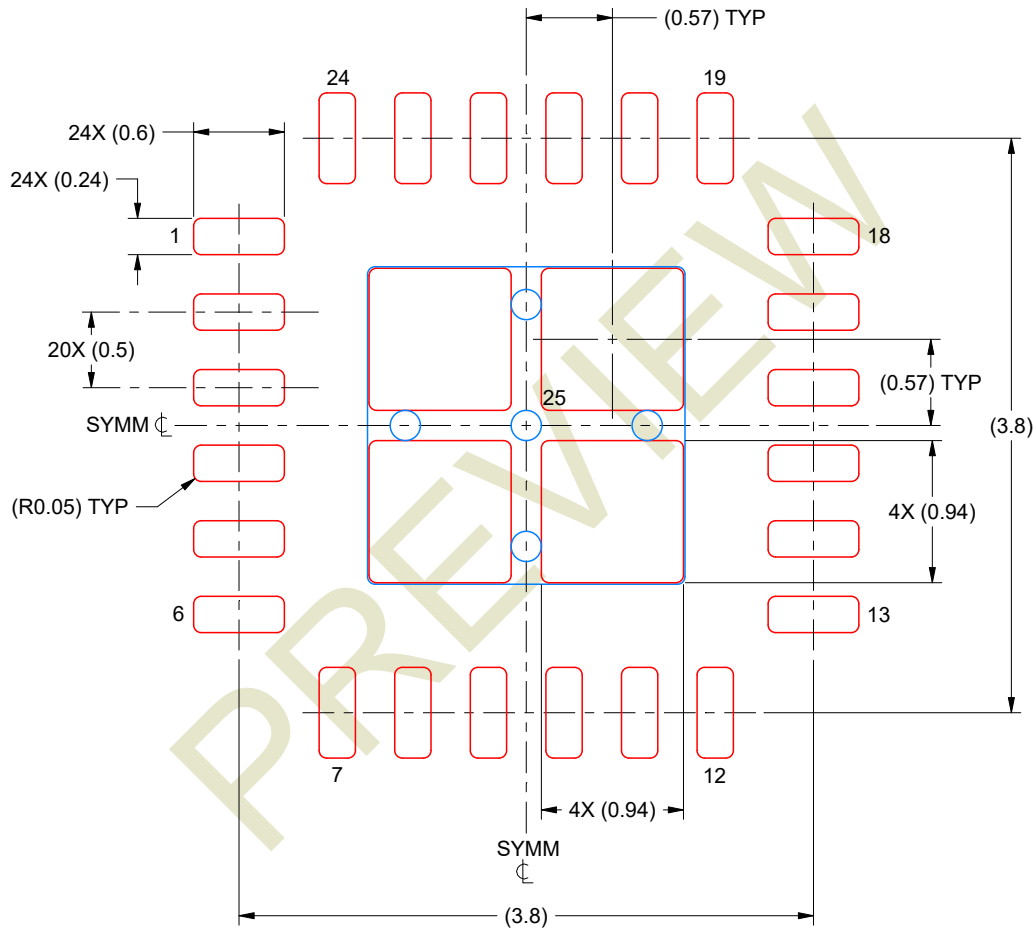
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTW0024C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS					
REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER	
A	RELEASE NEW DRAWING	2210847	2024	M. ZHANG / K. SINCERBOX	
PREVIEW					
SCALE		SIZE	4214981		REV
		A			A
				PAGE	
				5 OF 5	