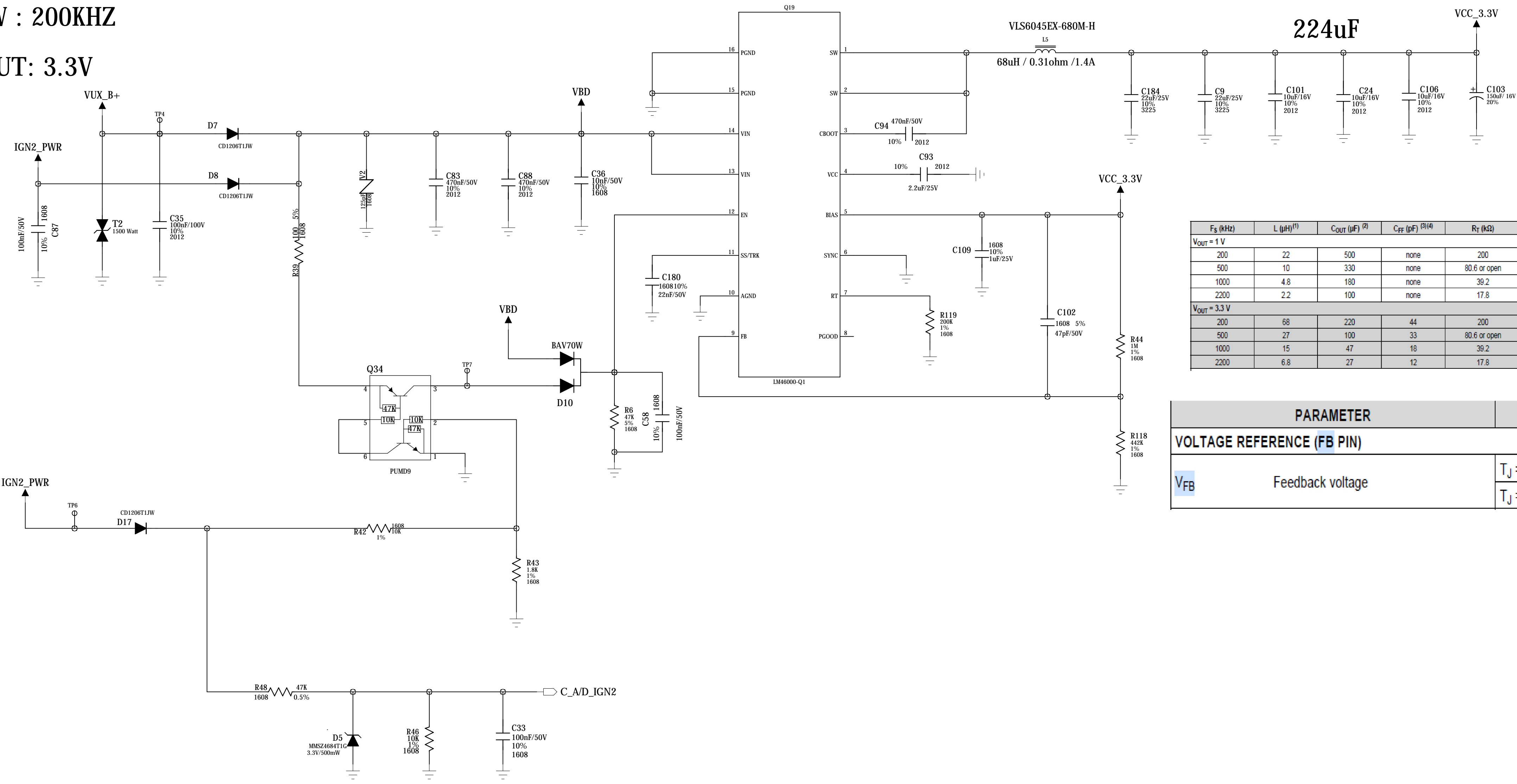


VIN 8~ 16V  
 FSW : 200KHZ  
 VOUT: 3.3V

REVISION RECORD			
ITR	ECO NO.	APPROVED	DATE



Fs (kHz)	L (uH) [1]	Cout (uF) [2]	Cin (uF) [3]	Rz (mOhm)	Rpsm (mOhm) [4]
<b>Vout = 1 V</b>					
200	22	500	none	200	100
500	10	330	none	50.6 or open	100
1000	4.8	180	none	39.2	100
2200	2.2	100	none	17.8	100
<b>Vout = 3.3 V</b>					
200	68	220	44	200	442
500	27	100	33	50.6 or open	442
1000	15	47	18	39.2	442
2200	6.8	27	12	17.8	442

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOLTAGE REFERENCE (FB PIN)</b>					
V <sub>FB</sub>	Feedback voltage				V
		T <sub>J</sub> = 25°C	1.009	1.016	
		T <sub>J</sub> = -40°C to 125°C	0.999	1.016	1.039

DRAWN: JH CHO		DATE: 18.02.28		COMPANY:	
CHECKED: JH CHO		DATE: 12.06.18		TITLE: BMS	
QUALITY CONTROL: <QC By>		DATE: <QC Date>		CODE: <Code>	SIZE: E
RELEASED: <Released By>		DATE: <Release Date>		SCALE: <Scale>	DRAWING NO: REVISION
				SHEET: 1st	REV: 2.00

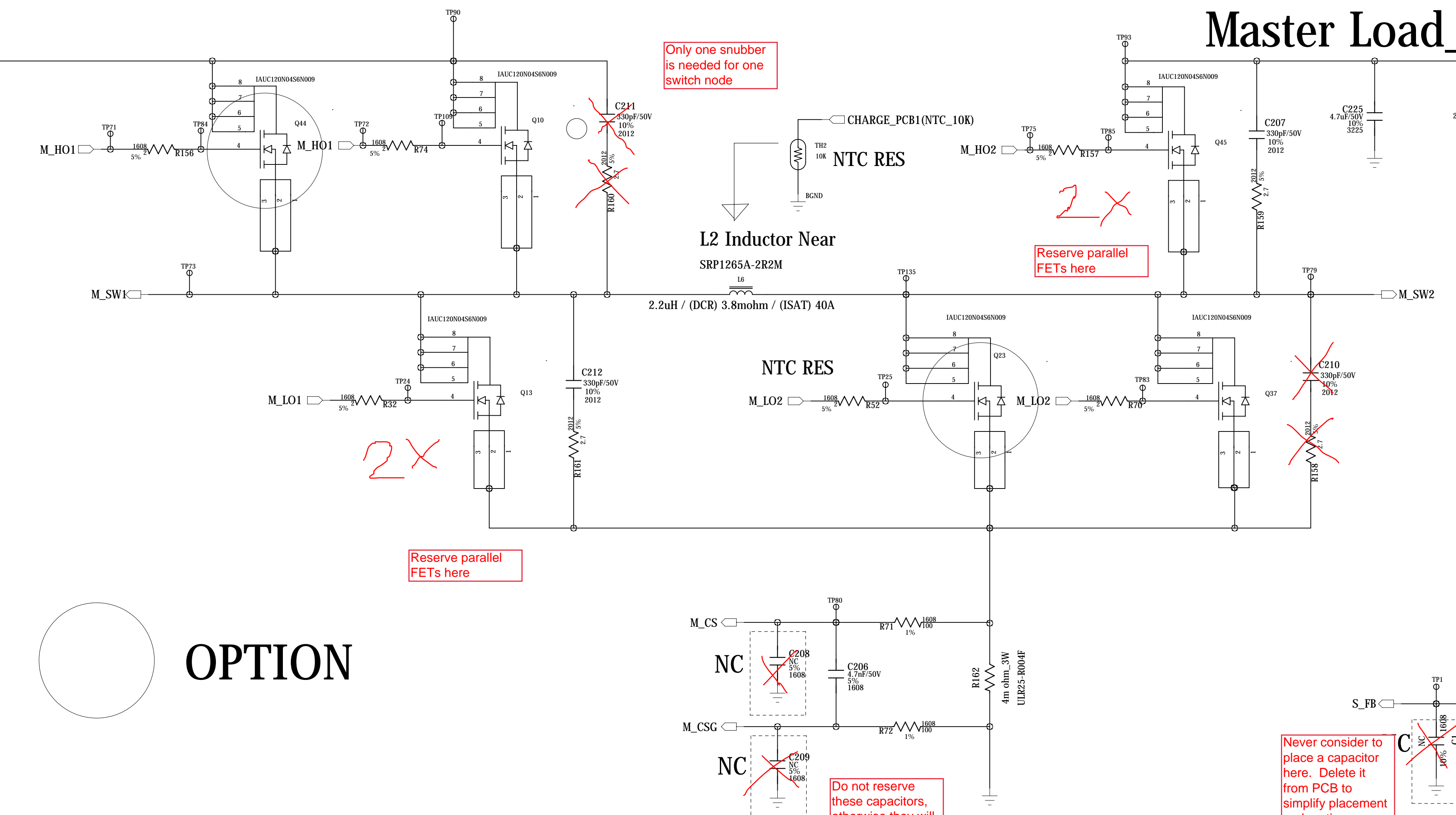
REVISION RECORD			
REV	REV NO	APPROVED	DATE

$ID (FET) = \text{Square} \left( \frac{175-75}{(4.4\text{mohm} * 40)} \right) = 23.8A \quad (23.8*2 = 47.6A)$

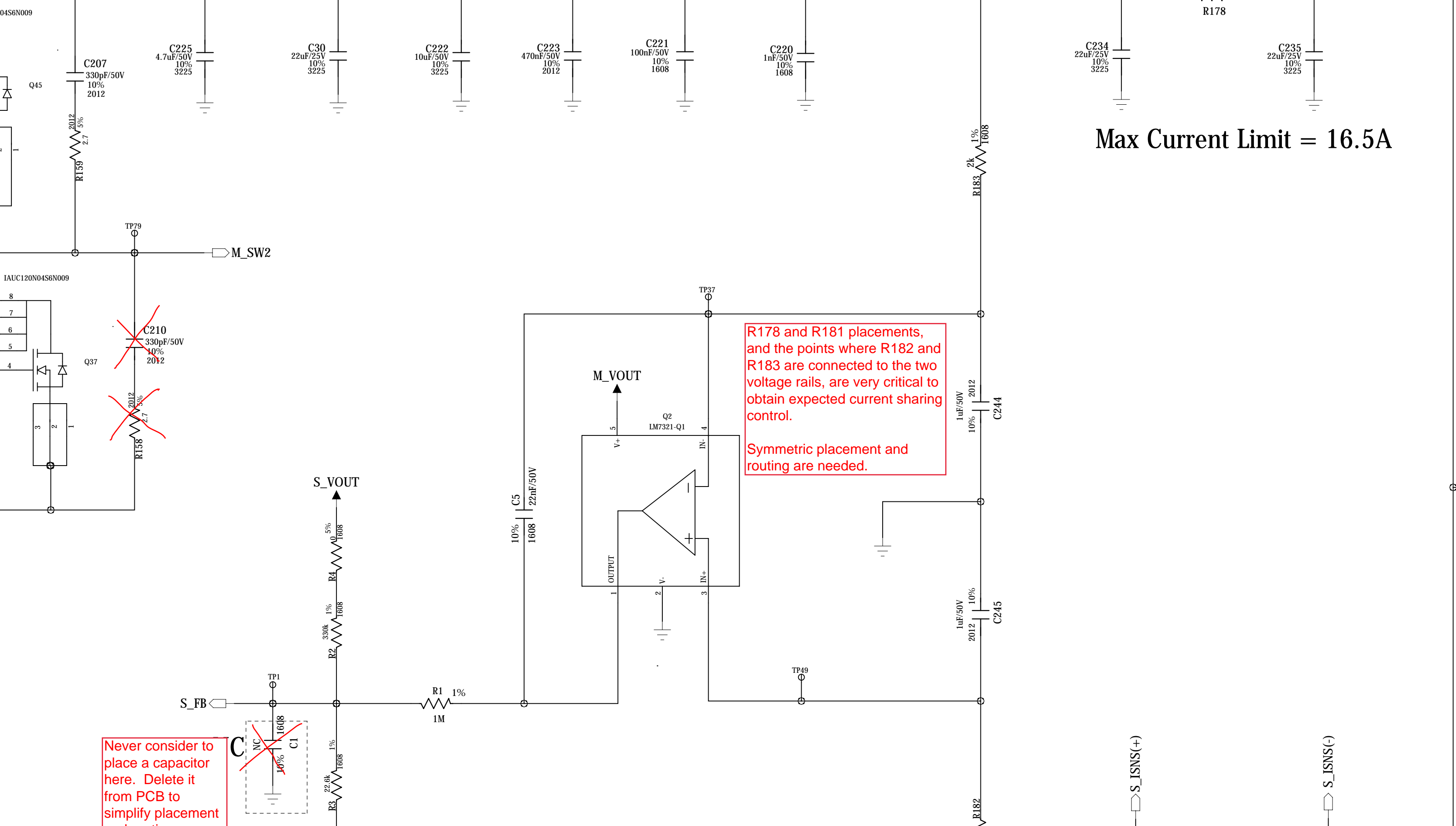
$I (\text{INPUT A}) = 12.6V * 33A / (10V*0.9) = 46.2A$

- Ø VIN : 8~16V (Charging starts from 10V)
- Ø FSW : 300KHZ (Master / Slave)
- Ø 2Phase Max Charging Current Limit 33A : 16.5A Per 1Phase
- Ø Charging Voltage : 12.6V
- Ø LM5176 2EA Applications : Master 1EA / Slave 1EA
- Ø CC (Constant Current) Variable Control
- Ø NC : (NOT Connect)

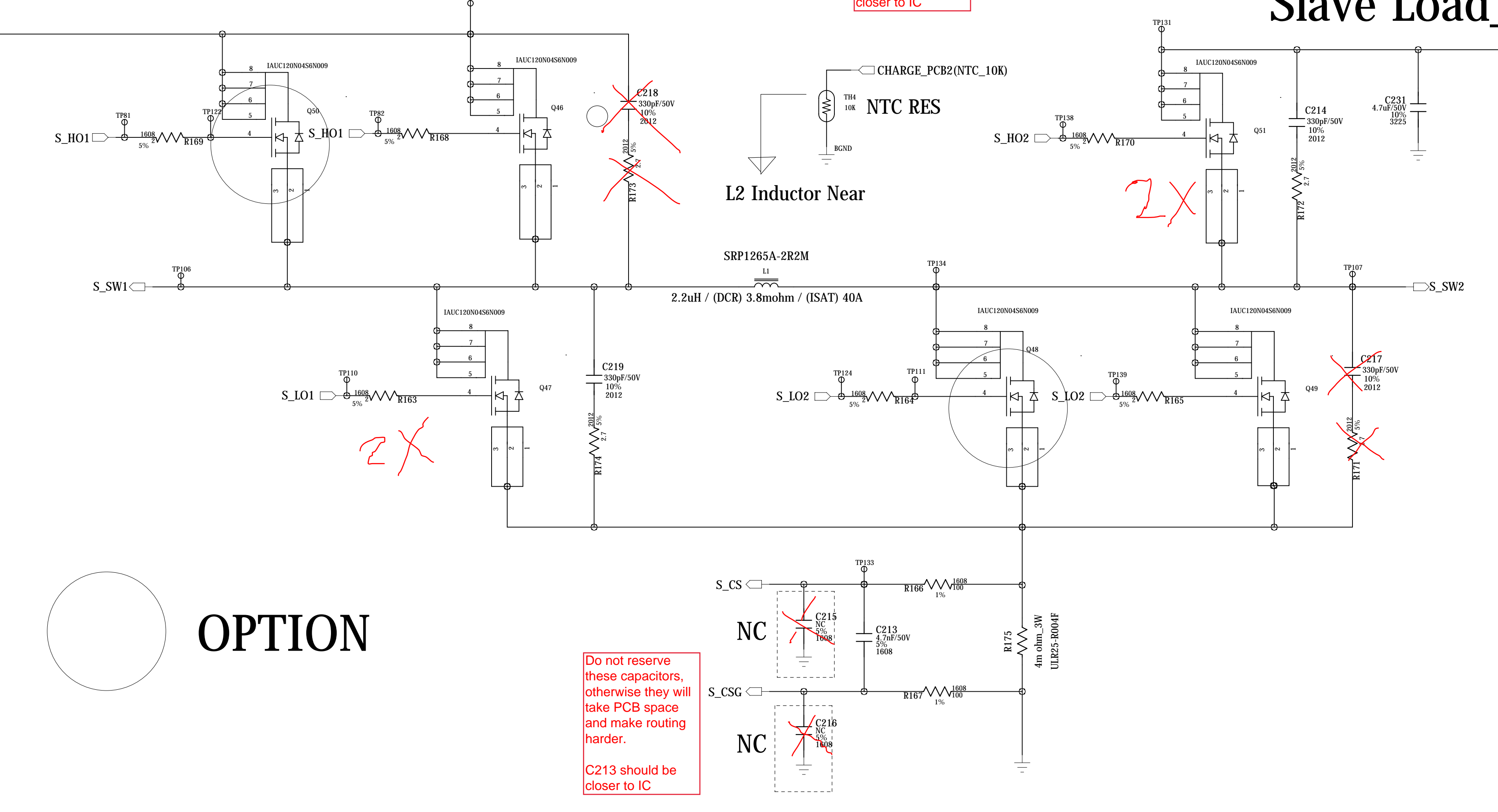
**Master Control\_ 12.6V / 16.5A**



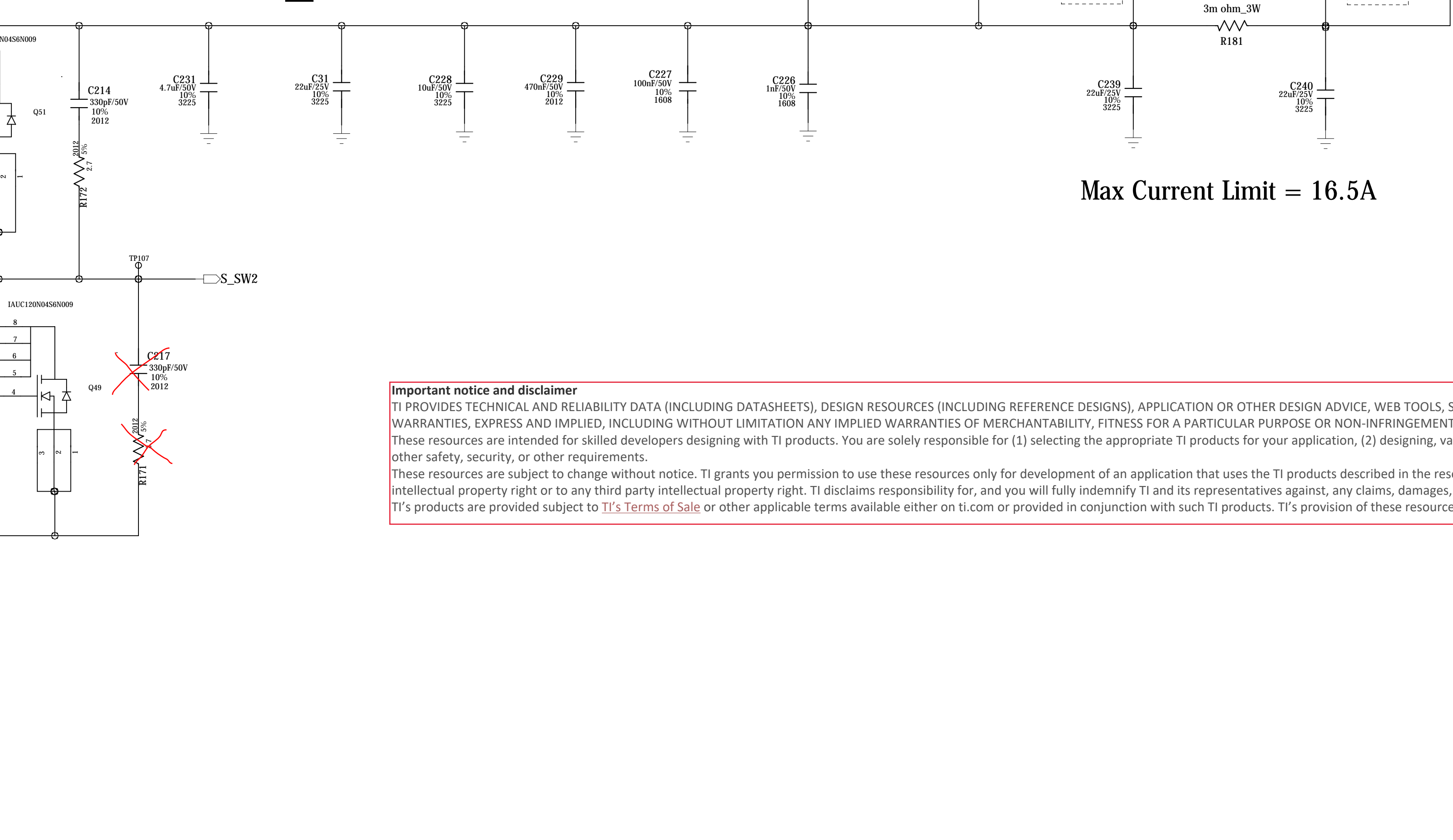
**Master Load\_ 12.6V / 16.5A**



**Slave Control\_ 12.6V / 16.5A**



**Slave Load\_ 12.6V / 16.5A**



**Important note:** Please refer to the layout guidelines in the datasheet, and also our EVM layout and signal routing.

1. Pay special attention to the gate driver and the return paths. The pair of traces should be closely side by side.
2. Current sense traces should be routed closely side by side.
3. Power circuit AC current loops should be compact and do not enclose large spatial area by the ac current loop.
4. Separating the AGND and PGND, and use single point connection for each IC at the location of IC underpad. All control signals should refer to AGND. Please create an AGND polygon for each IC, and only connect it to PGND through the IC underpad. Refer to the EVM layout for details.
5. VCC should be beside the IC across VCC and PGND pins
6. BOOT capacitor should be beside the IC across BOOT and SW pins.
7. Since the resistor R162 and R175 shared by both the buck and boost legs, the buck and boost leg should be placed symmetrically to connect to these current sense resistors.

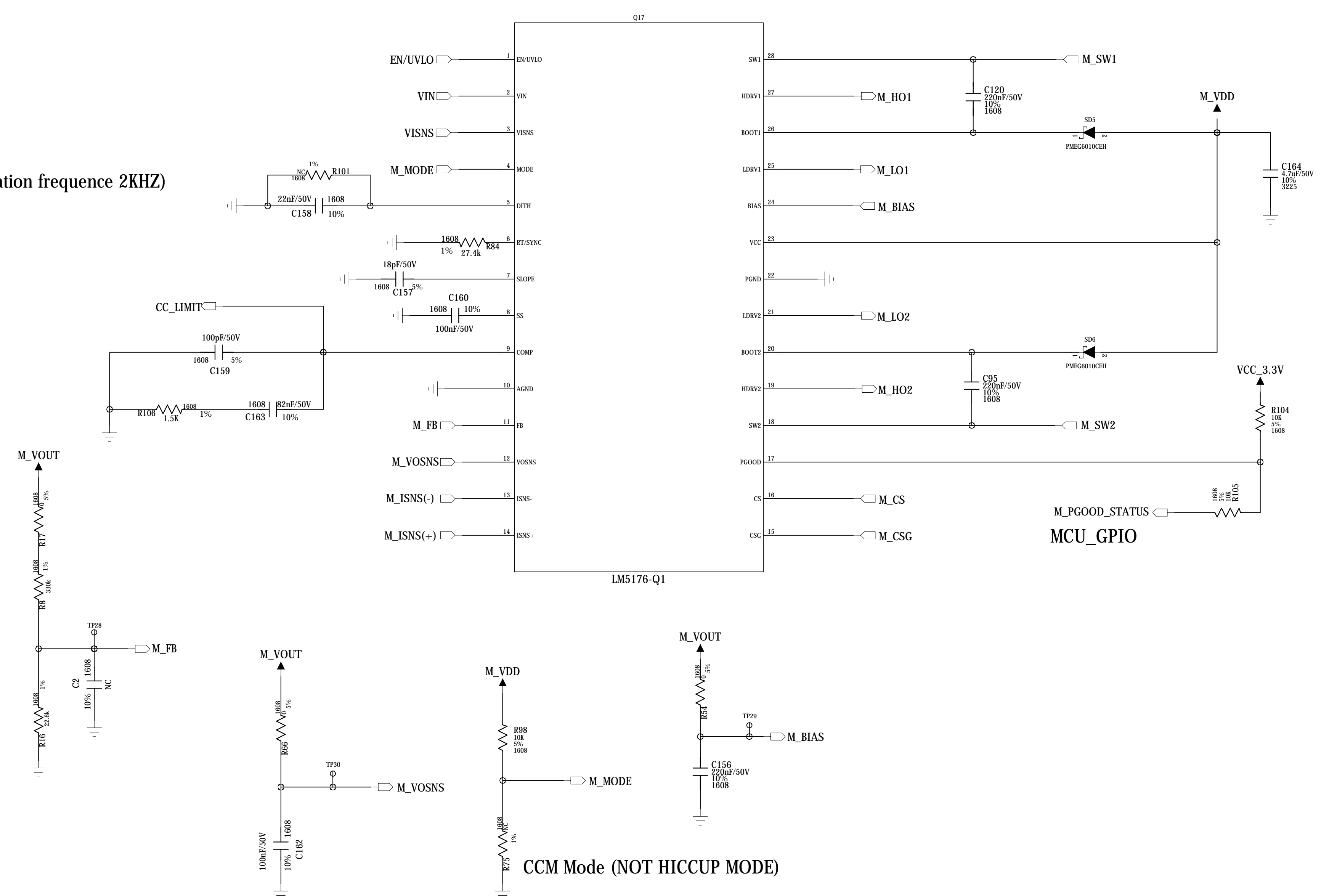
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COMPANY:		TITLE:	
BMS		BMS	
DESIGNED BY: JH CHO	DATE: 18.02.28	CORR:	SIZE:
CHECKED BY: JH CHO	DATE: 12.06.18	SCALE:	DRAWING NO:
QUALITY CONTROL: <QC By>	DATE: <QC Date>	REVISION: <Code>	REV: 2.00
RELEASED: <Released By>	DATE: <Release Date>	SCALE: <Scale>	SHEET: 2 of 3

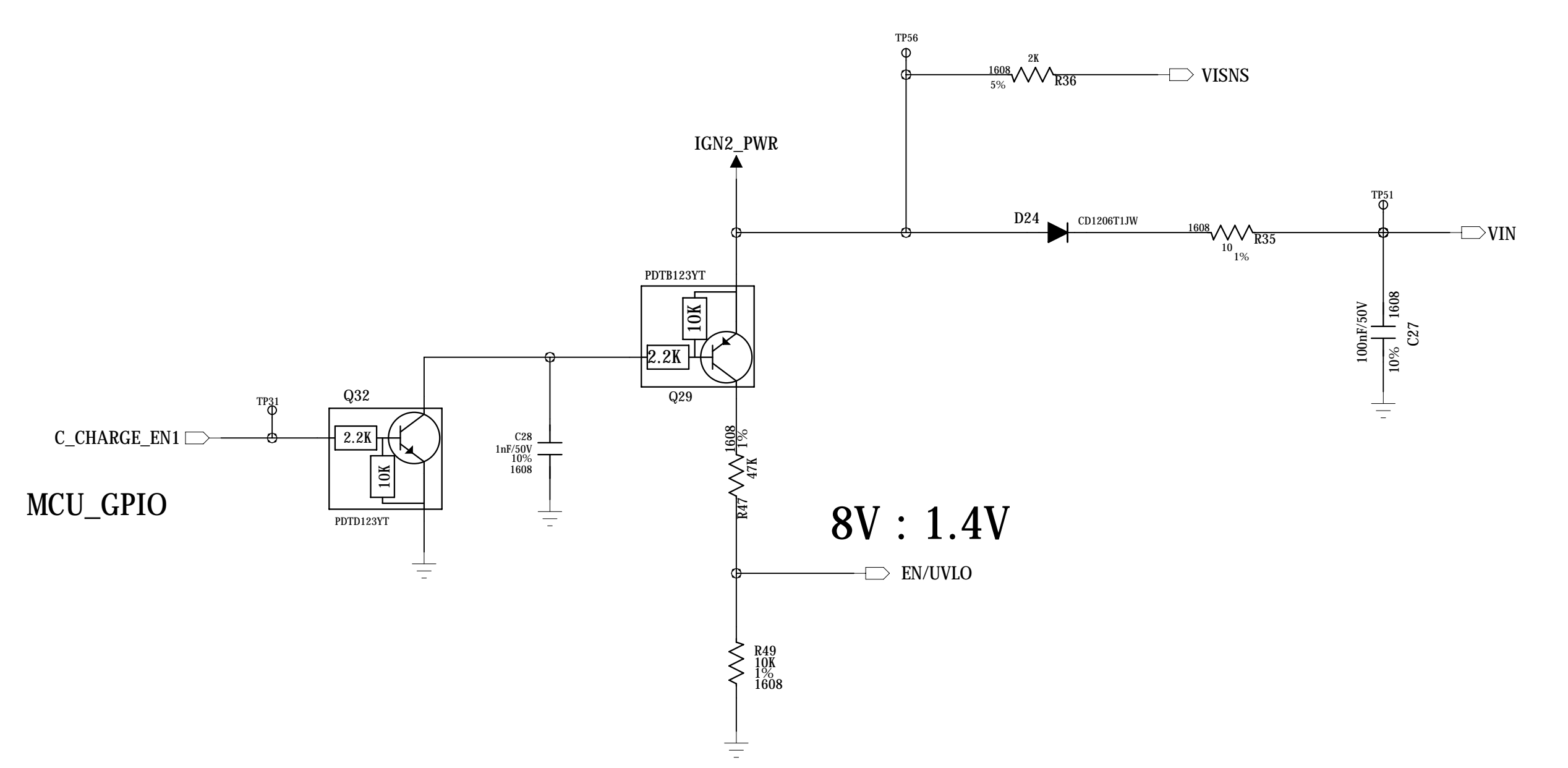
REVISION RECORD			
ITR	ECO NO.	APPROVED	DATE

# MASTER #1 LM5176

(Modulation frequency 2KHZ)



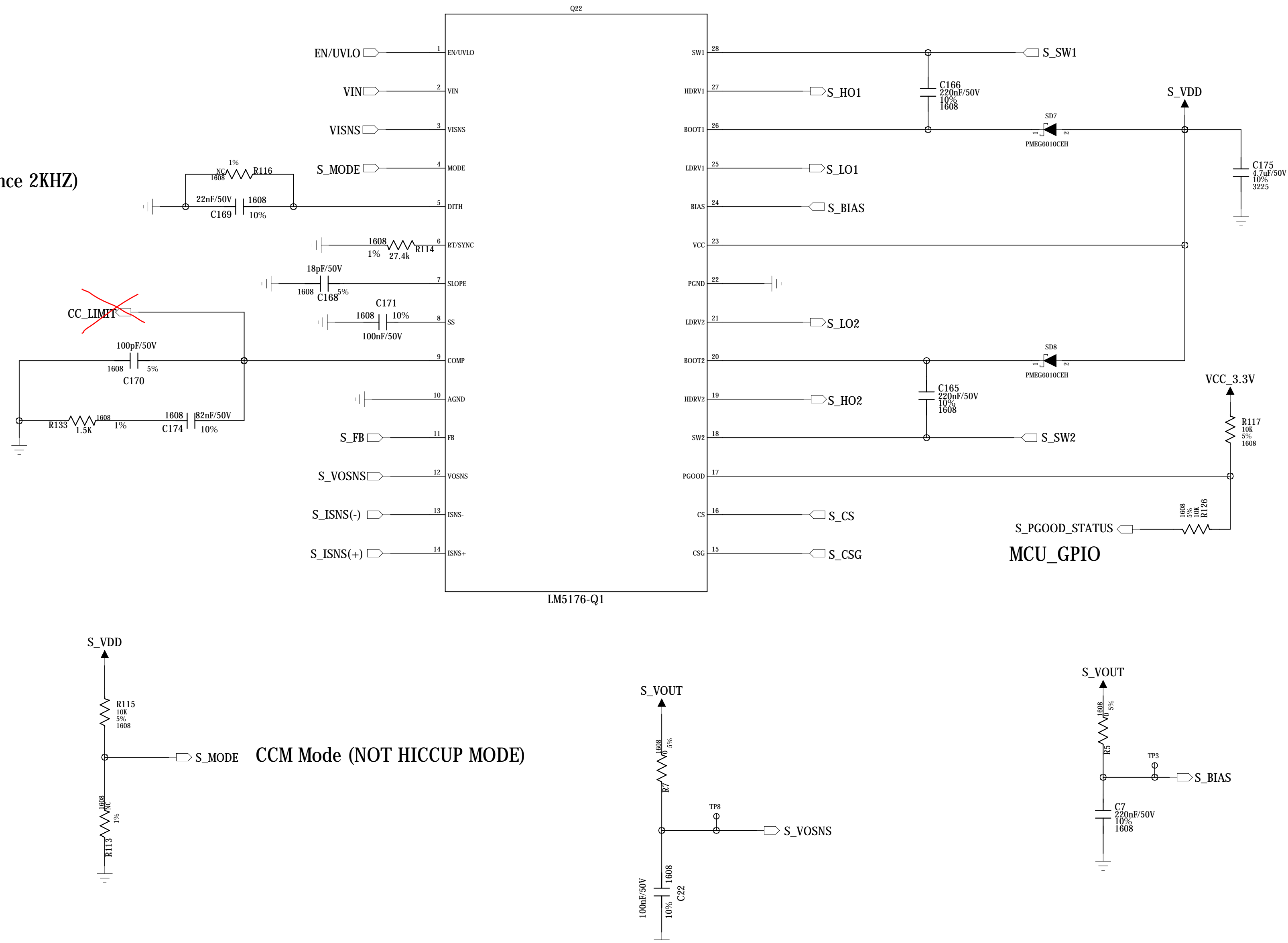
# Power Supply of Master and Slave



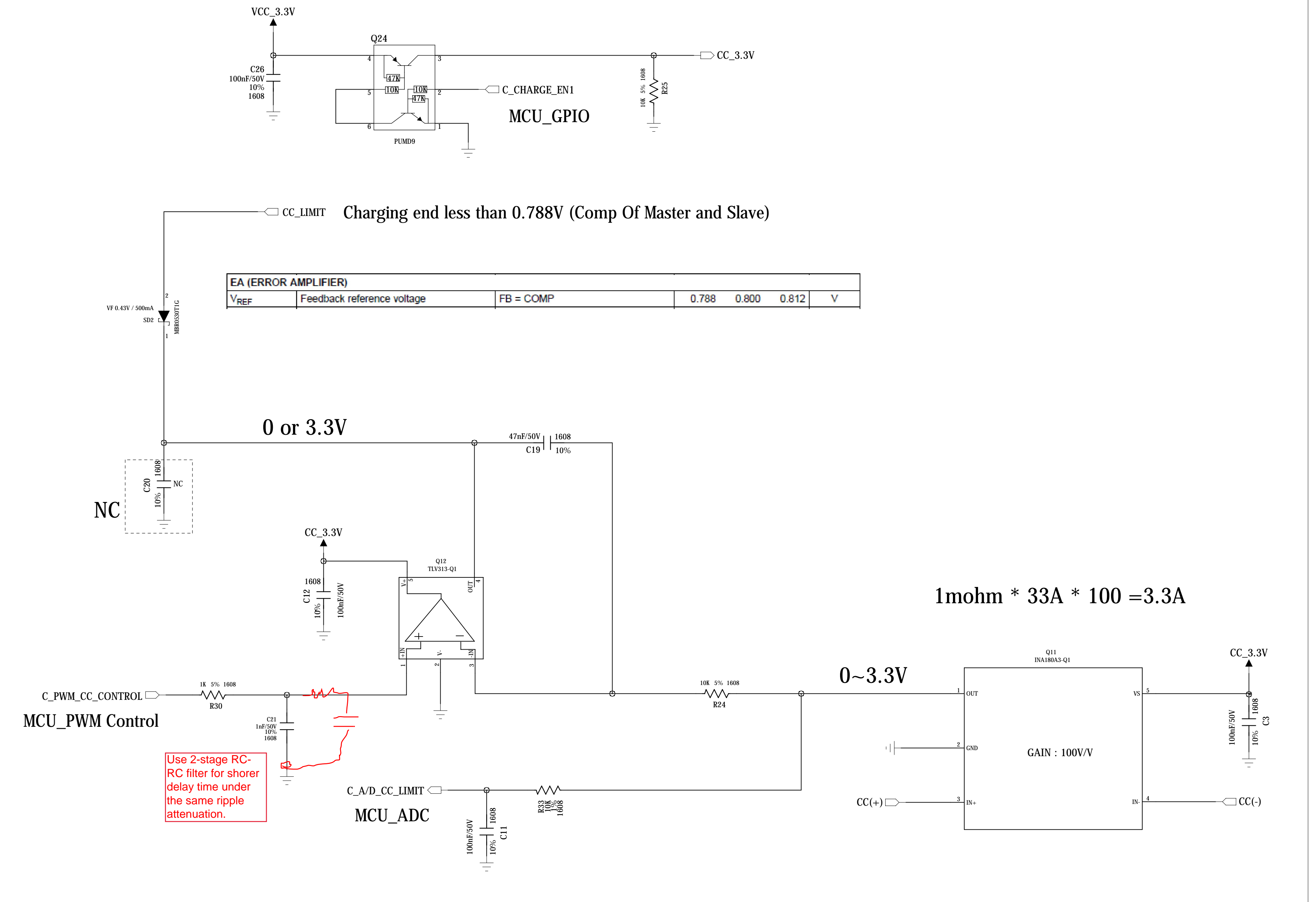
# SLAVE #2 LM5176

(Modulation frequency 2KHZ)

Use the CC\_LIMIT to control the master. The slave will follow by the sharing circuit.  
Delete the connector, or you simply short the two COMP pins.



# CC (Constant Current) Variable Control



COMPANY:		TITLE:	
		BMS	
DESIGNED: JH CHO	DATE: 18.02.28	CODR:	SIZE:
CHECKED: JH CHO	DATE: 12.06.18	DRAWING NO:	REV: 2.00
QUALITY CONTROL: <QC By>	DATE: <QC Date>	REVISION	
RELEASED: <Released By>	DATE: <Release Date>	SCALE: <Scale>	SHEET: 2 of 3