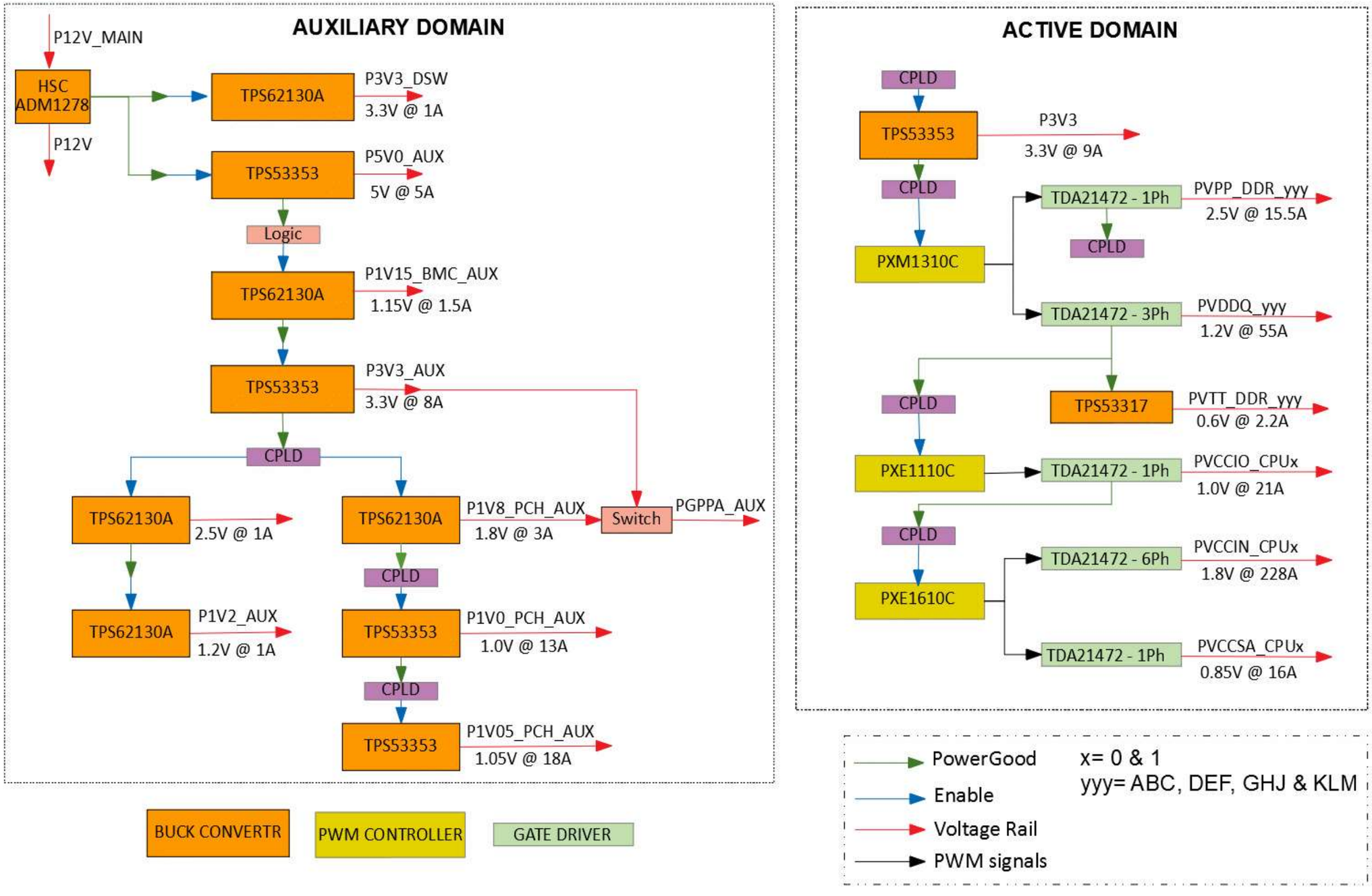
POWER DISTRIBUTION NETWORK

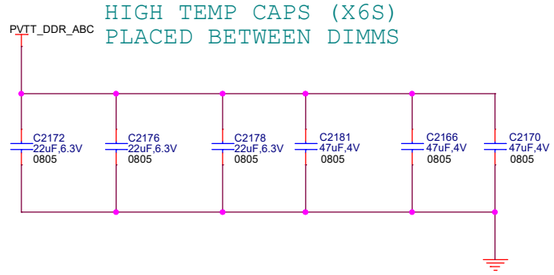


Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	11 OF 209	

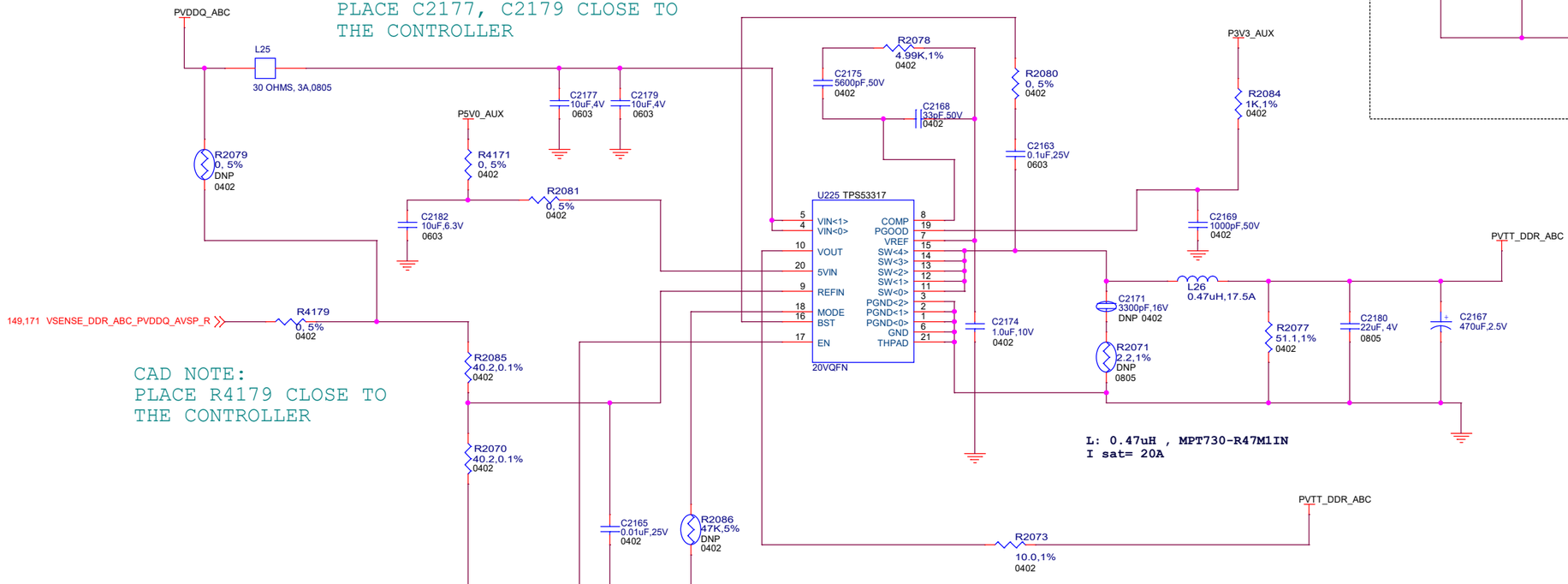
VR DDR ABC VTT

PVTT DDR SPECIFICATION:
VOUT = 0.6 VDDQ
IOUT PEAK=3.0A
SW FREQ = 1MHZ

HIGH TEMP CAPS (X6S)
PLACED BETWEEN DIMMS



CAD NOTE:
PLACE C2177, C2179 CLOSE TO
THE CONTROLLER



CAD NOTE:
PLACE R4179 CLOSE TO
THE CONTROLLER

L: 0.47uH , MPT730-R47M1IN
I sat= 20A

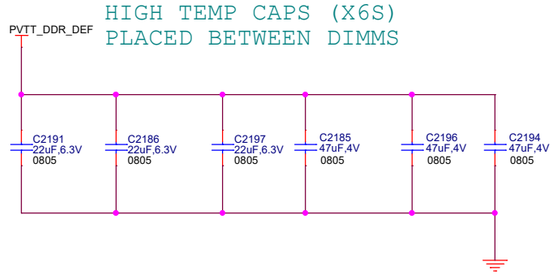
CAD NOTE:
PLACE R2073 NEAR
CENTRE OF VTT PLANE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	174 OF 209	

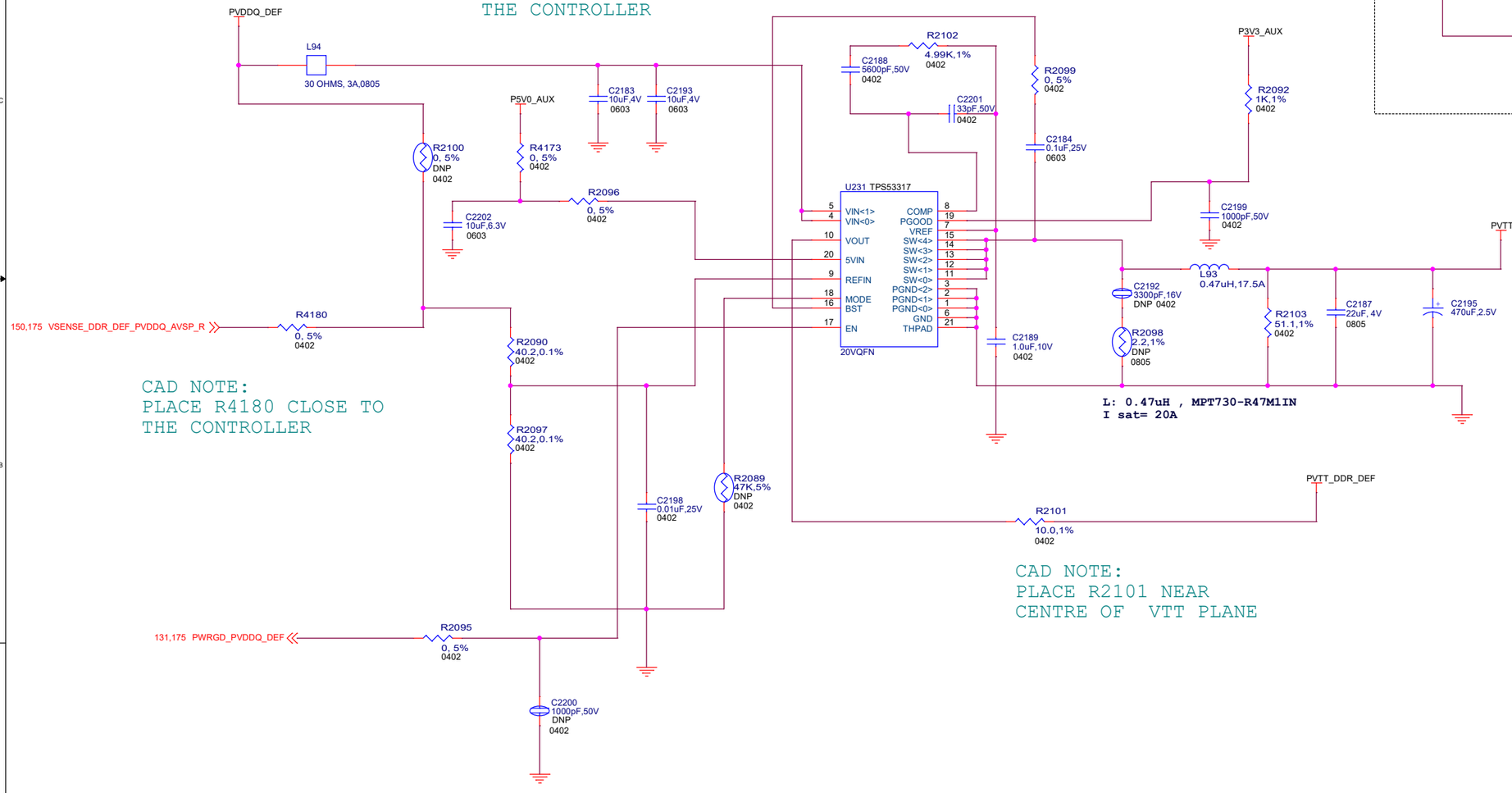
VR DDR DEF VTT

PVTT DDR SPECIFICATION:
VOUT = 0.6 VDDQ
IOUT PEAK=3.0A
SW FREQ = 1MHZ

HIGH TEMP CAPS (X6S)
PLACED BETWEEN DIMMS



CAD NOTE:
PLACE C2183, C2193 CLOSE TO
THE CONTROLLER



CAD NOTE:
PLACE R4180 CLOSE TO
THE CONTROLLER

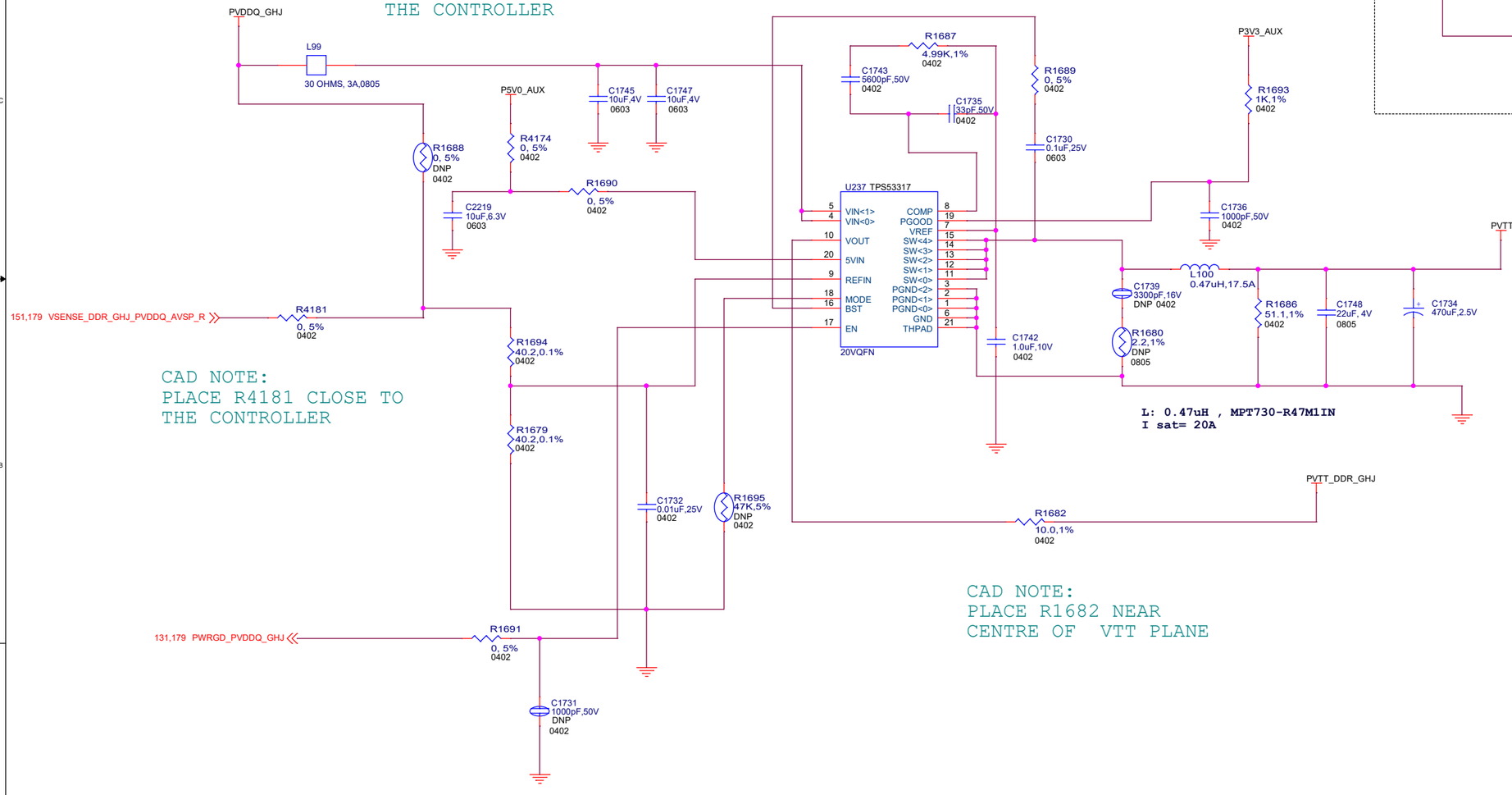
CAD NOTE:
PLACE R2101 NEAR
CENTRE OF VTT PLANE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	178 OF 209	

VR DDR GHJ VTT

PVTT DDR SPECIFICATION:
VOUT = 0.6 VDDQ
IOUT PEAK=3.0A
SW FREQ = 1MHZ

CAD NOTE:
PLACE C1745, C1747 CLOSE TO
THE CONTROLLER

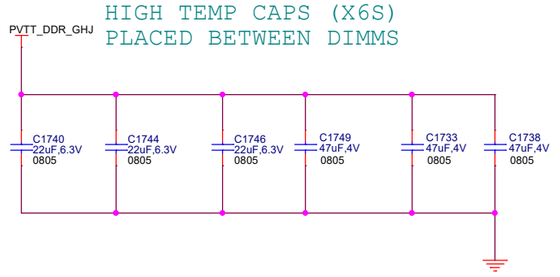


CAD NOTE:
PLACE R4181 CLOSE TO
THE CONTROLLER

L: 0.47uH , MPT730-R47M1IN
I sat= 20A

CAD NOTE:
PLACE R1682 NEAR
CENTRE OF VTT PLANE

HIGH TEMP CAPS (X6S)
PLACED BETWEEN DIMMS

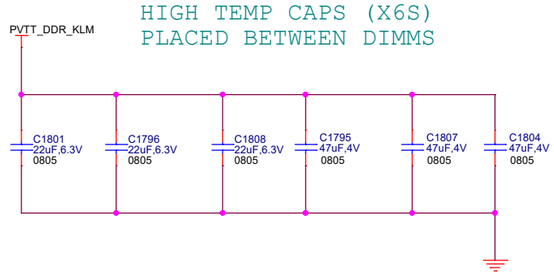


Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	182 OF 209	

VR DDR KLM VTT

PVTT DDR SPECIFICATION:
VOUT = 0.6 VDDQ
IOUT PEAK=3.0A
SW FREQ = 1MHZ

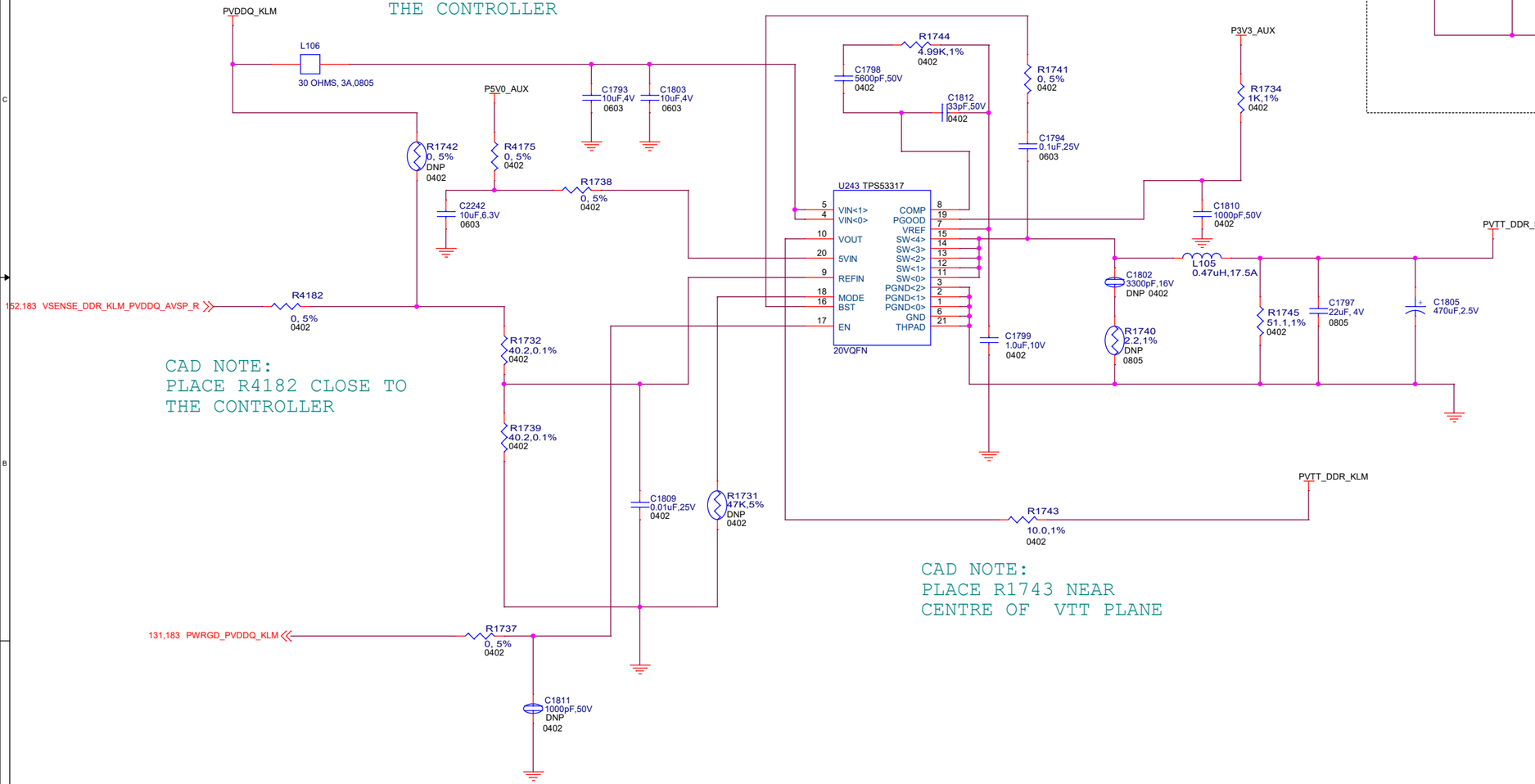
HIGH TEMP CAPS (X6S)
PLACED BETWEEN DIMMS



CAD NOTE:
PLACE C1793, C1803 CLOSE TO
THE CONTROLLER

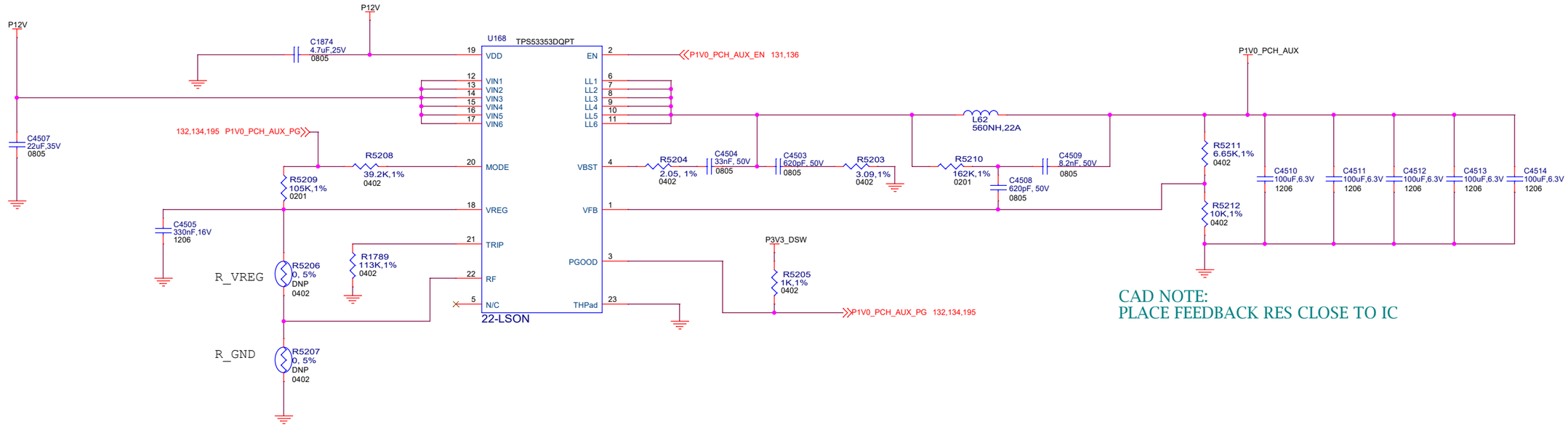
CAD NOTE:
PLACE R4182 CLOSE TO
THE CONTROLLER

CAD NOTE:
PLACE R1743 NEAR
CENTRE OF VTT PLANE



Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	186 OF 209	

P1V0_PCH_AUX POWER RAIL



CAD NOTE:
PLACE FEEDBACK RES CLOSE TO IC

VIN =12V
Device =TPS53353DQPR
Vout =1.0
Ioutmax = 13A
SW Freq = 500kHZ
I peak= 14.636A
soft start= 0.7ms

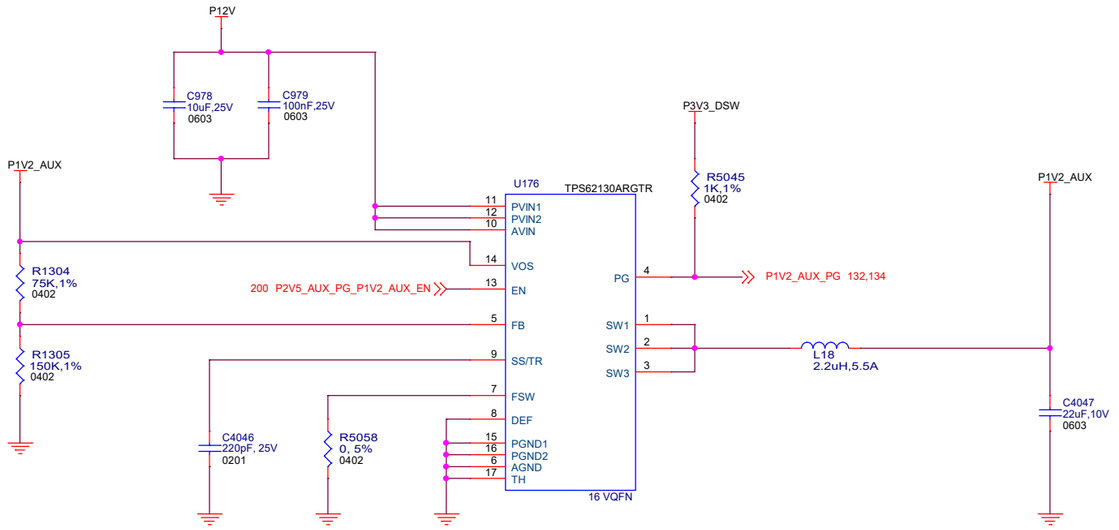
L: 0.56 µH, XAL6030-561MEB
I sat= 29A

COUT:
Cap= 100.0 uF
ESR= 1.0 mOhm
VDC= 6.3 V
GRM31CR60J107ME39L

R_VREG(k Ohm)	R_GND(k Ohm)	Frequency(khz)
open	0	250
open	187	300
open	619	400
open	open	500
866	open	650
309	open	750
124	open	850
0	open	970

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	195 OF 209	

P1V2_AUX POWER RAIL



VIN =12V Vout =1.2v

Device =TPS62130ARGTR

Ioutmax = 1A

I Peak= 1.09A

Softstart = 0.11ms

FSW=2.5MHZ

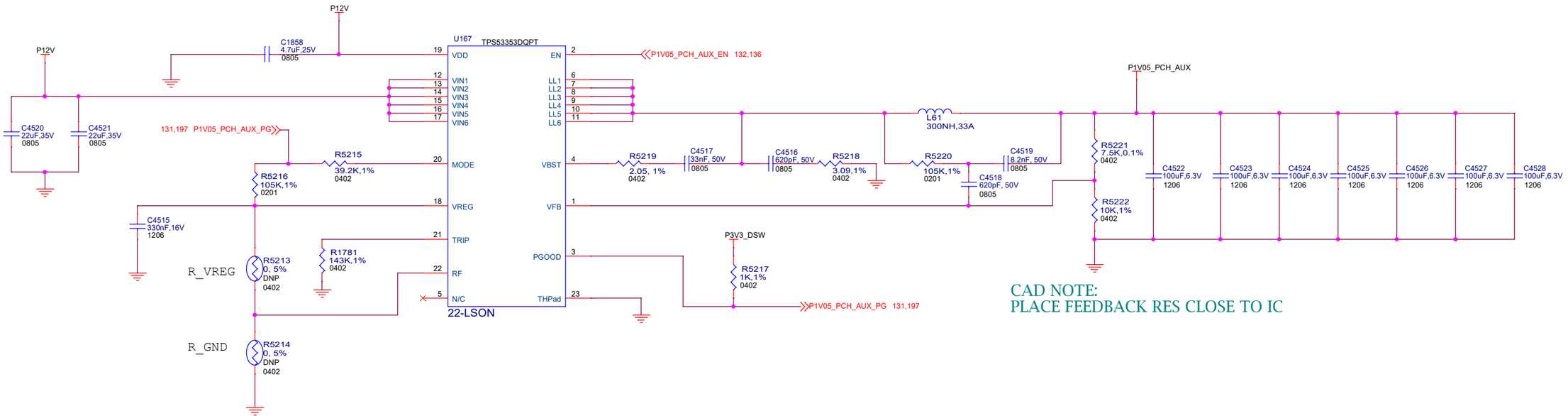
L: 2.2 µH 5.5A, XAL4020-222MEB

I sat= 5.6A

COUT:
Cap= 22.0 uF
VDC= 10 V
CL10A226MP8NUNE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	196 OF 209	

P1V05_PCH_AUX POWER RAIL



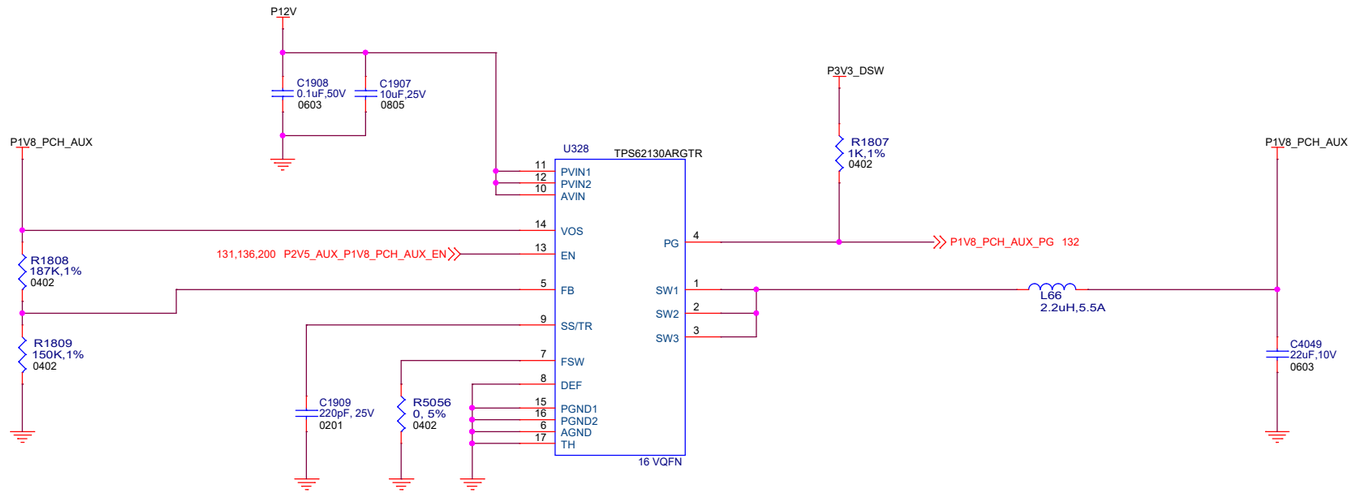
CAD NOTE:
PLACE FEEDBACK RES CLOSE TO IC

```
VIN =12V
Device =TPS53353DQPR
Vout =1.05
Ioutmax = 18A
SW Freq = 500kHZ
I peak= 21.19A
soft start= 0.7ms

L:  0.30 µH, XAL7070-301MEB
I sat= 55A

COUT:
Cap= 100.0 uF
ESR= 1.0 mOhm
VDC= 6.3 V
GRM31CR60J107ME39L
```

R_VREG(k Ohm)	R_GND(k Ohm)	Frequency(khz)
open	0	250
open	187	300
open	619	400
open	open	500
866	open	650
309	open	750
124	open	850
0	open	970

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	197 OF 209	

P1V8_PCH_AUX



VIN =12V Vout =1.8v

Device =TPS62130ARGTR

Ioutmax = 3A

I Peak= 3.139A

Softstart = 0.11ms

FSW=2.5MHZ

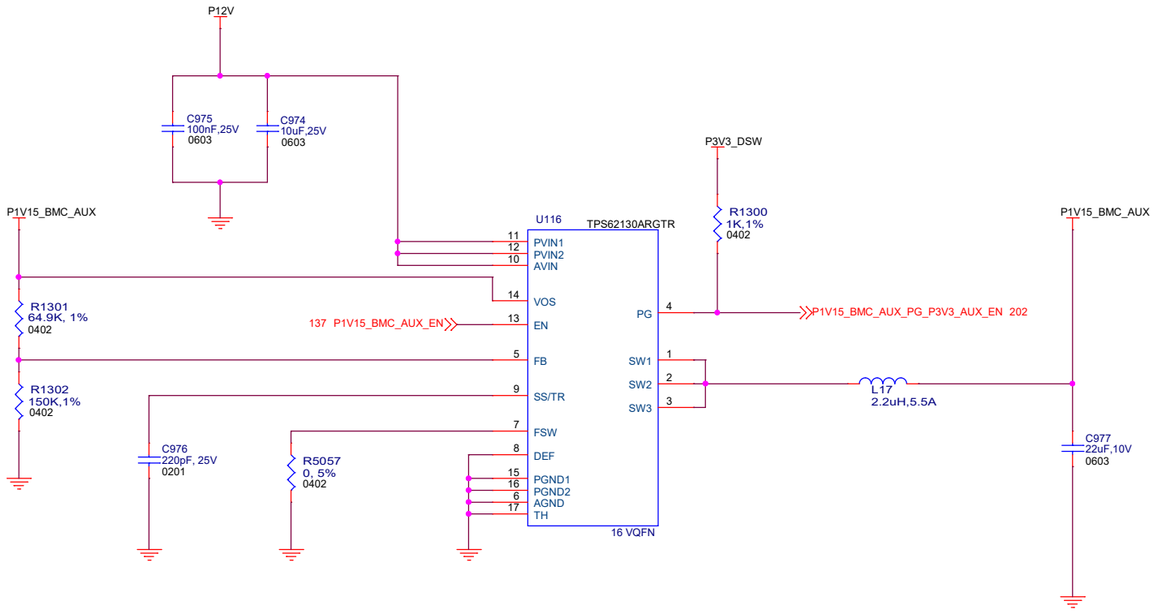
L: 2.2 µH 5.5A, XAL4020-222MEB

I sat= 5.6A

COUT:
Cap= 22.0 uF
VDC= 10 V
CL10A226MP8NUNE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	198 OF 209	

P1V15_BMC_AUX POWER RAIL



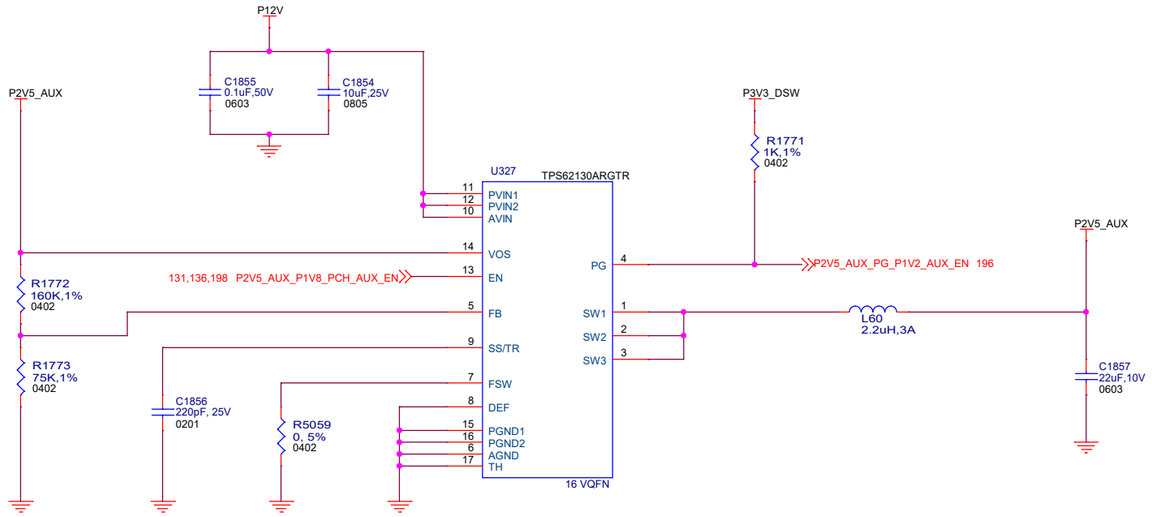
VIN =12V Vout =1.15v
Device =TPS62130ARGTR
Ioutmax = 1.5A
I Peak= 1.59A
Softstart = 0.11ms
FSW=2.5MHZ

L: 2.2 µH 5.5A, XAL4020-222MEB
I sat= 5.6A

COUT:
Cap= 22.0 uF
VDC= 10 V
CL10A226MP8NUNE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	199 OF 209	

P2V5_AUX POWER RAIL



VIN =12V Vout =2.5v

Device =TPS62130ARGTR

Ioutmax = 1A

I Peak= 1.179A

Softstart = 0.11ms

FSW=2.5MHZ

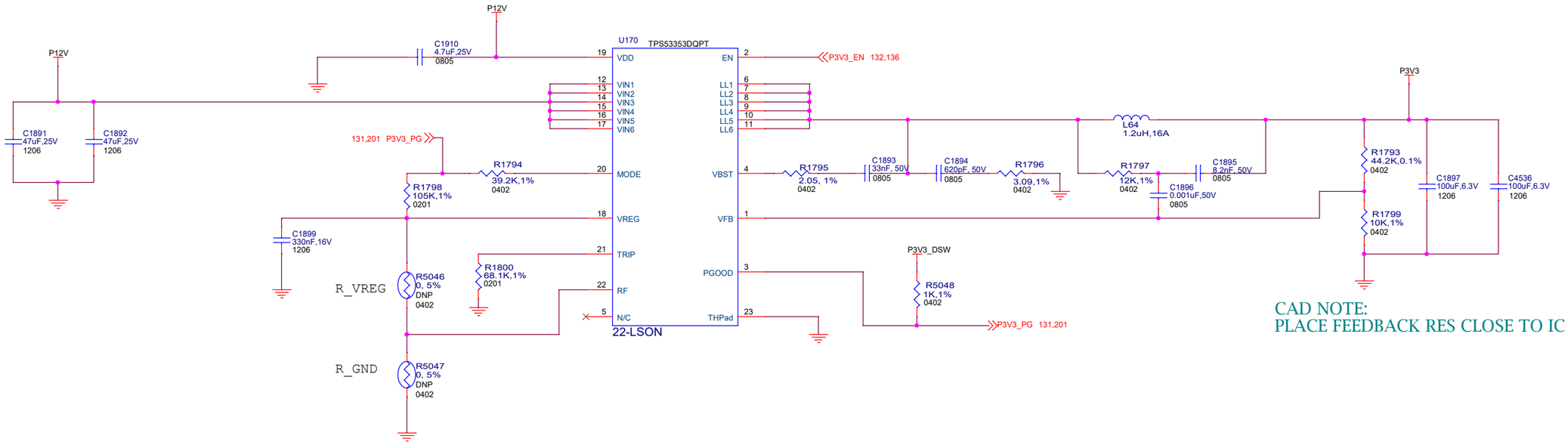
L: 2.2 µH 5.5A, XAL4020-222MEB

I sat= 5.6A

COUT:
Cap= 22.0 uF
VDC= 10 V
CL10A226MP8NUNE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	200 OF 209	

P3V3 POWER RAIL



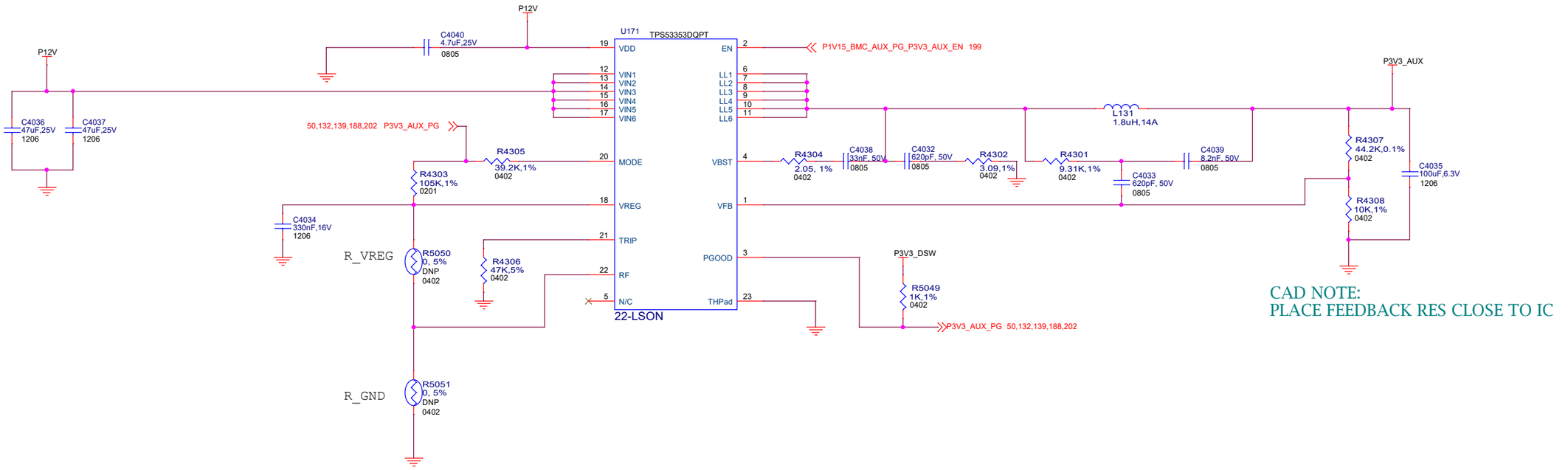
CAD NOTE:
PLACE FEEDBACK RES CLOSE TO IC

```
VIN =12V
Device =TPS53353DQPR
Vout =3.3
Ioutmax = 9A
SW Freq = 500kHZ
I peak= 10.329A
soft start= 0.7ms

L:  1.2 µH, XAL6030-122MEB
I sat= 22.0A

COUT:
Cap= 100.0 uF
ESR= 1.0 mOhm
VDC= 6.3 V
GRM31CR60J107ME39L
```

R_VREG(k Ohm)	R_GND(k Ohm)	Frequency(khz)
open	0	250
open	187	300
open	619	400
open	open	500
866	open	650
309	open	750
124	open	850
0	open	970

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	201 OF 209	

P3V3_AUX POWER RAIL



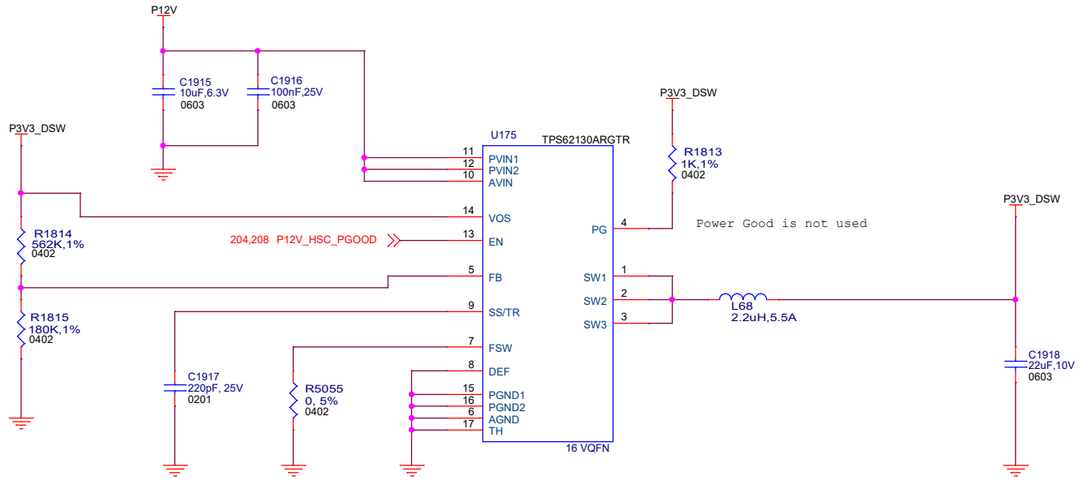
CAD NOTE:
PLACE FEEDBACK RES CLOSE TO IC

```
VIN =12V
Device =TPS53353DQPR
Vout =3.3
Ioutmax = 8A
SW Freq = 500kHZ
I peak= 9.329A
soft start= 0.7ms

L:  1.8 µH, XAL6030-182MEB
I sat= 18.2A

COUT:
Cap= 100.0 uF
ESR= 1.0 mOhm
VDC= 6.3 V
GRM31CR60J107ME39L
```

R_VREG(k Ohm)	R_GND(k Ohm)	Frequency(khz)
open	0	250
open	187	300
open	619	400
open	open	500
866	open	650
309	open	750
124	open	850
0	open	970

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	202 OF 209	

P3V3_DSW POWER RAIL



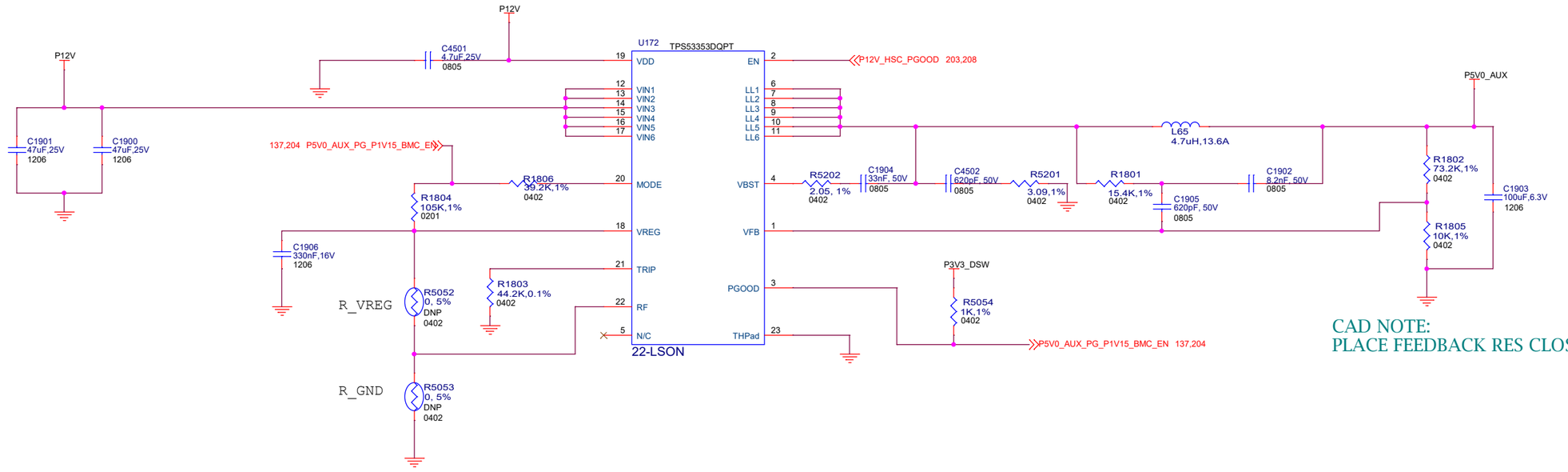
VIN =12V Vout =3.3v
Device =TPS62130ARGTR
Ioutmax = 1A
I Peak= 1.217A
Softstart = 0.11ms
FSW=2.5MHZ

L: 2.2 µH 5.5A, XAL4020-222MEB
I sat= 5.6A

COUT:
Cap= 22.0 uF
VDC= 10 V
CL10A226MP8NUNE

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	203 OF 209	

P5V0_AUX POWER RAIL



CAD NOTE:
PLACE FEEDBACK RES CLOSE TO IC

```
VIN = 12V
Device =TPS53353DQPR
Vout =5
Ioutmax = 5A
SW Freq = 500kHZ
I peak= 5.6205A
soft start= 0.7ms

L: 4.7uH , XAL7070-472MEB
I sat= 15.2A

COUT:
Cap= 100.0 uF
ESR= 1.0 mOhm
VDC= 6.3 V
GRM31CR60J107ME39L
```

R_VREG(k Ohm)	R_GND(k Ohm)	Frequency(khz)
open	0	250
open	187	300
open	619	400
open	open	500
866	open	650
309	open	750
124	open	850
0	open	970

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	204 OF 209	

HOT SWAP CONTROLLER

DESIGNED FOR 140A

12V_MAIN

J63

46207-0024

C2261 0.1uF,50V 0402
C2262 0.1uF,50V 0402
C2263 0.1uF,50V 0402
C2264 0.1uF,50V 0402
C2265 0.1uF,50V 0402
C2266 0.1uF,50V 0402
C2267 0.1uF,50V 0402
C2268 0.1uF,50V 0402
C2269 0.1uF,50V 0402
C2270 0.1uF,50V 0402
C2271 0.1uF,50V 0402
C2272 0.1uF,50V 0402

Date: Dec 27, 2019

Rev 2.0:
Q72, Q73 are added

RSENSE = 0.000166 OHM
(R2174 || R2175 || R2176)

R2174 0.0005,1% 2512
R2175 0.0005,1% 2512
R2176 0.0005,1% 2512

Q72 Q62 Q63 Q73
LFPAK (SOT669)
PSMN0R9-25YLC

P12V

C2274 1uF,25V 0603

R2196 10,1% 0603
R2213 10,1% 0603
R2180 10,1% 0603
R2181 10,1% 0603
R2194 10,1% 0603
R2207 10,1% 0603
R2171 10,1% 0603
R2208 1K,1% 0603
R3111 0, 5% 0402
C2273 22nF,50V 0603
C2277 0.1uF,16V 0603

R2193 100K,1% 0603
R2185 100K,1% 0603
R2203 10,1% 0603
R2184 7.68K,1% 0603
C2283 0.1uF,16V 0603
R2201 11K,1% 0603
C2280 0.1uF,16V 0603
C2259 1uF,25V 0603
C2279 1uF,25V 0603
R2186 100K,1% 0603
R2198 100K,1% 0603
HS_OV
HS_UV
HS_VCAP

SGND1

U248
ADM1278

VCC
VCAP
UV
OV
PSET
ISET
ISTART
TIMER
GPIO1/ALERT1_N
GPIO2/ALERT2_N
RETRY
PWGIN
ENABLE
FAULT_N
GND
PGND
TH_PAD
HS-
HS+
MO-
MO+
GATE
VOUT
PWRGD
SCL
SDA
ADR1
ADR2
SPISS_N
MCLK
MDAT
CSOUT
TEMP
32LFSCP

HS_ISENS_N
HS_ISENS_P
R2190 2.2,1% 0603
C2260 0.1uF,16V 0402
R2205 2.2,1% 0603
HOTSWAP_PG 208
TP1317 HS_TIMER
TP21 CSOUT

R2214 100K,1% 0603
R3108 1K,1% 0402
R3109 75K,1% 0402
HS_ISET
HS_ISTART
HS_PSET
C2281 0.1uF,16V 0603
R2179 19.3K,1% 0402
C2282 1000pF,25V 0603
R2178 26.5K,1% 0402
C2275 0.1uF,16V 0603
C2276 22nF,50V 0603

R3112 0, 5% 0402
R3113 0, 5% 0402
SMB_PMBUS1_STBY_LVC3_SCL 103
SMB_PMBUS1_STBY_LVC3_SDA 103

P3V3_DSW
R2192 4.7K,1% 0402
R2210 4.7K,1% 0402
R2211 4.7K,1% 0402 DNP
R2200 4.7K,1% 0402 DNP
R2191 4.7K,1% 0402
R2219 4.7K,1% 0402

R3115 0, 5% 0402
R3116 0, 5% 0402
R3117 0, 5% 0402
R3118 0, 5% 0402
131 HSC_ALERT1
131 HSC_ALERT2

Date: Oct 24, 2019

Rev2.0:
Added R5340 PU on HSC_ALERT2

R5339 4.7K,1% 0402
R5340 4.7K,1% 0402
R2188 4.7K,1% 0402
C2278 0.1uF,16V 0603

12V_MAIN
R2173 100K,1% 0603
R2172 100K,1% 0603
Q64 MMBT3906-7-F SOT23
R2212 16K,1% 0603
R2216 100K,1% 0603
R2209 16K,1% 0603

Q65 MMBT3904-7-F SOT-23-3

R2218 100,1% 0402

P12V
R2202 100K,1% 0603
R2189 15K,1% 0603

R3114 0, 5% 0402

P12V
R3100 10K,1% 0402
R2182 4.7K,1% 0402
R3101 3.83K,1% 0402
208 HOTSWAP_PG
P12V_HSC_PGOOD 203,204

HSC PWRGD SCALED FOR 3.3V

JP3
22-28-4020

R2195 4.7K,1% 0402
116,131 HSC_FAULT_N

Date: Dec 27, 2019

Rev 2.0:
Supply voltage of PWGIN pin is changed to P12V
from 12V_MAIN

Organisation Name: Centre for Development of Advanced Computing HPC Technologies, Pune		
Title: Rudra Main Board	Engineer: System Design Team	
Size: C	Document Number: mainboard_rudra_v2.0	Rev: 2.0
Date: Jan 22, 2020	208 OF 209	