SEE PAGE A1 FOR REVISION HISTORY

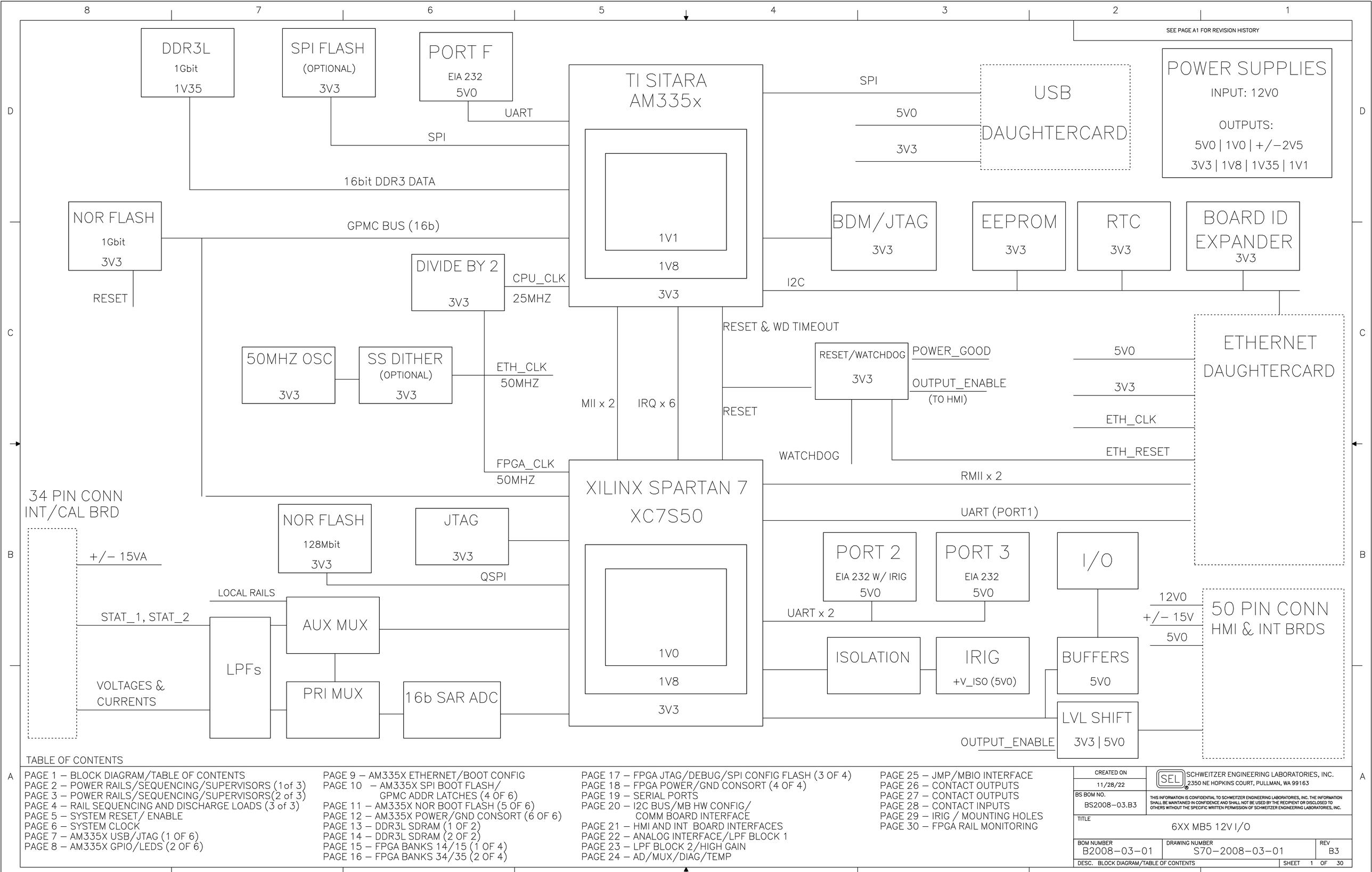

TABLE OF CONTENTS

CREATED ON 11/28/22	SEL SCHWEITZER ENGINEERING LABORATORIES, INC. 2350 NE HOPKINS COURT, PULLMAN, WA 99163
BS BOM NO. BS2008–03.B3	
TITLE 6XX MB5 12V I/O	
BOM NUMBER B2008–03–01	DRAWING NUMBER S70–2008–03–01 REV B3
DESC. BLOCK DIAGRAM/TABLE OF CONTENTS	SHEET 1 OF 30

5V_STBY, 1V, 5V LOCAL POWER SUPPLIES

MODE AND PWR SEQUENCE CONFIGURATION

TP215 V7V

100k,1/16W,1% R529 — 463-100K — 100k,1/16W,1% R536 — 463-100K

Forced Continuous Current Mode

TP214 TP207 TP213

5V_STDBY_LEN1
PS_MODE
5V_PS_EN1
1V_PS_EN2
5V_PS_EN3 — 4B8

DNP

Q63 BSS138 (1, 2, 3) — 326-0298

0,1/16W,5% R523 — 463-0000 — 1V_EN_SEQ — 4B5

0.01uF,50V,5% C429 — 406-0147

3B6 +5V_2V5_1V8_DISABLE

DGND

Dual Comparator Circuit
Ch 1 – 1.8V UV Supervisor
Ch 2 – 1V Shutdown RC Timer

Depopulate if using Primary Sequence Circuit

+5V_STBY +1V8 DNP +1V8_PGOOD +1V_DISABLE

1.8V Supervisor Circuit from Primary Sequence Page — 4C6

3A6 +12V_UVLO

+5V_STBY — 20k,1/16W,1% R715 — 463-20K0 — Q66 BSS138

Slave PGOOD Debounce (Place by the slave PMIC)

+3V3 — 3.32k,1/16W,1% R705 — 463-3K32

Q68 BSS138 — Q67 BSS138

0,1/16W,5% R404 — 463-0000 — DDR3_VREF_EN — 14C8,6D4

3D4 1V1_3V3_1V35_PGOOD — 1uF,10V,15% C577 — 041-0265

326-0298

+/– 2.5V Supervisor

+2V5A +5V_STBY DNP

20k,1/10W,1% R461 — 462-20K0

16.5k,1/10W,1% R723 — 462-16K5

TP705 TP689

U43 MC33161 (VREF, MS, IN1, IN2, OUT1, OUT2) — 151-0586

0,1/16W,5% R451 — 463-0000

0.1uF,16V,10% C583 — 406-0012

24.9k,1/16W,1% R460 — 252-2492

43.2k,1/10W,1% R450 — 462-43K2

0.1uF,16V,10% C578 — 406-0012

−2V5A

MS = GND: Ch1 & Ch2 Non-Inverting
MS = VREF: Ch1: Non Ch2: Inverting
MS = VCC: Ch1 & Ch2 Inverting

+12V FAIL Monitor & Power Rails Supervisor

+5V_STBY +12V +3V3

20k,1/16W,1% R385 — 463-20K0

100k,1/16W,1% R405 — 463-100K

1M,1/16W,1% R330 — 463-1M00

10k,1/16W,1% R331 — 463-10K0

U30 MC33161 (VREF, MS, IN1, IN2, OUT1, OUT2) — 151-0586

TP517

PWR_ON_RESET — 5C8

12V_POWER_FAIL — 8D7

PGOOD

12V POWER FAIL Falling Threshold – 8.9V
(To alert FW that +12V power may turn-off)

1uF,10V,15% C320 — 041-0265

470pF,50V,5% C321 — 406-0006

15k,1/10W,1% R387 — 462-16K5

5ms PGOOD delay
To meet 1.5ms CPU_CLK Enable to POR deassertion setup requirement

Master PGOOD Debounce

+5V_STBY — 20k,1/16W,1% R550 — 463-20K0

Q64 BSS138 — Q62 BSS138

1uF,10V,15% C423 — 041-0265

5V0_1V0_PGOOD

326-0298

+12V — 120ohm,@100MHz,3A L9 — 440-0019

+5V_PS

Place only one.

0,1/4W,5% R94 — 255-000

Place one at each capacitor next to the VIN inputs in front of the bulk capacitors.

0.022uF,25V,10% C44 — 406-0196
0.022uF,25V,10% C48 — 406-0196
0.022uF,25V,10% C45 — 406-0196

10uF,25V,10% C40 — 406-0187
10uF,25V,10% C41 — 406-0187

10uF,25V,10% C38 — 406-0094
10uF,25V,10% C39 — 406-0094
10uF,25V,10% C50 — 406-0094
10uF,25V,10% C49 — 406-0094
10uF,25V,10% C42 — 406-0094
10uF,25V,10% C43 — 406-0094

TP246 TP234 TP267

+5V_STBY — 10k,1/16W,1% R96 — 463-10K0

10uF,25V,20% C32 — 406-0227

5V0_1V0_PGOOD

PS_MODE

5V_PS_EN1
1V_PS_EN2
5V_PS_EN3

0.01uF,50V,10% C29 — 406-0016

COMP1

+12V — 0,1/16W,5% R530 — 463-0000

10uF,25V,10% C418 — 406-0094

+5V_STBY TP690

1k,1/8W,1% R115 — 255-1001

1k,1/8W,1% R116 — 255-1001

0,1/4W,5% L11 — 255-000

TP254

1uF,16V,10% C53 — 406-0045

1uF,16V,10% C54 — 406-0045

10k,1/16W,1% R85 — 463-10K0 — LFB1 — 5V_STDBY_LEN1

1.33k,1/16W,1% R84 — 252-1331

10k,1/16W,1% R538 — 463-10K0

10k,1/16W,1% R85 — 463-10K0

10k,1/16W,1% R537 — 463-10K0

U11 TPS65262-2RHB

VIN1	28	BST1	25
VIN2	12	LX1	26
VIN3	13	FB1	23
V7V	20	BST2	9
PGOOD	5	LX2	10
MODE	6	FB2	7
EN1	24	BST3	16
EN2	8	LX3	15
EN3	17	FB3	18
SS1	22		
COMP1	21		
LVIN1	32		
LOUT1	31		
LFB1	30		
LEN1	29		
LVIN2	1		
LOUT2	2		
LFB2	3		
LEN2	4		
AGND	19		
PGND1	27		
PGND2	11		
PGND3	14		
PWRPAD	33		

431-1476

XXX-039 PP1

10uH, 3A L6 — 412-0152

0.047uF,16V,10% C36 — 406-0129

10,1/16W,1% R518 — 463-10R0

10k,1/16W,1% R517 — 463-10K0

22pF,50V,5% C415 — 406-0192

0.022uF,16V,10% C28 — 041-0658

47uF,10V,10% C26 — 406-0182

47uF,10V,10% C27 — 406-0182

TP199

0,1/4W,5% L4 — 255-000 — TP188 +5V

Place on Bottom Side

1k,1/8W,1% R52 — 255-1001

1k,1/8W,1% R51 — 255-1001

1.33k,1/16W,1% R521 — 252-1331

XXX-039 PP3

0.047uF,16V,10% C55 — 406-0129

10uH, 3A L13 — 412-0152

TP268

0,1/4W,5% L12 — 255-000 — TP225 +1V

10,1/16W,1% R549 — 463-10R0

10k,1/16W,1% R542 — 463-10K0

22pF,50V,5% C430 — 406-0192

0.022uF,16V,10% C61 — 041-0658

47uF,10V,10% C59 — 406-0182

1k,1/16W,1% R113 — 463-1K00

15k,1/10W,1% R543 — 462-15K0

XXX-039 PP2

0.047uF,16V,10% C37 — 406-0129

10uH, 3A L7 — 412-0152

TP184

0,1/4W,5% L8 — 255-000 — TP255 +5V_PS

10,1/16W,1% R516 — 463-10R0

10k,1/16W,1% R515 — 463-10K0

22pF,50V,5% C414 — 406-0192

0.022uF,16V,10% C33 — 041-0658

47uF,10V,10% C34 — 406-0182

1k,1/8W,1% R53 — 255-1001

1k,1/8W,1% R54 — 255-1001

2.2k,1/10W,1% R520 — 462-2K20

5V BUCK1 COMPENSATION

TP198 — COMP1 — +5V_STBY

5.6pF,50V,+/-0.25pF C30 — 041-0231

47.5k,1/16W,1% R59 — 463-47K5

3300pF,50V,10% C31 — 406-0066

+5V_STBY — 0.1uF,16V,10% C278 — 406-0012 — U30 MC33161 (VCC, GND) — 151-0586 — 1uF,16V,10% C287 — 406-0045

+5V_STBY — 0.1uF,16V,10% C366 — 406-0012 — U43 MC33161 (VCC, GND) — 151-0586

POWER SUPPLY TEST POINTS

TP230 TP440 TP565 TP327 TP200 TP426

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TITLE	6XX MB5 12V I/O		
BOM NUMBER	B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. +5V_STBY/+5V/+1V/+5V_PS		SHEET 2 OF 30	

CREATED ON 11/28/22

SEL SCHWEITZER ENGINEERING LABORATORIES, INC.
2350 NE HOPKINS COURT, PULLMAN, WA 99163

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TITLE: 6XX MB5 12V I/O

BOM NUMBER: B2008–03–01 | DRAWING NUMBER: S70–2008–03–01 | REV: B3

DESC. +3V3/+1V35/+1V1/+1V8/+2V5 RAILS | SHEET 3 OF 30

PRIMARY POWER RAIL SEQUENCE CIRCUIT

Power–Up Rail Enable Sequencing
+12V –> +5V_STBY –> PWR_UP_EN –> 1V (FPGA CORE/BRAM) –> 5V/ 3.3V (CPU, FPGA, BOARD I/O) –> 1.35V (CPU DDR3L) –> 1.1V (CPU CORE)
1.8V (CPU/FPGA) / 2.5VA (DAQ)

Power–Down Rail Disable Sequencing
+12V UVLO –> NOT (PWR_UP_EN) –> 1V1(CPU Core) –> 1.35V (CPU DDR3L) –> 5V/3.3V (CPU, FPGA, BOARD I/O) –> 1V (FPGA CORE/BRAM) –> +5V_STBY
1.8V (CPU/FPGA)/ 2.5VA (DAQ)

Dual Comparator Circuit
Ch1 – +12V Power Up/Down Detection
Ch2 – 1.8V Supervisor

(Populate both comparator circuits if using PRI SEQ circuit.)

+1V8
3.32k,1/16W,1%
R510
463–3K32
0.01uF,50V,10%
C406
406–0016
10k,1/16W,1%
R509
463–10K0
DGND

+12V
180k,1/10W,1%
R508
462–180K
0.01uF,50V,10%
C403
406–0016
36.5k,1/10W,1%
R507
462–36K5
DGND

+5V_STBY
10k,1/16W,1%
R504
463–10K0
DNP

U54
MC33161
VREF
MS
IN1
IN2
OUT1
OUT2
151–0586

MS = GND: Ch1 & Ch2
Non–InvertingMS = VREF: Ch1: Non Ch2: Inv
MS = VCC: Both Ch1 & Ch2 Inverting

PWR_UP_EN
0,1/16W,5%
R495
463–0000
PGOOD
2B7

DGND

Logic "OR" Enable Circuit

+5V_STBY
10k,1/16W,1%
R495
463–10K0
10k,1/16W,1%
R490
463–10K0

Q56 BSS138 326–0298
Q59 BSS138 326–0298
Q58 BSS138 326–0298
DGND

0.01uF,50V,5%
C393
406–0147
DGND

Three Rail Power Up/Down Rail Sequencer ICs
10ms delay

+5V_STBY
U50
LM3880MF
VCC
EN
GND
FLAG1
FLAG2
FLAG3
431–1484

F1_1V_EN_SEQ
F2_GRP_EN
F3_1V35_EN

U51
NC7SZ08P5X
431–0412

DNP

+5V_STBY
U53
LM3880MF
431–1484
10k,1/16W,1%
R32
463–10K0
F1_SEQ2_1V1_EN

0.01uF,50V,5%
C398
406–0147
DGND

DNP

0,1/16W,5%
R33
463–0000

+5V_STBY
10k,1/16W,1%
R41
463–10K0
Q7 BSS138 326–0298

+3V3
10k,1/16W,1%
R51
463–10K0
Q6 BSS138 326–0298
PWR_DOWN
5D7

0,1/16W,5%
R491
463–0000

+5V_STBY
10k,1/16W,1%
R16
463–10K0
10k,1/16W,1%
R11
463–10K0
Q4 BSS138 326–0298
Q1 BSS138 326–0298
F1_1V_EN_SEQ
1V_EN_SEQ
2D6
DGND
DNP

+5V_STBY
10k,1/16W,1%
R8
463–10K0
10k,1/16W,1%
R9
463–10K0
Q2 BSS138 326–0298
Q3 BSS138 326–0298
F2_GRP_EN
3V3_5V_1V8_2V5_EN_SEQ
3C5
DGND
DNP

+5V_STBY
10k,1/16W,1%
R489
463–10K0
10k,1/16W,1%
R488
463–10K0
Q57 BSS138 326–0298
Q55 BSS138 326–0298
F3_1V35_EN
1V35_EN_SEQ
3C6
DGND
DNP

+5V_STBY
10k,1/16W,1%
R497
463–10K0
10k,1/16W,1%
R498
463–10K0
Q60 BSS138 326–0298
Q61 BSS138 326–0298
F1_SEQ2_1V1_EN
1V1_EN_SEQ
3C7
DGND
DNP

+12V
TP730
MBR0530T3G
D65
424–0104
10,1/2W,5%
R405
464–10R0
10k,1/16W,1%
R65
463–10K0
Q12 BSS138 326–0298
Q11 BSS138 326–0298
2D6
5V_PS_EN3
33,1/8W,1%
R64
255–33R0
+5V_PS
DGND

RAIL DISCHARGE CIRCUITS

10uF,25V,10%
C326
406–0094
DGND

+5V
10k,1/16W,1%
R294
463–10K0
33,1/8W,1%
R277
255–33R0
Q37 BSS138 326–0298
Q36 BSS138 326–0298
3V3_5V_1V8_2V5_EN_SEQ1

+3V3
33,1/8W,1%
R367
255–33R0
Q42 BSS138 326–0298

+1V8
80,5,1/8W,1%
R225
255–82R5
Q35 BSS138 326–0298

DGND

+1V35
10k,1/16W,1%
R160
463–10K0
10,1/2W,5%
R148
464–10R0
Q22 BSS138 326–0298
Q18 BSS138 326–0298
1V35_EN_SEQ

+1V1
10k,1/16W,1%
R159
463–10K0
10,1/2W,5%
R147
464–10R0
Q21 BSS138 326–0298
Q20 BSS138 326–0298
1V1_EN_SEQ

+1V
10k,1/16W,1%
R104
463–10K0
10,3/4W,5%
R103
461–0229
Q16 BSS138 326–0298
Q14 BSS138 326–0298
1V_EN_SEQ

DGND

+5V_STBY
U54
MC33161
VCC
GND
151–0586
0.1uF,16V,10%
C405
406–0012
U51
NC7SZ08P5X
VCC
GND
431–0412
0.01uF,50V,5%
C394
406–0147
1uF,16V,10%
C395
406–0045
DGND

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11/28/22	2350 NE HOPKINS COURT, PULLMAN, WA 99163

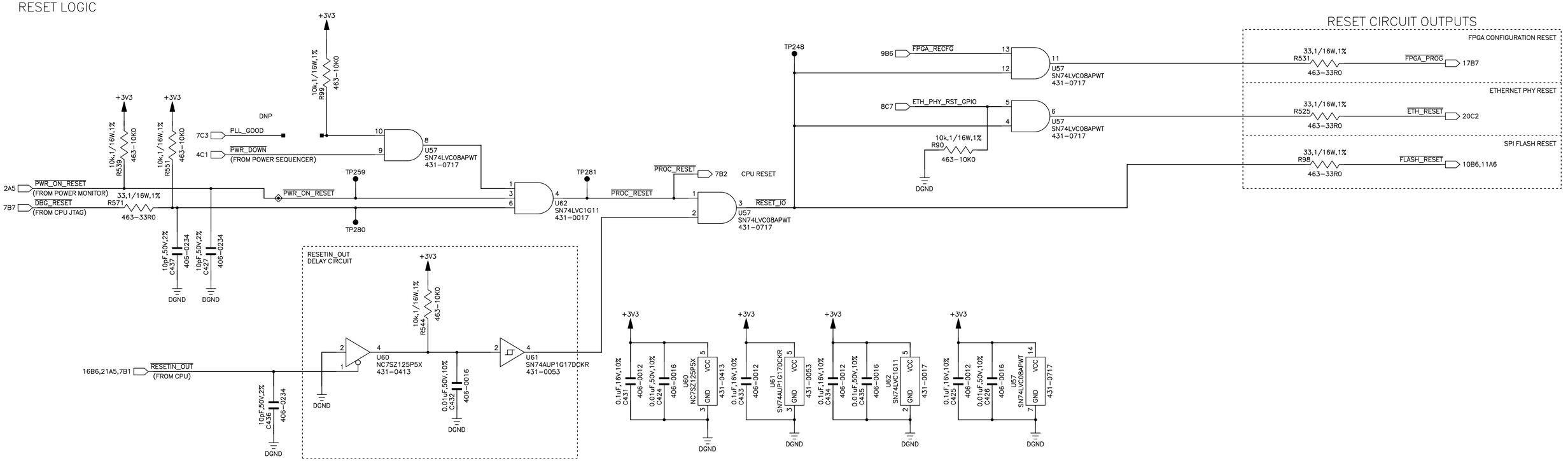
TITLE: 6XX MB5 12V I/O

BOM NUMBER	DRAWING NUMBER	REV
B2008–03–01	S70–2008–03–01	B3

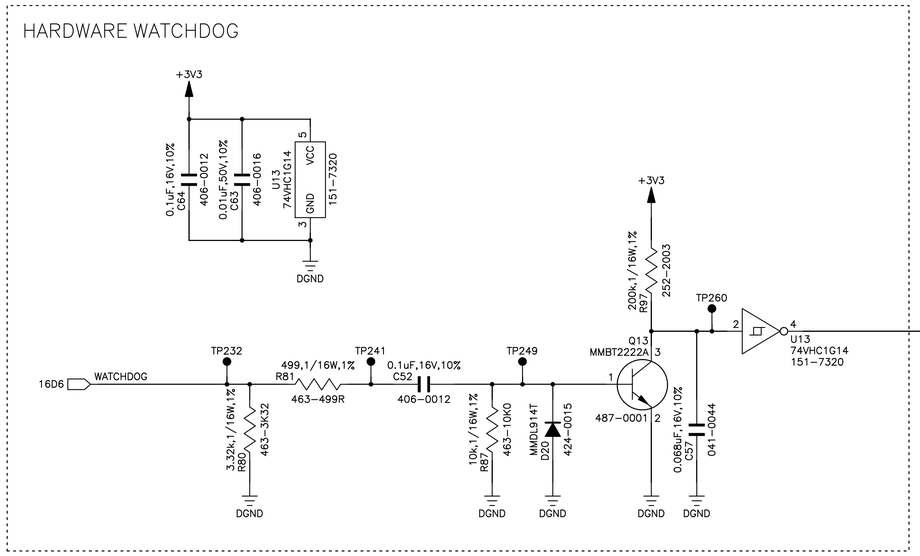
DESC. PRIMARY RAIL SEQUENCE, POWER DOWN RAIL DISCHARGE — SHEET 4 OF 30

RESET AND WATCHDOG

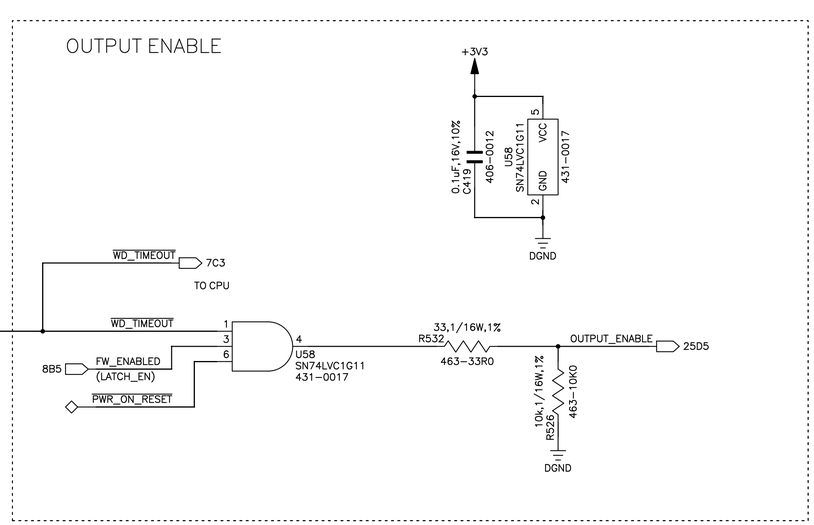
RESET LOGIC



HARDWARE WATCHDOG



OUTPUT ENABLE



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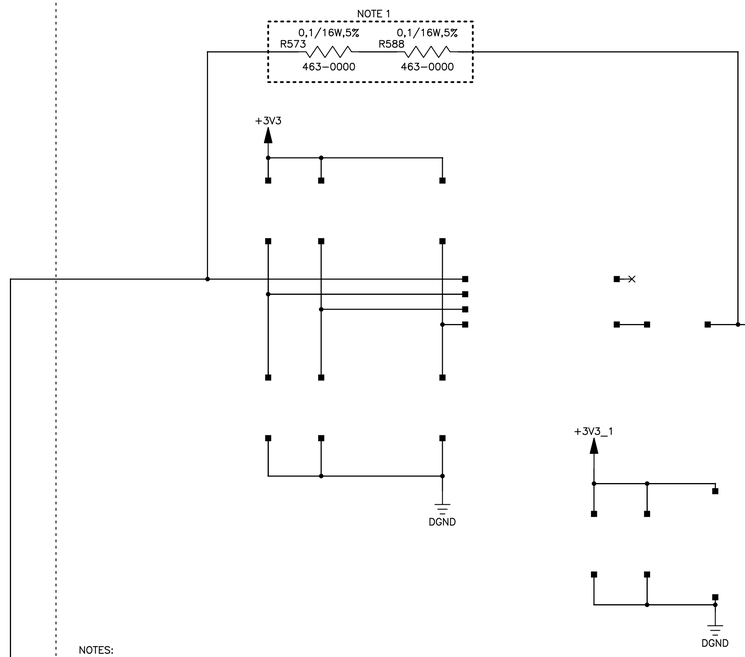
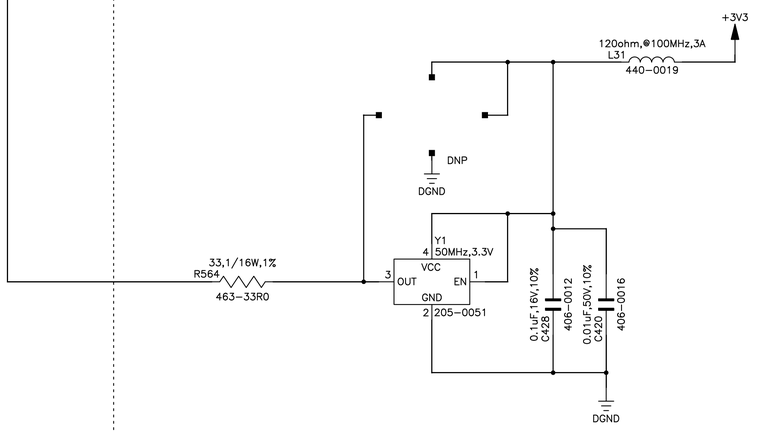
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. RESET, WATCHDOG, OUTPUT_ENABLE	SHEET 5 OF 30

SPREAD SPECTRUM MODULATOR

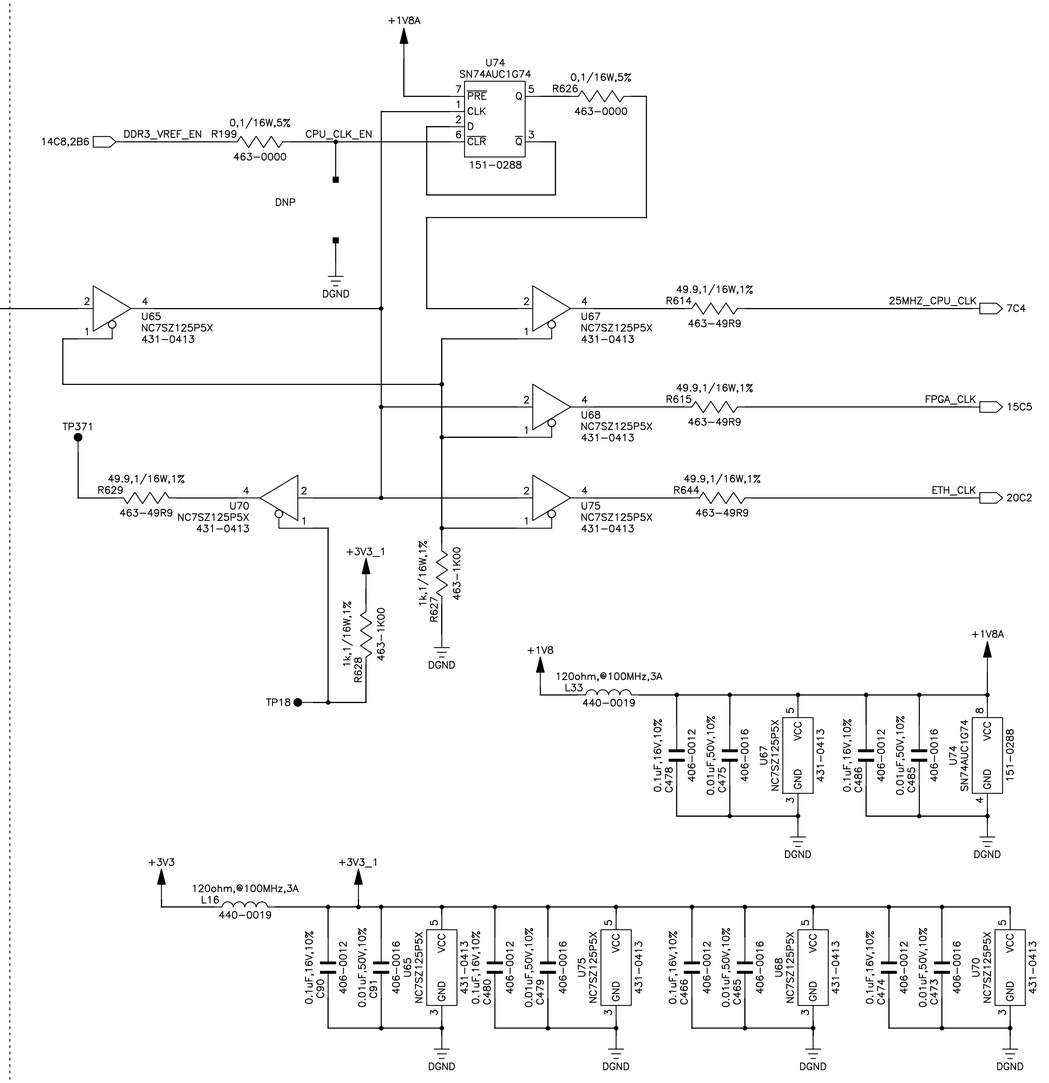


NOTES:
1. PLACE 0 Ohm RESISTORS SO AS TO REDUCE STUB LENGTHS TO JUNCTIONS. INSTALL BYPASS RESISTORS OR SS MOD

50MHz MAIN SYSTEM CLOCK



CLOCK BUFFER AND DIVIDER



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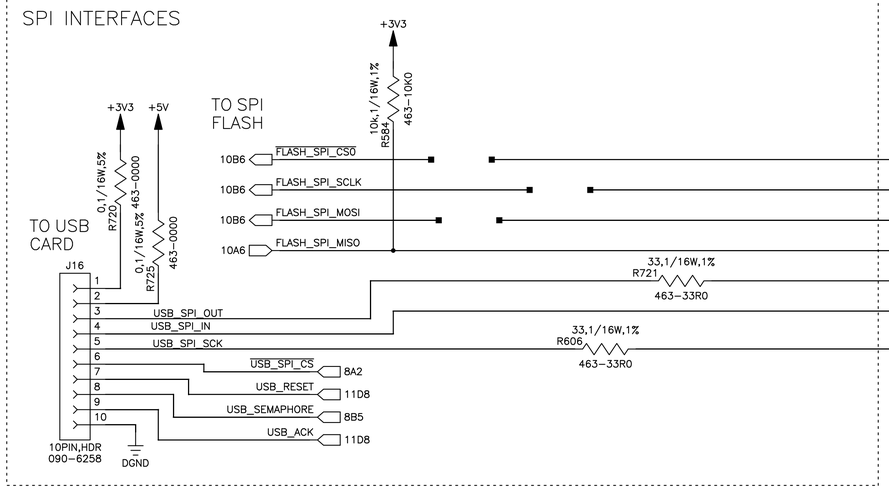
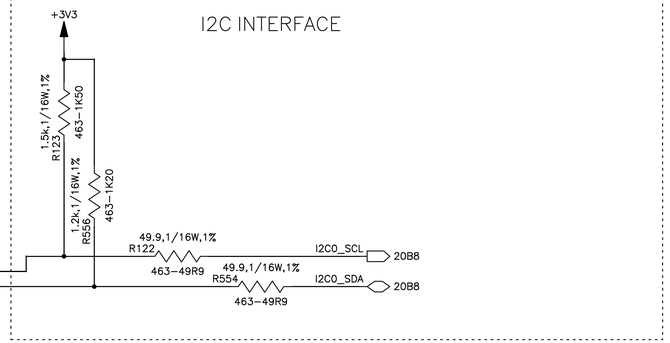
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. MAIN CLOCK/SPREAD SPECTRUM/CLOCK BUFFERS	SHEET 6 OF 30

AM355X (1 OF 6)
CPU SPI, I2C, JTAG, CLOCK, RESET

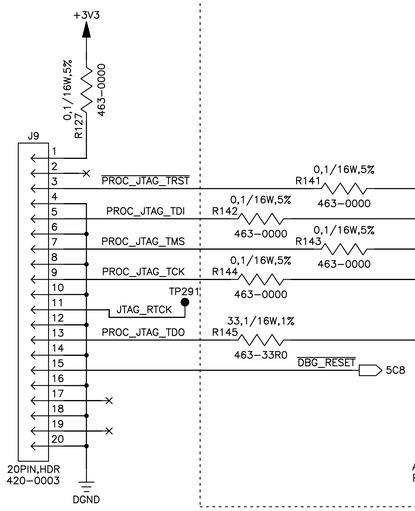
SPI INTERFACES



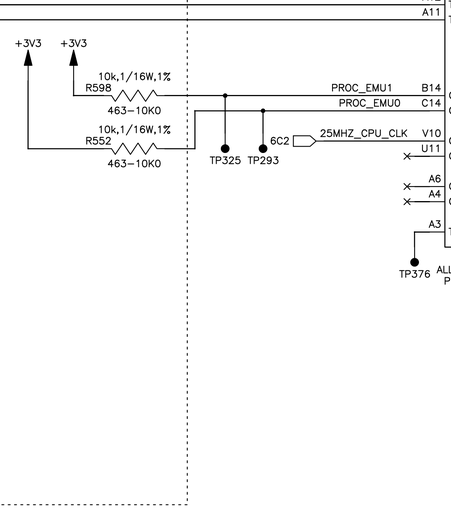
I2C INTERFACE

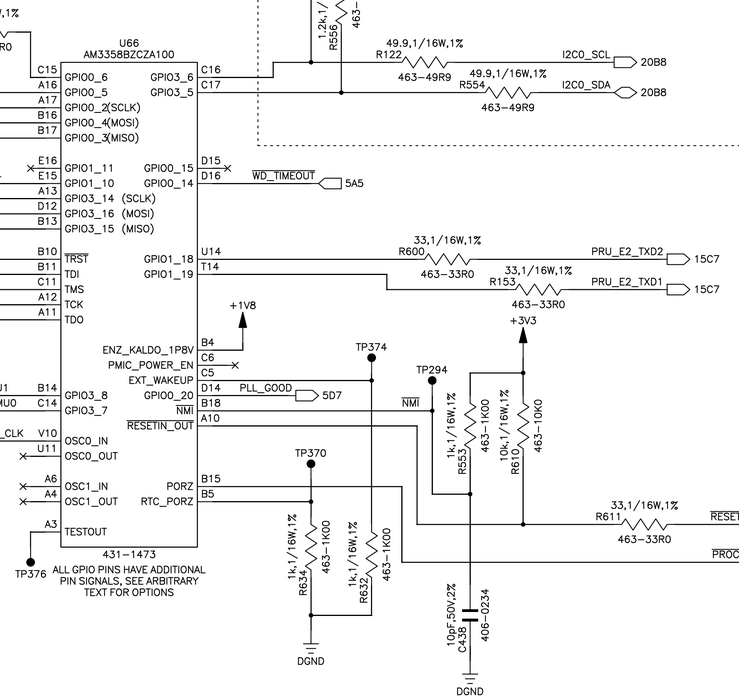


CPU JTAG HEADER
(NOT INSTALLED IN PRODUCTION)



CPU JTAG INTERFACE





I2C LOADING:
REFER TO
AM335X SILICON ERRATA
ADVISORY 1.0.26

ENZ_KALDO_1P8V CONNECTION:
REFER TO AM335X DATASHEET
PAGE 102
REFER TO AM335X TRM PAGE 1123

OSC1 CONNECTION:
REFER TO SILICON ERRATA 3.1.7 – HW LOG #4154

EMU[1:0] CONSTRAINT:
REFER TO SILICON ADVISORY 1.0.3 – HW LOG #4155
REFER TO SILICON ADVISORY 1.0.36 – HW LOG #4160

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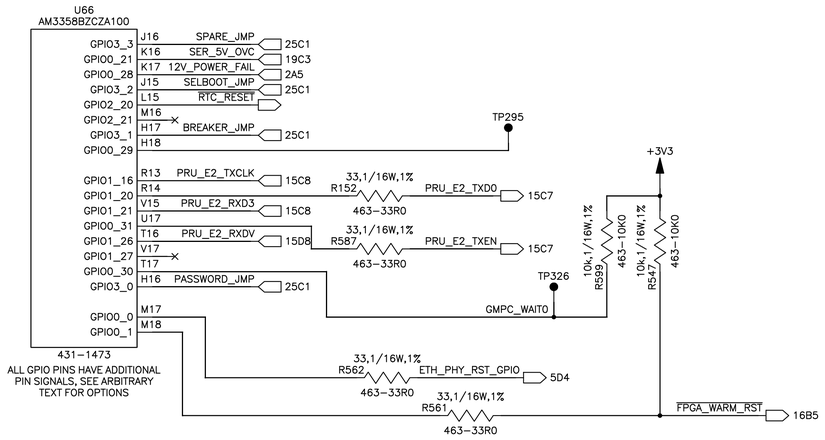
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 REV: B3
DESC. CPU SPI/USB CARD IF, I2C,JTAG, CLOCK, RESET	SHEET 7 OF 30

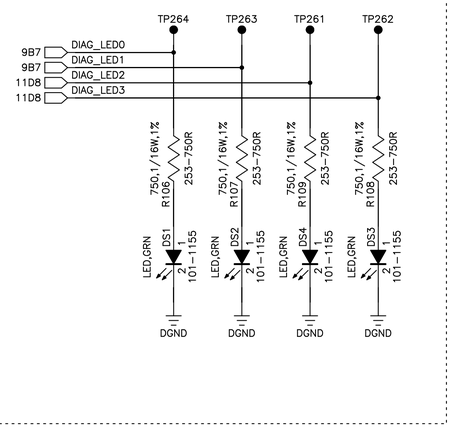
AM355X CONSORT (2 OF 6)

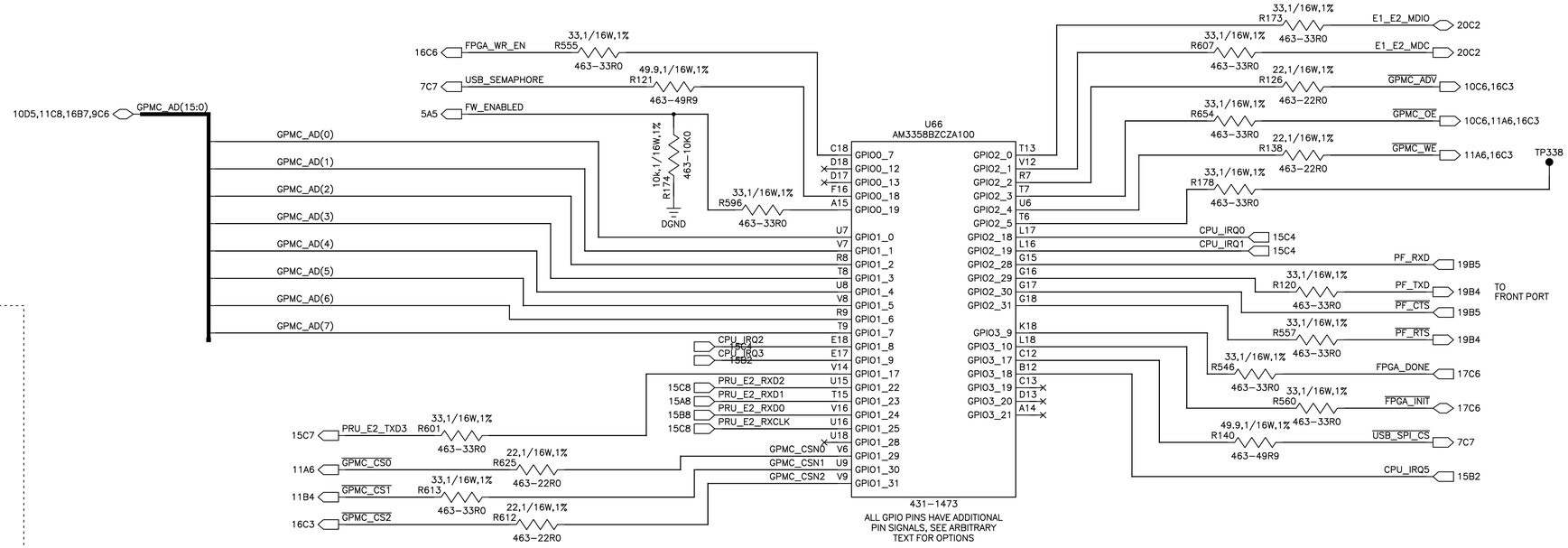
GPMC BUS, LEDS, ETH

HMI ETHERNET CONSORT



DIAGNOSTIC LEDS





GPMC CHIP SELECT ASSIGNMENTS:

GPMC_CS0_N – CONNECTED TO THE PARALLEL NOR FLASH. THIS WILL BE THE BOOT FLASH.

GPMC_CS1_N – CURRENTLY UNCONNECTED. FOR FUTURE USE WITH ADDITIONAL FLASH.

GPMC_CS2_N – CONNECTED TO THE FPGA. THIS IS THE MAIN COMMUNICATION BUS BETWEEN THE FPGA AND CPU.

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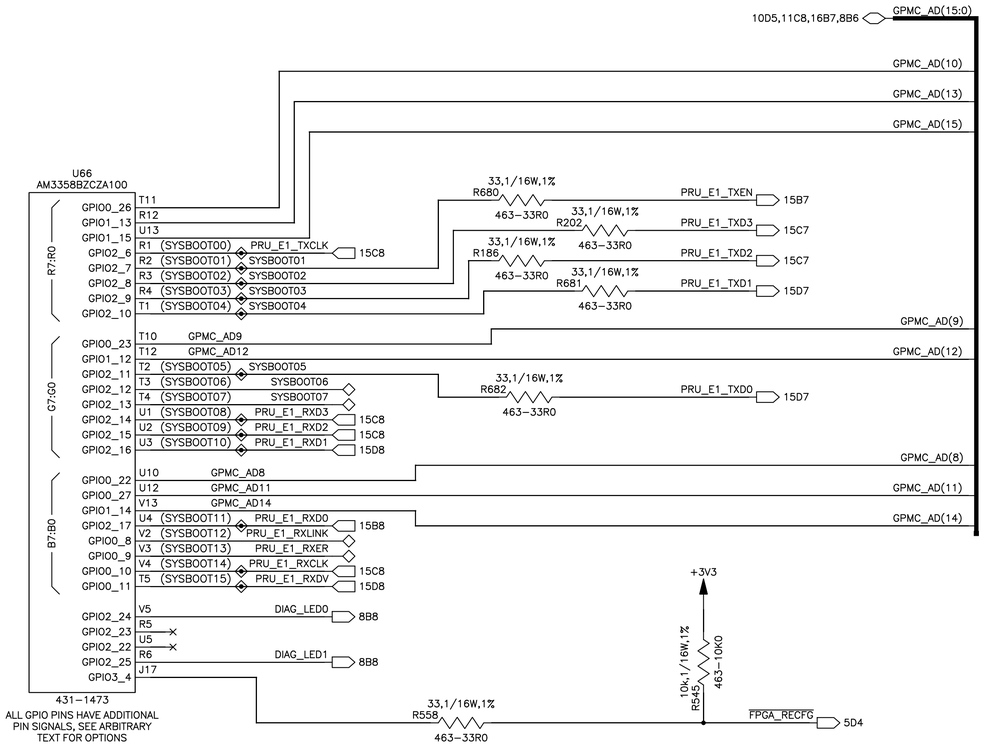
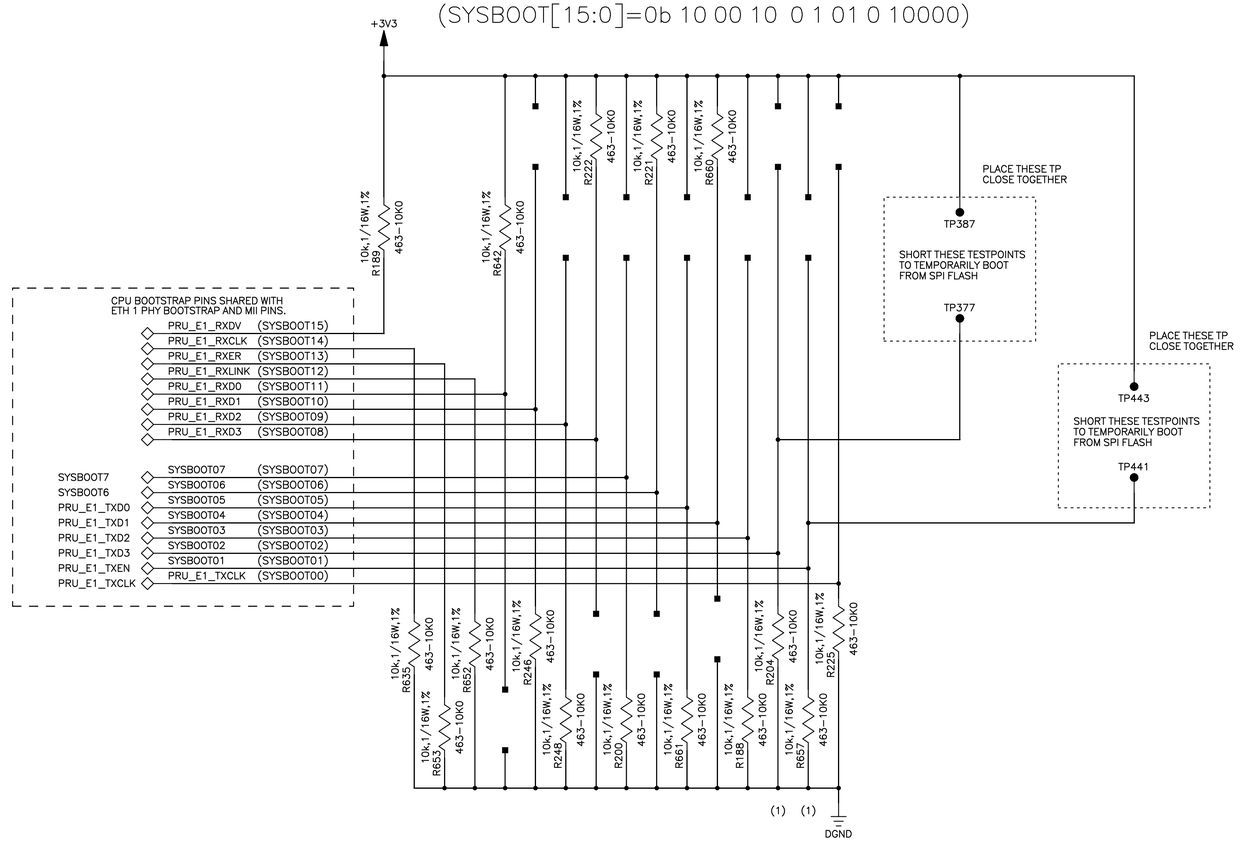
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 REV: B3
DESC. CPU: GPMC BUS, JUMPERS, DIAG. LEDS, ETH., CPU ADC	SHEET 8 OF 30

AM355X CONSORT (3 OF 6)
ETHERNET INTERFACE, AND CPU BOOT STRAPPING

GPMC, MEMORY AND ETHERNET INTERFACE



AM3358 BOOT STRAPPING
(SYSBOOT[15:0]=0b 10 00 10 0 1 01 0 10000)



PRIMARY BOOT CONFIGURATION 0b10 00 10 0 1 01 0 10000

25MHZ CLOCK, MUXED 16 BIT XIP, RMII BOOT PHY, CLKOUT1 DISABLED, BOOT FROM XIP

ETHERNET BOOT CONSTRAINTS:
REFER TO SILICON ADVISORY 1.0.25 – HW LOG #4158

REFER TO AM335X DATASHEET PAGE 48 NOTE (5)
REFER TO AM335X TRM SECTION 26.1.6.2.1

(1) CHANGE RESISTOR VALUES FOR ALTERNATE BOOT CONFIGURATION .

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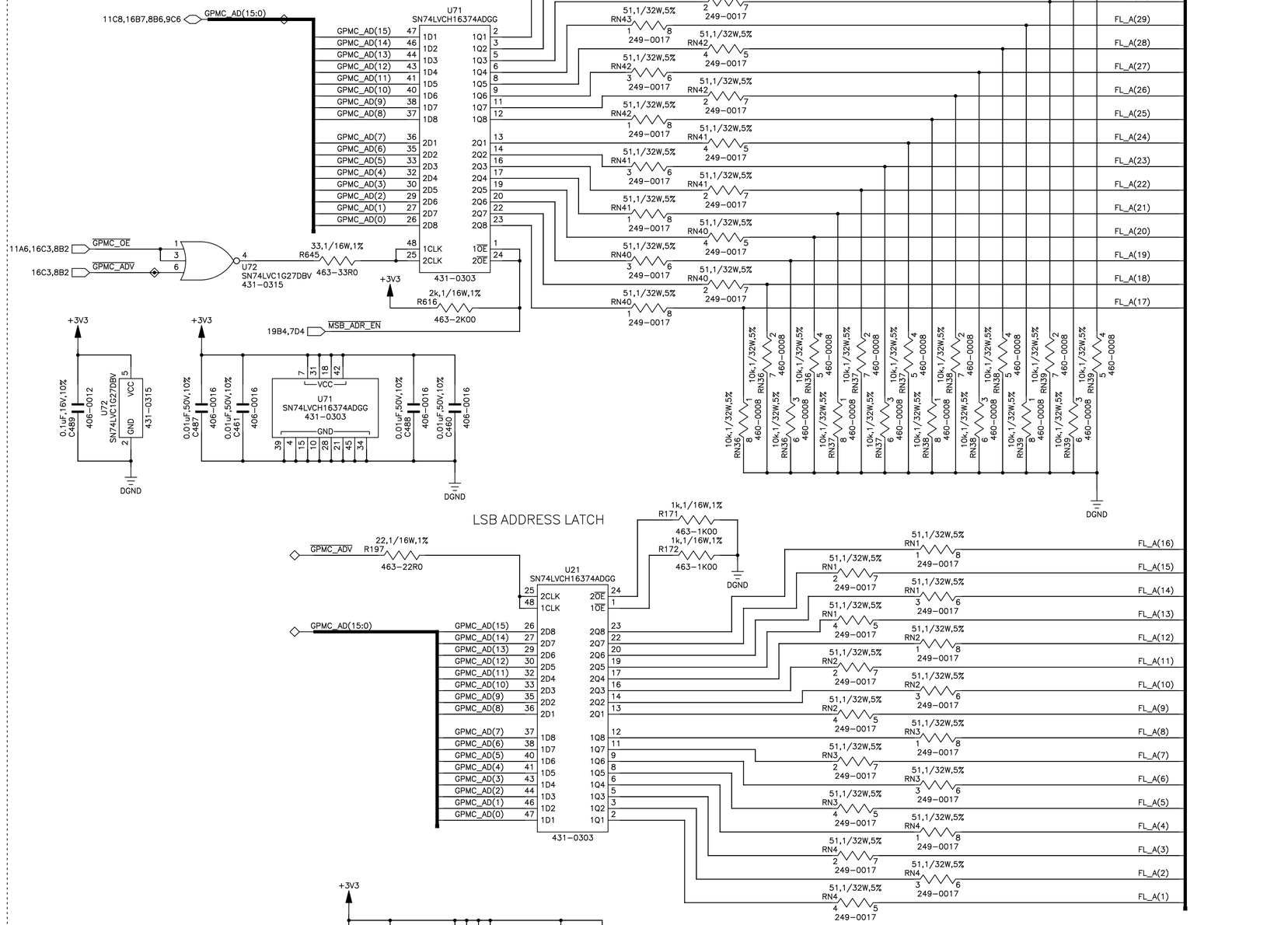
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 REV: B3
DESC. CPU: GPMC/ETHERNET INTERFACE, AND CPU BOOT STRAPPING	SHEET 9 OF 30

AM335X (4 OF 6)

SPI FLASH, NOR FLASH ADDRESS LATCHES

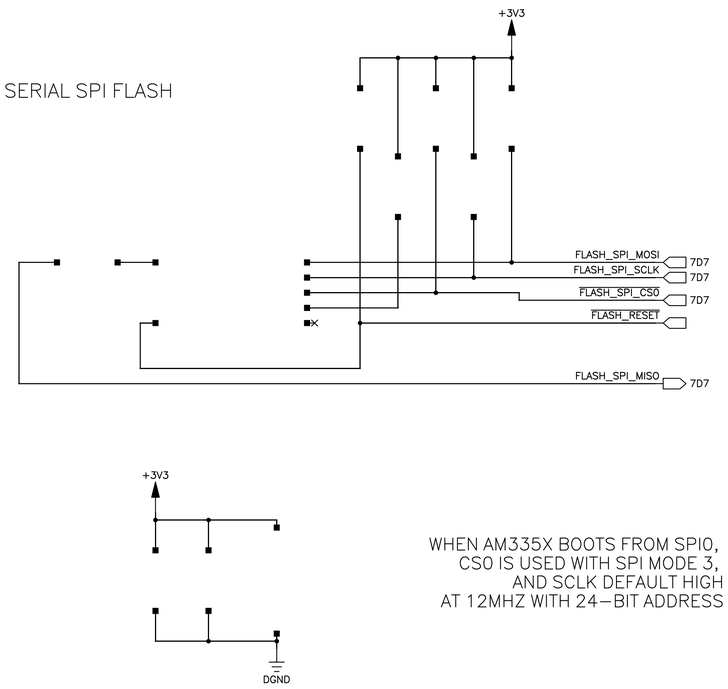
ADDRESS LATCHES

MSB ADDRESS LATCH



LSB ADDRESS LATCH

SERIAL SPI FLASH



WHEN AM335X BOOTS FROM SPI0,
CS0 IS USED WITH SPI MODE 3,
AND SCLK DEFAULT HIGH
AT 12MHZ WITH 24-BIT ADDRESS

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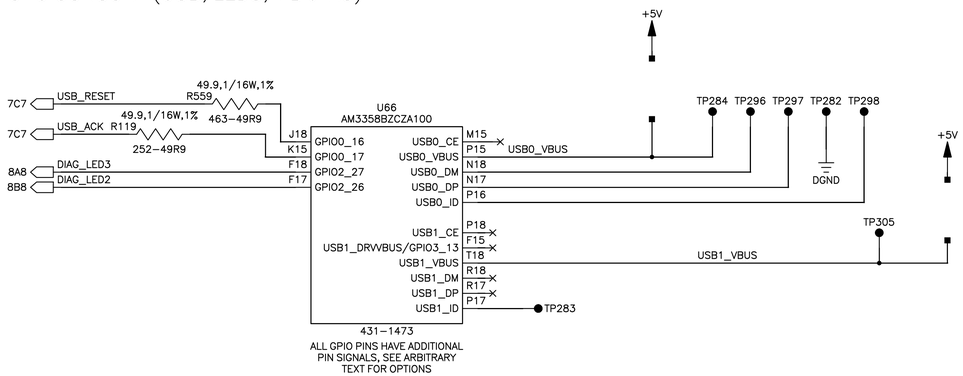
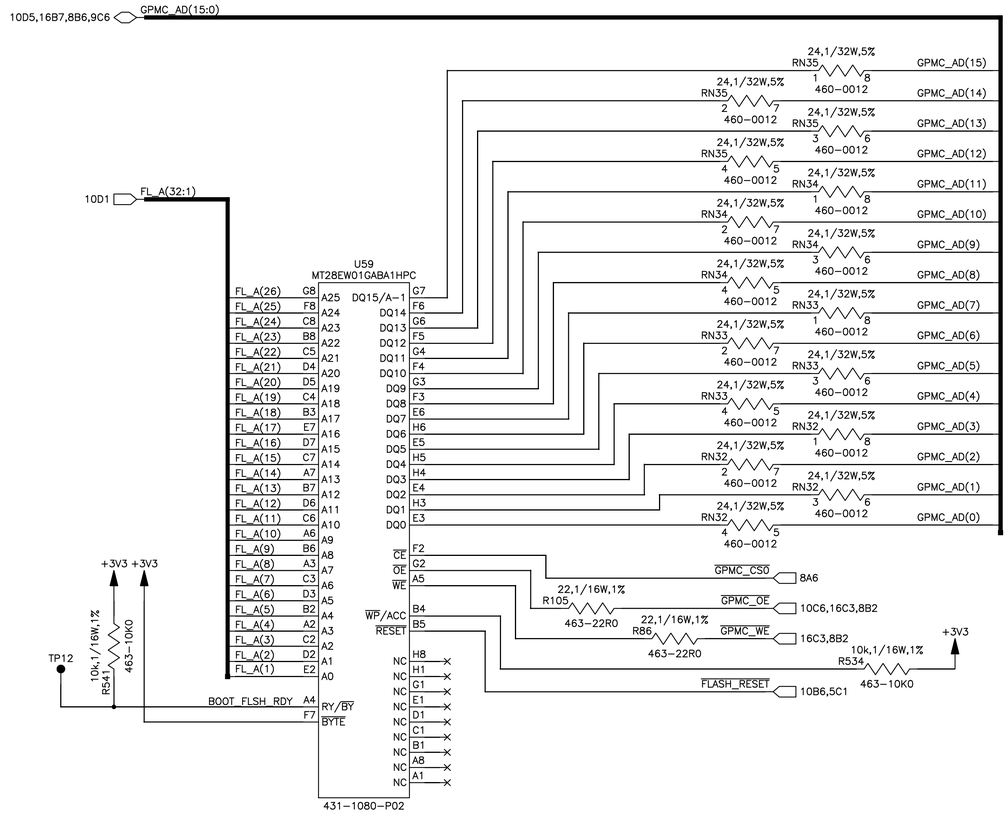
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 REV: B3
DESC. REAL TIME CLOCK, SPI FLASH, AND ADDRESS LATCHES	SHEET 10 OF 30

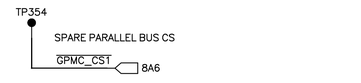
AM3556 CONSORT (5 OF 6)
USB PORTS, LEDS, MB JTAG, PARALLEL FLASH

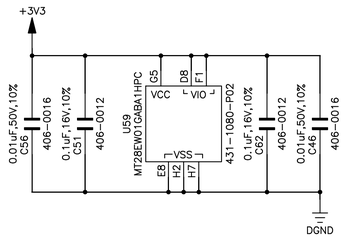
CPU CONSORT (USB, LEDS, MB JTAG)



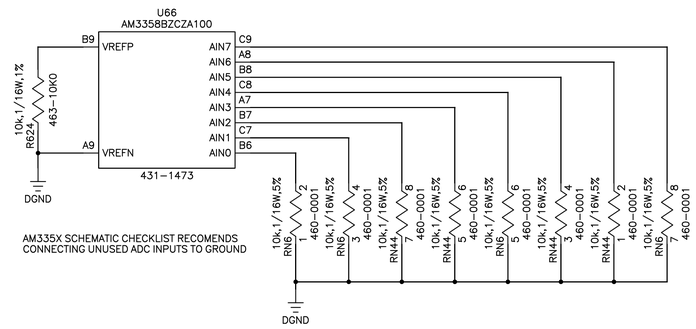
NOR FLASH







CPU ADC



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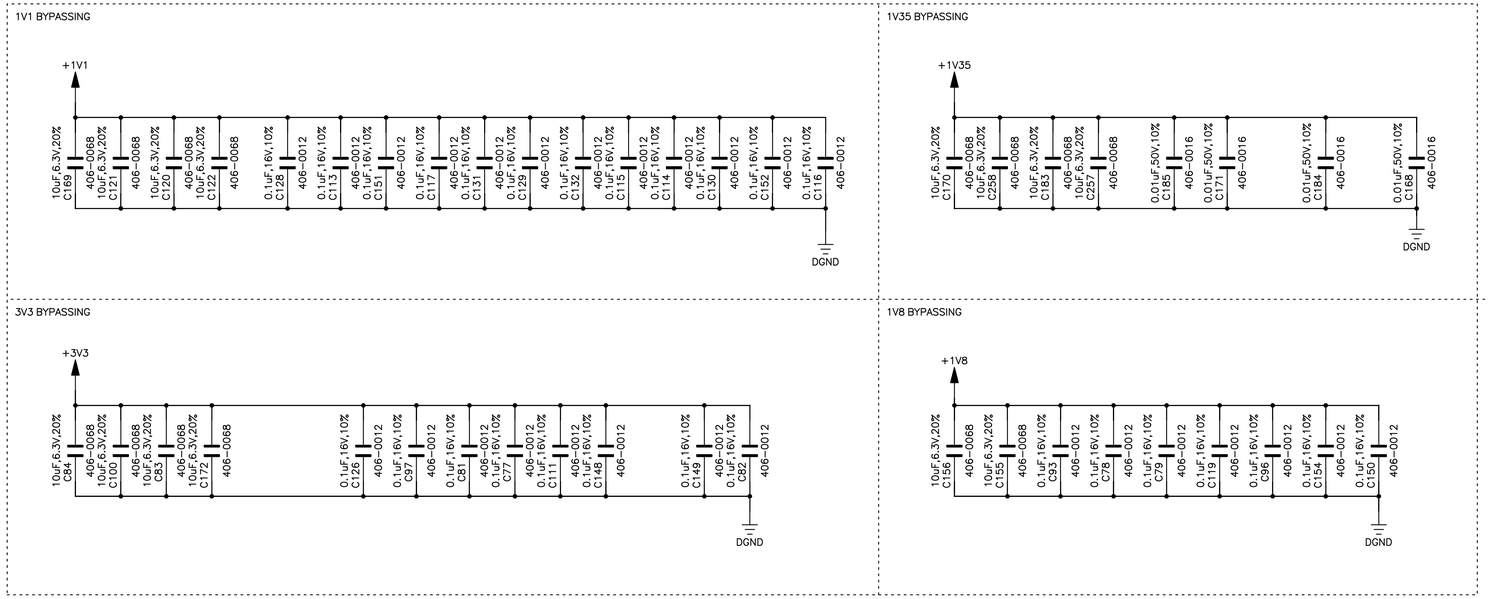
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. CPU: USB PORTS & PARALLEL FLASH	SHEET 11 OF 30

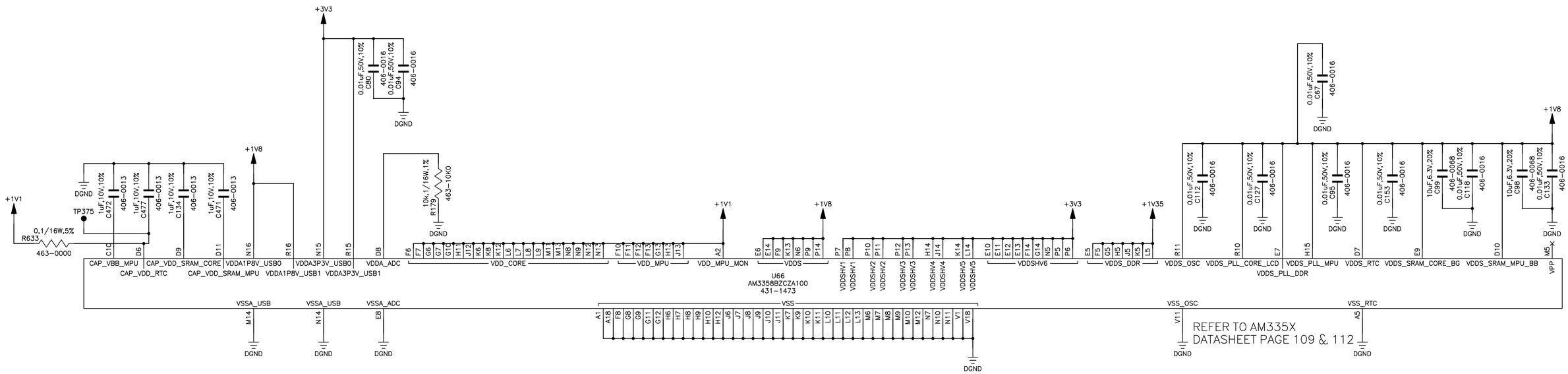
AM3556 CONSORT (6 OF 6)

AM3356 POWER, GROUND, BYPASSING, AND MOUNTING HOLES

CPU BYPASSING



AM335X POWER CONSORT



REFER TO AM335X DATASHEET PAGE 84, 93

VSS_OSC & VSS_RTC ROUTING:
REFER TO SILICON ADVISORY 1.0.30 – HW LOG #4159

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TITLE	6XX MB5 12V I/O
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01 / REV B3
DESC. CPU: AM3356 POWER, GROUND, BYPASSING, AND MOUNTING HOLES	SHEET 12 OF 30

DDR3L SDRAM (1 OF 2)
CPU DDR CONTROLLER & DDR DEVICE

+0V675

TP40

10uF,10V,10% C309
406-0011 0.1uF,16V,10% C279
406-0012 0.1uF,16V,10% C306
406-0012 0.1uF,16V,10% C288
406-0012 0.01uF,50V,10% C252
406-0016 0.01uF,50V,10% C308
406-0016 0.01uF,50V,10% C307
406-0016

DGND

PLACE CLOSE TO DDR

DRIVER=40 OHMS (RZQ/6), TRANSMISSION LINE=50, RECEIVER=60 OHMS (RZQ/4)
WRITE: CONTROLLER ODT=OFF, MEMORY ODT=60 OHMS
READ : CONTROLLER ODT=60 OHMS, MEMORY ODT=OFF

DDR_D(15:0)

U66
AM3358BZCZA100

DDR_D(15)	M1	DDR_D15	D3	DDR_A15
DDR_D(14)	L4	DDR_D14	H4	DDR_A14
DDR_D(13)	L3	DDR_D13	H3	DDR_A13
DDR_D(12)	K4	DDR_D12	E3	DDR_A12
DDR_D(11)	K3	DDR_D11	F2	DDR_A11
DDR_D(10)	K2	DDR_D10	F4	DDR_A10
DDR_D(9)	K1	DDR_D9	C1	DDR_A09
DDR_D(8)	J1	DDR_D8	D4	DDR_A08
DDR_D(7)	P4	DDR_D7	E2	DDR_A07
DDR_D(6)	P3	DDR_D6	D5	DDR_A06
DDR_D(5)	N4	DDR_D5	B1	DDR_A05
DDR_D(4)	N3	DDR_D4	C2	DDR_A04
DDR_D(3)	N2	DDR_D3	C3	DDR_A03
DDR_D(2)	N1	DDR_D2	E4	DDR_A02
DDR_D(1)	M4	DDR_D1	H1	DDR_A01
DDR_D(0)	M3	DDR_D0	F3	DDR_A00
DDR_DQM1	J2	DDR_DQM1	B3	DDR_BA2
DDR_DQM0	M2	DDR_DQM0	E1	DDR_BA1
			C4	DDR_BA0
			G1	DDR_ODT
DDR_DQS1	L1	DDR_DQS1	H2	DDR_CS0
DDR_DQS1 (100-OHM DIFF PAIR)	L2	DDR_DQS1	G4	DDR_RAS
DDR_DQS0	P1	DDR_DQS0	F1	DDR_CAS
DDR_DQS0 (100-OHM DIFF PAIR)	P2	DDR_DQS0	B2	DDR_WE
14C5,30C2 DDR3_VREF	J4	DDR_VREF	G3	DDR_CKE
	J3	DDR_VTP	D2	DDR_CK
DDR_RESET	G2	DDR_RESET	D1	DDR_CK (100-OHM DIFF PAIR)

431-1473

DDR_A15

U78
IS46TR16640CL-125JBLA25

T7	NC		
T3	NC		
N7	A12/BC		
R7	A11		
L7	A10/AP		
R3	A9		
T8	A8		
R2	A7		
R8	A6		
P2	A5		
P8	A4		
N2	A3		
P3	A2		
P7	A1		
N3	A0		
M3	BA2		
N8	BA1		
M2	BA0		
K1	ODT		
L2	CS		
J3	RAS		
K3	CAS		
L3	WE		
K9	CKE		
J7	CK		
K7	CK (100-OHM DIFF PAIR)		
L8	ZQ		
T2	RESET		
E7	LDM	A3	DDR_D(15)
D3	UDM	B8	DDR_D(14)
		A2	DDR_D(13)
		A7	DDR_D(12)
		C2	DDR_D(11)
		C8	DDR_D(10)
		C3	DDR_D(9)
		D7	DDR_D(8)
		H7	DDR_D(7)
		G2	DDR_D(6)
		H8	DDR_D(5)
		H3	DDR_D(4)
		F8	DDR_D(3)
		F2	DDR_D(2)
		F7	DDR_D(1)
		E3	DDR_D(0)

DDR_D(15:0)

Match length on all data and DQS lines.

LDQS	F3	DDR_DQS0
LDQS	G3 (100-OHM DIFF PAIR)	DDR_DQS0
UDQS	C7	DDR_DQS1
UDQS	B7 (100-OHM DIFF PAIR)	DDR_DQS1

Match length on clock, all address and all control lines

+1V35 +1V35

10K,1/16W,1% R700
463-10K0
0.01uF,50V,10% C202
406-0016
0.01uF,50V,10% C203
406-0016
49.9,1/16W,1% R705
463-49R9
IO BUFFERS CALIBRATION

TP34

DGND DGND

TP567

10K,1/16W,1% R205
463-10K0

DGND

+1V35

0.1uF,16V,10% C220
406-0012

39,1/32W,5% RN8 1 460-0015
39,1/32W,5% RN8 2 460-0015

PLACE CLOSE TO DDR

DDR_ZQ
DDR_RESET
DDR_DQM0
DDR_DQM1

TP28

240,1/16W,1% R272
463-240R

DGND

NC J1
NC J9
NC L1
NC L9
NC M7 DDR_A15

431-1222

39,1/32W,5% RN8 3 460-0015
39,1/32W,5% RN8 4 460-0015

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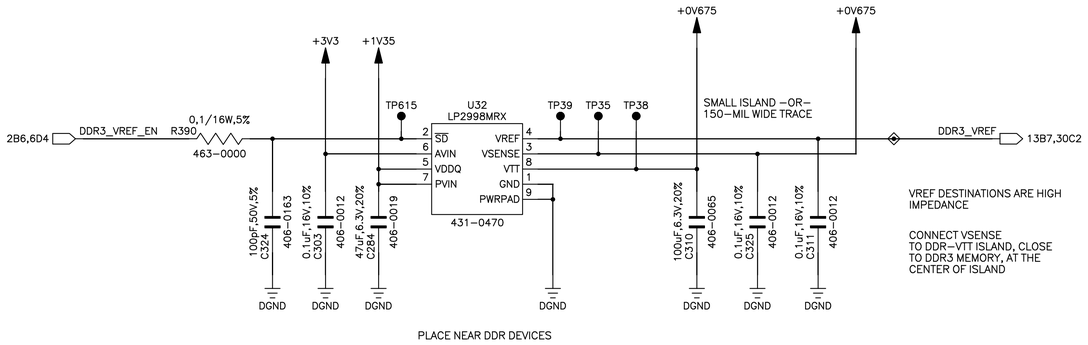
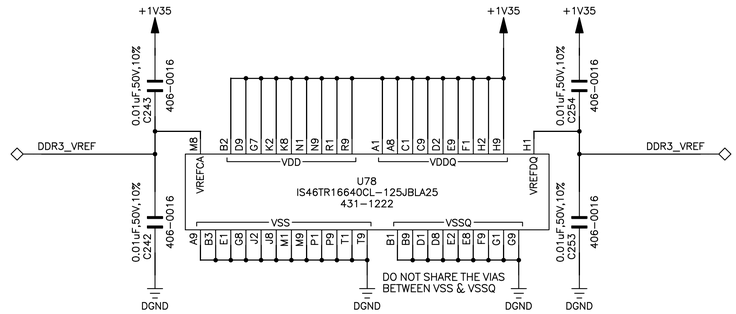
TITLE	6XX MB5 12V I/O				
BOM NUMBER	B2008-03-01	DRAWING NUMBER	S70-2008-03-01	REV	B3
DESC. DDR: CPU DDR CONTROLLER & DDR DEVICE				SHEET	13 OF 30

DDR3L SDRAM (2 OF 2)
DDR3 POWER–CONSORTS, 0V675 VREF POWER SUPPLY

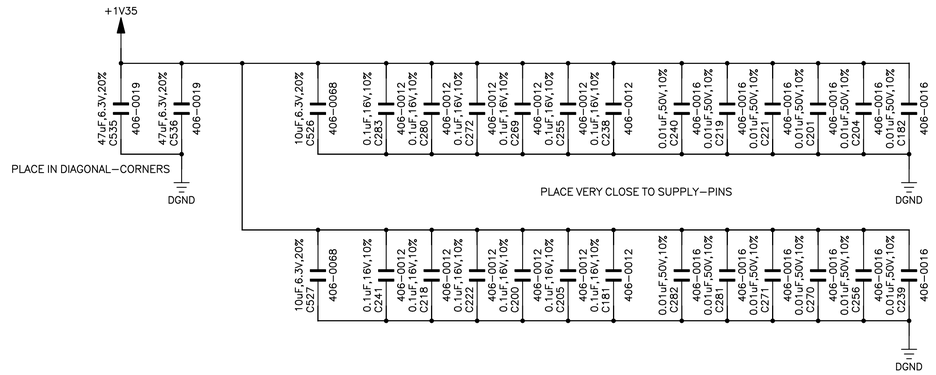
0V675–LV VTT & VREF POWER SUPPLY



DDR3L SDRAM POWER CONSORT



DDR3L BYPASSING



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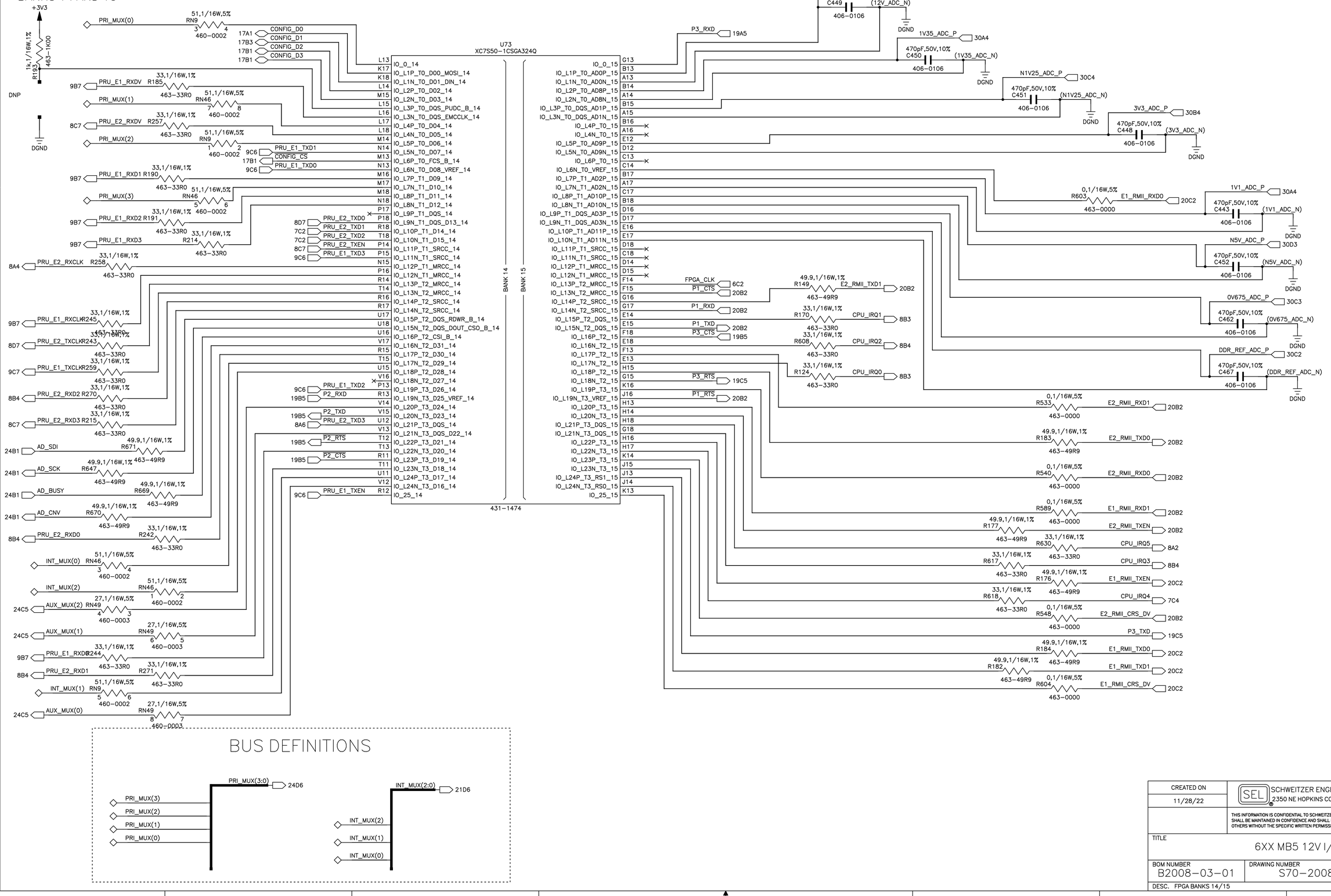
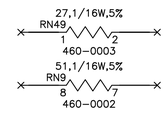
TITLE: 6XX MB5 12V I/O		
BOM NUMBER: B2008–03–01	DRAWING NUMBER: S70–2008–03–01	REV: B3
DESC. DDR: POWER CONSORTS, 0V675 VREF POWER SUPPLY		SHEET 14 OF 30

FPGA BANKS (1 OF 4)

BANKS 14 AND 15



BUS DEFINITIONS



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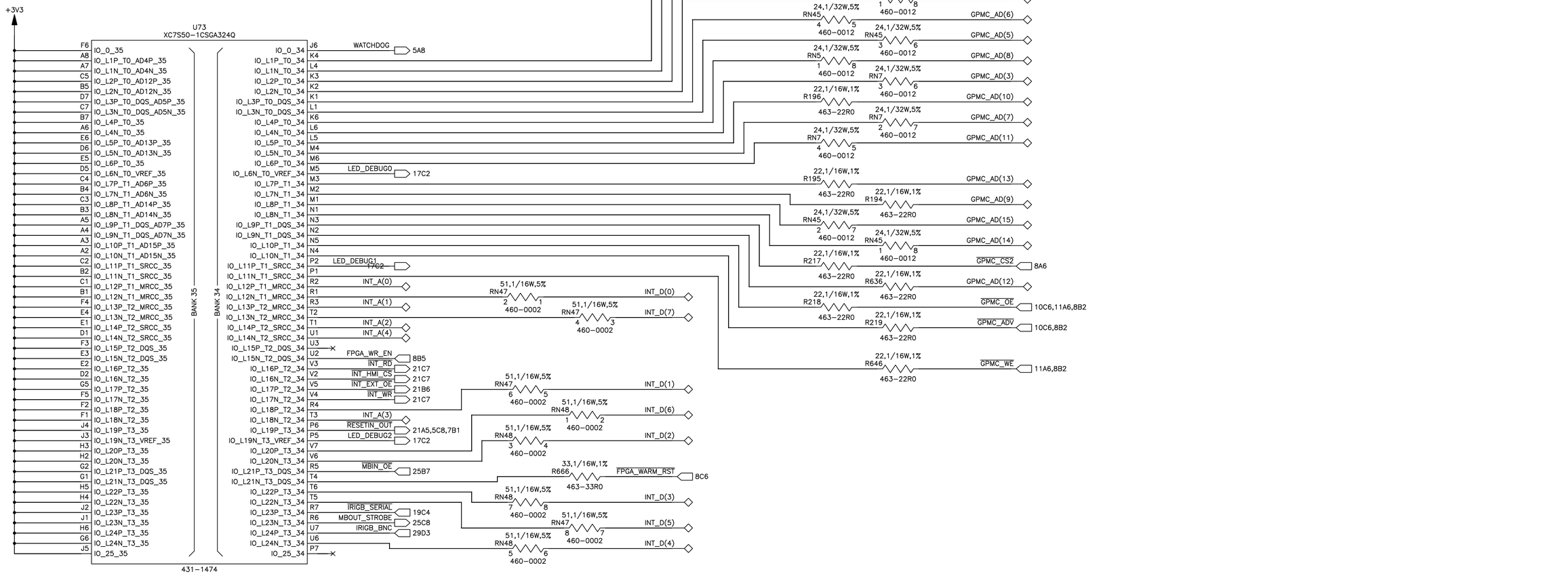
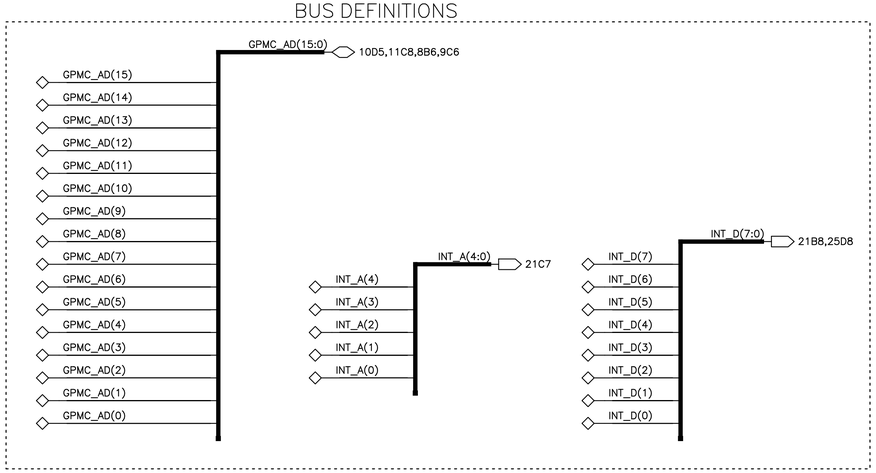
TITLE: 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. FPGA BANKS 14/15	SHEET 15 OF 30	

FPGA CONSORT (2 OF 4)
BANK 34 AND 35 CONNECTIONS



BUS DEFINITIONS



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TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 REV: B3
DESC. FPGA BANKS 34/35	SHEET 16 OF 30

FPGA CONSORT (3 OF 4)

BANK 0, BANK 16, JTAG, DEBUG HEADER, CONFIG FLASH

BANK 0, BANK 16, AND JTAG INTERFACE

U73
XC7S50-1CSGA324Q
431-1474

BANK 16: C10 IO_L11P_T1_SRCC_16, C9 IO_L11N_T1_SRCC_16, A10 IO_L12P_T1_MRCC_16, A9 IO_L12N_T1_MRCC_16, C12 IO_L13P_T2_MRCC_16, C11 IO_L13N_T2_MRCC_16, B11 IO_L14P_T2_SRCC_16, A11 IO_L14N_T2_SRCC_16, D11 IO_L6N_T0_VREF_16, D10 IO_L19N_T3_VREF_16

BANK 0: V9 CFGBVS_0, V8 DONE_0, L10 DXP_0, L9 DXN_0, U8 INIT_B_0, R8 PROGRAM_B_0, K10 VREFP_0, J9 VREFN_0, J10 VP_0, K9 VN_0, T10 M0_0, U10 M1_0, U9 M2_0, C8 CCLK_0, T9 TMS_0, D9 TCK_0, R9 TDI_0, T8 TDO_0

+3V3

DGND

FPGA_PROG

XADC_VREF

M0_0

10k,1/16W,1% R300 463-10K0
10k,1/16W,1% R297 463-10K0
10k,1/16W,1% R690 463-10K0
4.7k,1/16W,5% R667 463-4K70
330,1/10W,1% R668 462-330R

TP478 TP477 TP476 TP475
TP453 TP452 TP451 TP448

ALIGN JTAG AND GND TEST POINTS IN TWO ROWS TO SUPPORT MANUFACTURING TEST

FPGA_INIT 8B2
CONFIG_CLK 8B2
FPGA_DONE 8B2

0,1/16W,5% R216 463-0000 M0_0

FPGA CONFIG MODE SELECT
'001' = MASTER SPI
QUAD MODE

TP479
4.7k,1/16W,5% R683 463-4K70
5D1 FPGA_PROG

PULSE FPGA_PROGLOW FOR MIN 250NS TO TRIGGER RE-CONFIGURATION

10pF,50V,2% C501 406-0234

SPARTAN7 JTAG HEADER
(NOT INSTALLED IN PRODUCTION)

D49 SP3004-04 424-0023

TP569
0,1/16W,5% R329 463-0000

J11
S7_TMS 4 TMS
S7_TCK 6 TCK
S7_TDO 8 TDO
S7_TDI 10 TDI
14PIN,HDR 420-0009

49.9,1/16W,1% R298 463-49R9
49.9,1/16W,1% R689 463-49R9
49.9,1/16W,1% R688 463-49R9
49.9,1/16W,1% R299 463-49R9

10pF,50V,2% C285 406-0234
10pF,50V,2% C517 406-0234
10pF,50V,2% C516 406-0234
10pF,50V,2% C266 406-0234

FPGA DEBUG HEADER
(NOT INSTALLED IN PRODUCTION)

750,1/16W,1% R260 253-750R
750,1/16W,1% R261 253-750R
750,1/16W,1% R262 253-750R

LED,GRN DS5 2 1 101-1155
LED,GRN DS6 2 1 101-1155
LED,GRN DS7 2 1 101-1155

0.1uF,16V,10% C490 406-0012

16C6 LED_DEBUG0
16C6 LED_DEBUG1
16B6 LED_DEBUG2

49.9,1/16W,1% R665 463-49R9
49.9,1/16W,1% R664 463-49R9
49.9,1/16W,1% R663 463-49R9

J10
20PIN,HDR 420-0784

TP447

10pF,50V,2% C493 406-0234
10pF,50V,2% C492 406-0234
10pF,50V,2% C491 406-0234
10pF,50V,2% C217 406-0234

FPGA CONFIGURATION SPI FLASH

0.1uF,16V,10% C494 406-0012

U76
MX25L12835F
VCC GND
431-1475-P01

4.7k,1/16W,5% R675 463-4K70
4.7k,1/16W,5% R620 463-4K70
2.4k,1/16W,5% R623 463-2K40

TP456 TP342

U76
MX25L12835F
RESET/SIO3 7
WP/SIO2 3
CS 1
SCLK 6
SO/SIO1 2
SI/SIO0 5
431-1475-P01

CONFIG_D1 15D7
24.9,1/16W,1% R621 463-24R9

24.9,1/16W,1% R676 463-24R9 CONFIG_D3 15D7
24.9,1/16W,1% R619 463-24R9 CONFIG_D2 15D7
24.9,1/16W,1% R622 463-24R9 CONFIG_CS 15D7
24.9,1/16W,1% R674 463-24R9 CONFIG_CLK
24.9,1/16W,1% R672 463-24R9 CONFIG_D0 15D7

4.7k,1/16W,5% R673 463-4K70

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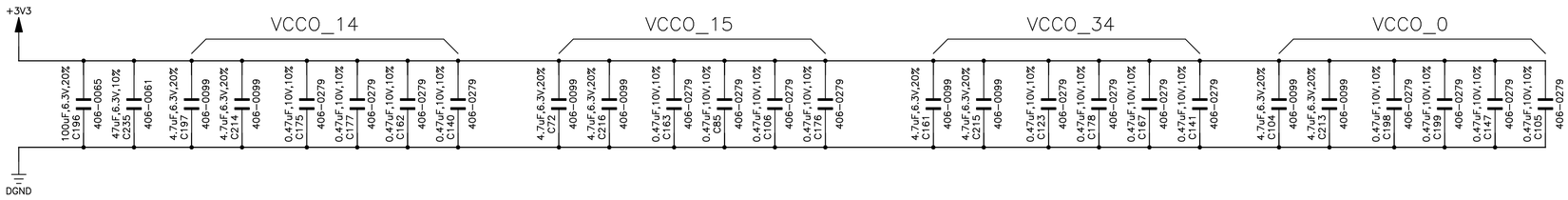
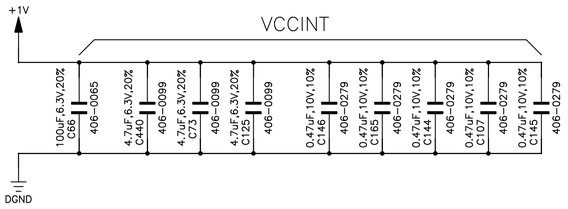
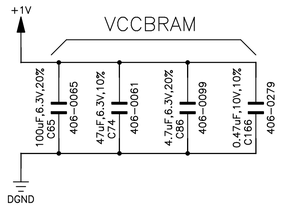
TITLE	6XX MB5 12V I/O
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01 REV B3
DESC. FPGA BANKS 16/0, JTAG,DEBUG HEADER, CONFIG FLASH	SHEET 17 OF 30

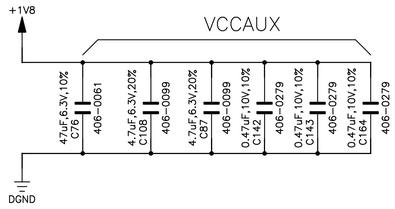
FPGA CONSORT (4 OF 4)
POWER CONNECTIONS

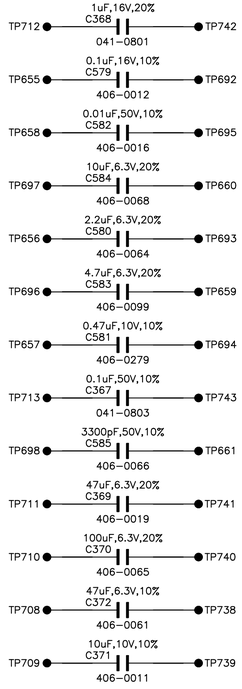
BYPASS CAPACITORS FOR I/O BANKS



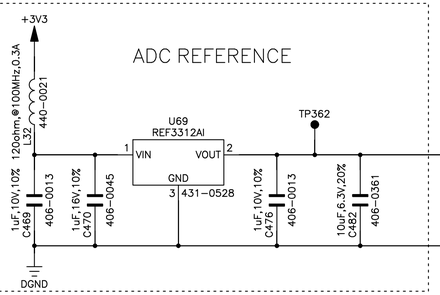








ADC REFERENCE



SPARTAN 7 FPGA POWER CONSORT

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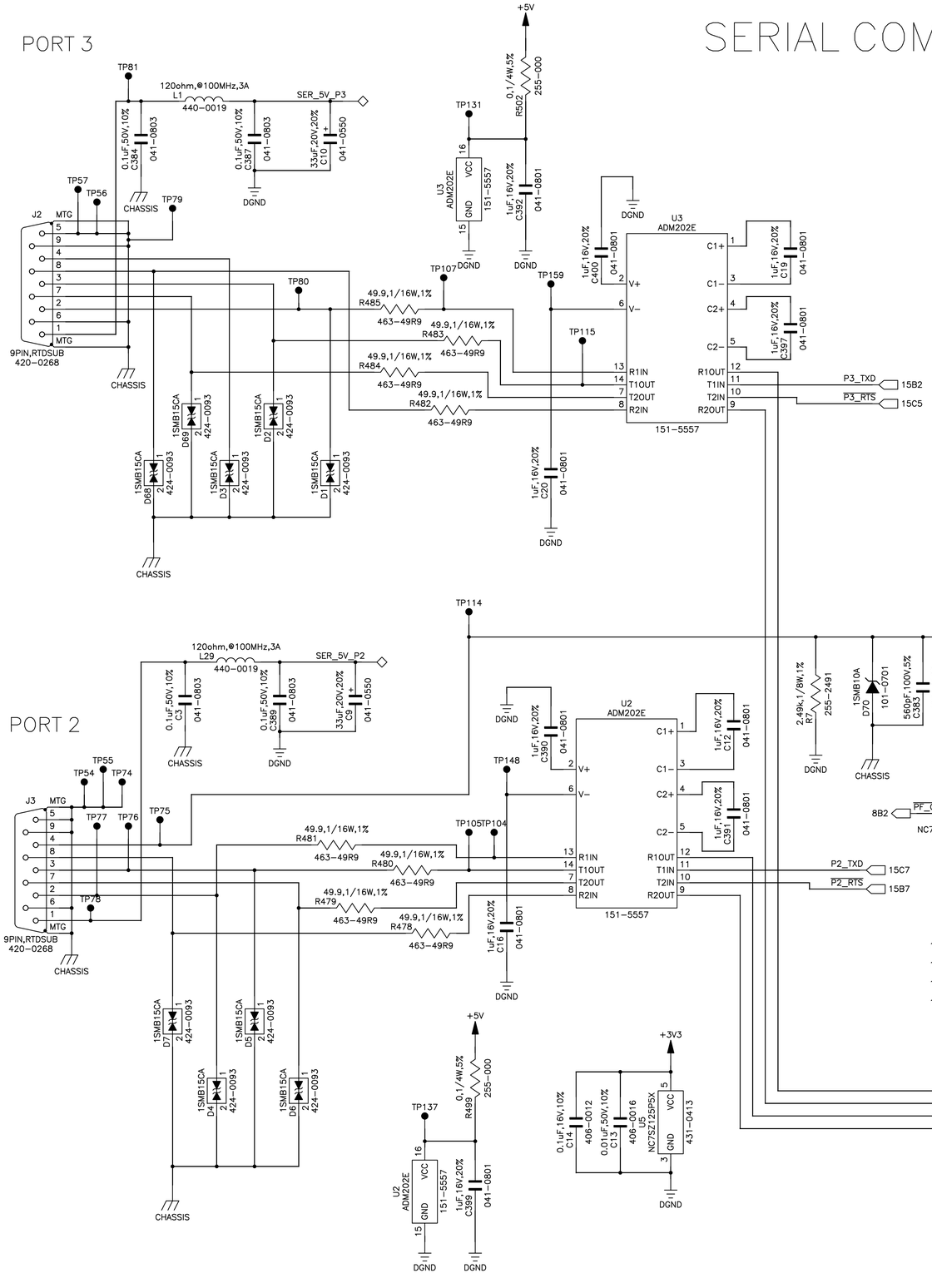
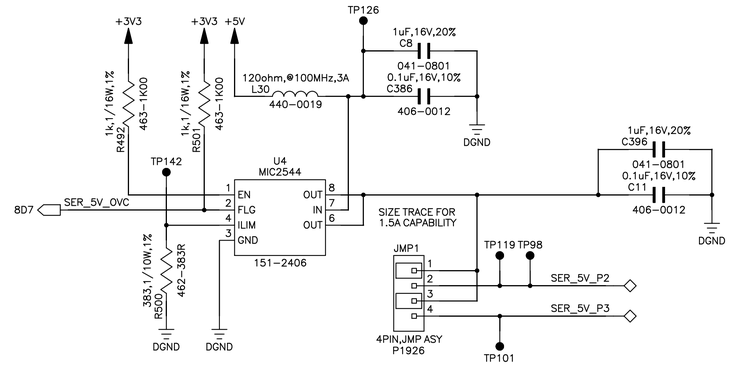
TITLE: 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. FPGA: SPARTAN 7 POWER CONNECTIONS		SHEET 18 OF 30

SERIAL COMMUNICATIONS

PORT 3

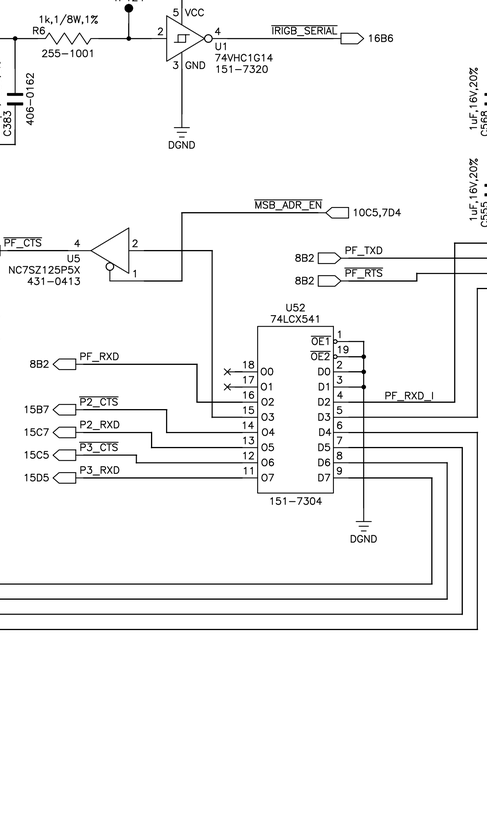


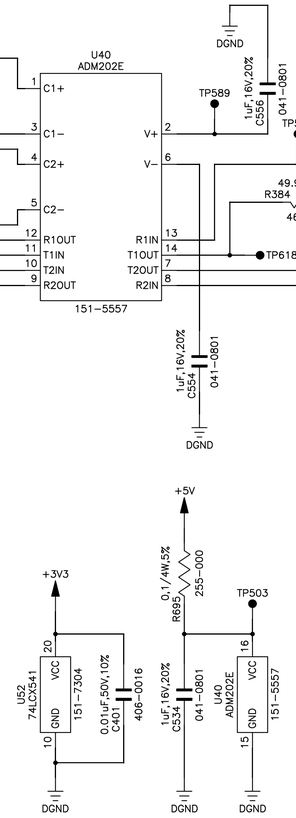
SERIAL PORT CURRENT LIMITER



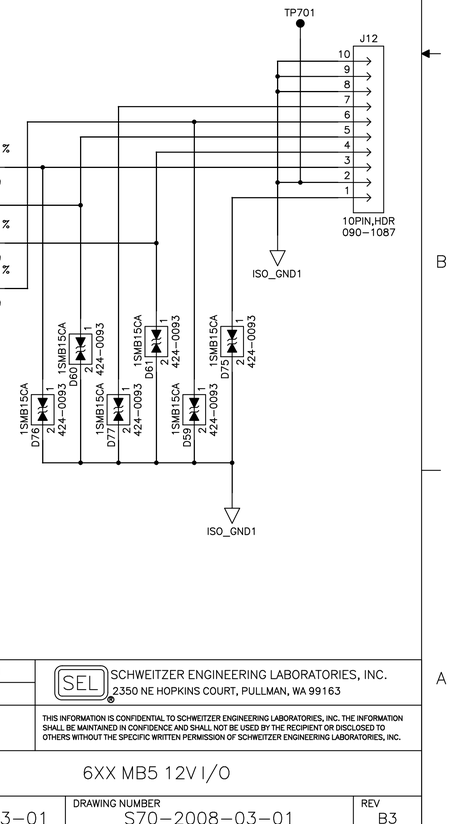
LIMIT SET BY R-VALUE ON ILIM PIN.
383OHMS = 600MA

PORT 2





PORT F



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BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01 — REV B3
DESC. RS232/DB9 CURRENT LIMITER	SHEET 19 OF 30

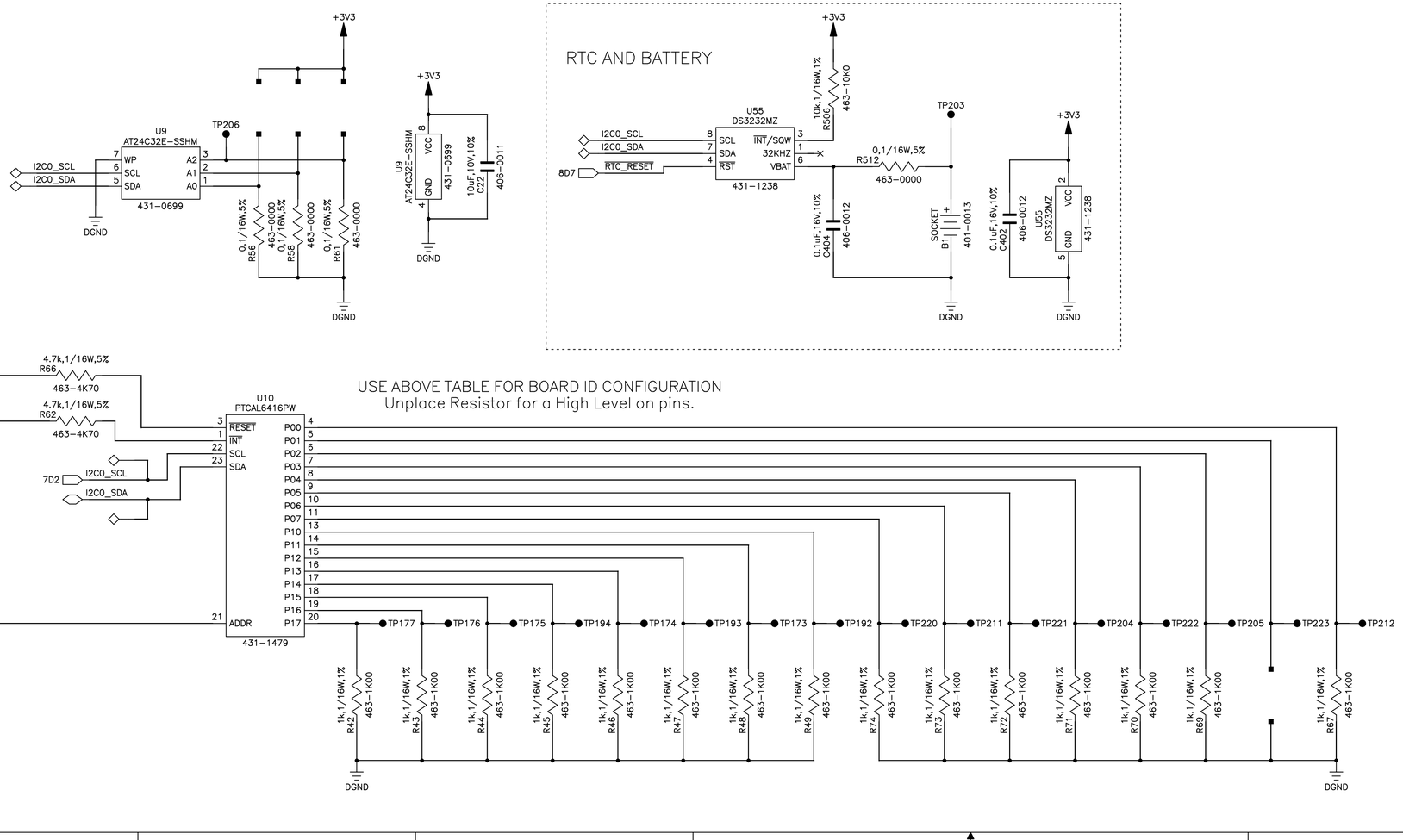
BOARD ID CONFIGURATION

P15:P4	DESCRIPTION	P3:P0	DESCRIPTION
0x000	Processor: Sitara AM3358 FPGA: Spartan 7 XC7S50	0x8	BINARY INPUTS (2) 220V (5) 12V
0x001	Processor: Sitara AM3356 FPGA: Spartan 7 XC7S50	0x6	BINARY INPUTS (2) 125V (5) 12 V
0x002	Processor: Sitara AM3358 FPGA: Spartan 7 XC7S25	0x4	BINARY INPUTS (2) 48V (5) 12 V
0x003	Processor: Sitara AM3356 FPGA: Spartan 7 XC7S25	0x2	BINARY INPUTS 12V
0x0004 – 0xFFF	Reserved	0x0	BINARY INPUTS None

I2C ADDRESS CONFIGURATION TABLE

DEVICE TYPE	I2C ADDRESS [A7:A0]
Mainboard HW Configuration	0x40h
Comm Daughter Card HW Configuration	0x42h
MB EEPROM	0xA0h
MB RTC	0xD0h

USE ABOVE TABLE FOR BOARD ID CONFIGURATION
Unplace Resistor for a High Level on pins.



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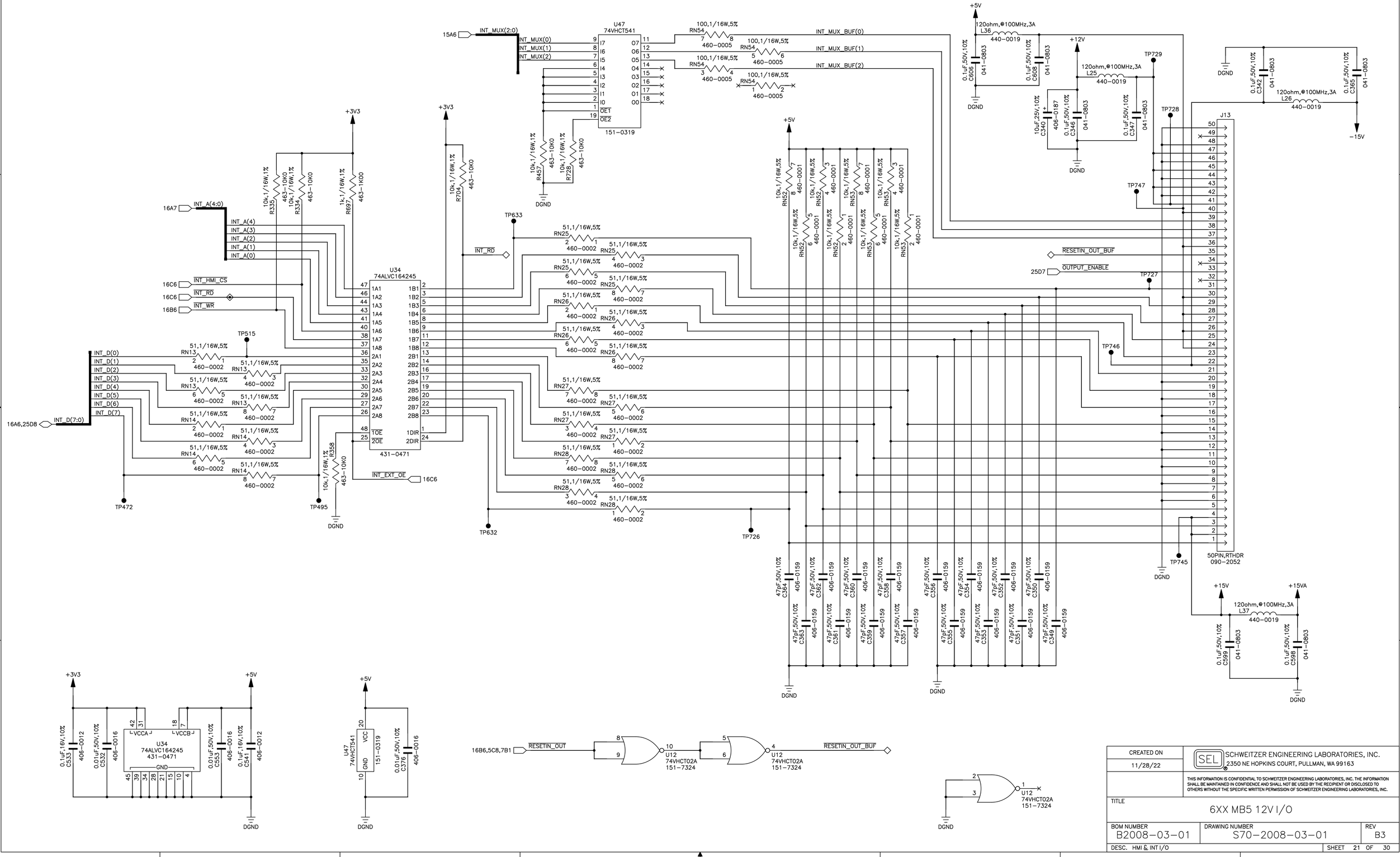
TITLE	6XX MB5 12V I/O
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. I2C, MB HW CONFIG, COMM BOARD INTERFACE	SHEET 20 OF 30



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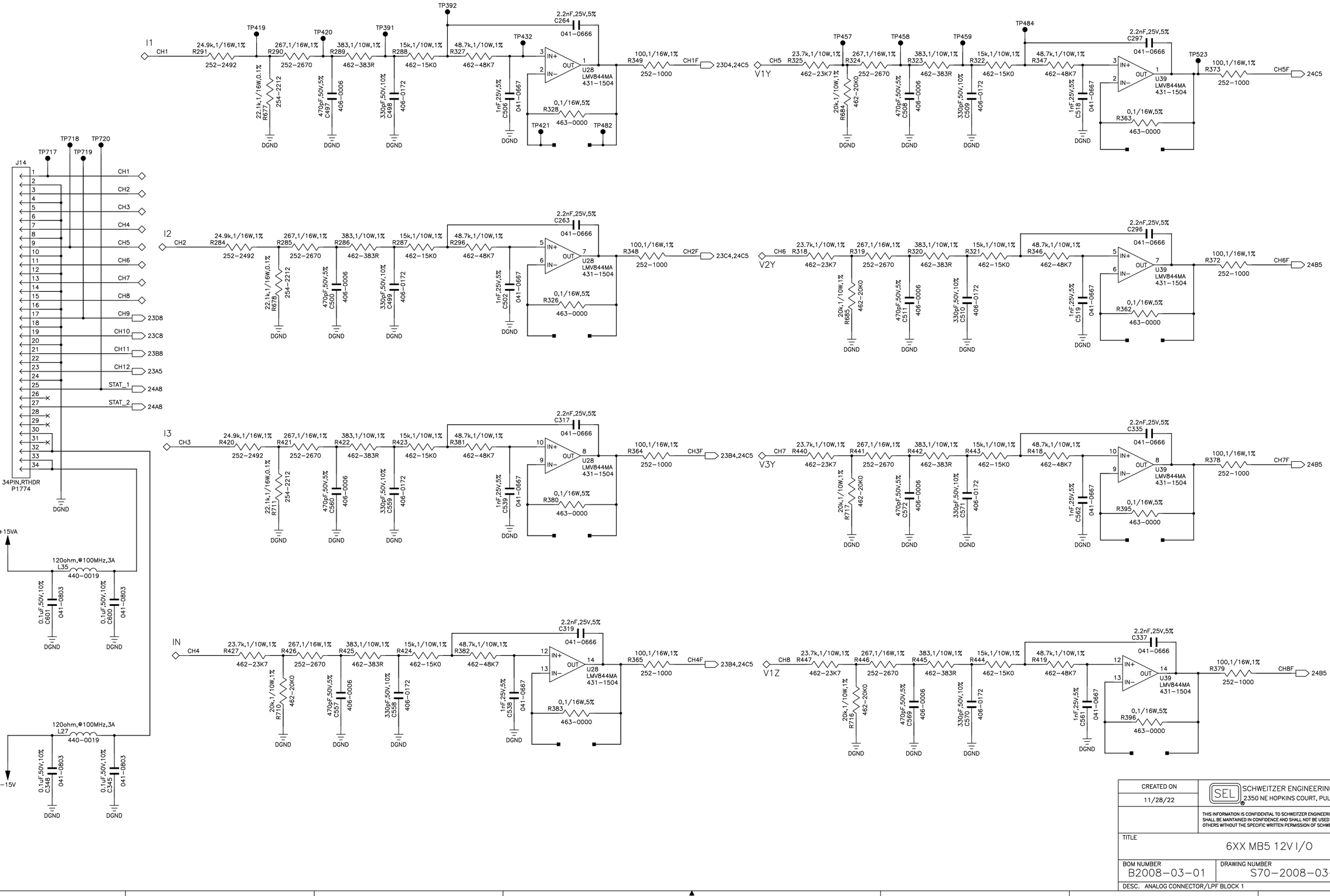
TITLE	6XX MB5 12V I/O	
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. HMI & INT I/O	SHEET 21 OF 30	



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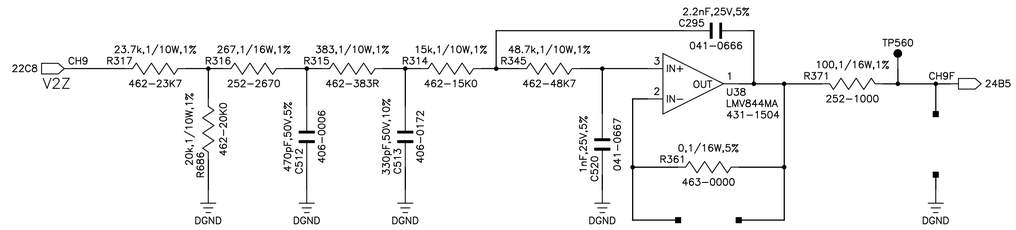
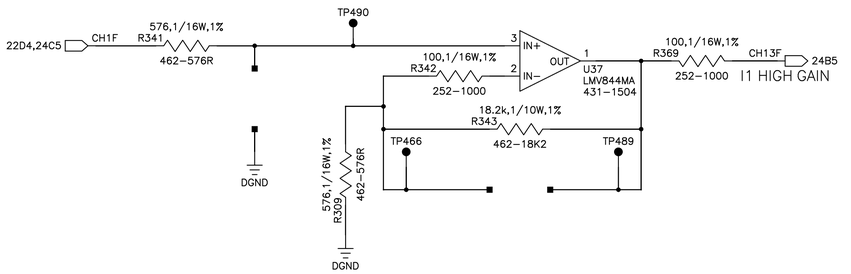
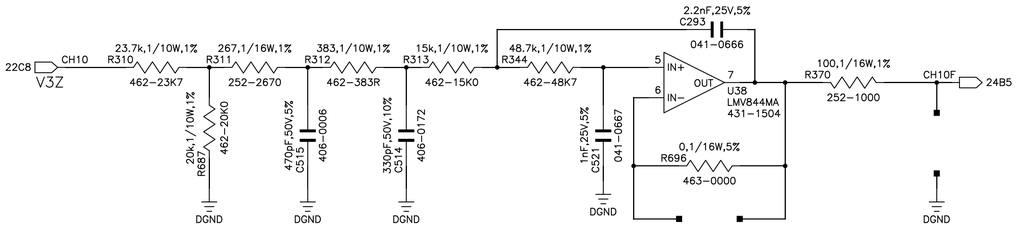
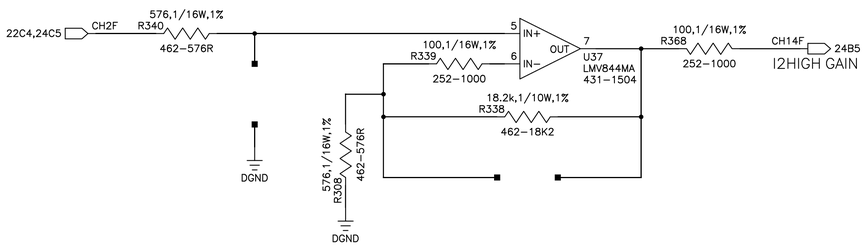
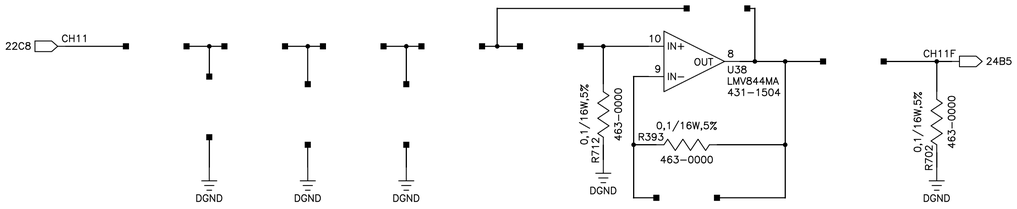
TITLE	6XX MB5 12V I/O
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01 REV B3
DESC. ANALOG CONNECTOR/LPF BLOCK 1	SHEET 22 OF 30

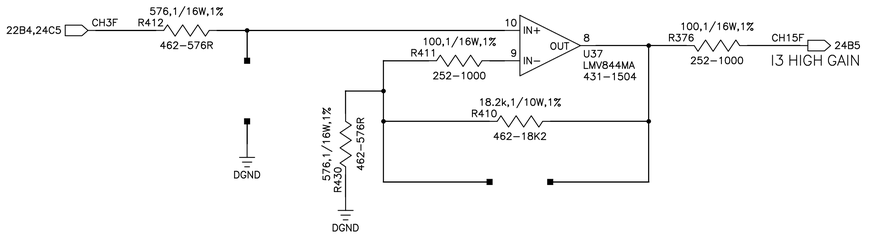


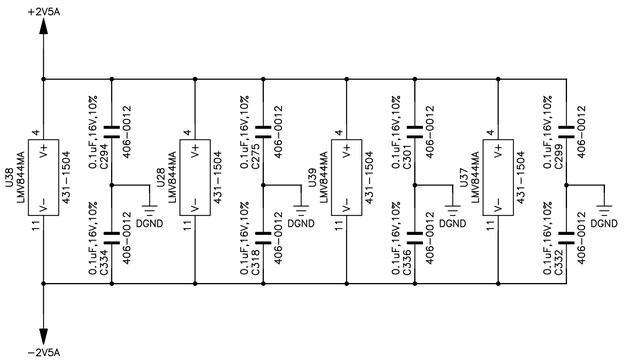


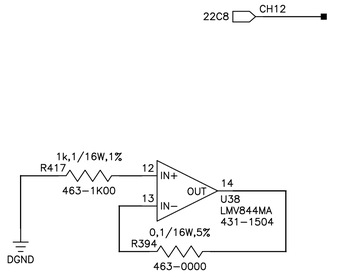


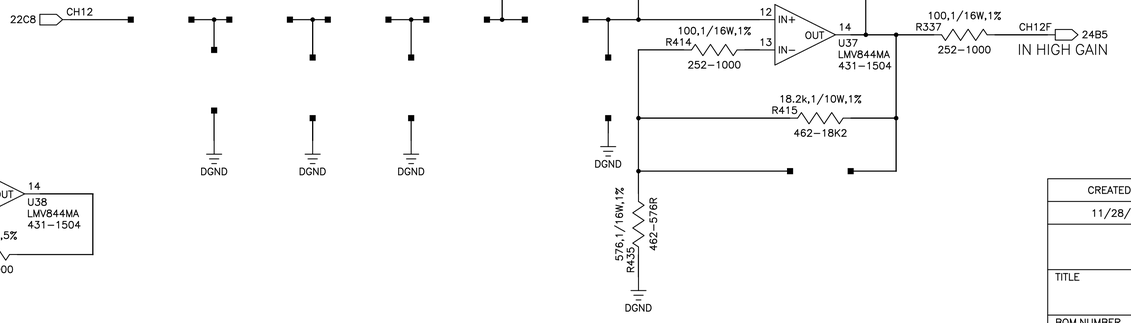












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TITLE 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. LPF BLOCK 2/HIGH GAIN	SHEET 23 OF 30	

−2V5 LDO SUPPLY

−5V SWITCHED CAP SUPPLY

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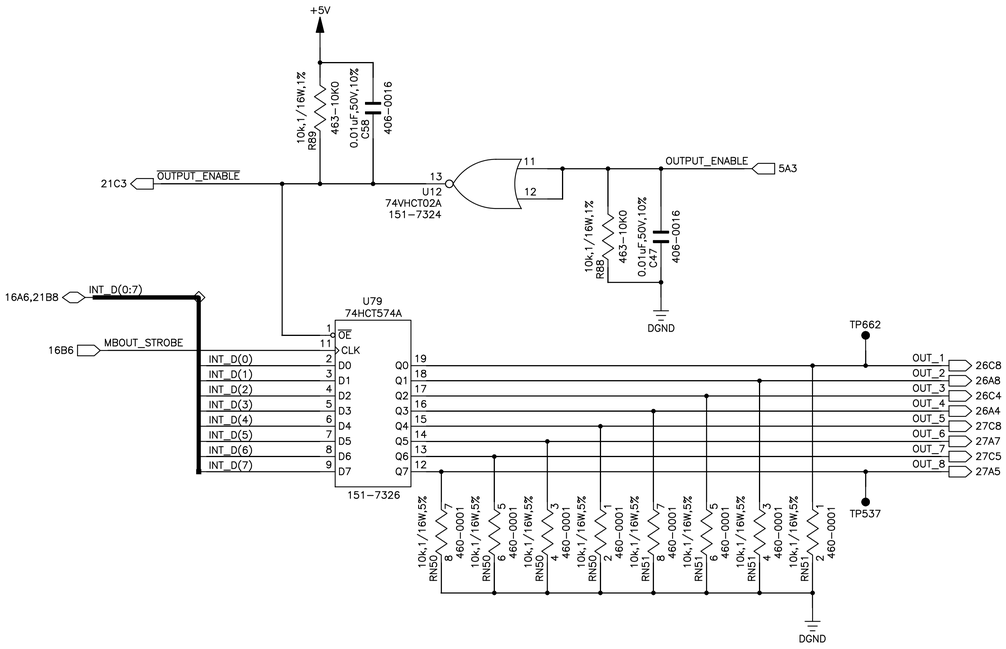
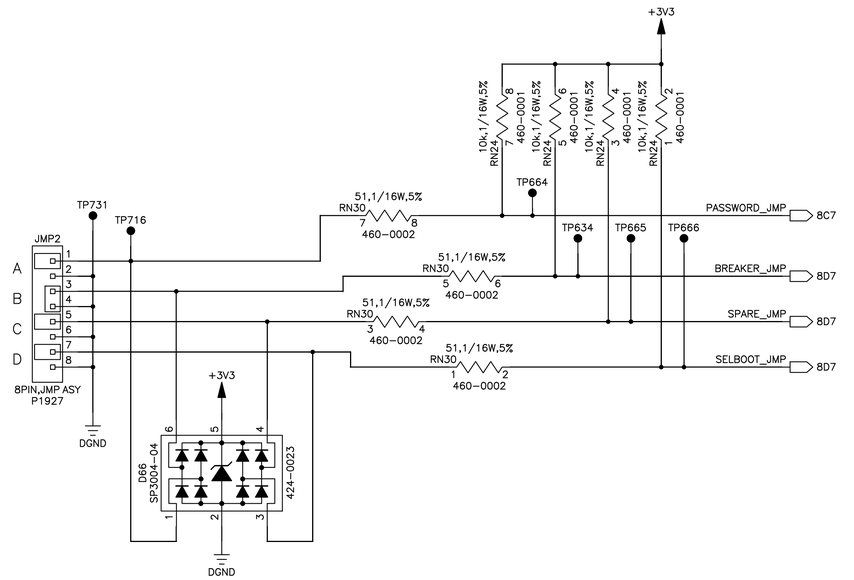
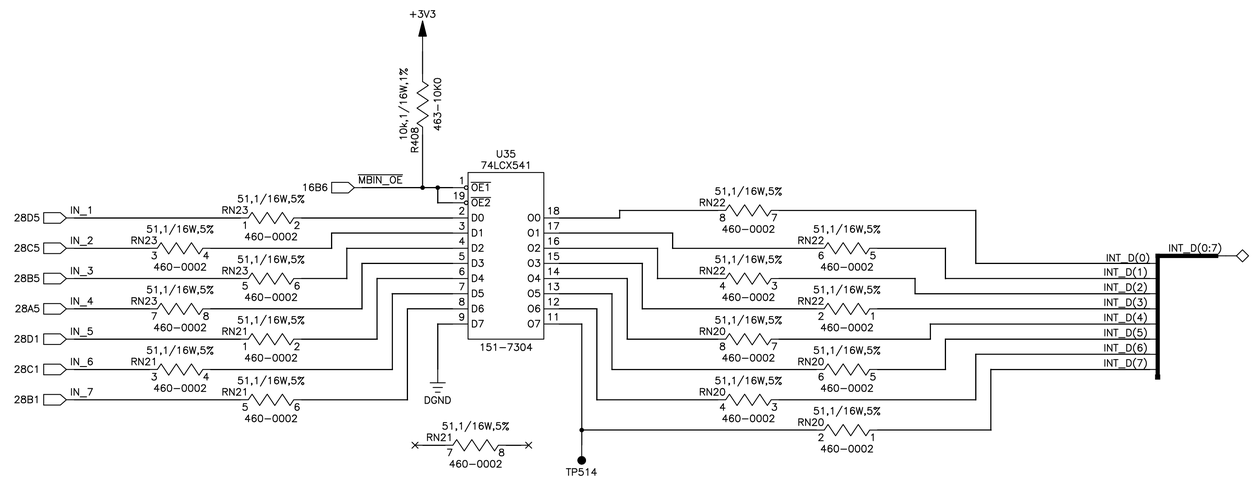
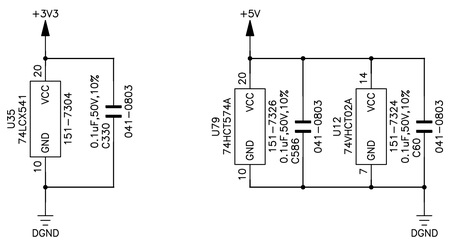
TITLE	6XX MB5 12V I/O	
BOM NUMBER B2008−03−01	DRAWING NUMBER S70−2008−03−01	REV B3
DESC. AD/MUX/DIAG/TEMP/−5V/−2V5 RAILS	SHEET 24 OF 30	









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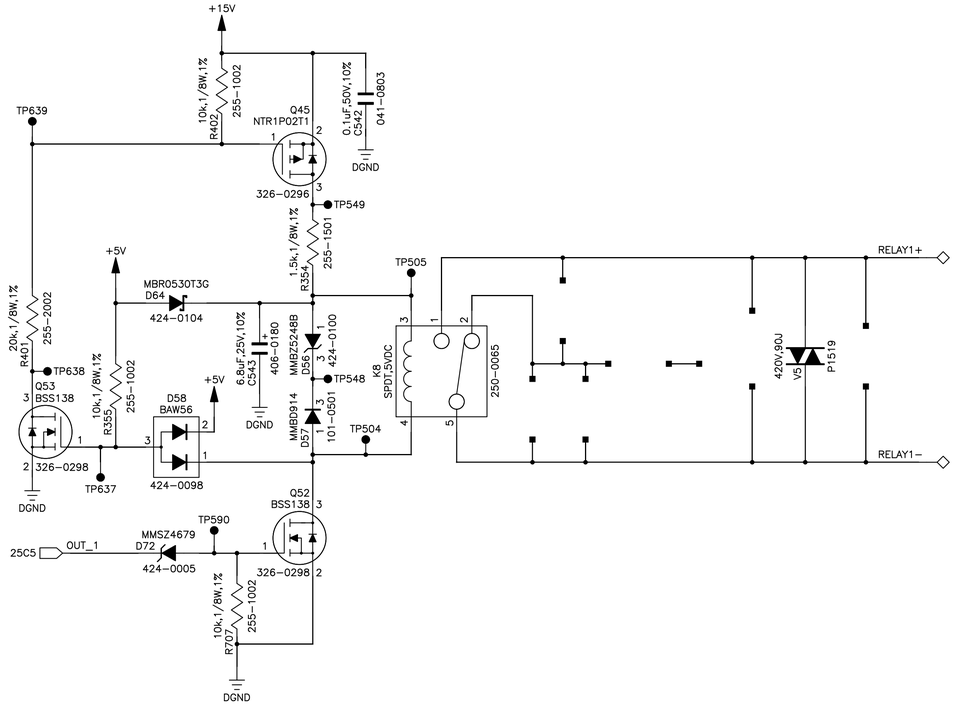
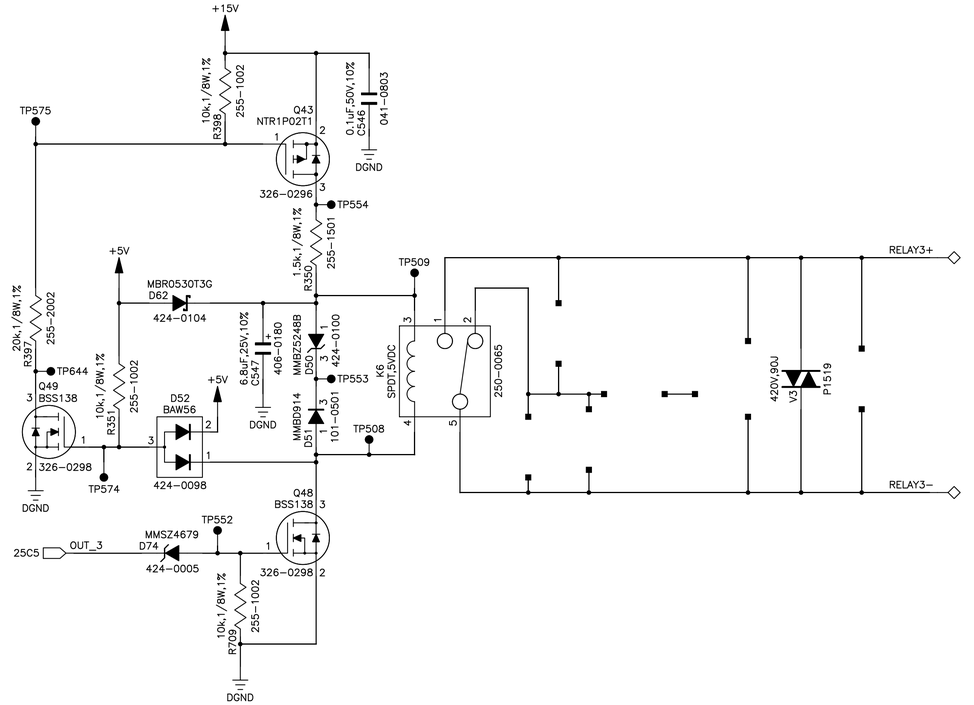
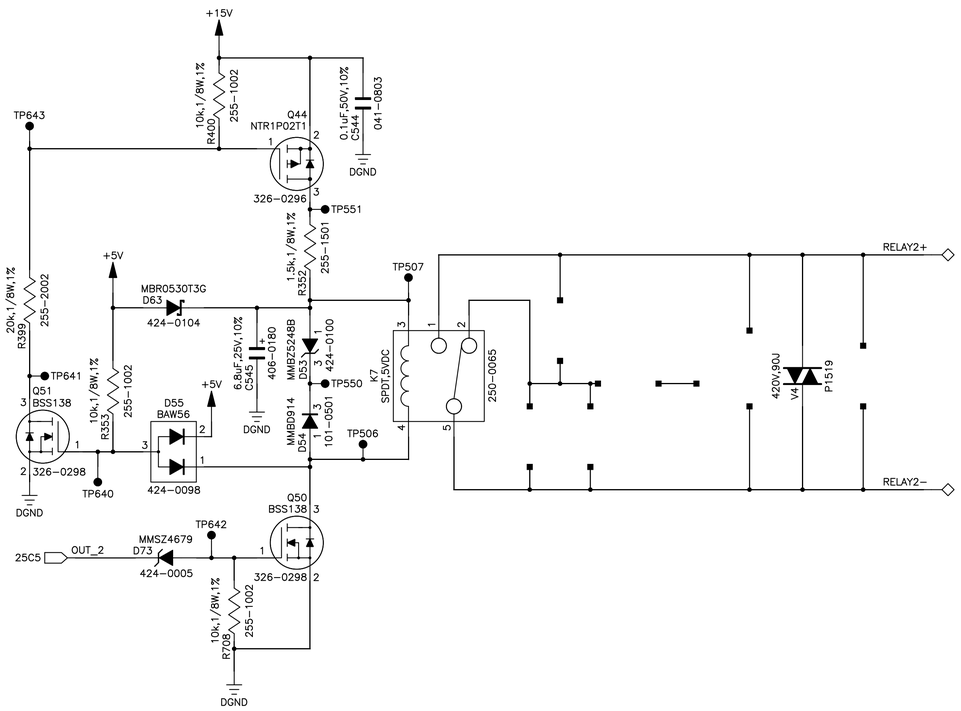
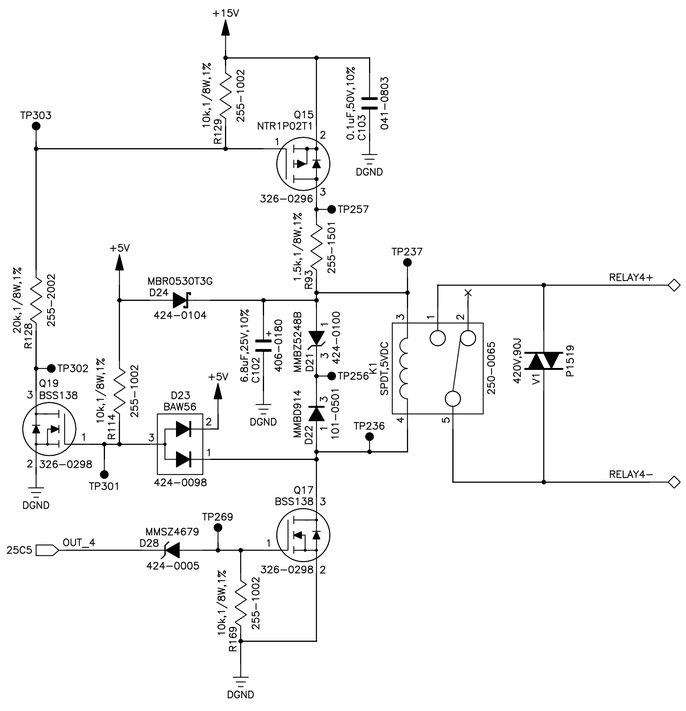
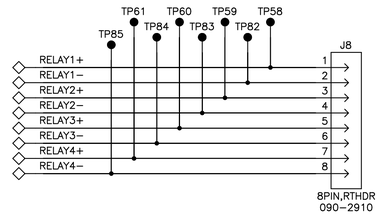
TITLE: 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. JUMPERS/MBIO	SHEET 25 OF 30	











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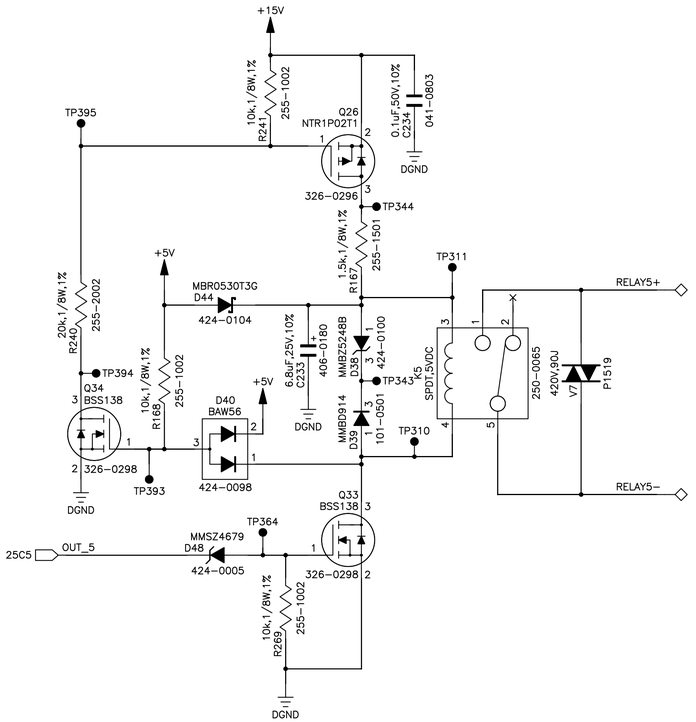
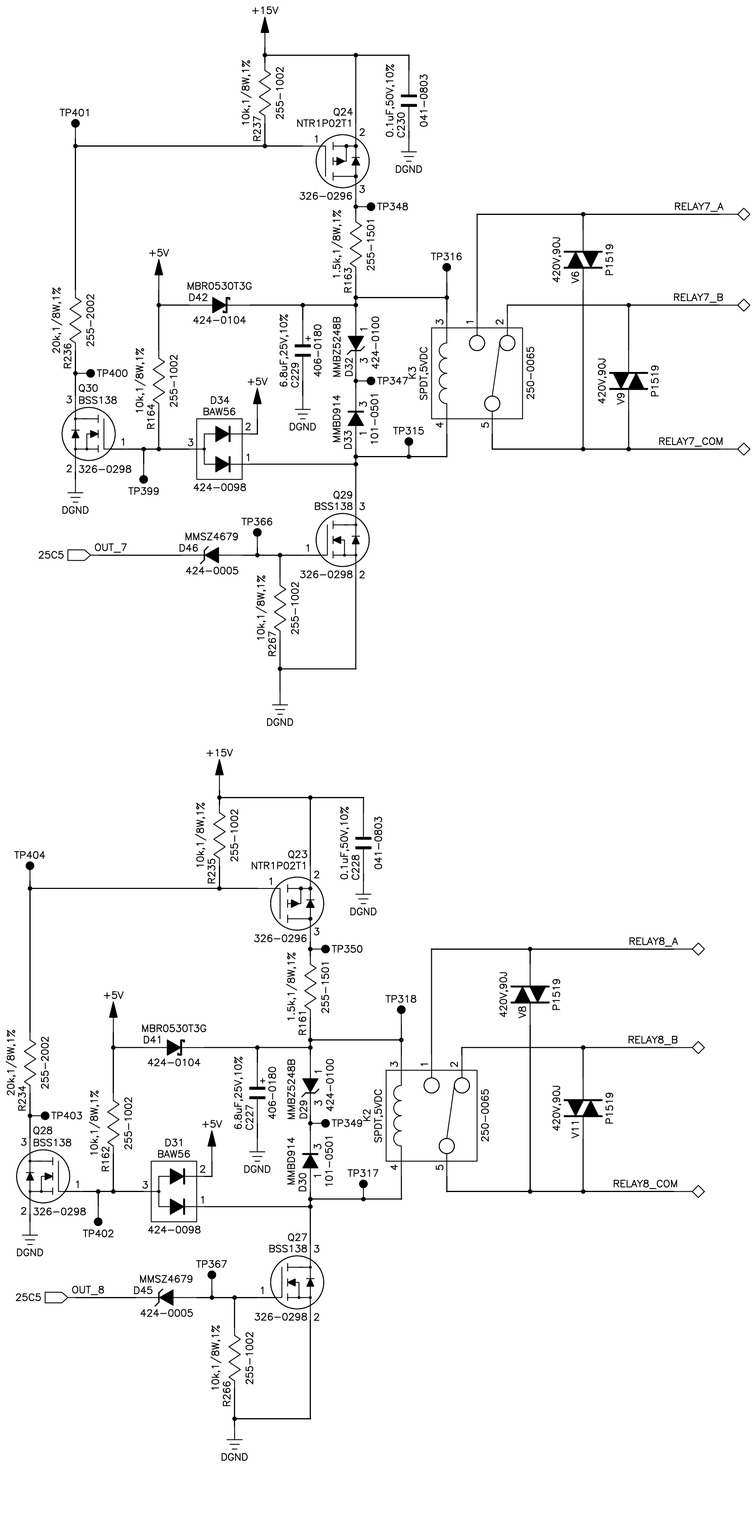
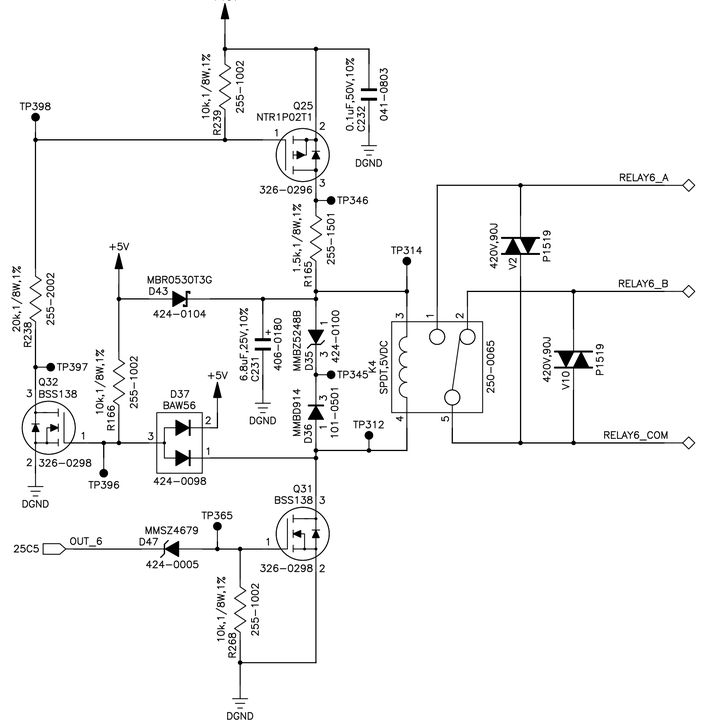
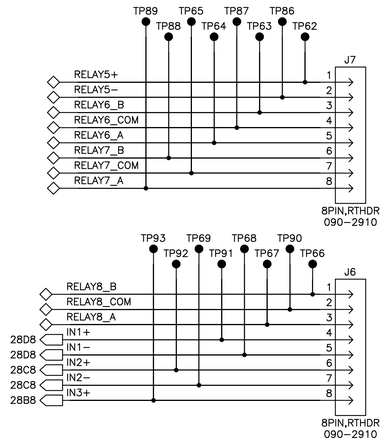
TITLE	6XX MB5 12V I/O
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. CONTACT OUTPUTS	SHEET 26 OF 30









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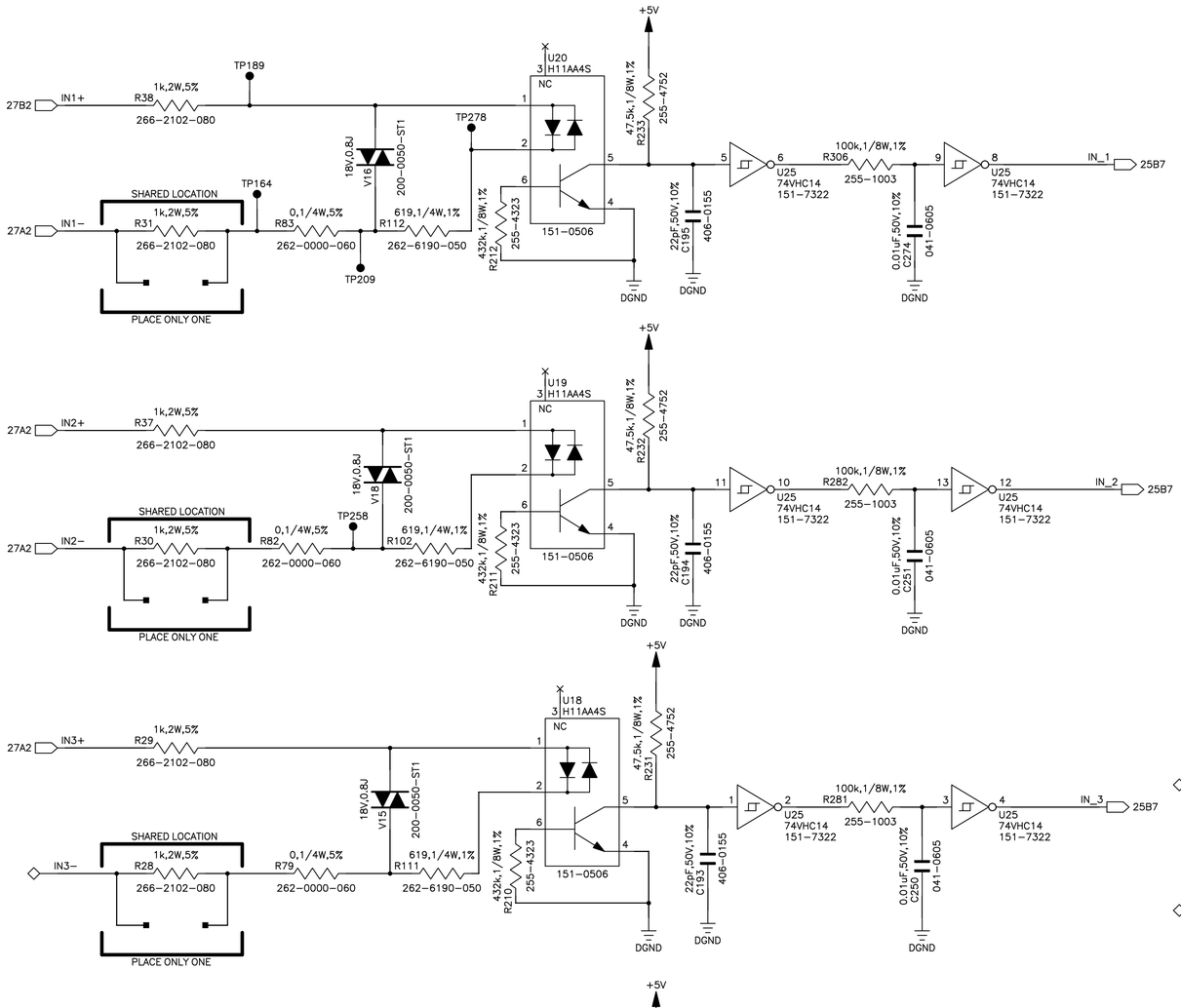
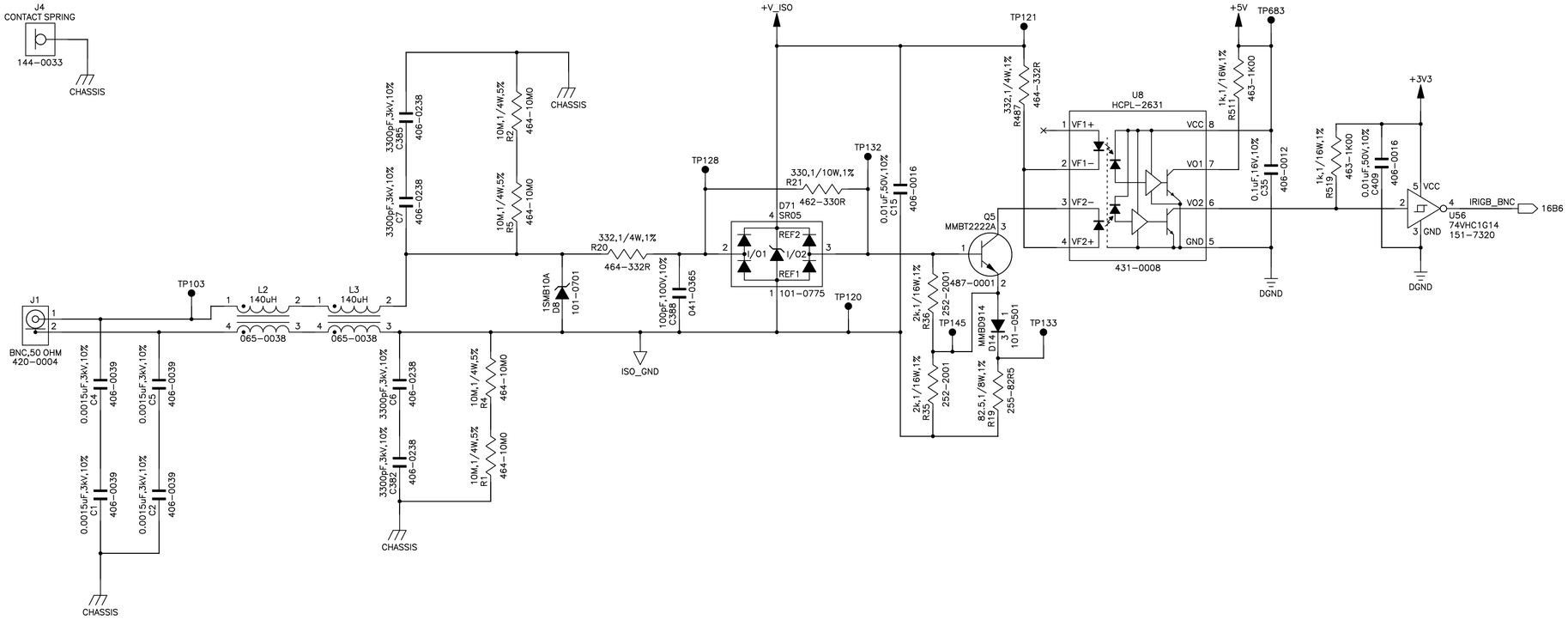
TITLE 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. CONTACT OUTPUTS		SHEET 27 OF 30

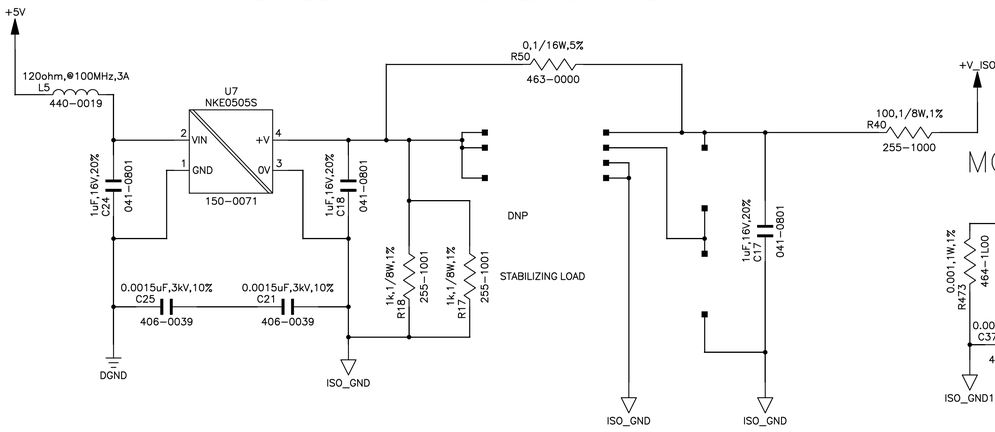


CREATED ON	SCHWEITZER ENGINEERING LABORATORIES, INC.
11/28/22	2350 NE HOPKINS COURT, PULLMAN, WA 99163
	THIS INFORMATION IS CONFIDENTIAL TO SCHWEITZER ENGINEERING LABORATORIES, INC. THE INFORMATION SHALL BE MAINTAINED IN CONFIDENCE AND SHALL NOT BE USED BY THE RECIPIENT OR DISCLOSED TO OTHERS WITHOUT THE SPECIFIC WRITTEN PERMISSION OF SCHWEITZER ENGINEERING LABORATORIES, INC.
TITLE	6XX MB5 12V I/O
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01
REV: B3	
DESC. CONTACT INPUTS	SHEET 28 OF 30

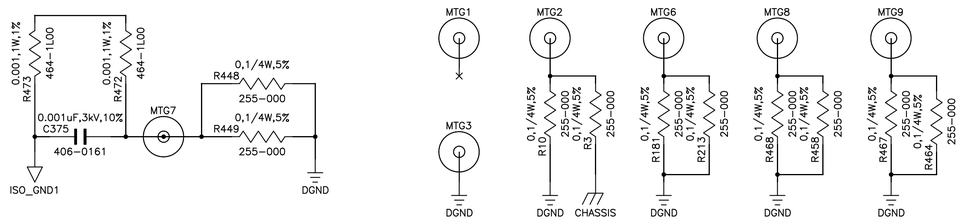
IRIG AND ISOLATED SUPPLY



ISOLATED IRIG 5V POWER SUPPLY



MOUNTING HOLES AND GROUND TIES



CREATED ON 11/28/22	SCHWEITZER ENGINEERING LABORATORIES, INC. 2350 NE HOPKINS COURT, PULLMAN, WA 99163	
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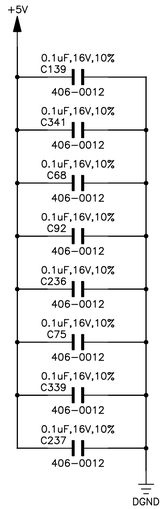
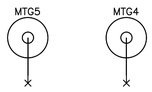
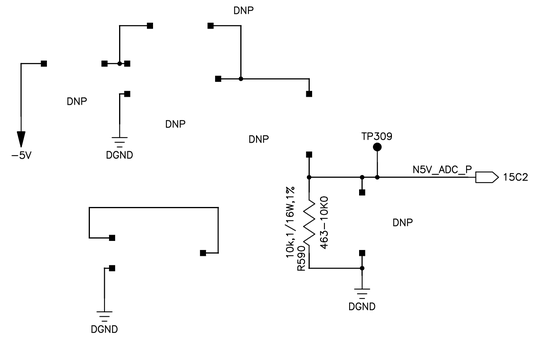
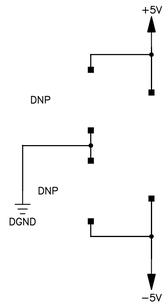
TITLE 6XX MB5 12V I/O		
BOM NUMBER B2008-03-01	DRAWING NUMBER S70-2008-03-01	REV B3
DESC. IRIG, ISOLATED SUPPLY		SHEET 29 OF 30

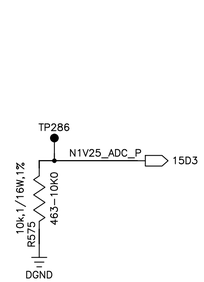


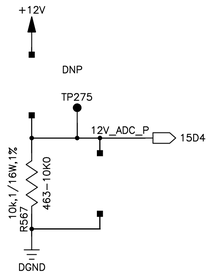


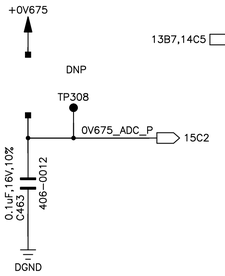
POWER RAIL MONITORING RESISTOR DIVIDERS

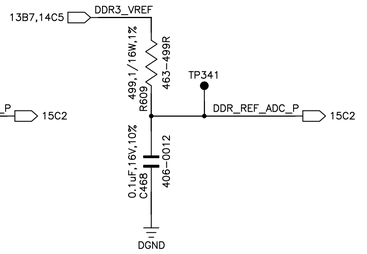


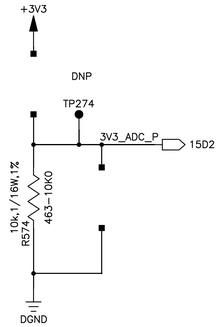


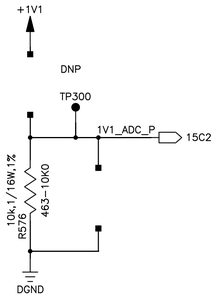


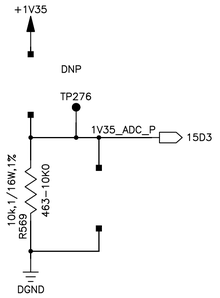












CREATED ON 11/28/22	SCHWEITZER ENGINEERING LABORATORIES, INC. 2350 NE HOPKINS COURT, PULLMAN, WA 99163
TITLE: 6XX MB5 12V I/O	
BOM NUMBER: B2008-03-01	DRAWING NUMBER: S70-2008-03-01 — REV: B3
DESC. +5V PLANE SIGNAL REFERENCE DECOUPLING, FPGA RAIL MONITORING	SHEET 30 OF 30

S70-2008-03-01 REVISION HISTORY

REV	ECO	DRN	EE	DATE

REV	ECO	DRN	EE	DATE

REV	ECO	DRN	EE	DATE

REV	ECO	DRN	EE	DATE

REV	ECO	DRN	EE	DATE

REV	ECO	DRN	EE	DATE

A 22-3329 KWH J. GRAHAM 12/30/2022

NEW DESIGN STARTED FROM 070-2029

REF DES	OLD PART	NEW PART

B 22-3329 TLB D. MCKEE 2/16/2023

PMIC LAYOUT UPDATES AND OTHER CIRCUIT UPDATES. DESIGN WAS RENUMBERED.

REF DES	OLD PART	NEW PART

B1 22-3329 KWH J. GRAHAM 3/3/2023

CHANGES TO: OPTIMIZE I2C WAVEFORMS. OPTIMIZE 5V BUCK COMPENSATION. MATCH 5V FEEDBACK CAPACITOR WITH OTHER PMIC RAILS. PREVENT PULLING DOWN ENABLE PINS WITH +5V_STBY AT STARTUP.

REF DES	OLD PART	NEW PART
C30	041-0859	041-0231
C31	406-0097	406-0066
C410	406-0021	406-0228
C413	406-0021	406-0228
C415	041-0381	406-0192
MSC2	BS2008-03.B	BS2008-03.B1
R123	463-3K32	463-1K50
R407	463-10K0	Unplaced
R556	463-3K32	463-1K20
R579	463-10K0	Unplaced
R580	463-10K0	Unplaced
R59	463-150K	463-47K5
R593	463-10K0	Unplaced

B2 22-3329 KWH J. GRAHAM 3/13/2023

CHANGES TO RESOLVE TEST FINDINGS

REF DES	OLD PART	NEW PART
C210	406-0012	406-0016
C29	406-0012	406-0016
L11	440-0019	255-000
L12	440-0019	255-000
L14	440-0019	255-000
L15	440-0019	255-000
L20	440-0019	255-000
L22	440-0019	255-000
L4	440-0019	255-000
L8	440-0019	255-000
MSC2	BS2008-03.B1	BS2008-03.B2
R520	252-1331	462-2K20
U28	151-0025	431-1504
U37	151-0025	431-1504
U38	151-0025	431-1504
U39	151-0025	431-1504
U59	431-1080	431-1080-P02
U76	431-1475	431-1475-P01

B3 22-3329 KWH J. GRAHAM 3/17/2023

FLOAT UNUSED VBUS PINS TO AVOID POTENTIAL OVERVOLTAGE FROM 5V RAIL EXTREMES

REF DES	OLD PART	NEW PART
MSC2	BS2008-03.B2	BS2008-03.B3
R118	463-0000	Unplaced
R586	463-0000	Unplaced