

PSR and SSR Flyback Aux Winding OVP and UVLO Fault Sensing Design tips and Troubleshooting



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ABSTRACT

Texas Instruments has developed discontinuous mode (DCM) flyback controllers that use transformer coupling to sense the input voltage (V_{IN}) and output voltage (V_{OUT}) for power supply control; as well as, circuit fault protection. These voltages are sensed across the flyback transformer (T1) auxiliary winding (V_{AUX}) of the flyback converter shown in Figure 1-1. The problem with this technique is if the aux winding is noisy it could falsely trigger and input under voltage lockout (UVLO) fault or an output over voltage protection (OVP) fault and unexpectedly shut down the system. The purpose of this application note is to give design guidance to resolve and avoid false OVP and UVLO faults caused by noise on the aux winding. TI primary side regulated (PSR) DCM flyback controllers that use this kind of aux winding sensing for OVP and UVLO are the UCC28700/1/2/3/4, UCC28710/1/2/3, UCC28910/1. The UCC28740/2 secondary side regulated (SSR) controllers also use aux winding fault as well.

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1 Introduction

Texas Instruments has developed discontinuous mode (DCM) flyback controllers that use transformer coupling to sense the input voltage (V_{IN}) and output voltage (V_{OUT}) for power supply control; as well as, circuit fault protection. These voltages are sensed across the flyback transformer (T1) auxiliary winding (V_{AUX}) of the flyback converter shown in Figure 1-1. The problem with this technique is if the aux winding is noisy it could falsely trigger and input under voltage lockout (UVLO) fault or an output over voltage protection (OVP) fault and unexpectedly shut down the system. The purpose of this application note is to give design guidance to resolve and avoid false OVP and UVLO faults caused by noise on the aux winding. TI primary side regulated (PSR) DCM flyback controllers that use this kind of aux winding sensing for OVP and UVLO are the UCC28700/1/2/3/4, UCC28710/1/2/3, UCC28910/1. The UCC28740/2 secondary side regulated (SSR) controllers also use aux winding fault sensing for as well.

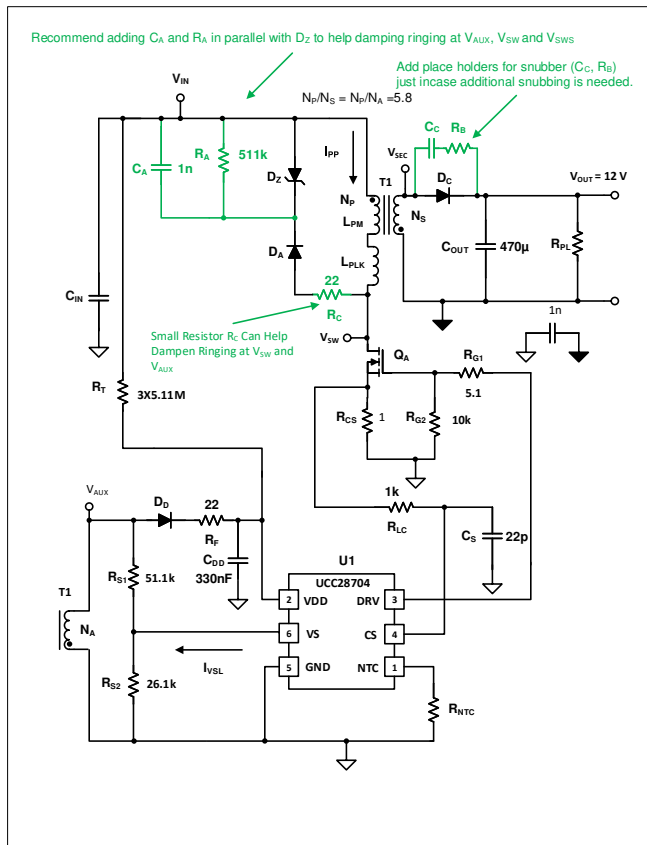


Figure 1-1. DCM Flyback Converter Using Aux Winding Sensing to Detect Input UVLO and OVP

2 Brief Review of DCM FM/AM/FM Flyback Control Law

The DCM controllers presented in this application note use Frequency Modulation (FM) and Primary Peak Current Modulation (AM) to control the flyback converters frequency, duty cycle, primary peak current and output voltage. These controllers will sense the output voltage at the VS pin of the flyback controller (Fig. 1-1) and will adjust an internal control voltage (V_{CL}) to adjust the primary peak current (I_{PP}) and the converters switching frequency (f_{SW}). This control technique is known as control law. The control law of the UCC28704 is presented in figure 2-1. Please note that all of the devices in this paper use similar control laws but are parametrically different. It is recommended that the reader review the data sheet of the specific controller they are using in their design for specific control law details.

When the converter is operating at maximum load and at the minimum input voltage. The design will be operating in critical conduction close to quasi resonant (QR) operation at the converters maximum switching frequency ($f_{SW(max)}$).

When the converter is operating in region 4 if less duty cycle is required the internal feedback amplifier will adjust V_{CL} from 4.85 V to 3.0 V to decrease f_{SW} to obtain the correct duty cycle to maintain V_{OUT} . The f_{SW} will be adjusted from $f_{SW(max)}$ down to 25 kHz minimum in region 4.

In region 3 when the converter is operating at 25 kHz to adjust the duty cycle of the converter the primary peak current (I_{PP}) amplitude will be adjusted to maintain the duty cycle. It will vary from the max programmed I_{PP} to $I_{PP}/4$ to maintain the duty cycle. V_{CL} will be adjusted from 3 V to 2.2 V in this region.

In region 2 with the primary peak current controlled to $I_{PP}/4$ if the controller needs less duty cycle it will decrease the switching from 25 kHz to control the duty cycle. In this region V_{CL} will be controlled from 2.2 V to 1.3V.

In region 1 when V_{CL} is below 1.3V the converter is operating at the minimum switching frequency and will require a pre-load resistor (R_{PL}) to keep the design in regulation.

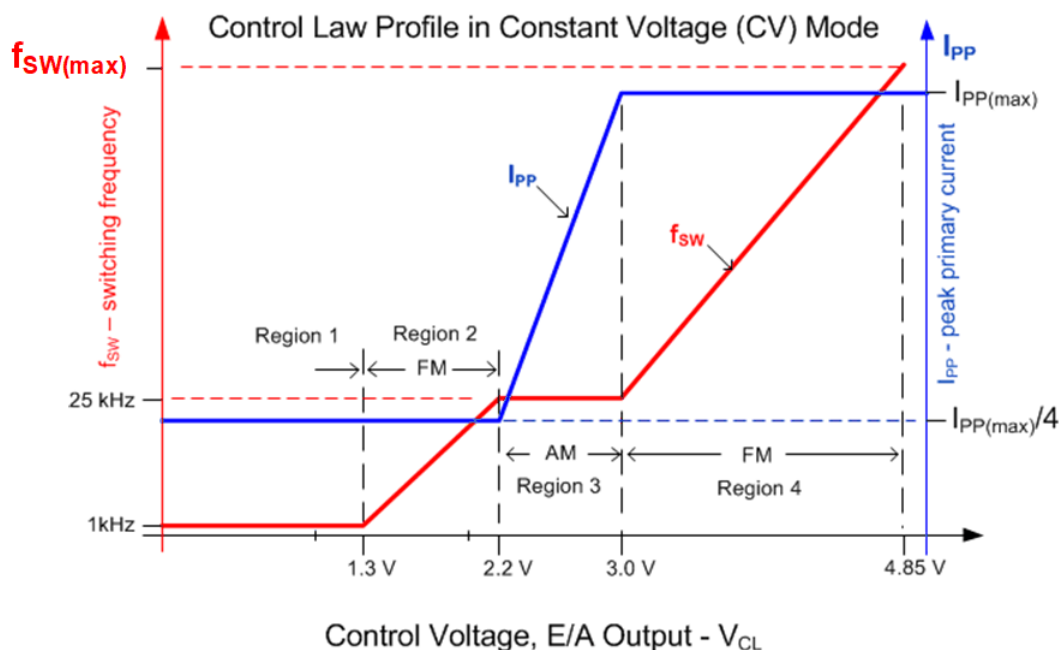


Figure 2-1. Control Law of UCC28704

3 Input (V_{IN}) and Output (V_{OUT}) Voltage Sensing for UVLO and OVP Fault Protection

V_{IN} and V_{OUT} can be sensed and measured across the auxiliary winding (V_{AUX}) that is used to provide power to the flyback controller (U1) while the transformer is being energized. Figure 3-1 shows the switching wave form of DCM flyback converter operating near critical conduction. Where DRV is the logic level of the flyback controllers gate driver and CS is the voltage measured across the current sense resistor (R_{CS}). When the transformer is being energized during the flyback FETs (Q_A) on time (t_{ON}) V_{IN} can be measured directly across V_{AUX} . Please refer to equation 1 and figures 1-1 and 3-1 for details.

$$V_{IN} \approx \left| V_{AUX} \times \frac{N_P}{N_A} \right| \quad (1)$$

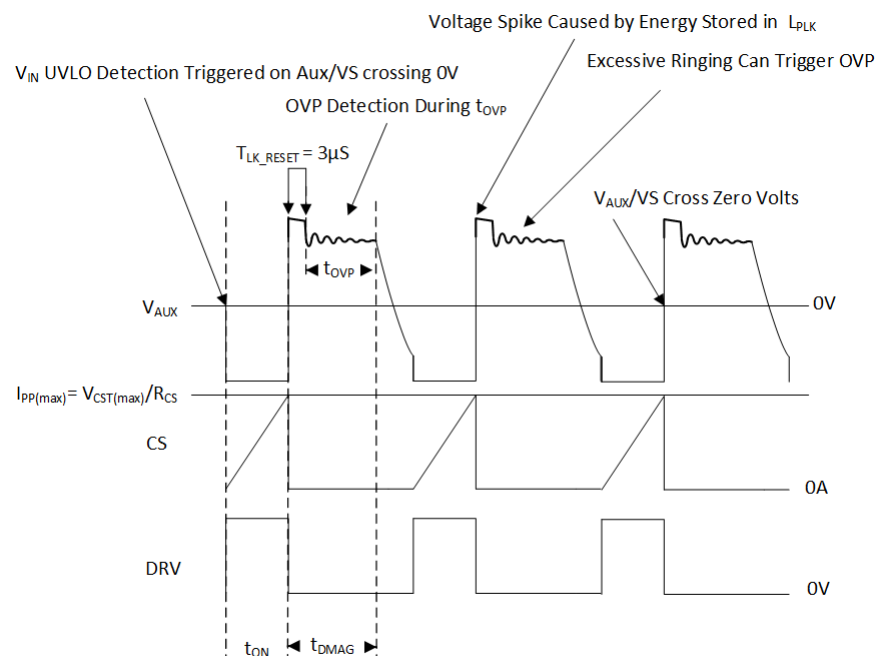


Figure 3-1. Aux, CS and DRV Signals at Max Load Minimum Line Voltage

V_{OUT} can be sensed while the transformer is delivering energy after the flyback converters transformer leakage spike that occurs during the T_{LK_RESET} time period has dissipated during t_{DMAG} . Please refer to equation 2 to and figure 1-1 and equation 2 for details.

$$V_{OUT} \approx \left| V_{AUX} \times \frac{N_S}{N_A} \right| \quad (2)$$

To prevent false measurements of V_{OUT} the flyback controllers discussed in this paper have a blanking circuit. The controllers will not sense V_{OUT} during pre-programmed blanking time (T_{LK_RESET}). Please note T_{LK_RESET} moves with loading. For example the UCC28704 controller will not sense V_{OUT} for 3 us (T_{LK_RESET}) at full load. When operating in the AM band to control the duty cycle the transformer primary peak current will be adjusted linearly down from I_{PP} to $I_{PP}/4$ to control the duty cycle. When the UCC28704 is operating in AM T_{LK_RESET} will be adjusted from 3 μ s down to 750 ns as the primary peak current is decreased. When this occurs the flyback converter will go deeper into DCM operation. Please refer to figure 3-2 for details.

When operating in the AM range when I_{PP} is decreased T_{LK_RESET} blanking time also decreases as well. Please check the data sheet of the part you are using, because T_{LK_RESET} changes are different with different flyback controllers.

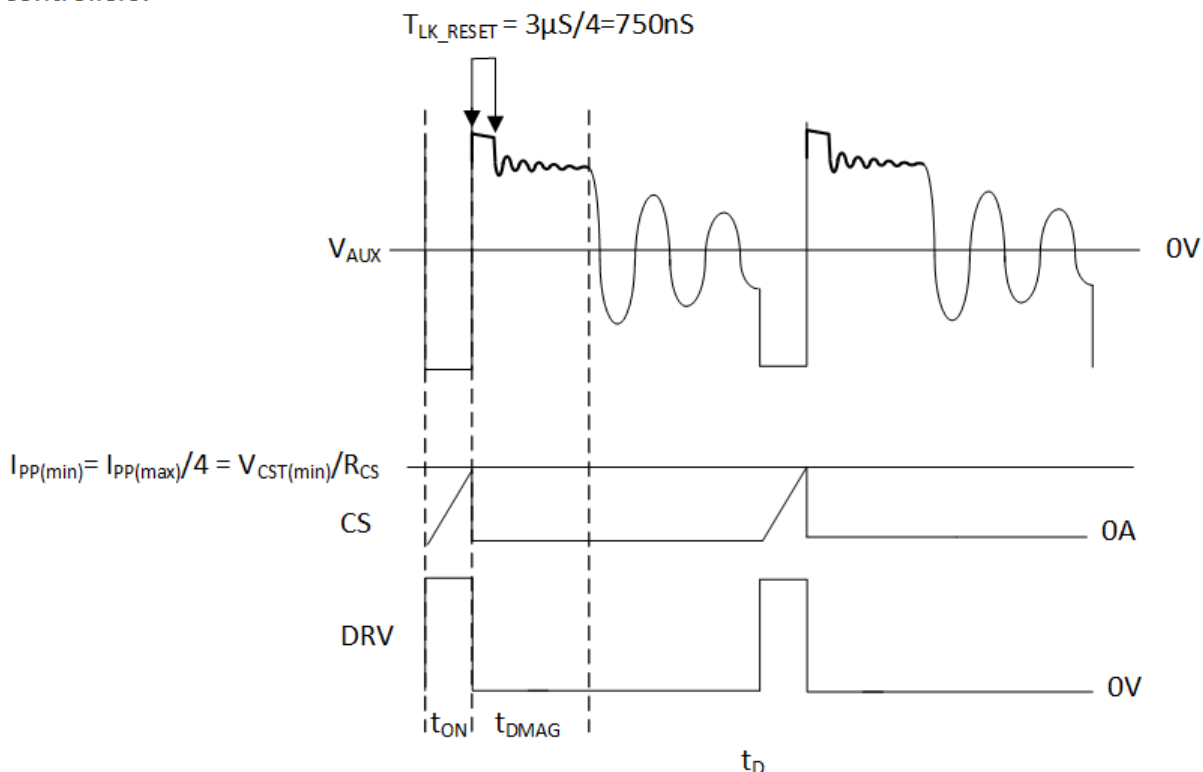


Figure 3-2. V_{AUX} , CS and DRV while the Flyback Operating Deep into DCM Operation

4 Input Under Voltage Lockout (UVLO) Protection

Please note these flyback controller have programable input under voltage detection that can be set and adjusted primary to auxiliary turns ration and properly selecting R_{S1} and R_{S2} . Details of exactly how to program the input UVLO can be found in the specific flyback controllers data sheet.

The VS pin of these flyback controllers have an internal clamp on the VS pin that clamps the VS pin to roughly ground (GND) to while Q1 is on (t_{on}), (Fig. 3-1 and 3-2). During this time the current coming out of the VS pin (I_{VSL}) in combination with R_{S1} and the N_P/N_A turns ratio will be used to program and determine what the input voltage level of the flyback converter will start at ($V_{IN(run)}$) and what input voltage the converter will stop switching at ($V_{IN(stop)}$). Please note the value $I_{VSL(run)}$ start and $I_{VSL(stop)}$ stop thresholds will vary based on the flyback controller that is used in the design, please refer to the flyback controller's data sheet for the correct values.

The design presented in Figure 1-1 will not start switching until V_{IN} is greater than 67 V and will stop switching when V_{IN} drops below 23.8 V. Please refer to equations 3 through 6 for details.

$$I_{VSL(run)} = 225\mu A, \text{ VS line sensed run current} \quad (3)$$

$$V_{IN(run)} \geq I_{VSL(run)} \times R_{S1} \times \frac{N_P}{N_A} = 225\mu A \times 51.1k\Omega \times 5.83 = 67V, \text{ } V_{IN} \text{ startup threshold} \quad (4)$$

$$I_{VSL(stop)} = 80\mu A \quad (5)$$

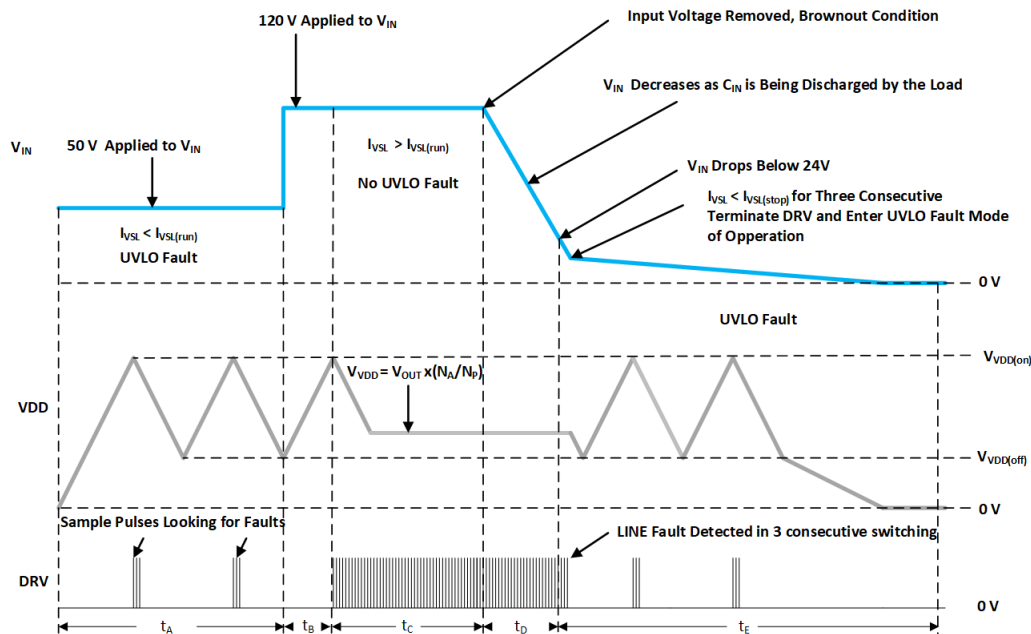
$$V_{IN(stop)} < I_{VSL(stop)} \times R_{S1} \times \frac{N_P}{N_A} = 80\mu A \times 51.1k\Omega \times 5.83 = 23.8V \quad (6)$$

When power is first applied the VDD capacitor (C_{DD}) will trickle charge through R_T of figure 1-1. Please note that some flyback controllers trickle charge the C_{DD} capacitor with an internal JFET startup circuit. The capacitor will continue to trickle charge until the flyback controllers turn on threshold is reached ($V_{VDD(on)}$) at this point it will deliver 3 gate drivers pulse to sample the V_{IN} and V_{OUT} at the controllers maximum switching frequency ($f_{SW(max)}$) to sample the input and output voltage. The UCC28704 will control the primary current to $I_{PP(max)}/4$. At this point t_{LK_RESET} will be at it's minimum. If the converter detects a UVLO and/or a OVP fault during this time the gate driver will stop switching and the I_{DD} current will discharge C_{DD} to the flyback controllers turnoff threshold ($V_{VDD(off)}$). After $V_{VDD(off)}$ is reached the C_{DD} will be charged up through R_T to $V_{VDD(on)}$ and the flyback controller will sample V_{OUT} and V_{IN} again.

$$V_{VDD(on)} = 21\text{ V} \quad (7)$$

$$V_{VDD(off)} = 8\text{ V} \quad (8)$$

Figure 4-1, shows an example of how the input fault protection would work with different input voltages. At the beginning of time interval t_A 50 V is applied at V_{IN} , the C_{DD} capacitor will be trickle charged up to $V_{VDD(on)}$. The flyback controller will then sample the input through N_P/N_A turns ratio and will detect an input UVLO fault and stop switching and enter fault mode operation during this time interval. At the beginning of time interval t_B the input voltage is increase to 120 V, however, the flyback controller is still not switching, it has to wait until C_{DD} is charge up to $V_{VDD(on)}$ to gives 3 DRV pulses to sample the input voltage. At the beginning of time interval t_C the flyback controller gives 3 DRV pulses to sample the input voltage, at this point the flyback controller has determined that the UVLO condition no longer remains and the gate driver continues to switch. The C_{DD} capacitor will discharge down to the reflected output voltage determined by the N_A/N_S turns ratio, at this point the flyback controller will be powered by the auxiliary winding (N_A) of T1. At the beginning of time interval t_D the input voltage was removed from V_{IN} simulating a brown out condition. The input bulk capacitor C_{IN} will discharge based on the load on the flyback output. At the beginning of time interval t_E capacitor C_{IN} will have discharged to a point where the input voltage will cause a UVLO fault. After the UVLO fault has been detected in three consecutive switching cycles, the flyback controller will terminate the DRV pulses and will reenter UVLO fault mode for the rest of time interval. The flyback controller will remain operating in this mode until an input voltage is applied to V_{IN} that causes the I_{VLS} current to be greater than $I_{VSL(run)}$.



While Gate Driver (DRV) is Switching Flyback Converter is Sampling for OVP, LINE and OCP FAULTS

- If a fault is detected for three consecutive switching cycles DRV stops switching
 1. C_{VDD} is discharge until the voltage at VDD reaches $V_{VDD(off)}$
 2. C_{VDD} is trickle charged by R_T or an internal trickle charge startup circuit until the voltage at VDD reaches $V_{VDD(on)}$ reaches

Figure 4-1. Example of UVLO Fault Detection

5 Output Over Voltage (OVP) Protection

The flyback controllers' presented in this paper will sense the output voltage on V_{AUX} through a resistor divider formed by R_{S1} and R_{S2} and flyback controller's sense pin (VS). If the VS pin exceeds the V_{OVP} threshold for three consecutive switching cycles it will determine that an OVP event has occurred and gate driver switching will stop.

$$V_{OVP} = 4.6 V \quad (9)$$

$$V_{OUT} \geq \frac{V_{OVP}(R_{S1} + R_{S2})}{R_{S2}} \times \frac{N_S}{N_A} \quad (10)$$

The schematic in figure 1-1 represents a flyback converter that was designed to step down an input voltage (V_{IN}) of 75 V to 390 V DC to a regulated 12 V, 10W output. The N_S/N_A turns ratio was selected/designed to be one. So in this example the flyback converter would shut down if V_{OUT} for three consecutive switching cycles was greater than 13.6V, equation 11.

$$V_{OUT} \geq \frac{4.6V(26.1k\Omega + 51.1k\Omega)}{26.1k\Omega} \times 1 = 13.6 V \quad (11)$$

If an OVP fault is detected DRV switching will stop and the C_{DD} capacitor will be discharged down to $V_{VDD(off)}$ and the C_{DD} capacitor will be trickle charge through R_T up when V_{CDD} reaches $V_{VDD(on)}$ the controller will then give three DRV pulses at $f_{SW(max)}$ controlling the primary current to $I_{PP(max)}/4$ and t_{LK_RESET} blanking is set to its minimum of 750 ns. Please remember that VS will detect an OVP from the end of T_{LK_RESET} to the end of t_{DMAG} . Please refer to figure 3-1 and 3-2 for details. The CDD and DRV behavior during an OVP fault behaves in similar to UVLO fault presented in figure 4-1.

6 Not Recognizing a UVLO or OVP Fault

Some designers have reported that on their initial prototypes that flyback controllers using PSR fault sensing will not startup up. They report either there are no gate drive pules and/or VDD looks like a saw tooth presented in figure 6-1. What is actually going on is the flyback controller is just going into UVLO, OVP or OCP fault protection. Once the fault is cleared VDD will stop cycling between $V_{VDD(on)}$ and $V_{VDD(off)}$ and the flyback will resume normal operation once the fault is cleared.

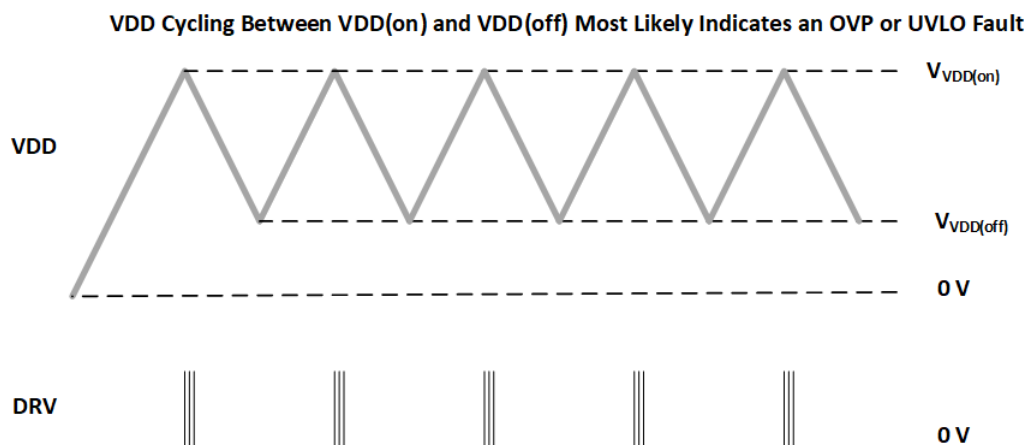


Figure 6-1. VDD Cycling During a Fault

7 Separate Bias Supply Startup Issue and Resolution

When initially starting up a prototype flyback converter some engineers use a separate bias supply for powering VDD of the flyback controller. Some of these designers have mentioned that there are no gate driver pulses observed and the flyback controller appears to be not functioning. Most of the time the issue is when power was applied to VDD there was no input voltage applied to the flyback converter. The flyback converter had already sampled the input voltage and because there was none present the controller entered input UVLO fault protection. The gate driver stopped switching and the external bias supply prevents cycling of the VDD pin between $V_{VDD(off)}$, $V_{VDD(on)}$ and $V_{VDD(off)}$ to reset the fault.

To resolve this issue is simple. It requires applying the input voltage to V_{IN} that is greater than the UVLO trip point. Then bring the bias voltage to VDD above $V_{VDD(on)}$. The other option is adjust the bias voltage at VDD below $V_{VDD(off)}$ and then above $V_{VDD(on)}$ to reset and clear the UVLO fault.

8 Not Having a Clean Aux Winding Signal:

The waveform in figure 8-1 is a simulation of a flyback converters switch node (V_{SW}), the aux winding voltage (V_{AUX}), and the flyback current sense signal (V_{CS}) of a flyback converter that uses a TVS clamp and no provisions for dampening aux winding ringing. This simulation was based on the flyback converter presented in figure 1-1 without the circuitry that was highlighted in green.

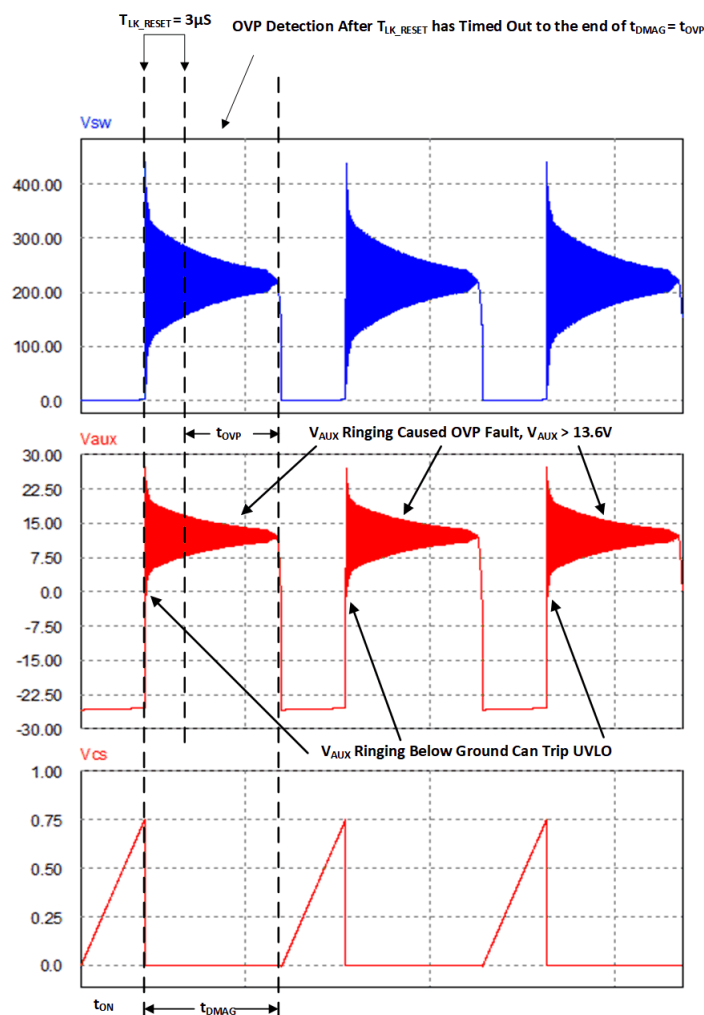


Figure 8-1. Noisy VAUX Falsely Trigger OVP and/or UVLO Fault Protection

The flyback converter was designed to trigger OVP when V_{OUT} and V_{AUX} were greater than 13.6V. This flyback converter did not have any provisions for dampening the switch node (V_{SW}) ringing cause by parasitic inductance and capacitance at the switch node. The noise at V_{SW} is couple through the auxiliary to primary turns ratio (N_A/N_P) and will falsely trip OVP fault protection.

The flyback controller will sample for an OVP (t_{OVP}) after T_{LK_RESET} has timed out to the end of the transformer demagnetizing time (t_{DMAG}). From the waveform in figure 8-1 it can be observed that the ringing on V_{AUX} is greater than 13.6 V during the over voltage protection sampling time (t_{OVP}). This will cause the design to shut down and not regulate the output voltage correctly.

It can be also observed the ringing on V_{aux} in figure 8-1 is excessive it rings down below ground during t_{LK_RESET} . This action has been known to trigger a UVLO fault as well and shut down the converter. This is because when the VS pin crosses ground it activates input and UVLO detection.

9 Removing Aux Winding Ringing to Resolve False Triggering of OVP and UVLO Faults

The major cause of aux winding ringing that can falsely trip OVP is parasitic inductances and capacitance in the design. To help reduce this ringing it is recommended through layout and transformer design that you keep the parasitic inductances and capacitances as small as possible.

When selecting and/or designing your transformer (T1) it is recommended that a transformer have a primary leakage inductance (L_{PLK}) of less than three percent of the primary magnetizing inductance (L_{PM}), (Figure 1-1). This will help reduce ringing at the switch nodes.

$$L_{PLK} \leq 0.03 \times L_{PM} \quad (12)$$

When laying out the printed circuit board keep the traces in the power stage; as short as, possible. Keep in mind that every inch of trace adds roughly 10 nH of parasitic trace inductance (L_{TRACE}). By keeping the traces as short as possible will also remove unwanted antennas from the design and will help improve noise impunity as well..

$$L_{TRACE} \approx \frac{10nH}{in} = \frac{10nH}{2.54cm} \quad (13)$$

To help reduce switch node ringing that could transformer couple into the V_{AUX} signal. It is recommended that you use an RCD clamp (R_A , R_C , C_A , D_A) over a TVS clamp (D_A , D_Z), (Figure 1-1). The reason for this is an RCD clamp will provide dampening at the switch node, where TVS clamp will only clamp the voltage when the switch node rings above the clamp voltage and provides very little to no dampening. Generally, we set the R_A and C_A time constant of the clamp to greater than 10 times the maximum switching period, equation 15 and 16. Please note for safety the designer want to use D_Z to clamp V_{SW} as well.

$$R_A \times C_A \geq \frac{10}{f_{SW(mx)}} = \frac{10}{100kHz} = 100us \quad (14)$$

$$R_A \times C_A = 511k\Omega \times 1nF = 511us \quad (15)$$

If you have excessive ringing across the secondary (V_{SEC}) winding it will couple into V_{AUX} through the auxiliary to primary turns ratio. The waveform presented in 9-1 shows ringing on the secondary of simulated from a 390 V to 12 V, 10 W, flyback converter. There is excessive ringing present on V_{SEC} that will couple to V_{AUX} and will most likely trigger and OVP and/or cause load regulation issues.

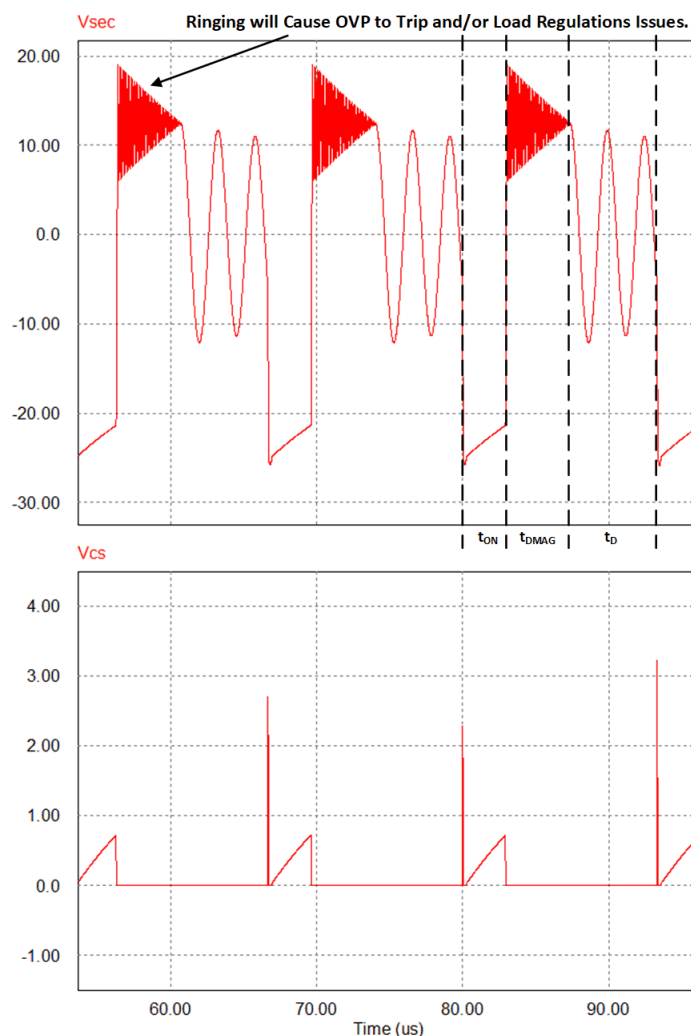


Figure 9-1. Flyback Secondary Voltage with Excessive Ringing

Contributors to V_{AUX} and V_{SEC} ringing that can accidentally trigger OVP is the cycle of energy between the primary and secondary leakage inductance (L_{PLK} , L_{SLK}) and the primary and secondary side switch node capacitances (C_{SW1} , C_{SW2}). Please note this excessive ringing can generally be dampened with an RC snubber (R_B , R_C) across the converters output rectifier (D_C) shown in figure 9-2.

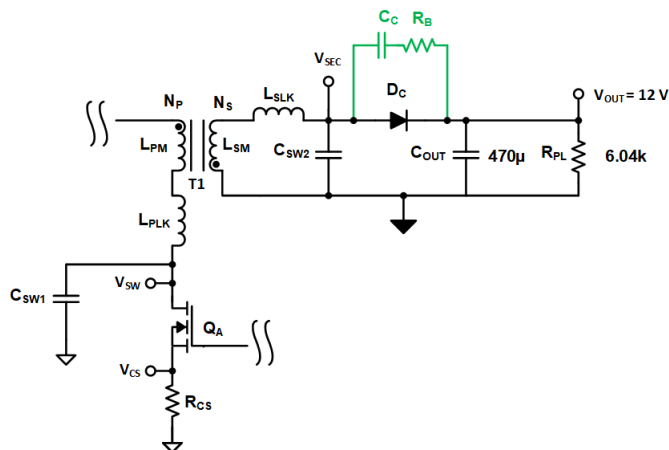


Figure 9-2. Simplified Flyback Schematic with Parasitic.

To show how to implement a snubber we will add a snubber circuit to the simulated 12 V, 10 W flyback design that created the waveforms presented in figure 9-2. To setup the snubber requires knowing or calculating L_{PM} , L_{SM} , L_{SLK} , C_{SW2} .

The secondary magnetizing inductance (L_{SM}) can be calculated by knowing the transformer primary to secondary turns ratio (N_P/N_S) and primary magnetizing inductance (L_{PM}) which are given in the transformer's data sheet and using equations 16 and 17. For this example the transformer had an L_{PM} of 680 μH and N_P/N_S of 5.8. L_{SM} for this design was calculated to be 20 μH .

$$\frac{N_P}{N_A} = 5.8 \quad (16)$$

$$L_{SM} = \frac{L_{PM}}{\left(\frac{N_P}{N_S}\right)^2} = \frac{680\mu H}{5.8^2} \approx 20\mu H \quad (17)$$

To calculate C_{SW2} requires have calculated L_{SM} and studying the V_{SEC} waveform and measuring the low frequency ringing (f_{r1}) during the t_D time interval, (Figure 9-3). Please note this should be done when the flyback converter is operating at light load and deep into DCM. In this example f_{r1} was measured to be 645 kHz. C_{SW2} can then be calculated using equation 19, which for this example was 3 nF

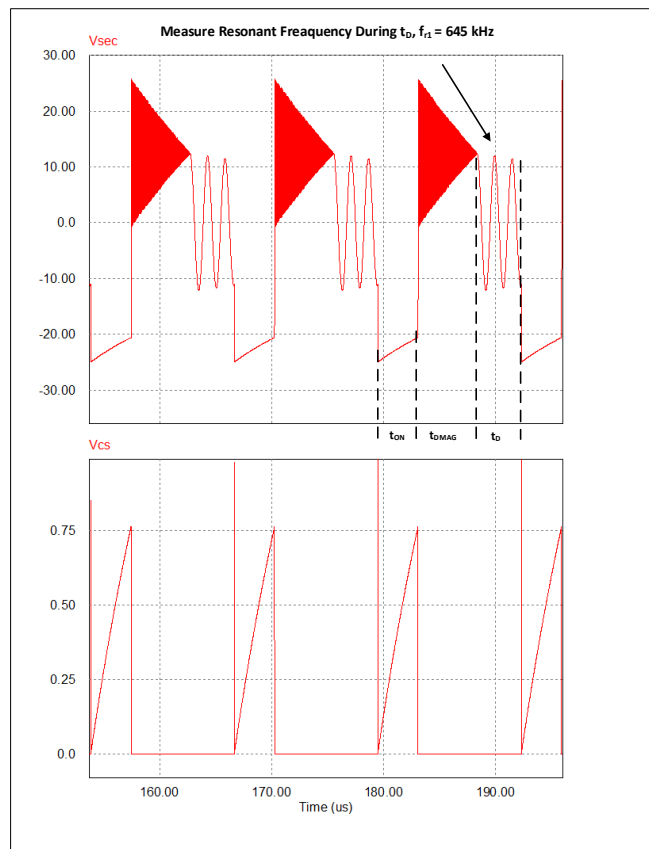


Figure 9-3. Measuring Low Frequency Ringing to Calculate C_{SW2}

$$f_{r1} = 645 \text{ kHz} \quad (18)$$

$$C_{SW2} = \frac{1}{(2 \times \pi \times f_{r1})^2 \times L_{SM}} = \frac{1}{(2 \times \pi \times 645kHz)^2 \times 20\mu H} \approx 3nF \quad (19)$$

The next step is to measure the high frequency ringing (f_{r2}), during time interval t_{DMAG} , (Figure 9-4). This resonant frequency is caused by the interaction of C_{SW2} and L_{SECP} . Based on f_{r2} and C_{SW2} , L_{SECP} can be calculated using equation 21. With a measured f_{r2} of 21 MHz and C_{SW2} of 3nF the calculated L_{SECP} would be roughly 43 nH.

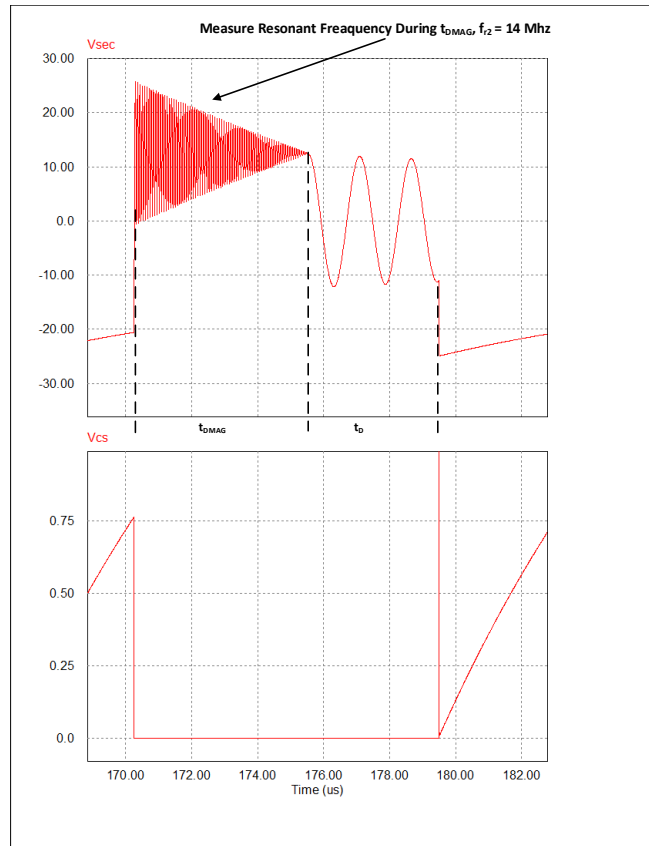


Figure 9-4. Measure high frequency ringing during time interval t_{DMAG}

$$f_{r2} = 14 \text{ MHz kHz, measure high frequency ringing during interval } t_{DMAG} \quad (20)$$

$$L_{SECP} = \frac{1}{(2 \times \pi \times f_{r2})^2 \times C_{SW2}} = \frac{1}{(2 \times \pi \times 14MHz)^2 \times 8nF} \approx 43nH \quad (21)$$

Snubbing resistor R_B is chosen to critically dampen the high frequency ringing and can be calculated using equation 22.

$$R_B = \frac{1}{Q} \sqrt{\frac{L_{SECP}}{C_{SW2}}} = \frac{1}{1} \sqrt{\frac{43nH}{3nF}} \approx 3.8ohm \quad (22)$$

A standard resistor was chosen for resistor R_B :

Choose a standard resistor value for R_B :

$$R_B = 3.83 \quad (23)$$

The snubbing capacitor C_C was chosen based on equation (23), based on the converter maximum nominal switching frequency (f_{SW}). This will allow the snubber to only be active for 1% of the switching period, keeping snubber losses to a minimum. The flyback design being evaluated had a f_{SW} of 75 kHz.

$$C_C = \frac{0.01}{f_{SW} \times R_B \times 5} = \frac{0.01}{75\text{kHz} \times 3.8\text{ohm} \times 5} \approx 7\text{nF} \quad (24)$$

A standard capacitance value for C_C was chosen for the design:

$$C_C = 6.8\text{nF} \quad (25)$$

The snubber components that were selected for R_B and R_C were applied to the circuit presented in figure 1-1 and figure 9-2 . The result was the secondary winding was critically damped. Please refer to figure 9-5 for damped waveforms results.

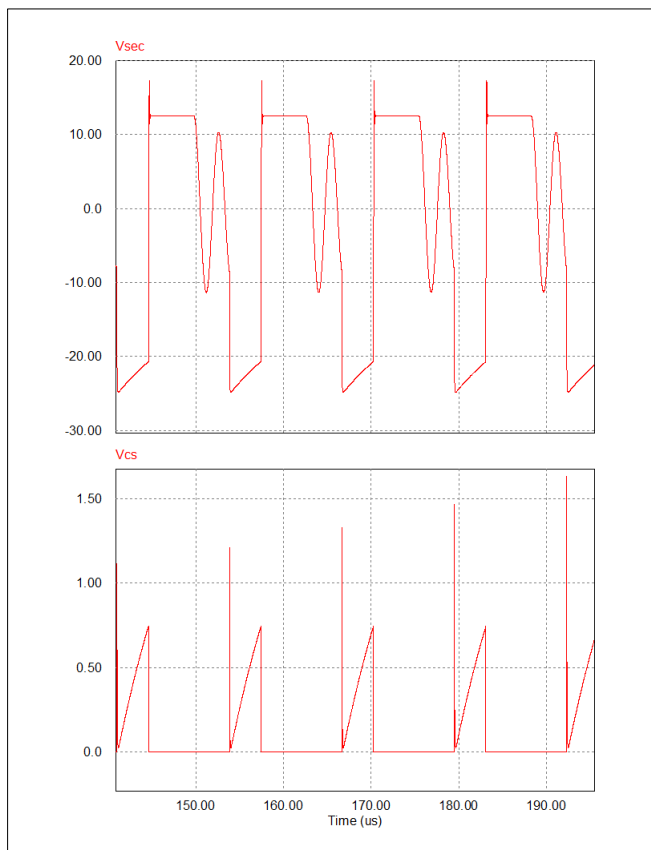


Figure 9-5. Snubber, R_B 3.83 ohms, C_C = 6.8nF

10 Noise on CS Pin Tripping Over Current Protection (OCP)

To help protect the FET from damage these flyback controllers have an over current protection (OCP) circuit that trips when the CS pin senses a current sense signal that is 2X the nominal peak. In the case of the UCC28704 this OCP trip point is 1.5 V.

When first turning on a FET there is a leading-edge current spike caused by the charging the gate to source capacitance of the FET used in the design. This generally can be seen on the current sense signal (V_{CS}), please refer to figure 10-1 for details. To prevent the controller from falsely tripping OCP due to this leading-edge gate

driver spike the flyback controller use current sense leading edge blanking. The flyback controller will not sense the current sense signal during a predetermined blanking time (T_{CSLEB}). In this example the UCC28704 was evaluated and had a T_{CSLEB} of 255 ns. Please note this time will vary based on flyback controller that is used in the design.

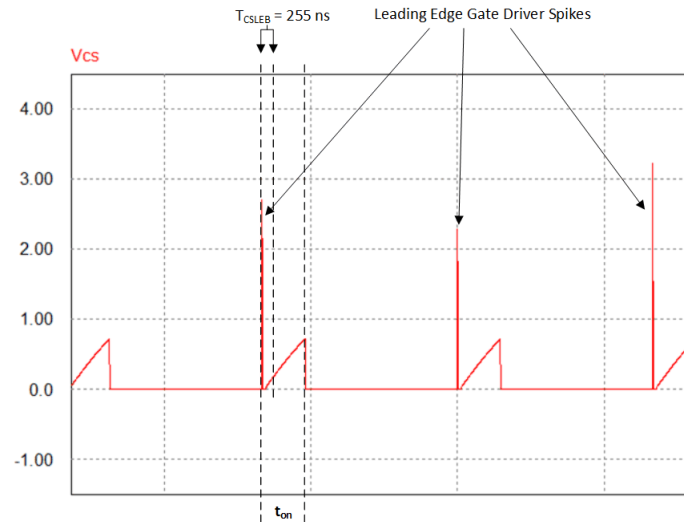


Figure 10-1. CS Leading Edge Blanking Helps Prevent False OCP Shutdown

On occasion I have seen these flyback designs shut down due to noise on the CS pin (V_{CS}). This is not related to OVP or input UVLO sensing. This occurs buy noise being coupled into the circuit through parasitic capacitance and/or poor layout. The problem occurs if these noise spikes are outside the T_{CSLEB} blanking window and are larger than the OCP trip point. Please refer to figure 10-2 for details.

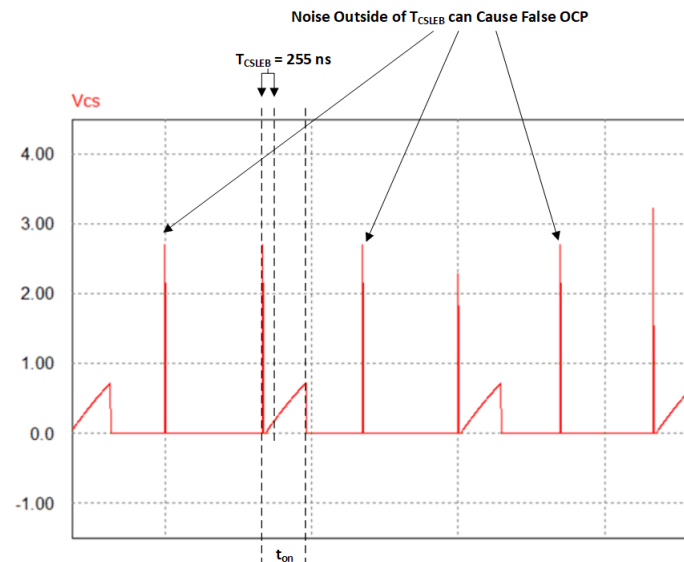


Figure 10-2. Noise Spikes Outside the T_{CSLEB} Window will Cause a False OCP Fault

To remove this fault you may have to correct your layout if it was done poorly. The data sheet of the flyback controllers have sections that give recommendations and examples on how to do layout that reader may find useful.

These noise spike may also be removed by using a low pass RC filter formed by R_{LC} and C_S presented in figure 1-1. Resistor R_{LC} is selected based on data sheet requirements and filter capacitor C_S sets the pole of the

low pass filter that can be adjusted. It is recommended that you select CS to put the filter pole at 10 times the converter's maximum frequency based on equation 25. Please note if your flyback was designed for a maximum frequency of 75 kHz and had an R_{LC} resistor of 1 k ohm would require a CS of roughly 212 pF.

$$C_S \leq \frac{1}{2 \times \pi \times 10 \times f_{sw} \times R_{LC}} = \frac{1}{2 \times \pi \times 10 \times 75 \text{ kHz} \times 1 \text{ k}\Omega} \approx 212 \text{ pF} \quad (26)$$

11 Summary

Remember when designing a DCM flyback controller that uses the transformer's aux winding for fault sensing to sample the input and output voltage for OVP and UVLO. It is critical that the aux winding waveform be as clean as possible with as little ringing on it as possible. Some designers struggle with this ringing caused by parasitic inductances and capacitances that cause false OVP or UVLO faults. As this application note showed to prevent false OVP and UVLO faults, A RCD clamp and/or a snubber across the flyback converter's output rectifier, should be used to dampen the aux winding ringing.

12 References:

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