User's Guide

BQ25620 and BQ25622 Evaluation Module

ABSTRACT

This user's guide provides detailed testing instructions for the BQ25620 and BQ25622 evaluation modules (EVM). Also included are descriptions of the necessary equipment, equipment setup, and procedures. The reference documentation contains the printed-circuit board layouts, schematics, and the bill of materials (BOM).

Throughout this user's guide, the abbreviations *EVM*, *BQ25620EVM*, BQ25622EVM, *BMS050*, and the term *evaluation module* are synonymous with the BMS050 evaluation module, unless otherwise noted.

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Trademarks

1 Introduction

The BMS050 evaluation module (EVM) is a complete charger module for evaluating the BQ25620 and BQ25622 devices. The BQ25620 and BQ25622 are I^{2}C-controlled single-cell chargers with NVDC Power Path Management, Integrated ADC, and OTG Output.

For detailed features and operation, see Table 1-1 table for a list of devices and their data sheets.

Table 1-1. Device Data Sheets

Device	Data Sheet	EVM Label
BQ25620	SLUSEG2	BQ25620EVM
BQ25622	SLUSEG2	BQ25622EVM

1.1 EVM Features

This EVM supports the following features:

- Evaluation module for the BQ25620 or BQ25622 devices.
- Narrow VDC (NVDC) power path management for powering the systems and charging the battery.
- Supports I^{2}C communication for systems configuration and status reporting.
- Test points for key signals available for testing purposes.
- Jumpers for easy configuration.
- One push-button for wake-up and reset input with adjustable timers.
- Charge status (STAT) and Power Good (PG) LEDS for charging monitoring.
- Connections for EV2400 or USB2ANY interface board controllers.

This EVM does not include the EV2400 or USB2ANY interface boards. To evaluate the EVM, an EV2400 or USB2ANY must be ordered separately.

1.2 General Descriptions

Table 1-2 lists the input and output connections available on this EVM and their respective descriptions.

Table 1-2. EVM I/O Connections

Jack	Description
J1(2) - VIN	Positive rail of the charger input voltage
J1(1) - GND	Ground
J2(1) - SYSTEM	Positive rail of the charger system output voltage, typically connected to the system load
J2(2) - GND	Ground
J3(1) - VPB	Positive rail of the charger output voltage for power bank applications in reverse boost mode (OTG). This output also shares the rail with the VIN input rail in forward buck mode
J3(2)-GND	Ground
J4(3) - BATTERY	Positive rail of the charger battery input, connected to the positive terminal of the external battery
J4(2) - ext_ts	Connection available for external thermistor if required
J4(1) - GND	Ground
J5	Input source Micro B USB port
J6	I^{2}C connector for the USB2ANY interface board
J7	I^{2}C connector for the EV2400 interface board

Table 1-3 lists the jumper and shunt installations available on this EVM and their respective descriptions.

Table 1-3. EVM Jumper Shunt and Switch Installation

Jack	Description	BQ25620 Setting	BQ25622 Setting
JP1	Not applicable	Not Installed	Not Installed
JP2	SCL pull-up rail. Not required if using EV2400 or USB2ANY	Not Installed	Not Installed
JP3	SDA pull-up rail. Not required if using EV2400 or USB2ANY	Not Installed	Not Installed
JP4	Not applicable	Not Installed	Not Installed
JP5	BQ25620EVM: Not applicable.BQ25622EVM: Connects ILIM pin resistor to ILIM pin.	Not Installed	Not Installed
JP6	BQ25620EVM: Micro B USB input D- connection to charger D- pin BQ25622EVM: Not applicable.	Installed	Installed
JP7	$\overline{PG}$ pin LED indicator connection. On $\overline{PG}$ enabled chargers, this indicates the Power Good status	Installed	Installed
JP8	STAT pin LED indicator connection. This indicates the current charger status	Installed	Installed
JP9	BQ25620EVM: Micro B USB input D- connection to charger D- pin BQ25622EVM: Not applicable.	Installed	Installed
JP10	Used to connect USB2ANY SDA and SCL lines to a power rail on the PCB.	Not Installed	Not Installed
JP11	BQ25620EVM: TS resistor divider pull-up rail to REGN. BQ25622EVM: TS resistor divider pull-up rail to TS_BIAS.	Short pins 1-2	Short pins 2-3
JP12	BQ25620EVM: Charger D+ pin and charger D- pin short connection. Connect this on D+/D- detection enabled chargers to simulate the connection of a DCP-type USB port as defined by USB BC1.2 and set IINDPM register to highest setting. BQ25622EVM: Not applicable.	Installed	Not Installed
JP13	Connect 10 kohm in parallel with TS resistor network to simulate a battery at 25 C. Disconnect if using external thermistor.	Installed	Installed
JP14	$\overline{CE}$ pin connection to ground to enable charging. When removed, $\overline{CE}$ pin pulls up to SYS through 10 kohm to disable charge	Installed	Installed
JP15	Not applicable	Not Installed	Not Installed
S1	$\overline{QON}$ control switch. Press either for exiting Shipping Mode or System Reset.	Default Off	Default Off

Table 1-4 lists the recommended operating conditions for this EVM.

Table 1-4. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
V_{VBUS}, V_{VAC}	Input voltage applied to VBUS pin	3.9		18.0	V
V_{BAT}	Battery voltage applied to BAT pin	0	4.208	4.8	V
I_{VBUS}	Input current into VBUS	0		3.2	A
I_{SW}	Output current from SW flowing to SYS pin load and battery at BAT pin			3.5	A
I_{BAT}	Fast charging current into battery at BAT pin	0		3.5	A
	Continuous RMS discharge current through internal BATFET			6	A

2 Testing Procedures

2.1 Equipment

This section includes a list of supplies required to perform tests on this EVM.

1. **Power Supplies:** Power Supply #1 (PS #1): A power supply capable of supplying 5 V at 3 A is required. While this part can handle larger voltage and current, it is not necessary for this procedure.
2. **Load #1 for simulating a battery:** 4-Quadrant Supply, Constant Voltage < 4.5 V) "Kepco" Load, BOP, 20-5M, DC 0 to ±20 V, 0 to ±3.5 A (or higher)
   Alternative Option: A 0–20V/0–3.5 A, > 30-W DC electronic load set in a constant voltage loading mode
3. **Load #2 for simulating a load at SYS or load at VBUS in reverse/OTG mode:** Electronic or Resistive Load capable sinking up to 5-A from up to 9V (or higher)
4. **Meters:** 4x "Fluke 75" multi-meters, (equivalent or better).
   Alternative Option: (2x) equivalent voltage meters and (2x) equivalent 3-A or higher rated current meters.
5. **Computer:** A Windows 10 based computer with at least one USB port and a USB cable. Must have the latest version of Battery Management Studio installed.
6. **USB-TO-GPIO Communication Kit:** EV2400 USB-based PC interface board.
7. **Software:** BQStudio software with latest .bqz file for BQ2562x provided by Texas Instruments. Download and install bqStudio from https://www.ti.com/tool/BQSTUDIO.

2.2 Hardware Setup

Use the following list to set up the EVM testing equipment:

1. Review EVM jumper connections in Table 1-3
2. Set PS #1 for 5-V DC, 2-A current limit and then turn off the supply.
3. Connect the output of PS#1 in series with a current meter to J1 (VBUS and PGND).
4. Connect a voltage meter across TP10 (VBUS) and TP31 (PGND), or across J1.
5. Turn on Load #1, set to constant voltage mode, and output to 2.5-V. Disable Load. Connect Load in series with a current meter (multimeter), ground side, to J4 (BAT and PGND) as shown in Figure 2-1 in not using a source meter with current measuring capabilities.
6. Connect a voltage meter across TP13 (BAT) and TP30 (PGND), or across J4-3 and J4-1 as in Figure 2-1
7. Connect a voltage meter across TP14 (SYS) and TP30 (PGND), or across J2-1 and J2-2 as in Figure 2-1
8. Connect a voltage meter across TP12 (PMID) or TP11 (VPB) and TP32 (PGND), or across J3-1 and J3-2 as in Figure 2-1
9. Connect the EV2400 USB interface board to the computer with a USB cable and from I2C port to J5 with the 4-pin cable as in Figure 2-1
10. Install shunts as shown in Table 1-3. Note that the shunts in Figure 2-1 are not necessarily installed per the table.

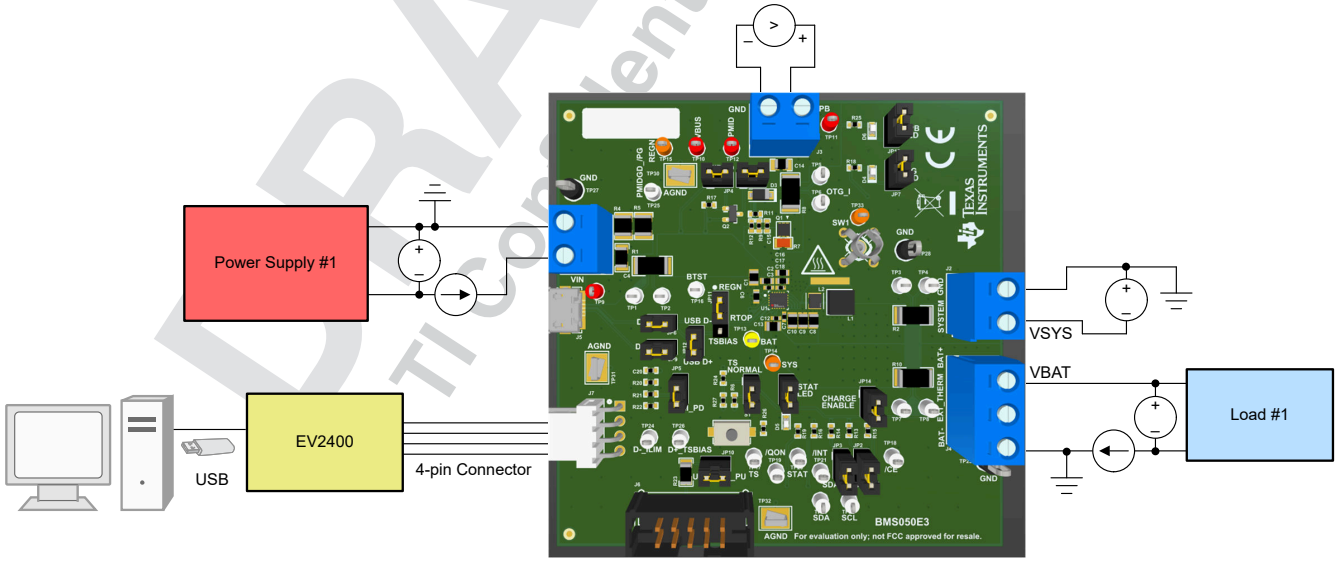


Figure 2-1. Test Setup for BQ25620EVM and BQ25622EVM

2.3 Software Setup

Use the following to set up the EVM testing software:

1. On the computer connected to the EV2400 interface board, launch Battery Management Studio (BQStudio). Select Charger as seen in Figure 2-2.

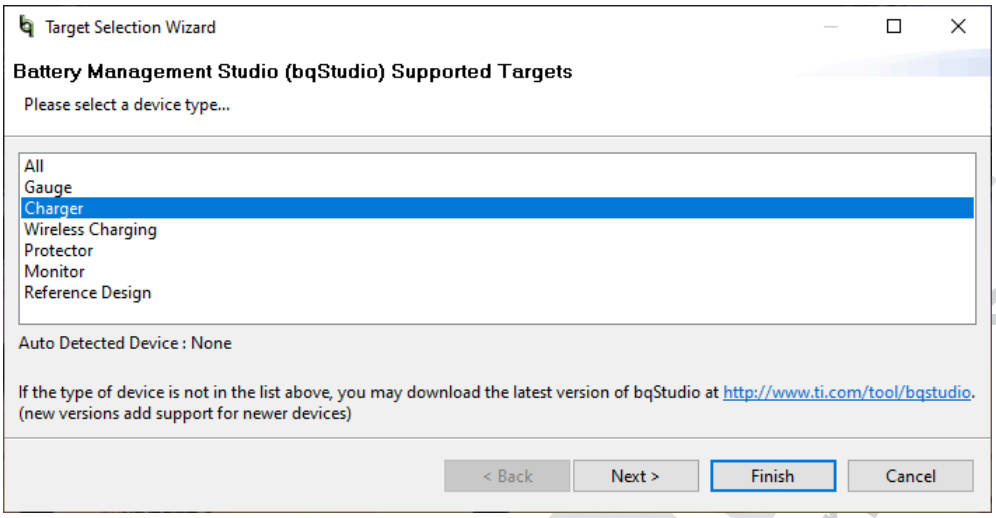


Figure 2-2. BQStudio Device Type Selection Window

2. Select the appropriate configuration file based on the device from the window shown in Figure 2-3.

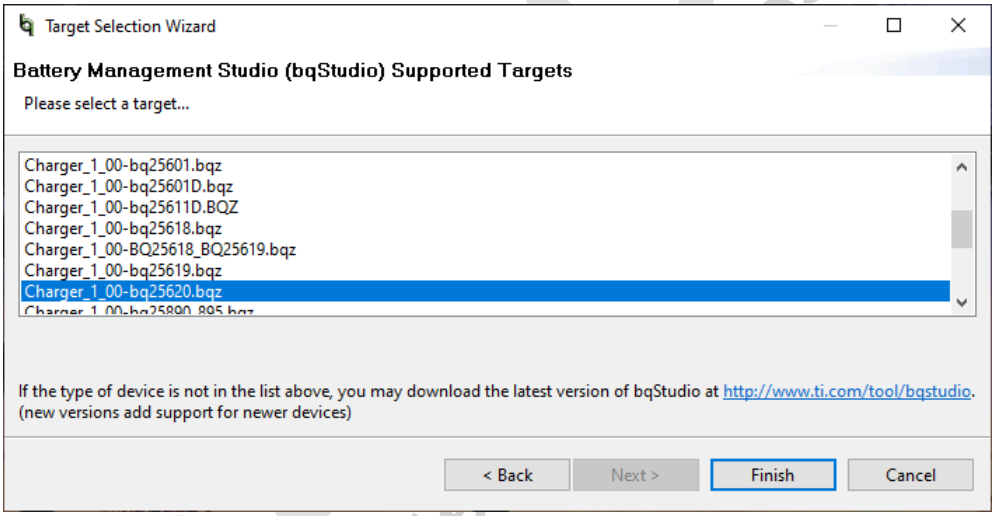
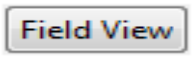


Figure 2-3. BQStudio Charger Selection Window

3. Choose 

, on the window that appears, and the main window of the BQ25620/2 EVM software will appear, as shown in Figure 2-4.

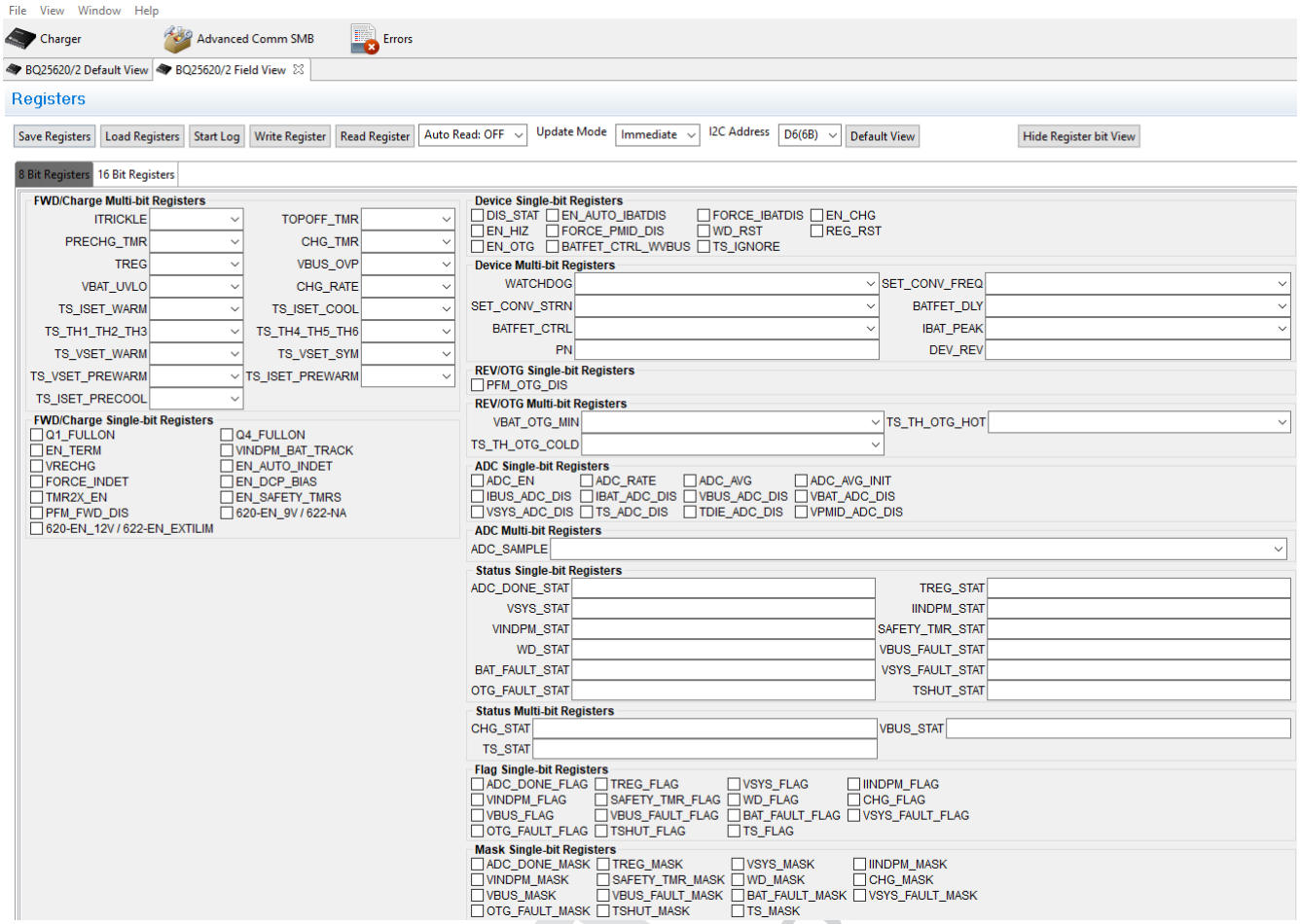


Figure 2-4. Main Window of BQ25620/2 EVM Software

2.4 Test Procedure

2.4.1 Initial Power Up

Use the following steps for enabling the EVM test setup:

1. Ensure that Section 2.2 steps have been followed.
2. Ensure that Section 2.3 steps have been followed.
3. Turn on PS #1:
   - **Measure** → V_{SYS} (SYS-TP19 and PGND-TP21) = 3.70V ±0.2V

Note

Completely disconnect Load #1 from BATTERY connections if different value is seen.

2.4.2 I²C Register Communication Verification

Use the following steps for communication verification :

1. In the EVM software, click the Read Register button
   - Verify that the GUI reads Device ACK OK in the top right corner.

Note

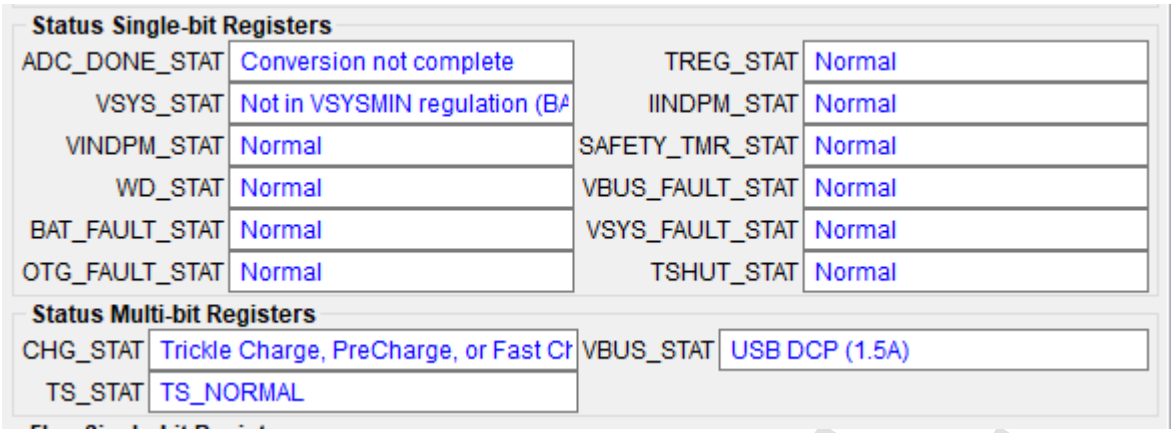
If the device reads Device ACK Error verify Section 2.2 and Section 2.4.1 steps have been followed.

2. In the Field View (see Figure 2-4), make the following changes as necessary:
   - Set WATCHDOG: Disable
   - Set VINDPM: 4200 mV
   - Set IINDPM: 500 mA
     - Note that BQ25622 ILIM pin resistor clamps the input current to 1-A unless that pin is disabled using ☐ 620-EN_12V / 622-EN_EXTILIM.
   - Set VREG: 4200 mV
   - Set ICHG: 480 mA
   - Set IPRECHG: 240 mA
   - Set VSYSMIN: 3520 mV
   - Check ☑ EN_CHG
   - Uncheck ☐ EN_TERM

2.4.3 Charger Mode Verification

Use the following steps for charger mode verification:

1. PS #1 should be on from Section 2.4.1. In the EVM software, click Read Register **twice**.
   - Verify that all Fault statuses read "Normal"



2. To confirm SYS voltage regulation, enable Load #1 (see Section 2.2) and take DMM measurements as follows:
   - **Measure** → V_{SYS} (SYS-TP14 and PGND-TP27 or TP28 or TP29) = 3.65V ±0.3V
   - **Measure** → V_{BAT} (BAT-TP13 and PGND-TP27 or TP28 or TP29) = 2.5V ±0.2V
   - **Measure** → I_{BAT} = 240mA ±50mA
3. To confirm battery charge current regulation, change Load #1 to 3.7V and take DMM measurements as follows:
   - **Measure** → V_{SYS} (SYS-TP14 and PGND-TP27 or TP28 or TP29) = 3.8V ±0.3V
   - **Measure** → V_{BAT} (BAT-TP13 and PGND-TP27 or TP28 or TP29) = 3.7V ±0.2V
   - **Measure** → I_{BAT} = 480mA ±100mA
4. To confirm input current limit operation, in the EVM software on the 16-bit tab, set fast charge current to 1040mA and then take DMM measurement (or PS #1 measurement if accurate) as follows:
   - **Measure** → I_{IN} = 500mA ±200mA

2.4.4 Boost Mode Verification

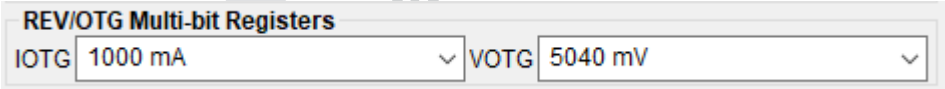
Use the following steps for boost mode verification:

1. Turn off and disconnect PS #1.
2. Set Load #1, the battery simulator, to 3.7V and 2A current limit.

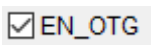
Note

If Load #1 connected from BATTERY-J4(3) to GND-J4(1) is not a four quadrant supply, remove Load #1 and use PS #1, set to 3.7V, 2A current limit and connect to BATTERY-J4(3) and GND-J4(1).

3. In the EVM software on the 16-bit tab, confirm that VOTG, the OTG regulation voltage, is set to 5.04V and IOTG, the OTG current limit, is set to 1000 mA.



4. In the EVM software on the 8-bit tab under the Device Single Bit registers, enable OTG (EN_CHG can remain enabled).



5. Connect Load #2 across VPB-J3(1) and PGND-J3(2).
6. Set Load #2 to 500mA constant current load (or resistance of 2.5 W) and the turn on the load.
7. To confirm the VOTG regulation,
   - **Measure**→ V_{BUS} = 5.04 V ± 25 mV
8. Turn off and disconnect the power supply.
9. Remove Load #2 from the connection.

2.4.5 Helpful Tips

1. The leads and cables to the various power supplies, batteries and loads have resistance. The current meters also have series resistance. The charger dynamically reduces charge current depending on the voltage sensed at its VBUS pin (using the VINDPM feature), BAT pin (as part of normal termination), and TS pin (through its battery temperature monitoring feature via battery thermistor). Therefore, voltmeters must be used to measure the voltage as close to the IC pins as possible instead of relying on the digital readouts of the power supply. If a battery thermistor is not available, that shunts JP11 and JP13 are in place.
2. When using a source meter that can source and sink current as your battery simulator, TI highly recommends adding a large (>=1000+ µF) capacitor at the EVM BATTERY and GND connector in order to prevent oscillations at the BAT pin due to mismatched impedances of the charger output and source meter input within their respective regulation loop bandwidths. Configuring the source meter for 4-wire sensing eliminates the need for a separate voltmeter to measure the voltage at the BAT pin. When using 4-wire sensing, always ensure that the sensing leads are properly connected in order to prevent accidental overvoltage by the power leads.
3. For precise measurements of input and output current, especially near termination, the current meter in series with the battery or battery simulator should not be set to auto-range and may need to be removed entirely. An alternate method for measuring charge current is to either use an oscilloscope with hall effect current probe or by a differential voltage measurement across the relevant sensing resistors populated on the BQ2526xEVM.

3 PCB Layout Guideline

Minimize the switching node rise and fall times for minimum switching loss. Proper layout of the components minimizing high-frequency current path loop is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. This PCB layout priority list must be followed in the order presented for proper layout:

1. For lowest switching noise during forward/charge mode, place the decoupling PMID capacitor and then bulk PMID capacitor positive terminals as close as possible to PMID pin. Place the capacitor ground terminal close to the GND pin using the shortest copper trace connection or GND plane on the same layer as the IC.
2. For lowest switching noise during reverse/OTG mode, place the SYS output capacitors' positive terminals near the SYS pin. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
3. Since REGN powers the internal gate drivers, place the REGN capacitor positive terminal close to REGN pin to minimize switching noise. The capacitor's ground terminal must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
4. Place the VBUS and BAT capacitors' positive terminals as close to the VBUS and BAT pins as possible. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
5. Place the inductor input pin near the positive terminal of the SYS pin capacitors. Due to the PMID capacitor placement requirements, the inductor's switching node terminal must be via'd down with multiple via's to a second internal layer with a wide trace that returns to the SW pin with multiple vias. Using multiple vias ensures that the via's additional resistance is negligible compared to the inductor's dc resistance and therefore does not impact efficiency. The vias additional series inductance is negligible compared to the inductor's inductance.
6. Place the BTST capacitor on the opposite side from the IC using vias to connect to the BTST pin and SW node.
7. A separate analog GND plane for non-power related resistors and capacitors is not required if those components are placed away from the power components traces and planes.
8. Ensure that the I^2C SDA and SCL lines are routed away from the SW node.

Additionally, it is important that the PCB footprint and solder mask cover the entire length of each of the pins. GND, SW, PMID, SYS and BAT pins extend further into the package than the other pins. Using the entire length of these pins reduces parasitic resistance and increases thermal conductivity from the package into the board.

See the EVM design for the recommended component placement with trace and via locations.

4 Board Layout, Schematic, and Bill of Materials

4.1 Board Layout

The following figures illustrate the PCB board layers.

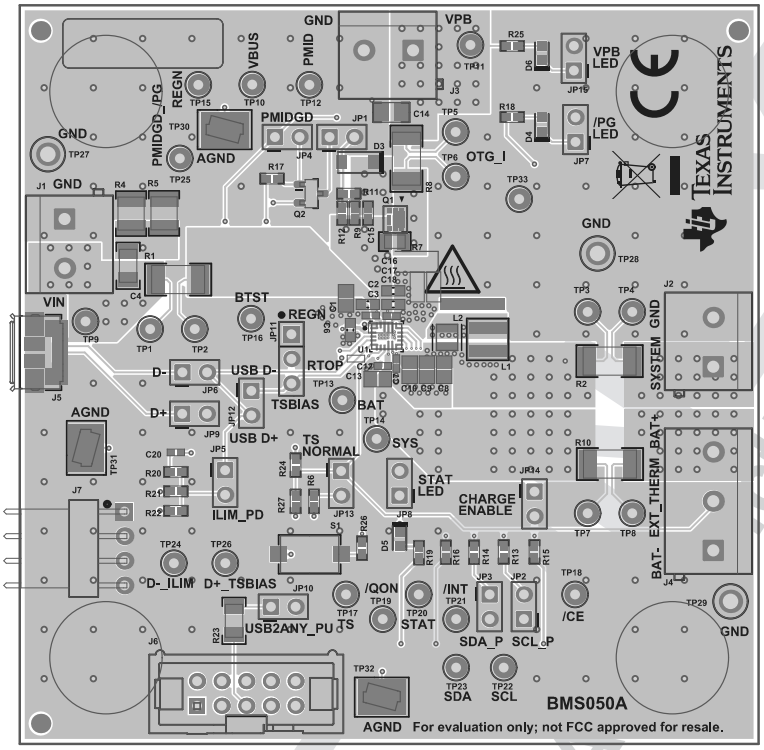


Figure 4-1. BMS050 Top Layer

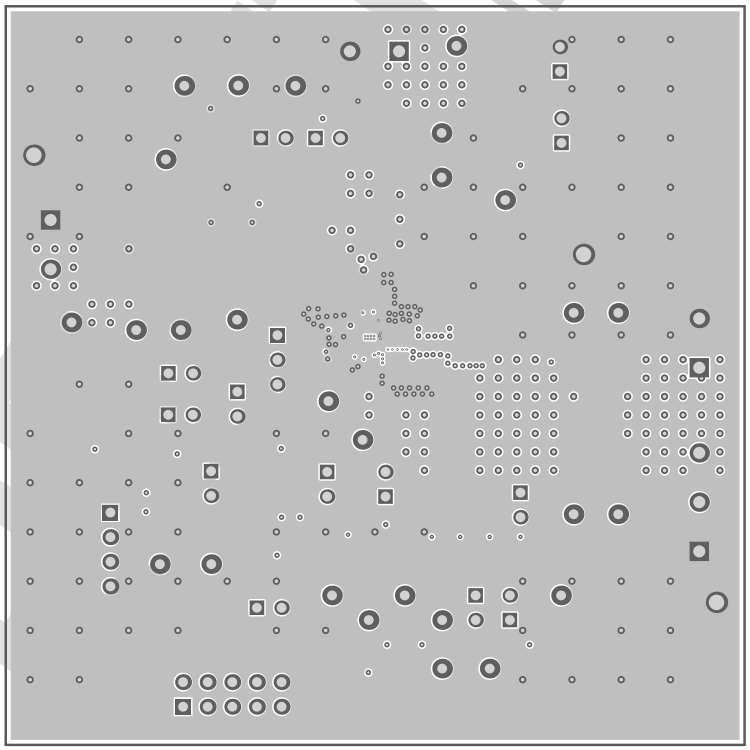


Figure 4-2. BMS050 Internal Layer 1

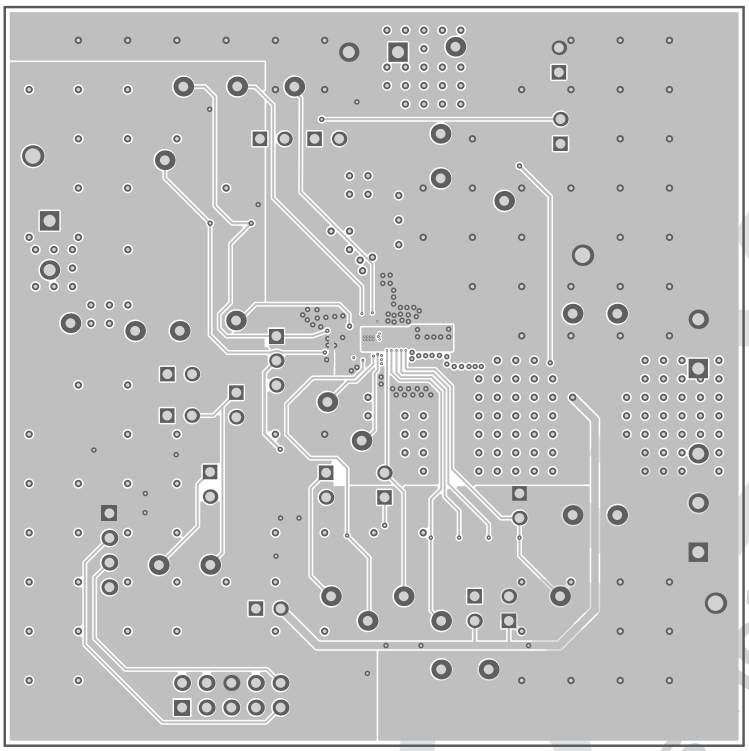


Figure 4-3. BMS050 Internal Layer 2

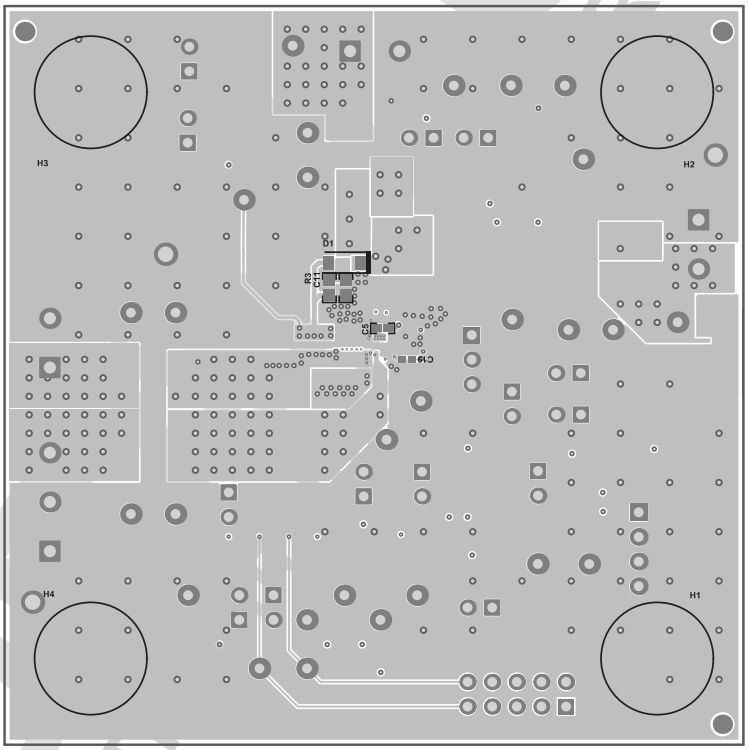


Figure 4-4. BMS050 Bottom Layer

4.2 Schematic

Figure 4-5 illustrates the schematic for the BQ25620EVM.

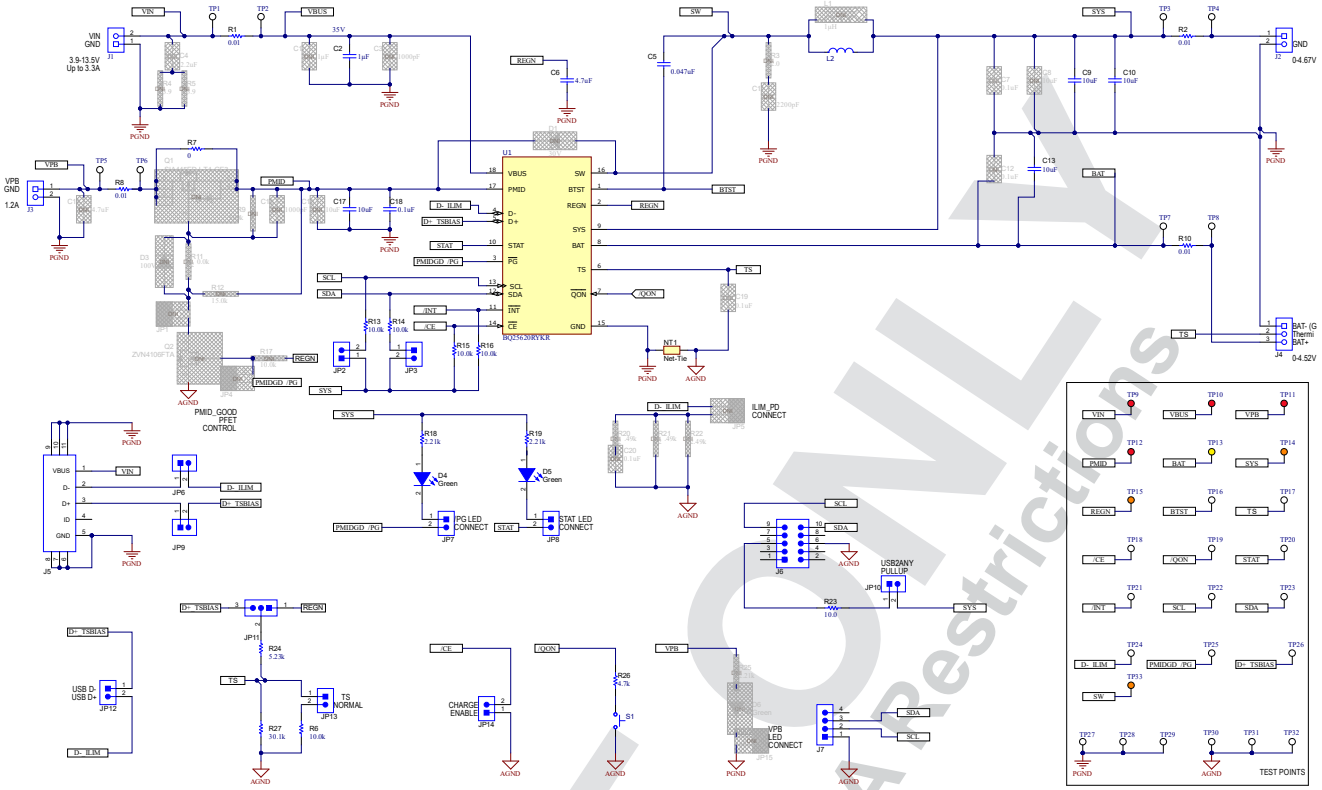


Figure 4-5. BQ25620EVM Schematic

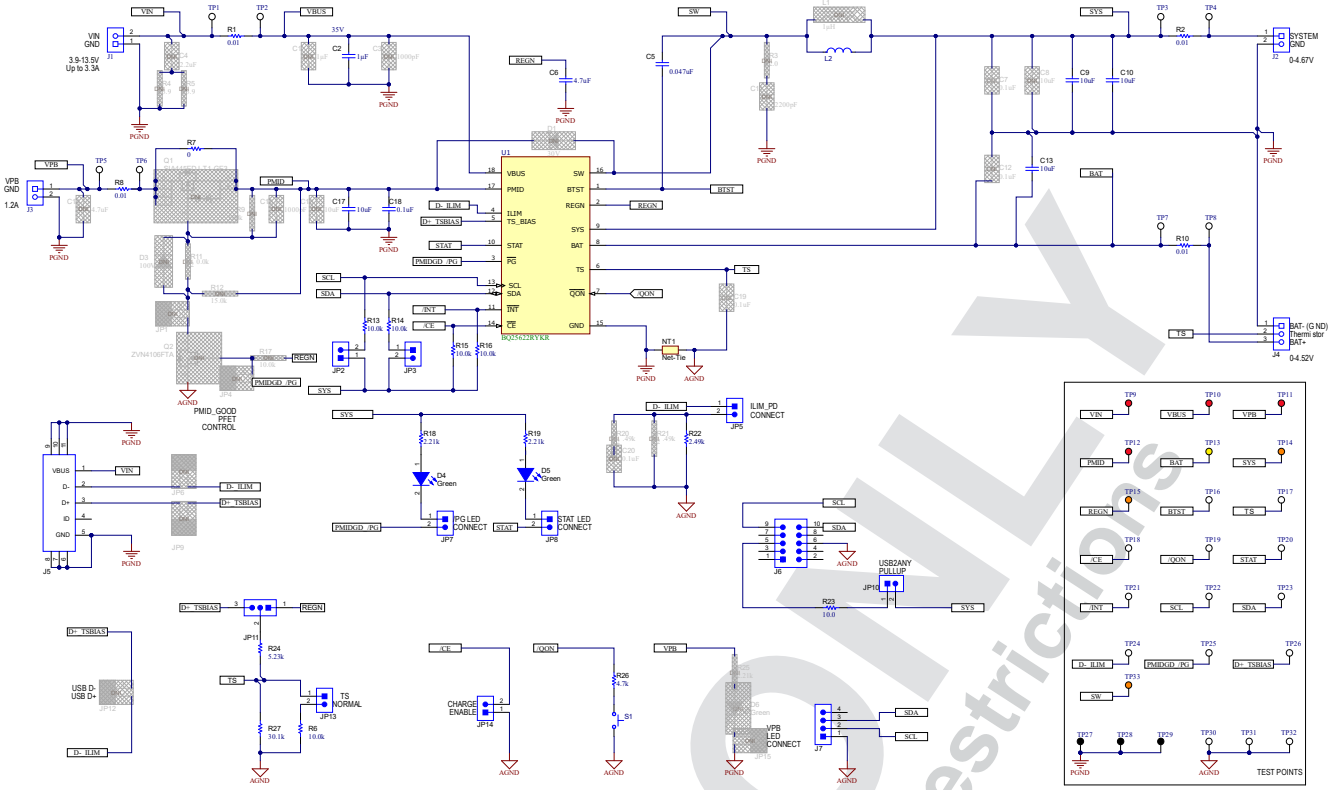


Figure 4-6. BQ25622EVM Schematic

4.3 Bill of Materials

Table 4-1 lists the BQ25620EVM BOM.

Table 4-1. BMS050 Bill of Materials

Designator	620EVM	622EVM	Value	Description	Package Reference	Part Number	Manufacturer
C2	1	1	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 0, 0603	603	GMK107AB7105KAHT	Taiyo Yuden
C5	1	1	0.047uF	CAP, CERM, 0.047 uF, 25 V, +/- 10%, X7R, 0402	402	GRM155R71E473KA88D	MuRata
C6	1	1	4.7uF	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X5R, 0603	603	GRM188R61E475KE11D	MuRata
C9, C10, C13	3	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	805	C2012X5R1E106K125AB	TDK
C17	1	1	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	603	GRT188R61E106ME13D	MuRata
C18	1	1	0.1uF	CAP, CERM, 0.1 uF, 50 V,+/- 10%, X7R, 0402	402	C1005X7R1H104K050BE	TDK
D4, D5	2	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
H1, H2, H3, H4	4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3	3	3		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J4	1	1		Terminal Block, 5.08 mm, 3x1, Brass, TH	3x1 5.08 mm Terminal Block	ED120/3DS	On-Shore Technology
J5	1	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	7.5x2.45x5mm	473460001	Molex
J6	1	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
J7	1	1		Header (friction lock), 100mil, 4x1, R/A, TH	4x1 R/A Header	22/05/3041	Molex
JP2, JP3, JP7, JP8, JP10, JP13, JP14	7	7		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions

Table 4-1. BMS050 Bill of Materials (continued)

Designator	620EVM	622EVM	Value	Description	Package Reference	Part Number	Manufacturer
JP6, JP9, JP12	3	0		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
JP5	0	1		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
JP11	1	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
L2	1	1	1uH	1µH @ 20% Shielded Molded Inductor 4.2A 42mOhm Max 1008 Isat: 4.6A (2520 Metric) -	SMT_IND_2MM0_2MM5	252012CDMCDDS-1R0MC	Sumida
R1, R2, R8, R10	4	4	0.01	RES, 0.01, 1%, 1 W, 2010	2010	WSL2010R0100FEA18	Vishay-Dale
R6, R13, R14, R15, R16	5	5	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040210K0FKED	Vishay-Dale
R7	1	1	0	RES, 0, 1%, 0.5 W, 0805	805	5106	Keystone
R18, R19	2	2	2.21k	RES, 2.21 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04022K21FKED	Vishay-Dale
R22	0	1	2.49k	RES, 2.49 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04022K49FKED	Vishay-Dale
R23	1	1	10	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8ENF10R0V	Panasonic
R24	1	1	5.23k	RES, 5.23 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04025K23FKED	Vishay-Dale
R26	1	1	4.7k	RES, 4.7 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04024K70JNED	Vishay-Dale
R27	1	1	30.1k	RES, 30.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040230K1FKED	Vishay-Dale
S1	1	1		Switch, Normally open, 2.3N force, 200k operations, SMD	KSR	KSR221GLFS	C&K Components
SH-JP2, SH-JP3, SH-JP7, SH-JP8, SH-JP10, SH-JP11, SH-JP13, SH-JP14	8	8	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec

Table 4-1. BMS050 Bill of Materials (continued)

Designator	620EVM	622EVM	Value	Description	Package Reference	Part Number	Manufacturer
SH-JP6, SH-JP9, SH-JP12	3	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
JP5	0	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	19	19		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP9, TP10, TP11, TP12	4	4		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP13	1	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP14, TP15, TP33	3	3		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
TP27, TP28, TP29	3			Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP30, TP31, TP32	3	3		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1	1	0		I2C Controlled, 3.5-A or 2-A, Maximum 17V or 18V Input, Charger with NVDC Power Path Management and OTG Output	WQFN-HR18	BQ25620RYKR	Texas Instruments
U1	0	1		I2C Controlled, 3.5-A or 2-A, Maximum 17V or 18V Input, Charger with NVDC Power Path Management and OTG Output	WQFN-HR18	BQ25622RYKR	Texas Instruments

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2022) to Revision A (November 2022) **Page**

- Added BQ25622EVM to user's guide 2

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