# TFT LCD Integrated Power Module

General Description

The SN18400P is an I2C interface programmable power management IC. The IC includes two synchronous AVDD/VGH boost converter, a two RESET function, a low dropout LDO, a VGL charge pump, a high performance VCOM with 7-bit Calibrator, 2-CH gamma, and a voltage detector. With available in a UQFN-28L 3.5x3.5 (FC) package, this device is suitable for TFT-LCD panel. The IC can operate from 2.5V to 5V input voltages. High frequency operation allows a compact PCB circuit area with small inductors and capacitor. Current-limit functions are provided for all internal-switch converters, and output-fault shutdown protects all converters against output-fault conditions. Programmable soft-start functions for all output voltage to limit input inrush current during startup.

Ordering and Marking Information

Part No.	Marking Information	Package Type
SN18400P	1Q=	UQFN-28L 3.5x3.5 (FC) (U- type)

Pin Configuration

(TOP VIEW)
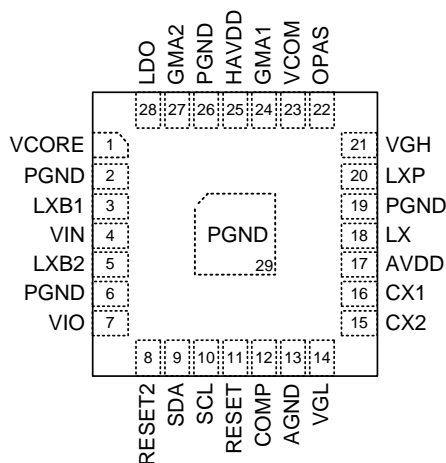
UQFN-28L 3.5x3.5 (FC)

Features

- **2.5V to 5V Input Supply Voltage**
- **I^{2}C Interface**
- **AVDD Current-Mode Sync. Boost Converter**
  - ▶ **Programmable Output Voltage 7V to 13.5V**
  - ▶ **High Efficiency (96%)**
- **Operational Amplifier**
  - ▶ **150mA Short Circuit Current**
  - ▶ **Programmable 7-Bit VCOM Calibrator**
- **Low Dropout Voltage Linear Regulator**
  - ▶ **Programmable Output Voltage 1.8V to 2.8V**
  - ▶ **100mA Maximum Output Current**
- **VCORE/VIO Programmable Sync. Buck**
- **VCORE Programmable Output Voltage 0.8V to 2V**
- **VIO Programmable Output Voltage 1V to 2.8V**
- **VGH Current-Mode Sync. Boost Converter**
- **Negative Charge Pump Regulator with Internal Switch**
  - ▶ **VGL Programmable Output Voltage −4.4V to −13V**
- **Programmable 2-CH Gamma**
- **Programmable Voltage Detector**
- **Over-Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Tablet Panels
- Notebook Panels

Typical Application Circuit

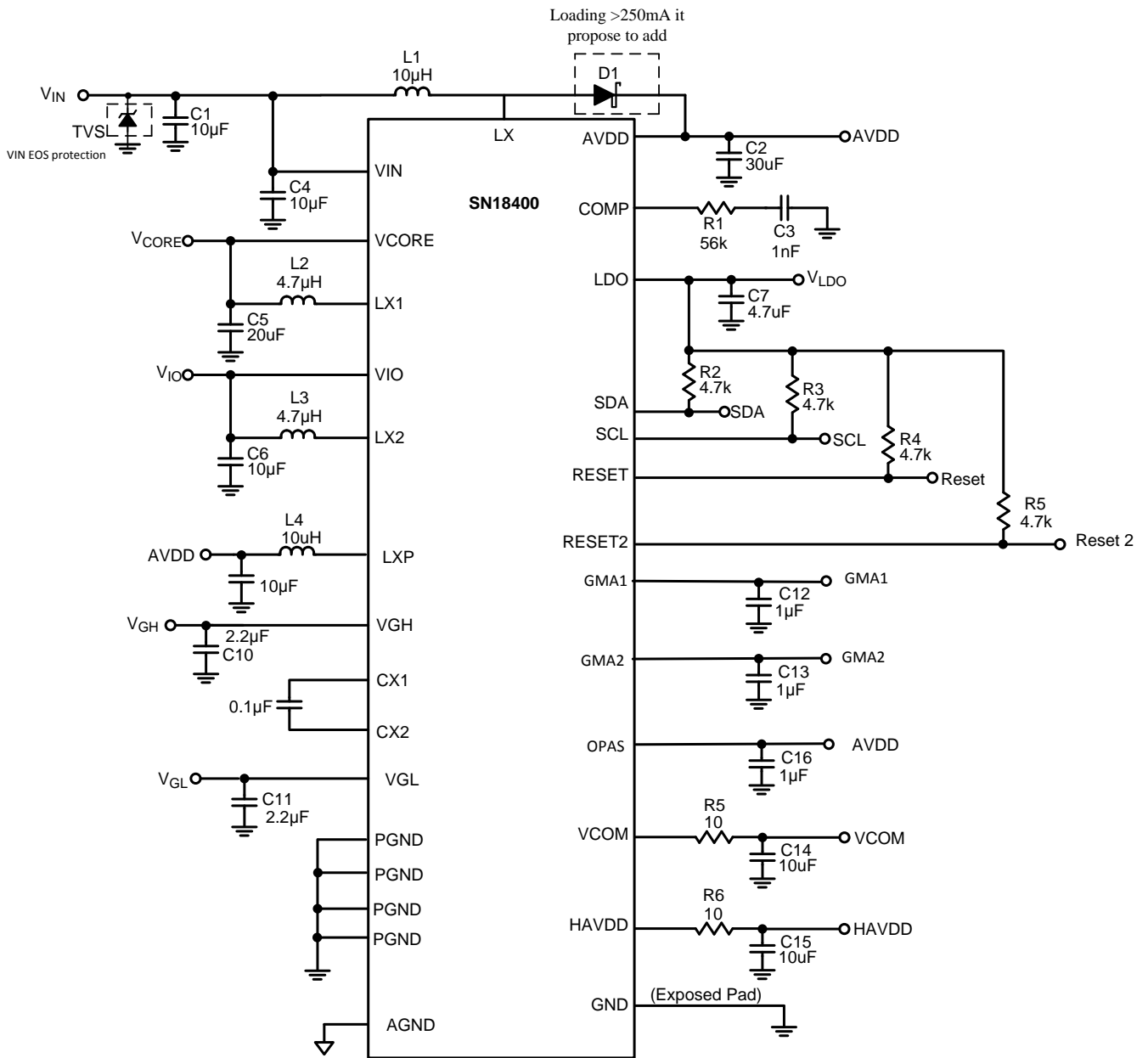Figure 1. The Application Circuit for VGL Internal

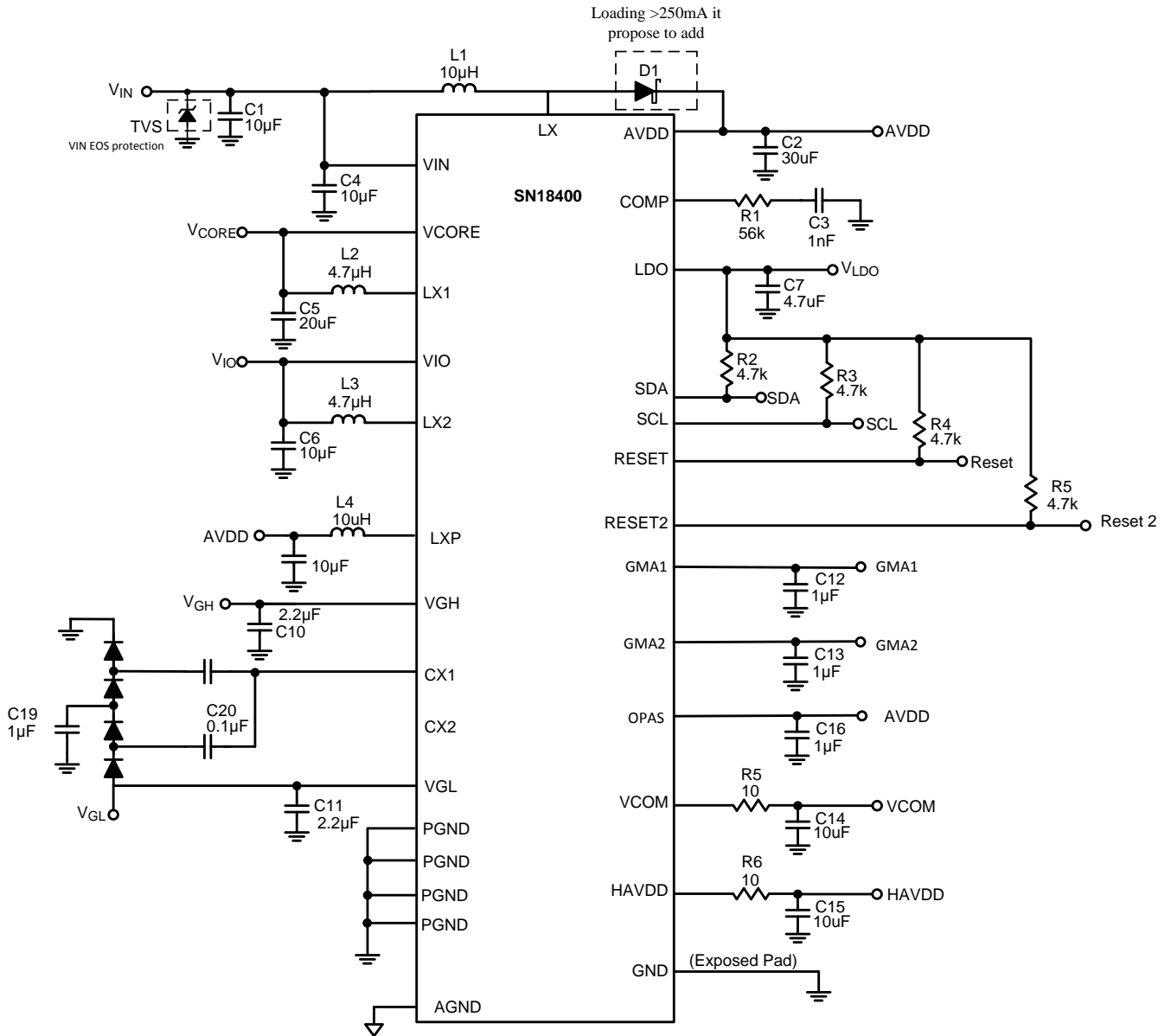|VGL = -8V| < |AVDD = 9V|

Register 0x10 Bit[7:6] = 00h (VGL > -(AVDD-0.5V))

Figure 2. The Application Circuit for V_{GL} Internal

$(|VGL = -12V| > |AVDD = 9V|)$ & $|VGL| > |VGL\ max = -13V|$

Register 0x10 Bit[7:6] = 01h $(-13V \leqq VGL \leqq -(AVDD - 0.5V))$

Figure 3. The Application Circuit for V_{GL} External Diode

$(|VGL = -18V|>|AVDD = 9V|)>|VGL max = -13V|$

Register 0x10 Bit[7:6] = 10h (VGL< −13V)

Timing Diagram

Power On/Off Sequence
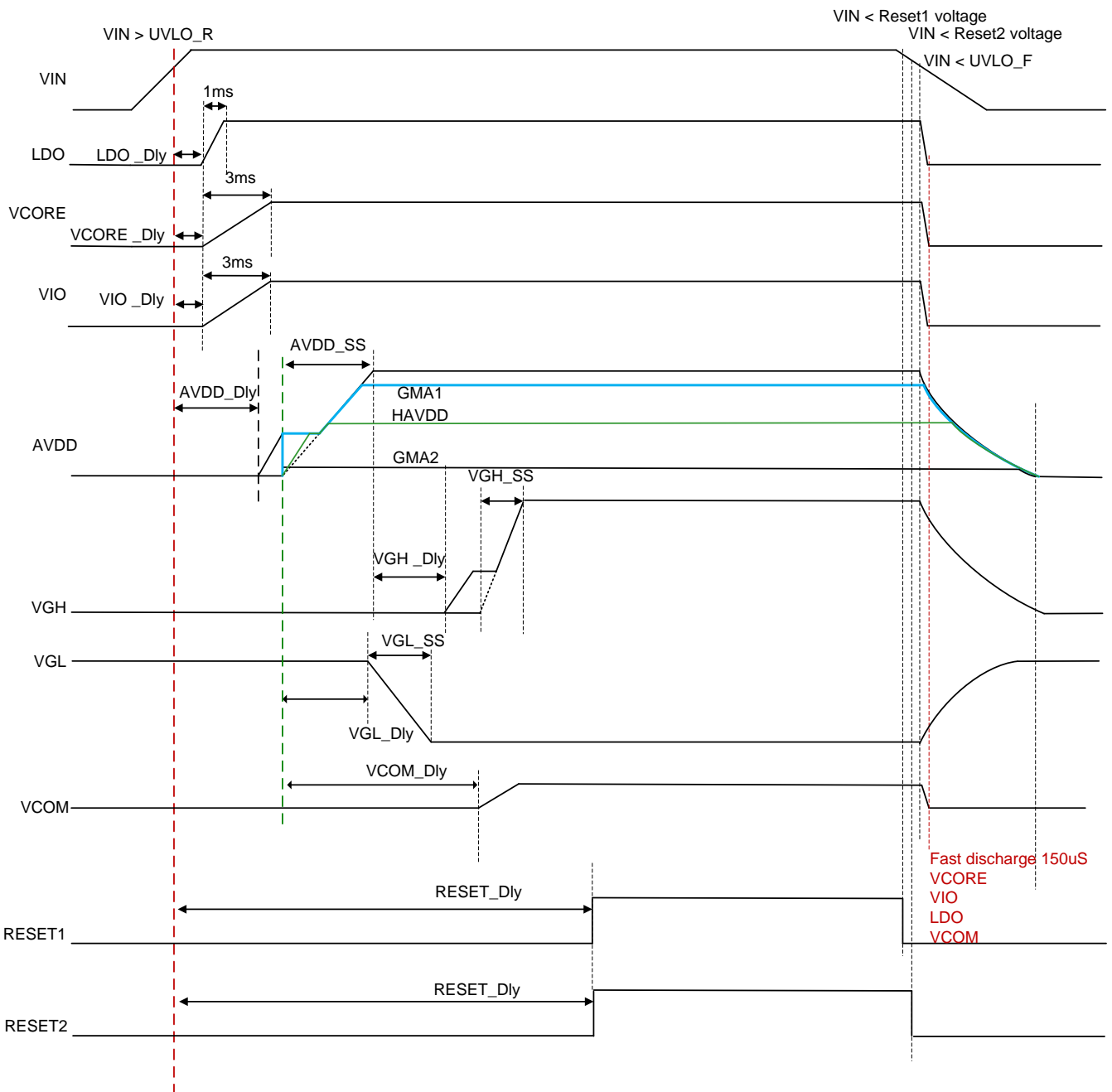
Note :

1. HAVDD/GAM1/GAM2 can power on with AVDD, but the voltage level can't be higher than AVDD

2. AVDD power on sequence : imbedded MOS for AVDD isolation.

3. VCOM power on delay time range : ~155ms, Power off VCOM to GND in 1ms.

Functional Pin Description

Pin No.	Pin Name	I/O/P	Pin Function
1	VCORE	I	Buck VCORE output feedback.
2	PGND	P	Power ground.
3	LXB1	P	VCORE buck switching node.
4	VIN	P	IC supply voltage input.
5	LXB2	P	VIO buck switching node.
6	PGND	P	Power ground.
7	VIO	I	Buck VIO output feedback.
8	RESET2	O	Output of voltage detector function.
9	SDA	I/O	Serial data input/output for I2C interface.
10	SCL	I	Clock input for I2C interface.
11	RESET1	O	Output of voltage detector function.
12	COMP	O	AVDD boost converter compensation input.
13	AGND	P	Analog ground.
14	VGL	O	VGL charge pump output voltage.
15	CX2	O	VGL charge pump flying cap node2.
16	CX1	O	VGL charge pump flying cap node1.
17	AVDD	O	Output of AVDD Boost Converter
18	LXA	P	Switching pin of AVDD boost converter
19	PGND	P	Power ground.
20	LXP	O	VGH switching node.
21	VGH	O	Output of VGH boost converter.
22	OPAS	I	Power of OP amplifier.
23	VCOM	O	VCOM OP-amp output.
24	GMA1	O	Gamma1 output pin.
25	HAVDD	O	HAVDD output pin.
26	PGND	P	Power ground.
27	GMA2	O	Gamma2 output pin.
28	LDO	O	LDO output.
29 (Exposed Pad)	PGND	P	GND. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Note : P : power/ground; I : Input; O : Output; I/O : Bi-direction

Functional Block Diagram
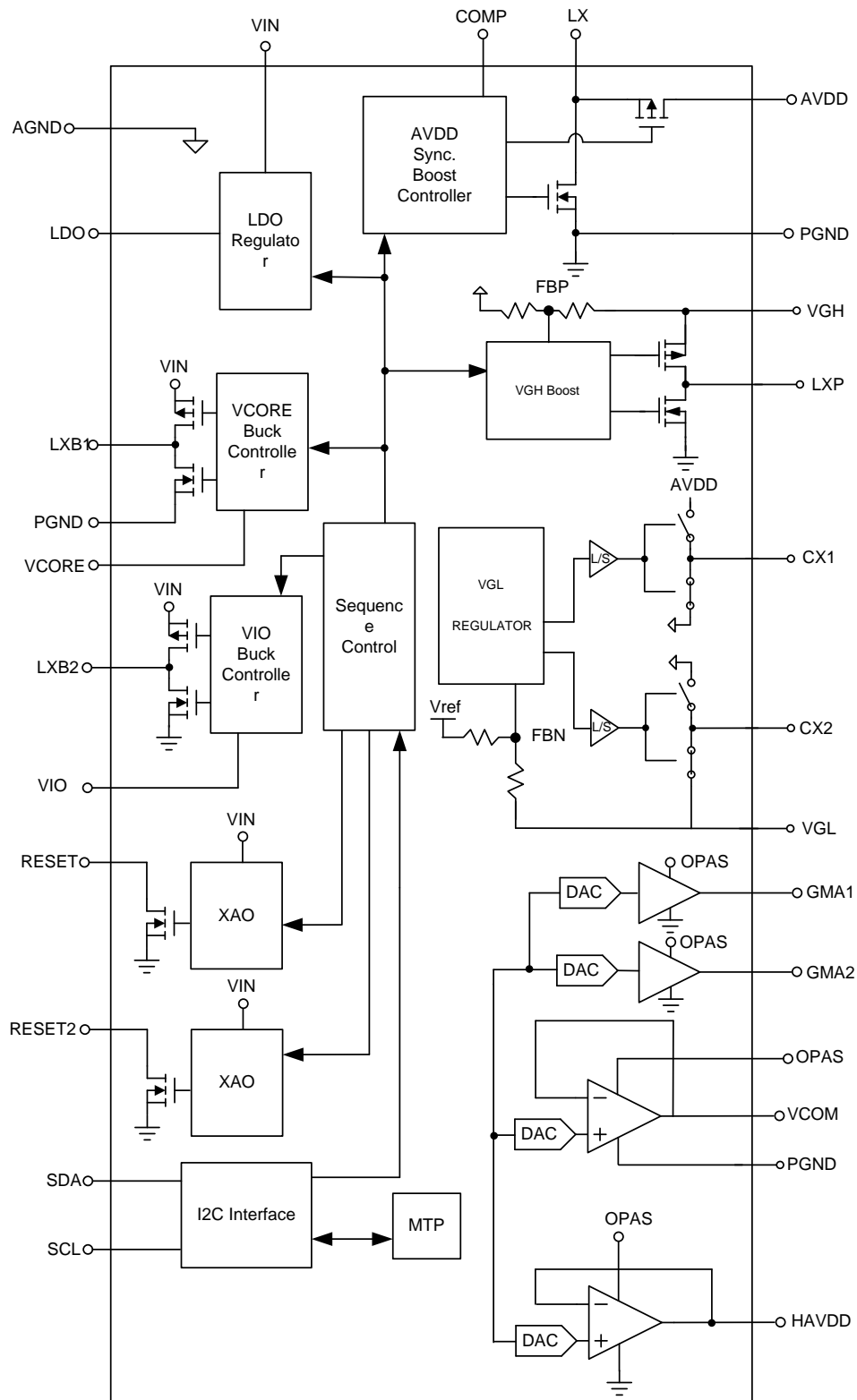
Absolute Maximum Ratings   (Note 1)

- VIN to GND -- 0.3V to 6V
- PGND, AGND to GND -- ±0.3V
- COMP, RESET1, LDO, GMA2 to GND--- −0.3V to 6V
- SCL, SDA to GND --- −0.3V to 6V
- RESET2, VCORE, VIO to GND -- −0.3V to 6V
- LXB1, LXB2 to PGND   -- −0.3V to 6V
- AVDD, LX, CX1, OPAS to PGND --- −0.3V to 15V
- VCOM, GMA1, HAVDD to AVDD --- 0.3V to (AVDD + 0.3V)
- VGL, CX2 to PGND   -- −14V to 0.3V
- VGH, LXP to PGND --- −0.3V to 35V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-28L 3.5x3.5 (FC) -- 3.2W
- Package Thermal Resistance   (Note 2)
  UQFN-28L 3.5x3.5 (FC), θ_{JA} --- 31.2°C/W
  UQFN-28L 3.5x3.5 (FC), θ_{JC} --- 2.2°C/W
- Storage Temperature Range --- −65°C to 150°C
- Lead Temperature (Soldering, 10 sec.)--- 260°C
- ESD Susceptibility   (Note 3)
  HBM (Human Body Mode) --- 2kV/

Recommended Operating Conditions   (Note 4)

- Supply Input Voltage, VIN--- 2.5V to 5V
- Ambient Temperature Range--- −40°C to 85°C
- Junction Temperature Range -- −40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.3V, AVDD = 9V, V_{CORE} = 1.2V, VIO = 1.8V, VLDO = 2.5V, VGH = 22V, VGL = −8V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Range	V_{IN}		2.5	--	5	V
VIN Quiescent Current	I_{IN}	SW not switching	--	2.5	--	mA
		SW switching	--	5.5	--	mA
VIN Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	--	2.3	--	V
		Hysteresis	--	0.4	--	
Sync. Boost Converter ---AVDD						
Output Voltage Range	AVDD	0.1V/step	7	--	13.5	V
Output Voltage Accuracy	$V_{ACC\text{-}AVDD}$	AVDD = 9V	−1	--	1	%
Switching Frequency Range	f_{OSC_AVDD}		600	--	1225	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switch Frequency Accuracy		f_{SW} = 715kHz	680	--	750	kHz
		others setting	−10	--	10	%
UVP Fault Delay	t_{FDT_AVDD}	Trigger base on UVP	--	60	--	ms
Output Current Ability			250	--	--	mA
LX Leakage Current	I_{LX}	VLX = 15V	--	1	5	μA
Over Current Protection		Programmable Current Limit (0.5A, 1A, 1.5A,2A), 1A as Default, 2Bits	--	1.5		A
Sync. Boost Converter ---VGH						
Output Voltage Range	V_{GH}	1V/step	10	--	34	V
Output Voltage Accuracy	$V_{ACC-VGH}$	VGH = 22V	−3	--	3	%
Switching Frequency Range			600	--	1225	kHz
Switch Frequency Accuracy		f_{SW} = 715kHz	680	--	750	kHz
		others setting	−10	--	10	%
Output Current Ability			30	--	--	mA
UVP Fault Delay	t_{FDT_VGH}	Trigger base on UVP	--	60	--	ms
LXH Leakage Current		VLXP = 35V	--	1	20	μA
Over Current Protection			--	0.7	--	A
Negative Charge-Pump Regulator ---VGL						
Output Voltage Range	V_{GL}	0.1V/step	−13	--	−4.4	V
Output Voltage Accuracy	$V_{acc-VGL}$	VGL = −8V	−3	--	3	%
Switching Frequency Range	f_{OSC_VGL}		0.5 x AVDD LX Freq.	--	AVDD LX Freq.	kHz
Output Current Ability		AVDD - VGL = 0.5V, Fly Cap = 0.1μF	20	--	--	mA
UVP Fault Delay Duration to IC Shutdown	t_{FDT_VGL}	Trigger base on UVP	--	60	--	ms
Line Regulation		V_{IN} = 2.5 to 5V	−0.3	--	0.3	%/V
Sync. Buck Converter ---VCORE						
Output Voltage Range	V_{CORE}	50mV/step	0.8	1.2	2	V
Output Voltage Accuracy	$V_{ACC-VCORE}$	V_{CORE} = 1.2V	−1	--	1	%
Switching Frequency Range			600	--	1225	kHz
Switch Frequency Accuracy		f_{SW} = 715kHz	680	--	750	kHz
		others setting	−10	--	10	%
UVP Fault Delay Duration to IC Shutdown	t_{FDT_VCORE}	Trigger base on UVP	--	60	--	ms
Output Current Ability			300	--	--	mA
Line Regulation		VIN = 2.5 to 5V	−0.3	--	0.3	%/V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LXB1 Leakage Current		VLXB1 = 3.3V and 0V	--	1	5	μA
Over Current Protection			--	1.2	--	A
Sync. Buck Converter ---VIO						
Output Voltage Range	V_{IO}	50mV/step	1	1.8	2.8	V
Output Voltage Accuracy	$V_{ACC\text{-}VIO}$	VIO = 1.8V	−1	--	1	%
Switching Frequency Range	f_{OSC_VIO}		600	715	1225	kHz
Switch Frequency Accuracy		f_{SW} = 715kHz	680	--	750	kHz
		others setting	−10	--	10	%
UVP Fault Delay Duration to IC Shutdown	t_{FDT_VIO}	Trigger base on UVP	--	60	--	ms
Output Current Ability			250	--	--	mA
Line Regulation		VIN = 2.5 to 5V	−0.3	--	0.3	%/V
LXB2 Leakage Current		VLXB2 = 3.3V and 0V	--	1	5	μA
Over Current Protection			--	1.2	--	A
Low Drop Output Regulator--LDO						
LDO Output Voltage	V_{LDO}	100mV/step	1.8	--	2.8	V
Output Voltage Accuracy		VLDO = 2.5V	−1	--	1	%
Output Current Ability			100	--	--	mA
UVP Fault Delay	t_{FDT_LDO}	Trigger base on UVP	--	60	--	ms
Over Current Protection			--	200	--	mA
HAVDD Output						
OPPWR Quiescent Current	I_{OPPWR}		--	2.5	--	mA
Output Voltage Range	VHAVDD	50mV/Step	3.5	--	6.5	V
Output Peak Current		Source = short to GND; sink = short to AVDD	--	250	--	mA
Output Source and Sink Current			--	75mA	--	mA
-3dB Bandwidth		R_L = 10kΩ, C_L = 10pF, Buffer configuration	--	10	--	MHz
Gain-Bandwidth Product		R_L = 10kΩ, C_L = 10pF, Buffer configuration	--	5	--	MHz
Integral Non-Linearity	INL	V_{OUT} = 3.5V to 6.5V	--	1	--	LSB
Differential Non-Linearity	DNL	V_{OUT} = 3.5V to 6.5V	--	1	--	LSB
Programmable V_{COM} and Output Buffer---D-VCOM						
Output Voltage Range	VCOM	20mV/step	1.5	--	6.2	V
Input Offset Voltage	VOS	VCOM = 3.7V	−15	--	15	mV
Input Bias Current			−100	--	100	nA
Soft start time		0V to 3.7V	--	3	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Peak Current	I_{VCOM_PC}	Unit gain source = short to AVDD, sink = short to GND	--	250	--	mA
Output Voltage Swing High	VOH	VNEG = GND, I_{OUT}= 100μA	AVDD − 0.03	AVDD − 0.005	--	V
		VNEG = GND, I_{OUT} = 75mA	AVDD − 1.9	AVDD − 1.5	--	V
Output Voltage Swing Low	VOL	VNEG = OPAS, I_{OUT} = 100μA	--	GND + 0.005	GND + 0.03	V
		VNEG = OPAS, I_{OUT} = 75mA	--	GND + 1.5	GND + 1.9	V
-3dB Bandwidth	-3dB	R_L = 10kΩ, C_L = 10pF, Buffer configuration	--	10	--	MHz
Gain-Bandwidth Product		R_L = 10kΩ, C_L = 10pF, Buffer configuration	--	5	--	MHz
Integral Non-Linearity	INL	Unit Gain, VCOM = 1.5 to 6.2V	--	1	--	LSB
Differential Non-Linearity	DNL	Unit Gain, VCOM = 1.5 to 6.2V	--	1	--	LSB
GMA1&GMA2 Output						
GMA1 Output Voltage Range	GMA1	5bit 50mV/step	AVDD − 1	--	AVDD − 0.1	V
GMA2 Output Voltage Range	GMA2	5bit 50mV/step	0.1	--	1	V
Output Current Ability			1	--	--	mA
GMA1 Output Voltage Swing High		I_{OUT} = 1mA	AVDD − 0.2	--	--	V
GMA2 Output Voltage Swing Low		I_{OUT} = 1mA	--	--	GND + 0.2	V
Programmable VCOM Calibrator						
Resolution		10mV/step	7	--	--	Bit
Integral Nonlinearity Error			--	1	--	LSB
Differential Nonlinearity Error			--	1	--	LSB
Voltage Detector---RESET1 / RESET2						
Detecting Voltage Range	V_{DET}	0.1V/step	2	2.2	2.7	V
Detecting Voltage Accuracy	$V_{acc-VDET}$		-2	-	+2	%
I2C interface---SDA,SCL						
Clock Frequency, SCL	f_{SCL}		0.2	400	1000	kHz
High Level Input Voltage	V_{IH}	SDA, SCL	1.2	--	--	V
Low Level Input Voltage	V_{IL}	SDA, SCL	--	--	0.4	V
Data Setup Time	$t_{SU.DAT}$		100	--	--	ns
Data Hold Time	$t_{HD.DAT}$		0	--	300	ns
SDA and SCL Rise Time	t_R		20 + 0.1CB	--	200	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA and SCL Fall Time	t_F		20 + 0.1CB	--	200	ns
SDA and SCL Input Capacitance			--	5	--	pF
Start Condition of Setup Time	$t_{SU.STA}$		0.25	--	--	μs
Start Condition of Hold Time	$t_{HD.STA}$	10% of SDA to 90% of SCL	0.25	--	--	μs
SDA_ACK on Voltage			--	--	0.4	V
I2C Input Filter Spike Suppression	t_{SP}		--	--	50	ns
Bus Free Time Between Stop to Start	t_{BUF}		0.5	--	--	μs
Clock Pulse Width Low	t_{LOW}		1.3	--	--	μs
Clock Pulse Width High	t_{HIGH}		0.6	--	--	μs
Bus Free Time Between Stop	$t_{SU.STO}$		0.6	--	--	μs
Clock Low to Data Out Valid	t_{AA}		0.1	--	0.9	μs
Data Out Hold Time	t_{DH}		50	--	--	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.
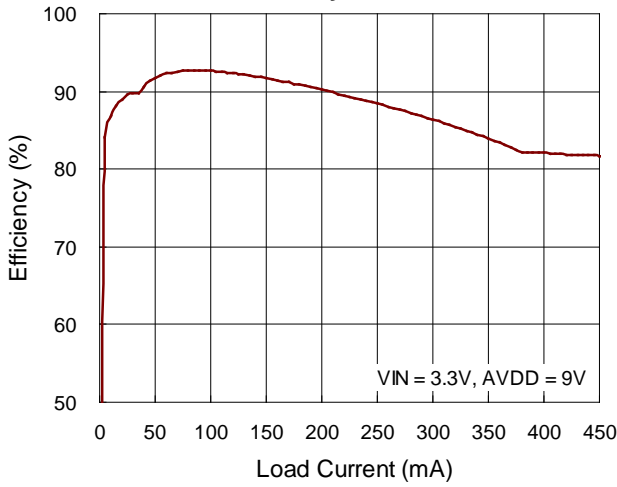
Note 4. The device is not guaranteed to function outside its operating conditions.
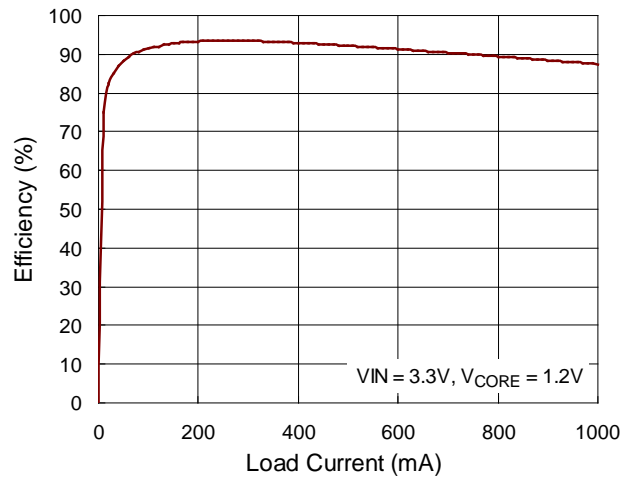
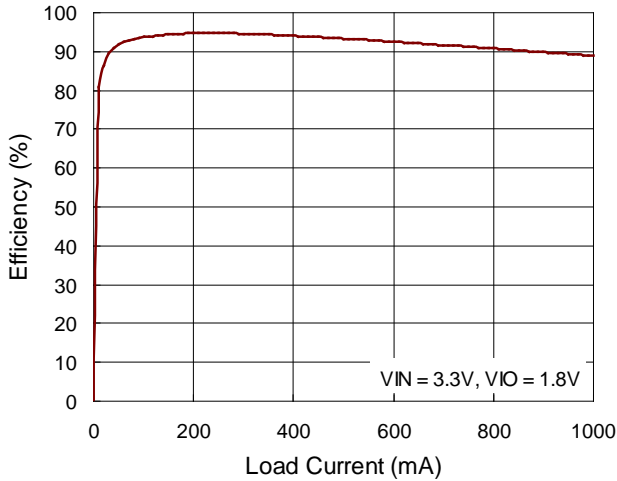**I2C Bus Timming :**
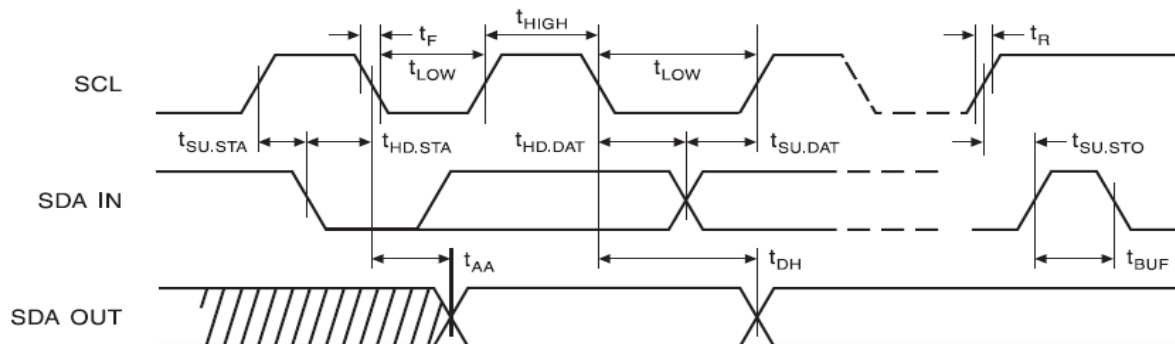
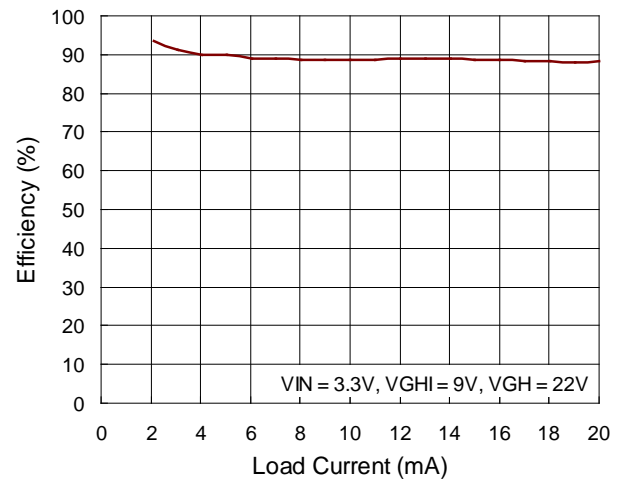## Typical Operating Characteristics

AVDD Efficiency vs. Load Current

VIN = 3.3V, AVDD = 9V

V_CORE Efficiency vs. Load Current

VIN = 3.3V, V_CORE = 1.2V

VIO Efficiency vs. Load Current

VIN = 3.3V, VIO = 1.8V

VGH Efficiency vs. Load Current
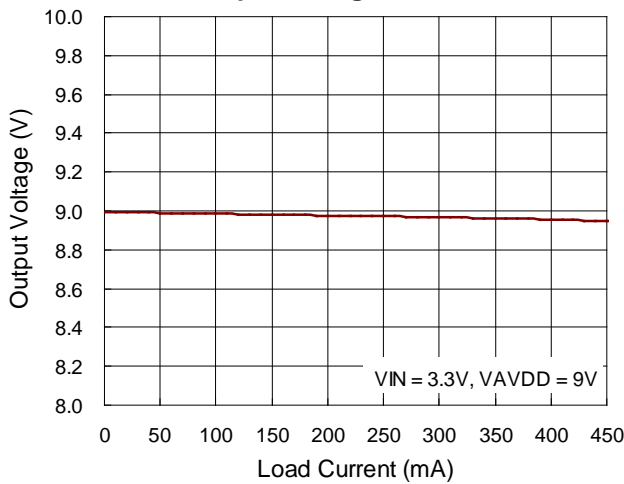
VIN = 3.3V, VGHI = 9V, VGH = 22V

AVDD Output Voltage vs. Load Current
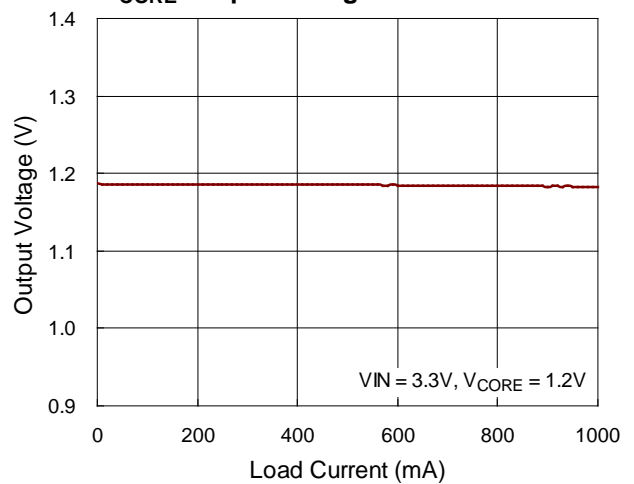
VIN = 3.3V, VAVDD = 9V

V_CORE Output Voltage vs. Load Current

VIN = 3.3V, V_CORE = 1.2V

VIO Output Voltage vs. Load Current

VIN = 3.3V, VIO = 1.8V

LDO Output Voltage vs. Load Current

VIN = 3.3V, VLDO = 2.5V

VGH Output Voltage vs. Load Current

VIN = 3.3V, VGHI = 9V, VGH = 22V

VGL Output Voltage vs. Load Current

VIN = 3.3V, AVDD = 9V, VGL = −8V

Power On

Time (10ms/Div)

Power Off

Time (10ms/Div)

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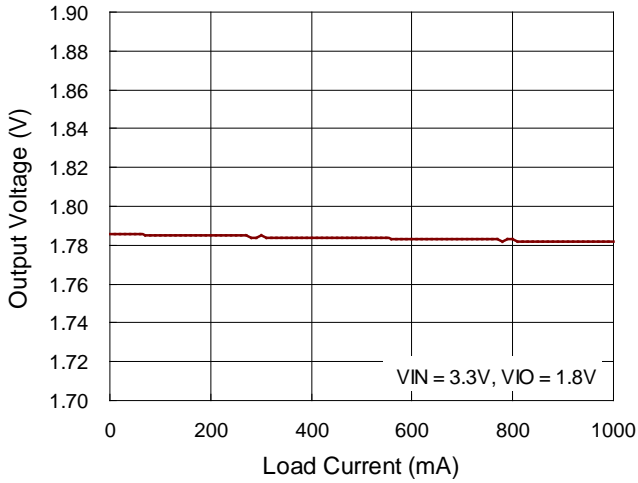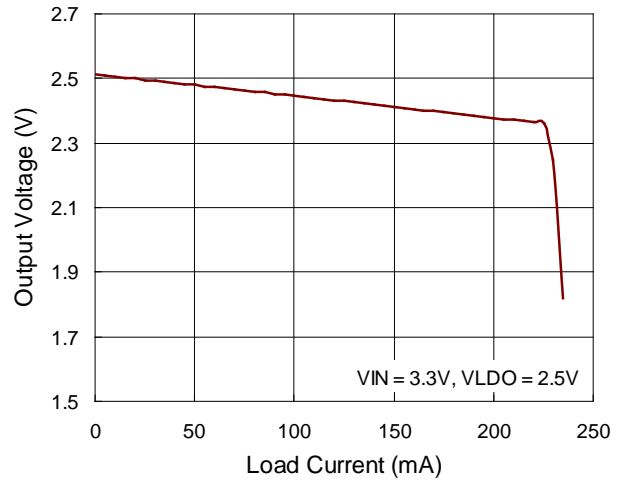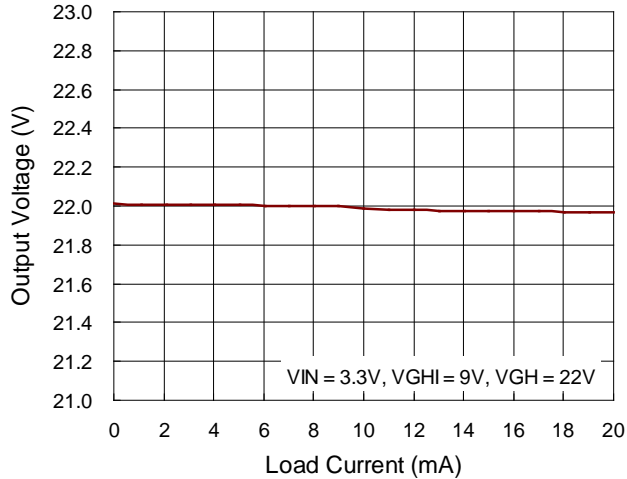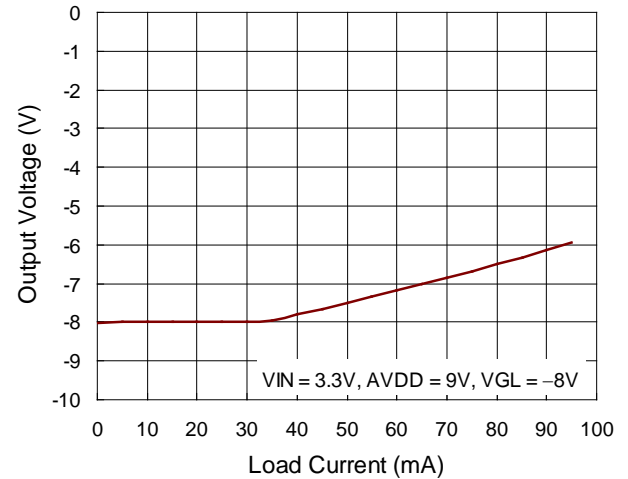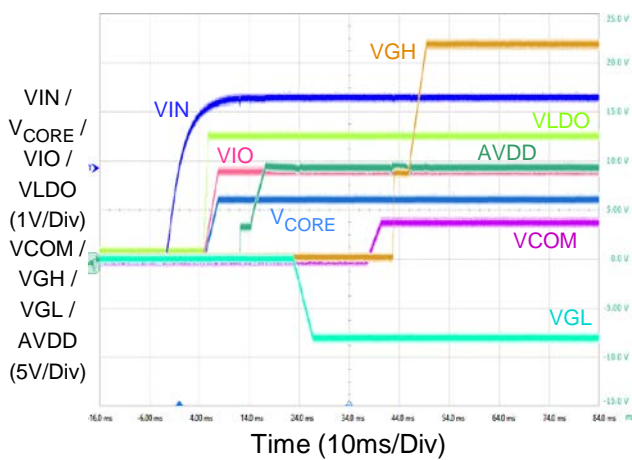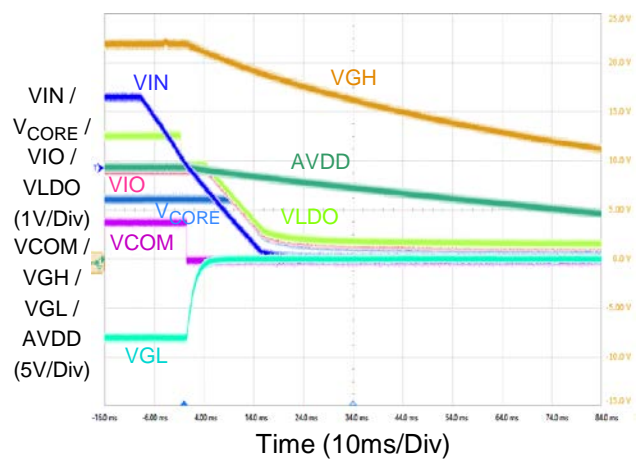
Applications Information

The SN18400P is a programmable multi-functional power solution with an I^{2}C interface for TFT LCD panel, and it can support general panel application. The SN18400P contains a AVDD synchronous boost converter, NAVDD negative charge pump with internal switch, a VGH synchronous boost converter, two digital (VCOM/HAVDD) operational amplifier, a high performance operation amplifier, and voltage detector. All channels of converters can be used to program such as output voltage, power on sequence and switching frequency of converter, and to disable each output channel selection.

AVDD Synchronous Boost Converter

The AVDD synchronous Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to generate voltage of source driver supplies for TFT-LCD display. The high operation frequency allows the use of smaller components to minimize the thickness of the LCD panel. The output voltage is controlled by a 7-bit register with 128 steps. The error amplifier varies the COMP voltage by sensing the AVDD pin to regulate the output voltage.

AVDD Switching Frequency Setting

The switching frequency of AVDD sync-boost converter is set by the I^{2}C interface. It has a 3-bit register with 6 steps. The switching frequency range is from 600kHz, 715kHz, 800kHz, 933kHz, 1MHz, 1.225MHz. The switching frequency default value is 715kHz (0x01). Please refer to the register map for details.

AVDD Slew Rate Setting

The AVDD sync-boost converter has a LX slew rate control function to optimize the efficiency and EMI performance. The slew rate range is from Slow, Normal, Fast, Fastest. The slew rate default value is Normal (0x10). Please refer to the register map for details.

AVDD Output Voltage Setting

The AVDD output voltage is set by I^{2}C interface. User can write the 03h[6:0] register to set AVDD output voltage. It has 7 bits for output voltage adjustable, the setting range is from 7V to 13.5V, and each voltage

step is about 100mV. The default voltage of AVDD is 9V (0x14). Please refer the register map for detail on how to adjust the output voltage.

AVDD Soft-start time Setting

The AVDD sync-boost converter has an integrated soft-start function to reduce the input inrush current of power on. The soft-start time is setting through the 0Fh[4:3] register by the I^{2}C interface. It has a 2-bit register with 4 steps. The soft-start time setting range is from 5ms to 20ms, and each step change is about 5ms. The soft-start time default value is 5ms (0x00). The soft- start time is defined from the AVDD voltage start rising to AVDD voltage ready. Please refer to Timimg Diagram, and register map for details.

AVDD Power-on Delay Time Setting

The AVDD sync-boost converter has integrated a power-on delay function. The delay time is adjustable by I^{2}C interface. It has 3 bits of 0Fh[2:0] register in 8 steps. The delay time setting range is from 0ms to 35ms, and each steps time is about 5ms. The delay time default value is 10ms (0x02). The delay time is defined from the VIN rising over UVLO to AVDD output voltage starting rising. Please refer the Timimg Diagram, and register map for detail.

AVDD Current Limit

The SN18400P can limit the peak current to achieve over-current protection. The IC senses the inductor current of on period that is flowing into LX pin. The typical value of the current limit is 1A. The internal N-MOSFET will be turned off if the peak inductor current reaches 1A, so that the output current at current limit boundary is denoted as $I_{OUT(CL)}$ and can be calculated as shown in the following equation :

$$I_{OUT(CL)} = \eta \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η is the efficiency of the AVDD sync-boost converter, I_{CL} is the value of the current limit and T_S is the switching period.

The AVDD current limit could be set through I^{2}C interface, and writing the register 0Eh[6:5]. It has four current limit options: 0.5A to 2A. Please refer to the

register map for details.

AVDD Fault Protection

The SN18400P equips a fault conditions to shut down the IC when AVDD output voltage is below the 80% output voltage. When the internal timer starts to count and the fault condition continues about 60ms, then IC is shutdown. Once the UVLO started again, the fault protection would be released.

Sync-Boost Inductor Selection

The inductance depends on the maximum input current. The inductor ripple current range is 20% to 40% of maximum input current that is a general rule. If 40% is selected as an example, the inductor ripple current can be calculated as following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

Where η is the efficiency of the synchronous boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. Beside, the input peak current can be calculated by maximum input current plus half of inductor ripple current shown as following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can be eventually determined as following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

Where f_{OSC} is the AVDD switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Sync-Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of

two parts, one is the product of $(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT})$ and

ESR of output capacitor, another part is formed by

charging and discharging process of output capacitor. Refer to Figure 4, evaluate ΔV_{OUT1} by ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right]$$
$$\times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

Where T_S is the inverse of switching frequency and the ΔI_L is the inductor ripple current. Move C_{OUT} to left side to estimate the value of ΔV_{OUT1} as following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Then take the ESR into consideration, the ESR voltage can be determined as the following equation :

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_{OSC}}{2L} \right) \times R_{ESR}$$

Finally, the output ripple voltage ΔV_{OUT} is combined from the ΔV_{OUT1} and ΔV_{ESR} as following equation :

$$\Delta V_{OUT} = \Delta V_{OUT1} + \Delta V_{ESR}$$

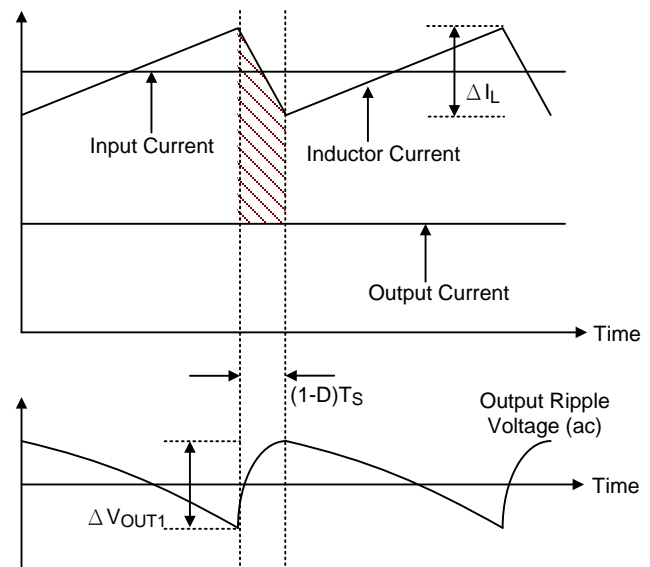In the general application, the output capacitor is recommended to use a 10μF/25V ceramic capacitor.

Figure 4. The Output Ripple Voltage without the Contribution of ESR

VGH Sync-Boost Converter

The VGH sync-boost converter is PWM architecture with programmable output voltage, switching frequency and power-on sequence by I^{2}C interface. It performs fast transient responses to provide the level shift high level voltage for ASG panel. The high operation frequency allows smaller components used to minimize the thickness of the LCD panel.

VGH Switching Frequency Setting

The switching frequency of VGH sync-boost converter is set by the I^{2}C interface, and write the 11h[7:5] register. It has 3-bit register with 6 steps. The switching frequency range is from 600kHz, 715kHz, 800kHz, 933kHz, 1MHz, 1.225MHz. The switching frequency default value is 715kHz (0x01). Please refer to the register map for details.

VGH Soft-start Time Setting

The VGH sync-boost converter has an integrated soft-start function to reduce the input inrush current of power on. The soft-start time is setting through the 11h[4:3] register by the I^{2}C interface. It has a 2-bit register with 4 steps. The soft-start time setting range is from 2ms to 8ms, and each step change is about 2ms. The soft-start time default value is 2ms (0x00). The soft-start time is defined from the VGH voltage start rising to VGH voltage ready. Please refer to Timimg Diagram, and register map for details.

VGH Power-on Delay Time Setting

The VGH boost converter has integrated a power-on delay function. The delay time is adjustable by I2C interface, and write the 11h[2:0] register. It has 3 bits register in 8 steps. The delay time can be chosen 0ms or 35ms. The delay time default value is 20ms (0x04). The delay time is defined from the AVDD output voltage ready to VGH output voltage start rising. Please refer the Timimg Diagram, and register map for detail.

VGH Current Limit

The SN18400P can limit the peak current to achieve over current protection. The IC senses the inductor current of on period that is flowing into VGHLXH pin.

The typical value of the current limit is 0.7A. The internal N-MOSFET will be turned off if the peak inductor current reaches 0.7A. So that, the output current at current limit boundary is denoted as I$_{OUT(CL)}$ and can be calculated as following equation :

$$I_{OUT(CL)} = \eta P \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

Where ηP is the efficiency of the VGH boost converter, I$_{CL}$ is the value of the current limit and T$_S$ is the switching period.

VGH Fault Protection

The SN18400P equip a fault conditions to shut down the IC when VGH output voltage is below 80% of the VGH output voltage. The internal timer starts to count, and the fault condition continued about 60ms, the IC is shut down. Once the UVLO started again, the fault protection would be released.

VGH Output Voltage Setting

The VGH output voltage set by I2C interface. User can write the 05h [5:0] register to set VGH output voltage. It has 5 bits for output voltage adjustable, the setting range is from 10V to 34V, and each voltage step is about 1V. The default output voltage is about 22V (0x0C). Please refer the register map for detail on how to adjust the output voltage. Please restart after adjustment.

VGL Output Voltage Setting

The VGL output voltage set by I2C interface. User can write the 04h[6:0] register to set VGL output voltage. It has 7 bits for output voltage adjustable, the setting range is from −4.4V to −13V, and each voltage step is about -100mV. The default output voltage is about −8V (0x24). Please refer the register map for detail on how to adjust the output voltage.

Owing to the VGL voltage is supplied by AVDD. Therefore the VGL maximum output voltage (VGL_max) is limited by AVDD, the maximum voltage could be calculated by below equation :

$$V_{GL1(MAX)} = -V_{AVDD} + 0.4V$$

Where the VAVDD is AVDD output voltage.

SN18400P

VGL Switching Frequency Setting

The switching frequency of VGL negative charge pump is set by the I2C interface, and write the 10h[5] register. It has 1-bit register with 2 steps. It can be chosen 0.5 x AVDD LX freq. or AVDD LX freq.. The switching frequency default value is AVDD LX freq. (0x01). Please refer to the register map for details.

VGL Soft-start Time Setting

The VGL negative charge pump regulator has an integrated soft-start function to reduce the input inrush current of power on. The soft-start time is setting through the 10h[4:3] register by the I2C interface. It has a 2-bit register with 4 steps. The soft-start time setting range is from 2ms to 8ms, and each step change is about 2ms. The soft-start time default value is 4ms (0x01). The soft- start time is defined from the VGL voltage start falling to VGL voltage ready. Please refer to Timimg Diagram, and register map for details.

VGL Delay Time Setting

The negative charge pump regulator has integrated a delay function. The delay time is adjustable by I2C interface. It has 3 bit of 10h[2:0] register in 8 steps. The delay time setting range is from 0ms to 35ms, and each steps time is about 5ms. The delay time default value is 10ms (0x02). The delay time is defined from the AVDD soft-stare rising to VGL output voltage start falling. Please refer the Timimg Diagram, and register map for detail.

VGL Fault Protection

The SN18400P equip a fault conditions to shut down the IC when VGL output voltage is below the 80% output voltage. The internal timer starts to count, and the fault condition continued about 60ms, the IC is shut down. Once the UVLO started again, the fault protection would be released.

VGL Architecture mode

The negative charge pump regulator has integrated a architecture mode, mode1 VGL>-(AVDD-0.5V), mode2 -13V $\leq$ VGL $\leq$ -(AVDD-0.5V) mode3 VGL<-13V, confirm VGL voltage to set mode, Please refer the Figure1, Figure2, Figure3, application circuit for detail.

V$_{CORE}$ & VIO Sync-Buck Converter

The V$_{CORE}$ and VIO sync-buck converter is high efficiency PWM architecture with high switching frequency and fast transient response. The output voltage, switching frequency, LXB1 & LXB2 slew rate, soft-start time and delay time setting all can be controlled by the I2C interface. The V$_{CORE}$ and VIO sync-buck converter integrate the high side MOSFET and low side MOSFET into IC internal.

V$_{CORE}$ Output Voltage Setting

The V$_{CORE}$ sync-buck output voltage is set by the I2C interface. Users can write the 07h register to set sync-buck output voltage. It has a 5-bit register for output voltage adjustment, the setting range is from 0.8V to 2V, and each voltage step is about 50mV. The default output voltage of V$_{CORE}$ is 1.2V (0x08). Please refer to the register map for details.

V$_{CORE}$ Delay Time Setting

The V$_{CORE}$ sync-buck converter has integrated a delay function. The delay time is adjustable by the I2C interface. It has a 2-bit register with 4 steps. The delay time setting range is from 0ms to 9ms, and each step change is about 3ms. The delay time default value is 3ms (0x01). The delay time is defined from the VIN rises over the UVLO to V$_{CORE}$ output voltage starts rising. Please refer to the Timimg Diagram, and register map for details.

V$_{CORE}$ Slew Rate Setting

The V$_{CORE}$ sync-buck converter has a LXB1 slew rate control function to optimize the efficiency and EMI performance. It has a 3bits register with 4 steps, user can wirte the 12h[6:5] register to set LXB1 slew rate. The slew rate range is from Slow, Normal, Fast, Fastest. The slew rate default value is normal (0x10). Please refer to the register map for details.

V$_{CORE}$ Switching Frequency Setting

The switching frequency of sync-buck converter is set by I2C interface. It has a 3-bit register with 8 steps. The switching frequency range is from 600kHz, 715kHz, 800kHz, 933kHz, 1MHz, 1.225MHz. The switching frequency default value is 715kHz (0x01). Please refer

to the register map for details.

VIO Output Voltage Setting

The VIO sync-buck output voltage is set by the I2C interface. Users can write the 08h register to set sync-buck output voltage. It has a 6-bit register for output voltage adjustment, the setting range is from 1V to 2.8V, and each voltage step is about 50mV. The default output voltage of VIO is 1.8V (0x10). Please refer to the register map for details.

VIO Delay Time Setting

The VIO sync-buck converter has integrated a delay function. The delay time is adjustable by the I2C interface. It has a 2-bit register with 4 steps, user can write the 13h[1:0] register to set VIO delay time. The delay time setting range is from 0ms to 9ms, and each step change is about 3ms. The delay time default value is 3ms (0x01). The delay time is defined from the VIN rises over the UVLO to VIO output voltage starts rising. Please refer to the Timimg Diagram, and register map for details.

VIO Slew Rate Setting

The VIO sync-buck converter has a LXB2 slew rate control function to optimize the efficiency and EMI performance. It has a 2bits register with 4 steps, user can wirte the 13h[2:0] register to set LXB2 slew rate. The slew rate range is from Slow, Normal, Fast, Fastest. The slew rate default value is Normal (0x02). Please refer to the register map for details.

VIO Switching Frequency Setting

The switching frequency of sync-buck converter is set by I2C interface. It has a 3-bit register with 6 steps, user can write the 13h[4:2] register to set VIO switching frequency. The switching frequency range is from 600kHz, 715kHz, 800kHz, 933kHz, 1MHz, 1.225MHz. The switching frequency default value is 715kHz (0x01). Please refer to the register map for details.

LDO Output Voltage Setting

The LDO linear regulator can supply up to 200mA current with an input voltage of 3.3V. It uses an internal P-MOSFET as the pass device. It is suitable as the supply voltage for the T-CON ASIC. The LDO output

voltage setting can be achieved by setting I2C register 09h[3:0]) from 1.8V to 2.8V. It has 4bit with 16 steps. The LDO default value is 2.5V (0x07).

Sync-Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, will increase with higher VIN and decrease with higher inductance, as shown in the equation below:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $I_{L(MAX)} / \Delta I_L = 0.4$ is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following :

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Sync-Buck Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

The output ripple will be the highest at the maximum input voltage since IL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement.

Sync-Buck Input Capacitor Selection

The input capacitance, CIN is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR

input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF/6.3V low ESR ceramic capacitor is recommended.

LDO Delay Time Setting

The LDO linear regulator has integrated a delay function. The delay time is adjustable by the I2C interface. It has a 2-bit register with 4 steps, user can write the 14h[1:0] register to set LDO delay time. The delay time setting range is from 0ms to 9ms, and each step change is about 3ms. The delay time default value is 3ms (0x01). The delay time is defined from the VIN rises over the UVLO to LDO output voltage starts rising. Please refer to the Timimg Diagram, and register map for details.

VCOM Delay Time Setting

The both of VCOM are integrated a delay function. The delay time is adjustable by I2C interface. It has 5 bit of 16h[4:0] register in 31 steps. The delay time setting range is from 0ms to 155ms, and each steps time is about 5ms. The delay time default value is 25ms (0x05). The delay time is defined from AVDD soft-start rising to VCOM output voltage start rising. Please refer the Timimg Diagram, and register map for detail.

Digital VCOM1

The SN18400P provides the ability to reduce the flicker of an LCD Panel by adjusting the VCOM voltage during production test and alignment. A 7bits resolution is provided under digital control, and it support two kind of temperature compensation, it works similar to VGH temperature compensation function. The output range is depended on $\overline{VCOMCOLD}$. The adjustment of the output is provided by the I2C interface. On the contrary,

it will follow with changes in ambient temperature decreasing, if the bit is set b0. It is suggested to connect a resistor between output pin and output capacitor for better stability.

VCOM Voltage Setting

The VCOM voltage is programmable by I2C interface. User can write the 0Ah[7:0] register to set VCOM voltage, it has 8bits with 235 step. The setting range is from 1.5V to 6.2V. The default value of VCOM is 3.7V (0x6E). The each voltage step is about 20mV. Please refer the register map for detail.

HAVDD Voltage Setting

The HAVDD voltage is programmable by I2C interface. User can write the 06h[5:0] register to set HAVDD voltage, it has 6bits with 60 step. The setting range is from 3.5V to 6.5V. The default value of HAVDD is 4V (0x0A). The each voltage step is about 50mV. Please refer the register map for detail.

GMA1/2 Voltage Setting

The GMA1/2 voltage is programmable by I2C interface. User can write the 0Ch[4:0] register to set GMA1 voltage, it has 5bits with 18 step. The setting range is from AVDD-0.1V to AVDD-1V. The default value of AVDD-0.2V (0x02). The each voltage step is about 50mV. GMA2 voltage set can write the 0Dh[4:0], it has 5bits with 18 step. The setting range is from 0.1V to 1V. The default value of 0.4V (0x06). The each voltage step is about 50mV. Please refer the register map for detail.

Voltage Detector

The voltage detector monitors the VIN voltage to generate a reset signal from RESET pin while V_{IN} is lower than the detecting level and not latched. Both detecting level and delay time are setting by I2C interface. The detecting level is set by the register (0x0B [2:0]) from 2V to 2.7V, each voltage step is about 100mV. The delay time is set by (0x15 [3:0]) from 0ms to 75ms, each time step is about 5ms. The start point of delay time is from VIN rising over UVLO to the RESET signal rising.

Control Register (FFH)

The SN18400P provides a register to define the write and read operation. User can write data into MTP by the bit 7 set high level. The bit 0 set high level; it means read data from MTP. If the bit 0 set low level, the data is read from DAC. Please refer the "I^2C Write/Read Timing Sequence" for detail.

Under-Voltage Lockout

The under-voltage lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold (2.3V rising, typ.) to ensure that the input voltage is high enough for reliable operation. The 400mV (typ.) hysteresis prevents supply transients from causing a shutdown. Once the input voltage exceeds the UVLO rising threshold (2.3V, typ.) and EN go high, the start-up is beginning. When the input voltage falls below the UVLO falling threshold (1.9V, typ.), all of output channels would be turned off by the controller.

RICHTEK

I²C Command

PMIC Slave Address

7	6	5	4	3	2	1	R/$\overline{W}$
0	1	0	0	0	1	1	0
0	1	0	0	0	1	1	1

Configuration Parameter VCOM Slave Address

7	6	5	4	3	2	1	R/$\overline{W}$
1	0	0	1	1	1	1	0
1	0	0	1	1	1	1	1

Write Command

(a) Write Single Byte to DAC Register

Example: Writing 29h to DAC Address 07h

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	0	1	1	1	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK	Stop

(b) Write Multi Byte to DAC Register

Example: Writing 29h, 2Ah, 2Bh to DAC Address 06h, 07h, 08h

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	0	1	1	0	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK

0	0	1	0	1	0	1	0	Slave ACK	0	0	1	0	1	0	1	1	Slave ACK	Stop

(c) Write All DAC Register into EEPORM

Example: Write All DAC Register into EEPROM

Start	0	1	0	0	0	1	1	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	1	0	0	0	0	0	0	0	Slave ACK	Stop

Read Command

(a) Read data from DAC Register

Example: Reading Data from DAC Register Address 08h, 09h, 0Ah, 0Bh

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Slave ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Slave ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Slave ACK | Stop |

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Slave ACK | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Slave ACK |

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | Slave ACK | D | D | D | D | D | D | D | D | Master ACK | D | D | D | D | D | D | D | D | Master ACK |

| D | D | D | D | D | D | D | D | Master ACK | D | D | D | D | D | D | D | D | Master N-ACK | Stop |

(b) Read data from EEPORM

Example: Reading Data from EEPORM Address 03h, 04h, 05h, 06h

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Slave ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Slave ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Slave ACK | Stop |

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Slave ACK | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Slave ACK |

| Start | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | Slave ACK | D | D | D | D | D | D | D | D | Master ACK | D | D | D | D | D | D | D | D | Master ACK |

| D | D | D | D | D | D | D | D | Master ACK | D | D | D | D | D | D | D | D | Master N-ACK | Stop |

Configuration Parameter VCOM I^{2}C Command

Write Command

(a) Write Single DATA to DAC

Example: Writing 77h (7bit data) to DAC

| Start | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Slave ACK | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | Slave ACK | Stop |

(b) Write Single DATA to DAC & EEPORM

Example: Writing 77h (7bit data) to DAC & EEPORM

| Start | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Slave ACK | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Slave ACK | Stop |

Read Command

Example: Read Data

Start	1	0	0	1	1	1	1	1	Slave ACK	D	D	D	D	D	D	D	X	Master N-ACK	Stop
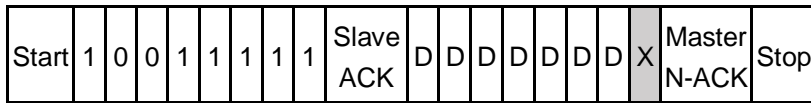
The data LSB is X. (Don't care)

I2C Command List and Description

Item	Address	Register	Default	EEPROM Bit	Default Value	Range	Resolution
Channel Setting	00h	AVDD_Enable[0]	FFh	1 Bit	Enable	0h=Disable 1h=Enable	
		VGL_Enable[1]		1 Bit	Enable	0h=Disable 1h=Enable	
		VGH_Enable[2]		1 Bit	Enable	0h=Disable 1h=Enable	
		HAVDD_Enable[3]		1 Bit	Enable	0h=Disable 1h=Enable	
		VCOER_Enable[4]		1 Bit	Enable	0h=Disable 1h=Enable	
		VIO_Enable[5]		1 Bit	Enable	0h=Disable 1h=Enable	
		VLDO_Enable[6]		1 Bit	Enable	0h=Disable 1h=Enable	
		VCOM_Enable[7]		1 Bit	Enable	0h=Disable 1h=Enable	
Channel Setting	01h	GMA1/GMA2_Enable[0]	0Fh	1 Bit	Enable	0h=Disable 1h=Enable	
		RESET_Enable[1]		1 Bit	Enable	0h=Disable 1h=Enable	
		VCVOER_FCCM_Enable[2]		1 Bit	Disable	0h=Enable 1h=Disable	
		VIO_FCCM_Enable[3]		1 Bit	Disable	0h=Enable 1h=Disable	
Channel Setting	02h	VCOM_ Discharge [0]	01h	1 Bit	Enable	0h=Disable 1h=Enable	
AVDD Voltage	03h	AVDDD [6:0]	14h	7 Bit	9V	7V to 13.5V 00h to 41h	0.1V
VGL Voltage	04h	VGL [6:0]	24h	7 Bit	-8V	-4.4 to -13V 00h to 56h	0.1V
VGH Voltage	05h	VGH [4:0]	0Ch	5 Bit	22V	10V to 34V 00h to 18h	1V
HAVDD Voltage	06h	HAVDD [5:0]	0Ah	6 Bit	4V	3.5V to 6.5V 00h to 3Ch	0.05V
VCOER Voltage	07h	VCOER [4:0]	08h	5 Bit	1.2V	0.8V to 2V 00h to 18h	0.05V
VIO Voltage	08h	VIO [5:0]	10h	6 Bit	1.8V	1V to 2.8V 00h to 24h	0.05V
LDO Voltage	09h	LDO [3:0]	07h	4 Bit	2.5V	1.8V to 2.8V 00h to Ah	0.1V
VCOM Voltage	0Ah	VCOM [7:0]	6Eh	8 Bit	3.7V	1.5V to 6.2V 00h to EBh	0.02V
RESET Voltage	0Bh	RESET [2:0]	02h	3 Bit	2.2V	2V to 2.7V 00h to 07h	0.1V
GMA1 Voltage	0Ch	GMA1 [4:0]	02h	5 Bit	AVDD-0.2V	AVDD-0.1V to AVDD-1V 00h to 12h	0.05V
GMA2 Voltage	0Dh	GMA2 [4:0]	06h	5 Bit	0.4V	0.1V to 1V 00h to 12h	0.05V

RICHTEK

Item	Address	Register	Default	EEPROM Bit	Default Value	Range	Resolution
AVDD Config	0Eh	AVDD LX Frequency [2:0]	31h	3 Bit	715kHz	000h=600kHz 001h=715kHz 010h=800kHz 011h=933kHz 100h=1000kHz 101h=1225kHz	
		AVDD LX Slew Rate [4:3]		2 Bit	Normal	00h=Fastest 01h=Fast 10h=Normal 11h=Slow	
		AVDD Current Limit [6:5]		2 Bit	1A	0.5A to 2A	0.5A
	0Fh	AVDD Delay Time [2:0]	02h	3 Bit	10mS	0mS to 35mS	5mS
		AVDD Soft-Start Time [4:3]		2 Bit	5mS	5mS to 20mS	5mS
VGL Config	10h	VGL Delay Time [2:0]	2Ah	3 Bit	10mS	0mS to 35mS	5mS
		VGL Soft-Start Time [4:3]		2 Bit	4mS	2mS to 8mS	2mS
		VGL Frequency [5]		1 Bit	AVDD LX	0h=0.5xAVDD LX 1h=AVDD LX	
		VGL Architecture mode [7:6]		2 Bit	Archiecture	00h=mode1 VGL > -(AVDD-0.5V) 01h=mode2 -13V $\leqq$ VGL $\leqq$ -(AVDD-0.5V) 10h=mode3 VGL<-13V	
VGH Config	11h	VGH Delay Time [2:0]	34h	3 Bit	20mS	0mS to 35mS	5mS
		VGH Soft-Start Time [4:3]		2 Bit	6mS	2mS to 8mS	2mS
		VGH Frequency [7:5]		3 Bit	715kHz	000h=600kHz 001h=715kHz 010h=800kHz 011h=933kHz 100h=1000kHz 101h=1225kHz	
VCOER Config	12h	VCORE Delay Time [1:0]	45h	2 Bit	3mS	0mS to 9mS	3mS
		VCORE LXB1 Frequency [4:2]		3 Bit	715kHz	000h=600kHz 001h=715kHz 010h=800kHz 011h=933kHz 100h=1000kHz 101h=1225kHz	
		VCORE LXB1 Slew Rate [6:5]		2 Bit	Normal	00h=Fastest 01h=Fast 10h=Normal 11h=Slow	

Item	Address	Register	Default	EEPROM Bit	Default Value	Range	Resolution
VIO Config	13h	VIO Delay Time [1:0]	45h	2 Bit	3mS	0mS to 9mS	3mS
		VIO LXB1 Frequency [4:2]		3 Bit	715kHz	000h=600kHz 001h=715kHz 010h=800kHz 011h=933kHz 100h=1000kHz 101h=1225kHz	
		VIO LXB1 Slew Rate [6:5]		2 Bit	Normal	00h=Fastest 01h=Fast 10h=Normal 11h=Slow	
LDO Config	14h	LDO Delay Time [1:0]	01h	2 Bit	3mS	0mS to 9mS	3mS
RESET Config	15h	RESET /RESET2 Delay Time [3:0]	07h	4 Bit	35mS	0mS to 75mS	5mS
VCOM Config	16h	VCOM Delay Time [4:0]	05h	5 Bit	25mS	0mS to 155mS	5mS
		VCOM power off Follow [5]		1 Bit	UVLO_F	0h=UVLO_F 1h=Reset	
RESET2	17h	RESET2 Enable [0]	0Bh	1 Bit	Enable	0h=Disable 1h=Enable	
		RESET2 [3:1]		3 Bit	2.5V	2V to 2.7V 00h to 07h	0.1V
		VCOM power off Follow [4]		1 Bit	disable, follow 16h	0h=disable, follow 16h[5] 1h=Reset2 ,don't care 16h[5]	
Power off Config	18h	VCORE discharge setting [0]	00h	1 Bit	Disable	0h=Disable 1h=Enable	
		VIO discharge setting [1]		1 Bit	Disable	0h=Disable 1h=Enable	
		VLDO discharge setting [2]		1 Bit	Disable	0h=Disable 1h=Enable	
	19h	VCORE Power off Follow [1:0]	00h	2 Bit	UVLO_F	00h=UVLO_F 01h=Reset 10h=Reset2 11h=Reset2	
		VIO Power off Follow [3:2]		2 Bit	UVLO_F	00h=UVLO_F 01h=Reset 10h=Reset2 11h=Reset2	
		VLDO Power off Follow [4]		1 Bit	UVLO_F	00h=UVLO_F 01h=Reset	
Configuration Parameter VCOM	X	VCOM_P[7:1]	1000000P	7bit	X	X	X
Control Register	FFh	00h : Read data form DAC register 01h : Read data form EEPROM 80h : Write all DAC into EEPROM		8bit	--	--	--

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
Data Address	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh
Bits	[6:0]	[6:0]	[4:0]	[5:0]	[4:0]	[5:0]	[3:0]	[7:0]	[2:0]
Min	7V	-4.4V	10V	3.5V	0.8V	1V	1.8V	1.5V	2.0V
Max	13.5V	-13V	34V	6.5V	2.0V	2.8V	2.8V	6.2V	2.5V
Default	14h	24h	0Ch	Ah	08h	10h	07h	6Eh	02h
Resolution	0.1V	0.1V	1V	0.05V	0.05V	0.05V	0.1V	0.02V	0.1V
0H	7V	-4.4V	10V	3.5V	0.8V	1V	1.8V	1.5V	2V
1H	7.1V	-4.5V	11V	3.55V	0.85V	1.05V	1.9V	1.52V	2.1V
2H	7.2V	-4.6V	12V	3.6V	0.9V	1.1V	2V	1.54V	2.2V
3H	7.3V	-4.7V	13V	3.65V	0.95V	1.15V	2.1V	1.56V	2.3V
4H	7.4V	-4.8V	14V	3.7V	1V	1.2V	2.2V	1.58V	2.4V
5H	7.5V	-4.9V	15V	3.75V	1.05V	1.25V	2.3V	1.6V	2.5V
6H	7.6V	-5V	16V	3.8V	1.1V	1.3V	2.4V	1.62V	2.6V
7H	7.7V	-5.1V	17V	3.85V	1.15V	1.35V	2.5V	1.64V	2.7V
8H	7.8V	-5.2V	18V	3.9V	1.2V	1.4V	2.6V	1.66V	
9H	7.9V	-5.3V	19V	3.95V	1.25V	1.45V	2.7V	1.68V	
AH	8V	-5.4V	20V	4V	1.3V	1.5V	2.8V	1.7V	
BH	8.1V	-5.5V	21V	4.05V	1.35V	1.55V		1.72V	
CH	8.2V	-5.6V	22V	4.1V	1.4V	1.6V		1.74V	
DH	8.3V	-5.7V	23V	4.15V	1.45V	1.65V		1.76V	
EH	8.4V	-5.8V	24V	4.2V	1.5V	1.7V		1.78V	
FH	8.5V	-5.9V	25V	4.25V	1.55V	1.75V		1.8V	
10H	8.6V	-6V	26V	4.3V	1.6V	1.8V		1.82V	
11H	8.7V	-6.1V	27V	4.35V	1.65V	1.85V		1.84V	
12H	8.8V	-6.2V	28V	4.4V	1.7V	1.9V		1.86V	
13H	8.9V	-6.3V	29V	4.45V	1.75V	1.95V		1.88V	
14H	9V	-6.4V	30V	4.5V	1.8V	2V		1.9V	
15H	9.1V	-6.5V	31V	4.55V	1.85V	2.05V		1.92V	
16H	9.2V	-6.6V	32V	4.6V	1.9V	2.1V		1.94V	
17H	9.3V	-6.7V	33V	4.65V	1.95V	2.15V		1.96V	
18H	9.4V	-6.8V	34V	4.7V	2V	2.2V		1.98V	
19H	9.5V	-6.9V		4.75V		2.25V		2V	
1AH	9.6V	-7V		4.8V		2.3V		2.02V	
1BH	9.7V	-7.1V		4.85V		2.35V		2.04V	
1CH	9.8V	-7.2V		4.9V		2.4V		2.06V	

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
1DH	9.9V	-7.3V		4.95V		2.45V		2.08V	
1EH	10V	-7.4V		5V		2.5V		2.1V	
1FH	10.1V	-7.5V		5.05V		2.55V		2.12V	
20H	10.2V	-7.6V		5.1V		2.6V		2.14V	
21H	10.3V	-7.7V		5.15V		2.65V		2.16V	
22H	10.4V	-7.8V		5.2V		2.7V		2.18V	
23H	10.5V	-7.9V		5.25V		2.75V		2.2V	
24H	10.6V	-8V		5.3V		2.8V		2.22V	
25H	10.7V	-8.1V		5.35V				2.24V	
26H	10.8V	-8.2V		5.4V				2.26V	
27H	10.9V	-8.3V		5.45V				2.28V	
28H	11V	-8.4V		5.5V				2.3V	
29H	11.1V	-8.5V		5.55V				2.32V	
2AH	11.2V	-8.6V		5.6V				2.34V	
2BH	11.3V	-8.7V		5.65V				2.36V	
2CH	11.4V	-8.8V		5.7V				2.38V	
2DH	11.5V	-8.9V		5.75V				2.4V	
2EH	11.6V	-9V		5.8V				2.42V	
2FH	11.7V	-9.1V		5.85V				2.44V	
30H	11.8V	-9.2V		5.9V				2.46V	
31H	11.9V	-9.3V		5.95V				2.48V	
32H	12V	-9.4V		6V				2.5V	
33H	12.1V	-9.5V		6.05V				2.52V	
34H	12.2V	-9.6V		6.1V				2.54V	
35H	12.3V	-9.7V		6.15V				2.56V	
36H	12.4V	-9.8V		6.2V				2.58V	
37H	12.5V	-9.9V		6.25V				2.6V	
38H	12.6V	-10V		6.3V				2.62V	
39H	12.7V	-10.1V		6.35V				2.64V	
3AH	12.8V	-10.2V		6.4V				2.66V	
3BH	12.9V	-10.3V		6.45V				2.68V	
3CH	13V	-10.4V		6.5V				2.7V	
3DH	13.1V	-10.5V						2.72V	
3EH	13.2V	-10.6V						2.74V	
3FH	13.3V	-10.7V						2.76V	
40H	13.4V	-10.8V						2.78V	

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	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
41H	13.5V	-10.9V						2.8V	
42H		-11V						2.82V	
43H		-11.1V						2.84V	
44H		-11.2V						2.86V	
45H		-11.3V						2.88V	
46H		-11.4V						2.9V	
47H		-11.5V						2.92V	
48H		-11.6V						2.94V	
49H		-11.7V						2.96V	
4AH		-11.8V						2.98V	
4BH		-11.9V						3V	
4CH		-12V						3.02V	
4DH		-12.1V						3.04V	
4EH		-12.2V						3.06V	
4FH		-12.3V						3.08V	
50H		-12.4V						3.1V	
51H		-12.5V						3.12V	
52H		-12.6V						3.14V	
53H		-12.7V						3.16V	
54H		-12.8V						3.18V	
55H		-12.9V						3.2V	
56H		-13V						3.22V	
57H								3.24V	
58H								3.26V	
59H								3.28V	
5AH								3.3V	
5BH								3.32V	
5CH								3.34V	
5DH								3.36V	
5EH								3.38V	
5FH								3.4V	
60H								3.42V	
61H								3.44V	
62H								3.46V	
63H								3.48V	
64H								3.5V	

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
65H								3.52V	
66H								3.54V	
67H								3.56V	
68H								3.58V	
69H								3.6V	
6AH								3.62V	
6BH								3.64V	
6CH								3.66V	
6DH								3.68V	
6EH								3.7V	
6FH								3.72V	
70H								3.74V	
71H								3.76V	
72H								3.78V	
73H								3.8V	
74H								3.82V	
75H								3.84V	
76H								3.86V	
77H								3.88V	
78H								3.9V	
79H								3.92V	
7AH								3.94V	
7BH								3.96V	
7CH								3.98V	
7DH								4V	
7EH								4.02V	
7FH								4.04V	
80H								4.06V	
81H								4.08V	
82H								4.1V	
83H								4.12V	
84H								4.14V	
85H								4.16V	
86H								4.18V	
87H								4.2V	
88H								4.22V	

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
89H								4.24V	
8AH								4.26V	
8BH								4.28V	
8CH								4.3V	
8DH								4.32V	
8EH								4.34V	
8FH								4.36V	
90H								4.38V	
91H								4.4V	
92H								4.42V	
93H								4.44V	
94H								4.46V	
95H								4.48V	
96H								4.5V	
97H								4.52V	
98H								4.54V	
99H								4.56V	
9AH								4.58V	
9BH								4.6V	
9CH								4.62V	
9DH								4.64V	
9EH								4.66V	
9FH								4.68V	
A0H								4.7V	
A1H								4.72V	
A2H								4.74V	
A3H								4.76V	
A4H								4.78V	
A5H								4.8V	
A6H								4.82V	
A7H								4.84V	
A8H								4.86V	
A9H								4.88V	
AAH								4.9V	
ABH								4.92V	
ACH								4.94V	

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
ADH								4.96V	
AEH								4.98V	
AFH								5V	
B0H								5.02V	
B1H								5.04V	
B2H								5.06V	
B3H								5.08V	
B4H								5.1V	
B5H								5.12V	
B6H								5.14V	
B7H								5.16V	
B8H								5.18V	
B9H								5.2V	
BAH								5.22V	
BBH								5.24V	
BCH								5.26V	
BDH								5.28V	
BEH								5.3V	
BFH								5.32V	
C0H								5.34V	
C1H								5.36V	
C2H								5.38V	
C3H								5.4V	
C4H								5.42V	
C5H								5.44V	
C6H								5.46V	
C7H								5.48V	
C8H								5.5V	
C9H								5.52V	
CAH								5.54V	
CBH								5.56V	
CCH								5.58V	
CDH								5.6V	
CEH								5.62V	
CFH								5.64V	
D0H								5.66V	

	AVDD	VGL	VGH	HAVDD	Vcore	VIO	LDO	VCOM	Reset Voltage
D1H								5.68V	
D2H								5.7V	
D3H								5.72V	
D4H								5.74V	
D5H								5.76V	
D6H								5.78V	
D7H								5.8V	
D8H								5.82V	
D9H								5.84V	
DAH								5.86V	
DBH								5.88V	
DCH								5.9V	
DDH								5.92V	
DEH								5.94V	
DFH								5.96V	
E0H								5.98V	
E1H								6V	
E2H								6.02V	
E3H								6.04V	
E4H								6.06V	
E5H								6.08V	
E6H								6.1V	
E7H								6.12V	
E8H								6.14V	
E9H								6.16V	
EAH								6.18V	
EBH								6.2V	

	GMA1	GMA2	AVDD Current Limit	AVDD LX Slew Rate	AVDD LX Frequency	AVDD Soft-start Time	AVDD Delay Time	VGL Architecture Mode	VGL Frequency	VGL Soft-Start Time	VGL Delay Time
Data Address	0Ch	0Dh	0Eh			0Fh		10h			
Bits	[4:0]	[4:0]	[6:5]	[4:3]	[2:0]	[4:3]	[2:0]	[7:6]	[5]	[4:3]	[2:0]
Min	AVDD-1V	0.1V	1A	Slow	600kHz	5ms	0ms	NA	0.5xAVDD LX	2ms	0ms
Max	AVDD-0.1V	1V	2A	Fastset	1225kHz	20ms	35ms	NA	AVDD LX	8ms	35ms
Default	02h	06H	1h	2h	1h	0h	2h	00h	1h	1h	2h
Resolution	50mV	0.05V	0.5A	NA	NA	5mS	5mS	NA	NA	2mS	5mS
0H	AVDD-(50mVx2)	0.1V	0.5A	Fastest	600kHz	5mS	0mS	VGL > -(AVDD-0.5V)	0.5 AVDD LX (50 % duty)	2mS	0mS
1H	AVDD-(50mVx3)	0.15V	1.0A	Fast	715kHz	10mS	5mS	-13V ≦ VGL ≦ -(AVDD-0.5V)	AVDD LX (50 % duty)	4mS	5mS
2H	AVDD-(50mVx4)	0.2V	1.5A	Normal	800kHz	15mS	10mS	VGL<-13V		6mS	10mS
3H	AVDD-(50mVx5)	0.25V	2A	Slow	933kHz	20mS	15mS			8mS	15mS
4H	AVDD-(50mVx6)	0.3V			1000kHz		20mS				20mS
5H	AVDD-(50mVx7)	0.35V			1225kHz		25mS				25mS
6H	AVDD-(50mVx8)	0.4V					30mS				30mS
7H	AVDD-(50mVx9)	0.45V					35mS				35mS
8H	AVDD-(50mVx10)	0.5V									
9H	AVDD-(50mVx11)	0.55V									
AH	AVDD-(50mVx12)	0.6V									
BH	AVDD-(50mVx13)	0.65V									
CH	AVDD-(50mVx14)	0.7V									

	GMA1	GMA2	AVDD Current Limit	AVDD LX Slew Rate	AVDD LX Frequency	AVDD Soft-start Time	AVDD Delay Time	VGL Architecture Mode	VGL Frequency	VGL Soft-Start Time	VGL Delay Time
DH	AVDD-(50mVx 15)	0.75V									
EH	AVDD-(50mVx 16)	0.8V									
FH	AVDD-(50mVx 17)	0.85V									
10H	AVDD-(50mVx 18)	0.9V									
11H	AVDD-(50mVx 19)	0.95V									
12H	AVDD-(50mVx 20)	1V									

	VGH Frequency	VGH Soft-Start Time	VGH Delay Time	Vcore LXB1 Slew Rate	Vcore LXB1 Frequency	Vcore Delay Time	VIO LXB2 Slew Rate	VIO LXB2 Frequency	VIO Delay Time
Data Address	11h			12h			13h		
Bits	[7:5]	[4:3]	[2:0]	[6:5]	[4:2]	[1:0]	[6:5]	[4:2]	[1:0]
Min	600kHz	2ms	0ms	Slow	600kHz	0ms	Slow	600kHz	0ms
Max	1225kHz	8ms	35ms	Fastest	1225kHz	9ms	Fastest	1225kHz	9ms
Default	1h	2h	5h	2h	1h	1h	2h	1h	1h
Resolution	NA	2mS	5mS	NA	NA	3mS	NA	NA	3mS
0H	600kHz	2mS	0mS	Fastest	600kHz	0mS	Fastest	600kHz	0mS
1H	715kHz	4mS	5mS	Fast	715kHz	3mS	Fast	715kHz	3mS
2H	800kHz	6mS	10mS	Normal	800kHz	6mS	Normal	800kHz	6mS
3H	933kHz	8mS	15mS	Slow	933kHz	9mS	Slow	933kHz	9mS
4H	1000kHz		20mS		1000kHz			1000kHz	
5H	1225kHz		25mS		1225kHz			1225kHz	
6H			30mS						
7H			35mS						

	LDO Delay Time	Reset Delay Time	VCOM Delay Time	VCOM Power Off Follow	RESET2	RESET2 Enable	VLDO Discharge Setting	VIO Discharge Setting	VCORE Discharge Setting
Data Address	14h	15h	16h	17h			18h		
Bits	[1:0]	[3:0]	[4:0]	[4]	[3:1]	[0]	[2]	[1]	[0]
Min	0ms	0ms	0ms	NA	2.0V	NA	NA	NA	NA
Max	9ms	75ms	155ms	NA	2.5V	NA	NA	NA	NA
Default	1h	07h	05h	0h	05h	1h	0h	0h	0h
Resolution	3mS	5mS	5mS	NA	0.1V	NA	NA	NA	NA
0H	0mS	0mS	0mS	follow 16h[5]	2V	Disable	Disable	Disable	Disable
1H	3mS	5mS	5mS	Reset2	2.1V	Enable	Enable	Enable	Enable
2H	6mS	10mS	10mS		2.2V				
3H	9mS	15mS	15mS		2.3V				
4H		20mS	20mS		2.4V				
5H		25mS	25mS		2.5V				
6H		30mS	30mS		2.6V				
7H		35mS	35mS		2.7V				
8H		40mS	40mS						
9H		45mS	45mS						
AH		50mS	50mS						
BH		55mS	55mS						
CH		60mS	60mS						
DH		65mS	65mS						
EH		70mS	70mS						
FH		75mS	75mS						
10H			80mS						
11H			85mS						
12H			90mS						
13H			95mS						
14H			100mS						
15H			105mS						
16H			110mS						
17H			115mS						
18H			120mS						
19H			125mS						
1AH			130mS						
1BH			135mS						
1CH			140mS						
1DH			145mS						
1EH			150mS						
1FH			155mS						

	VLDO Power off Follow	VCORE Power off Follow	VIO Power off Follow	Configuration Parameter VCOM
Data Address	19h			[7:1]
Bits	[4]	[3:2]	[1:0]	NA
Min	NA	NA	NA	NA
Max	NA	NA	NA	40h
Default	00h	00h	00h	40h
Resolution	NA	NA	NA	10mV
0H	UVLO_F	UVLO_F	UVLO_F	VCOM-(10mVx64)
1H	RESET1	RESET1	RESET1	VCOM-(10mVx63)
2H		RESET2	RESET2	VCOM-(10mVx62)
3H		RESET2	RESET2	VCOM-(10mVx61)
4H				VCOM-(10mVx60)
5H				VCOM-(10mVx59)
6H				VCOM-(10mVx58)
7H				VCOM-(10mVx57)
8H				VCOM-(10mVx56)
9H				VCOM-(10mVx55)
AH				VCOM-(10mVx54)
BH				VCOM-(10mVx53)
CH				VCOM-(10mVx52)
DH				VCOM-(10mVx51)
EH				VCOM-(10mVx50)
FH				VCOM-(10mVx49)
10H				VCOM-(10mVx48)
11H				VCOM-(10mVx47)
12H				VCOM-(10mVx46)
13H				VCOM-(10mVx45)
14H				VCOM-(10mVx44)
15H				VCOM-(10mVx43)
16H				VCOM-(10mVx42)
17H				VCOM-(10mVx41)
18H				VCOM-(10mVx40)
19H				VCOM-(10mVx39)
1AH				VCOM-(10mVx38)
1BH				VCOM-(10mVx37)
1CH				VCOM-(10mVx36)
1DH				VCOM-(10mVx35)
1EH				VCOM-(10mVx34)

	VLDO Power off Follow	VCORE Power off Follow	VIO Power off Follow	Configuration Parameter VCOM
1FH				VCOM-(10mVx33)
20H				VCOM-(10mVx32)
21H				VCOM-(10mVx31)
22H				VCOM-(10mVx30)
23H				VCOM-(10mVx29)
24H				VCOM-(10mVx28)
25H				VCOM-(10mVx27)
26H				VCOM-(10mVx26)
27H				VCOM-(10mVx25)
28H				VCOM-(10mVx24)
29H				VCOM-(10mVx23)
2AH				VCOM-(10mVx22)
2BH				VCOM-(10mVx21)
2CH				VCOM-(10mVx20)
2DH				VCOM-(10mVx19)
2EH				VCOM-(10mVx18)
2FH				VCOM-(10mVx17)
30H				VCOM-(10mVx16)
31H				VCOM-(10mVx15)
32H				VCOM-(10mVx14)
33H				VCOM-(10mVx13)
34H				VCOM-(10mVx12)
35H				VCOM-(10mVx11)
36H				VCOM-(10mVx10)
37H				VCOM-(10mVx9)
38H				VCOM-(10mVx8)
39H				VCOM-(10mVx7)
3AH				VCOM-(10mVx6)
3BH				VCOM-(10mVx5)
3CH				VCOM-(10mVx4)
3DH				VCOM-(10mVx3)
3EH				VCOM-(10mVx2)
3FH				VCOM-(10mVx1)
40H				VCOM
41H				VCOM+(10mVx1)
42H				VCOM+(10mVx2)
43H				VCOM+(10mVx3)
44H				VCOM+(10mVx4)

	VLDO Power off Follow	VCORE Power off Follow	VIO Power off Follow	Configuration Parameter VCOM
45H				VCOM+(10mVx5)
46H				VCOM+(10mVx6)
47H				VCOM+(10mVx7)
48H				VCOM+(10mVx8)
49H				VCOM+(10mVx9)
4AH				VCOM+(10mVx10)
4BH				VCOM+(10mVx11)
4CH				VCOM+(10mVx12)
4DH				VCOM+(10mVx13)
4EH				VCOM+(10mVx14)
4FH				VCOM+(10mVx15)
50H				VCOM+(10mVx16)
51H				VCOM+(10mVx17)
52H				VCOM+(10mVx18)
53H				VCOM+(10mVx19)
54H				VCOM+(10mVx20)
55H				VCOM+(10mVx21)
56H				VCOM+(10mVx22)
57H				VCOM+(10mVx23)
58H				VCOM+(10mVx24)
59H				VCOM+(10mVx25)
5AH				VCOM+(10mVx26)
5BH				VCOM+(10mVx27)
5CH				VCOM+(10mVx28)
5DH				VCOM+(10mVx29)
5EH				VCOM+(10mVx30)
5FH				VCOM+(10mVx31)
60H				VCOM+(10mVx32)
61H				VCOM+(10mVx33)
62H				VCOM+(10mVx34)
63H				VCOM+(10mVx35)
64H				VCOM+(10mVx36)
65H				VCOM+(10mVx37)
66H				VCOM+(10mVx38)
67H				VCOM+(10mVx39)
68H				VCOM+(10mVx40)
69H				VCOM+(10mVx41)
6AH				VCOM+(10mVx42)

	VLDO Power off Follow	VCORE Power off Follow	VIO Power off Follow	Configuration Parameter VCOM
6BH				VCOM+(10mVx43)
6CH				VCOM+(10mVx44)
6DH				VCOM+(10mVx45)
6EH				VCOM+(10mVx46)
6FH				VCOM+(10mVx47)
70H				VCOM+(10mVx48)
71H				VCOM+(10mVx49)
72H				VCOM+(10mVx50)
73H				VCOM+(10mVx51)
74H				VCOM+(10mVx52)
75H				VCOM+(10mVx53)
76H				VCOM+(10mVx54)
77H				VCOM+(10mVx55)
78H				VCOM+(10mVx56)
79H				VCOM+(10mVx57)
7AH				VCOM+(10mVx58)
7BH				VCOM+(10mVx59)
7CH				VCOM+(10mVx60)
7DH				VCOM+(10mVx61)
7EH				VCOM+(10mVx62)
7FH				VCOM+(10mVx63)

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-28L 3.5x3.5 (FC) package, the thermal resistance, θ_{JA}, is 31.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)} = (125°C - 25°C) / (31.2°C/W) = 3.2W$ for a UQFN-28L 3.5x3.5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.
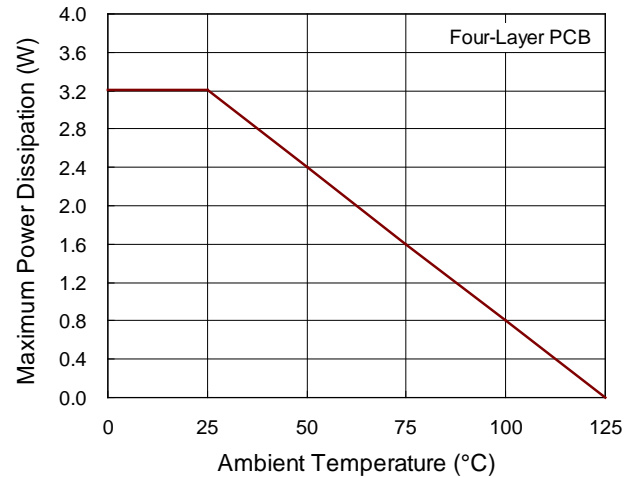
Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

► Place the capacitors as close to pin as possible for better performance.

► Minimize the size of the LXB1 and LXB2, node and keep it wide and shorter. Keep the LXB1 and LXB2 node away from the analog ground.

► The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.

► Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.

► Place the output capacitors as close to pin as possible for better performance.

► For good regulation, place the power components as close as possible. The traces should be wider and shorter especially for the high-current output loop.

► The power ground (PGND) consist input and output capacitor grounds.

► Minimize the size of the LX node and keep it wide and shorter. Keep the LX node away from the analog ground.

► PGND metal to increase the isolation.

► Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

► The output voltage (VCORE and VIO) must be near the output pin. The trace must be short and avoid the trace near any switching nodes.
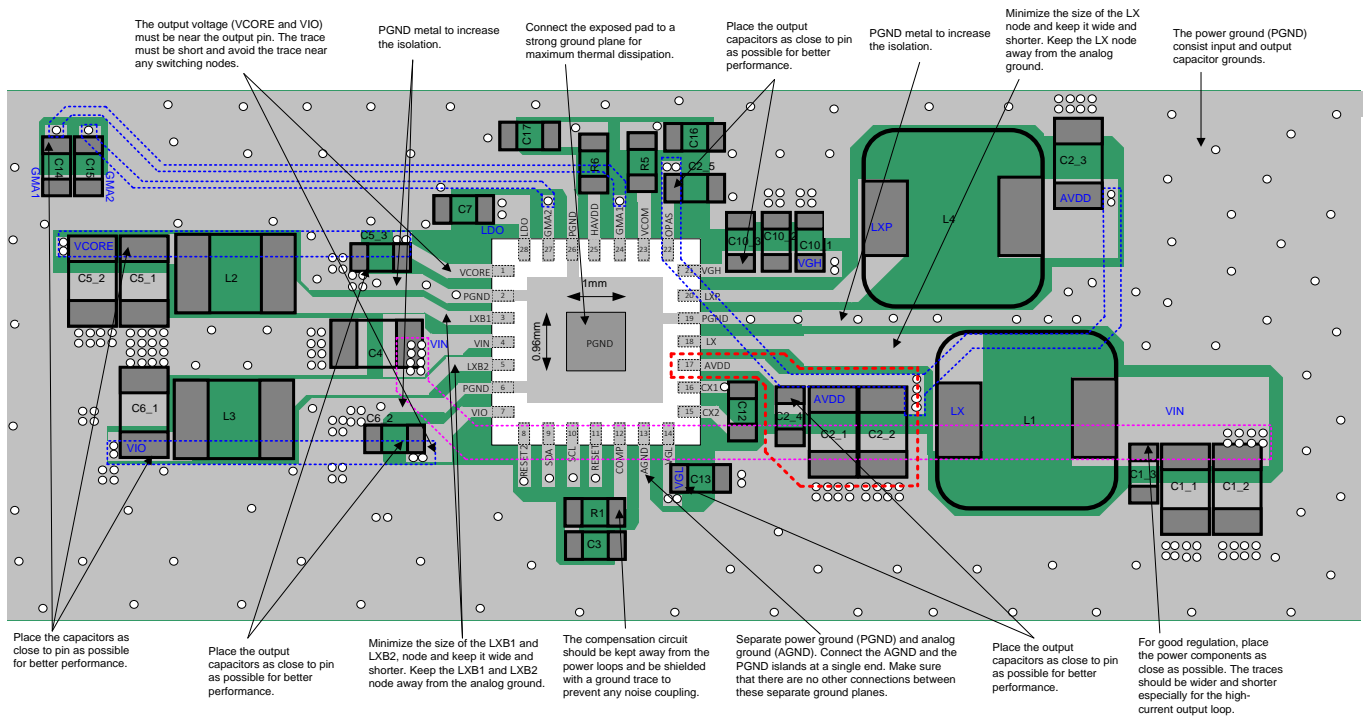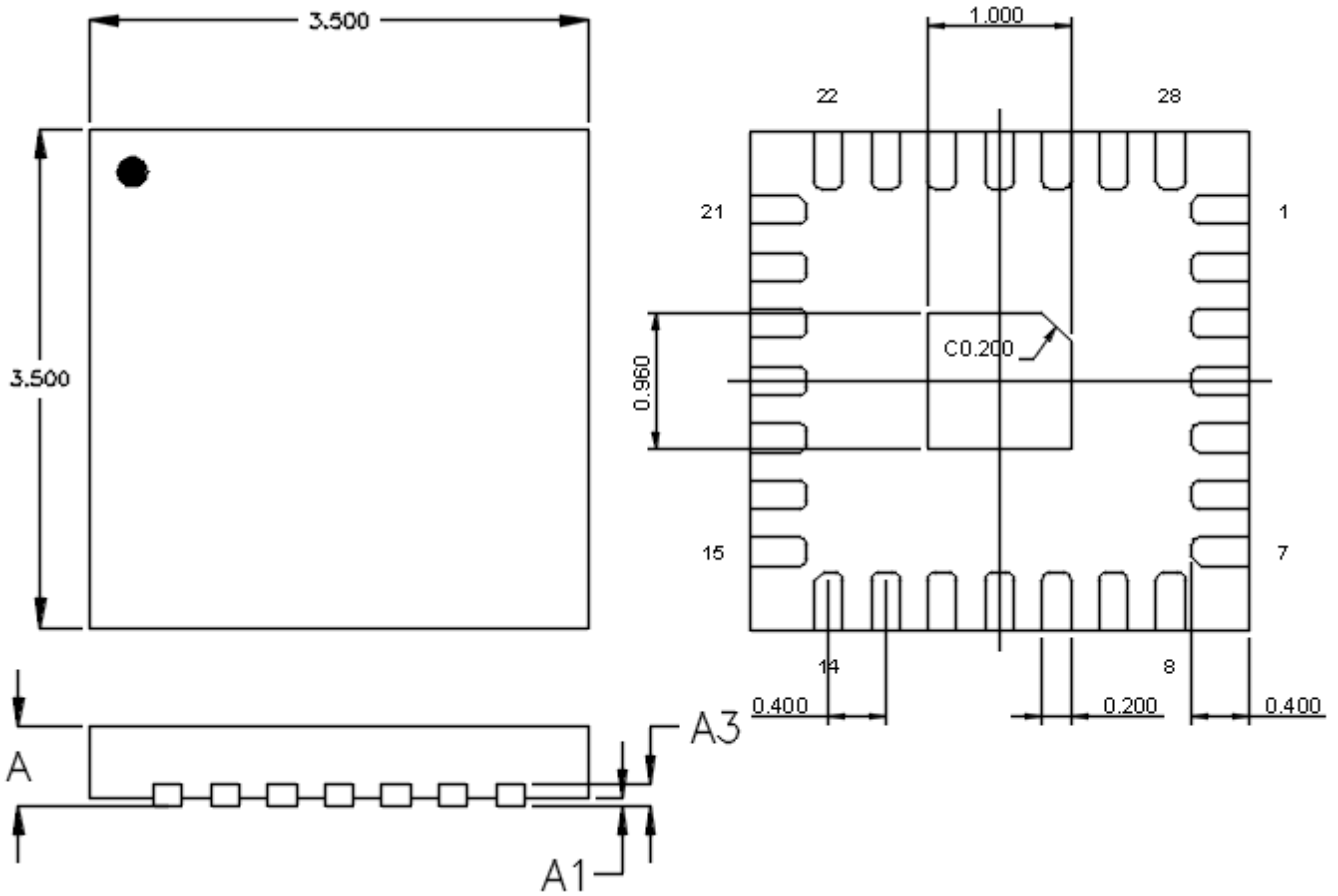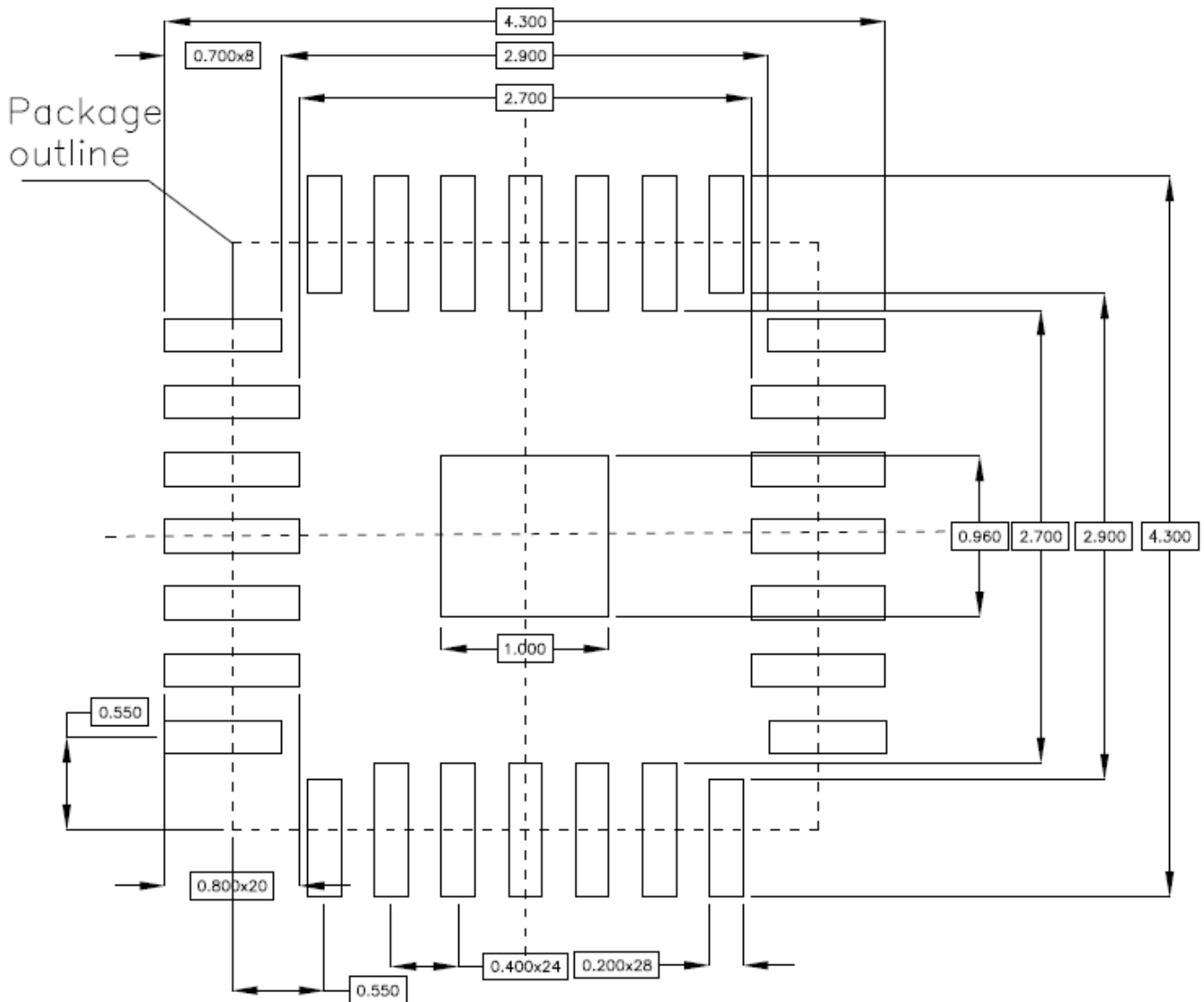

Figure 6. PCB Layout Guide

Outline Dimension

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008

Tolerance
±0.050

U-Type 28L QFN 3.5x3.5 (FC) Package

Footprint Information

Package	Number of Pin	Tolerance
V/W/U/XQFN3.5x3.5-28(FC)	28	±0.05

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