LM25184-Q1 Dual-Output EVM User's Guide

With input voltage range and current capability as specified in Table 1, the PSR flyback DC/DC converter family of parts from TI provides flexibility, scalability, and optimized solution size for a range of applications. Using an 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch, these converters enable isolated DC/DC solutions with high density and low component count.

Table 1. PSR Flyback DC/DC Converter Family

PSR FLYBACK DC/DC CONVERTER	INPUT VOLTAGE RANGE	PEAK SWITCH CURRENT (TYP)	MAXIMUM LOAD CURRENT, V_{OUT} = 12 V, N_{PS} = 1	
			V_{IN} = 4.5 V	V_{IN} = 13.5 V
LM5181-Q1	4.5 V to 65 V	0.75 A	90 mA	180 mA
LM5180-Q1	4.5 V to 65 V	1.5 A	180 mA	360 mA
LM25180-Q1	4.5 V to 42 V	1.5 A	180 mA	360 mA
LM25183-Q1	4.5 V to 42 V	2.5 A	300 mA	600 mA
LM25184-Q1	4.5 V to 42 V	4.1 A	500 mA	1 A

The LM25184EVM-DUAL evaluation module (EVM) is a flyback DC/DC converter that employs primary-side regulation (PSR) based on sampling of the transformer's primary winding voltage to achieve high conversion efficiency in a small footprint. It operates over a wide input voltage range of 6 V to 42 V and delivers dual isolated outputs of 15 V and –8 V at up to 500-mA load current. Operating without an optocoupler or transformer auxiliary winding, the converter provides an output voltage with better than ±2% load regulation. The flyback transformer has a turns ratio of 1 : 1.5 : 0.8 (PRI : SEC1 : SEC2) and provides 1500 VRMS primary-to-secondary isolation.

The EVM design uses the LM25184-Q1 PSR flyback converter with wide input voltage (wide V_{IN}) range. An integrated 65-V, 4.1-A power MOSFET provides ample margin for line transients and switch (SW) node voltage spikes related to transformer parasitic leakage inductance. Load regulation errors related to transformer secondary winding resistance are avoided by virtue of the quasi-resonant boundary conduction mode (BCM) control scheme.

Additional features includes current-mode control with internal compensation, hiccup-mode fault protection, low input quiescent current, programmable soft-start, and optional output voltage temperature compensation. UVLO protects the converter at low input voltage conditions, and the EN/UVLO pin supports adjustable input UVLO with user-defined hysteresis for application specific power-up and power-down requirements.

The LM25183-Q1 and LM25184-Q1 are available in a 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch to enable isolated DC/DC solutions with high density and low component count. Wettable flank pins provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs in high-reliability industrial and automotive applications. Refer to the LM25183-Q1 and LM25184-Q1 data sheets for more information.

Use the LM25184-Q1 with WEBENCH® Power Designer to create a custom regulator design. Furthermore, the user can download the *LM25184 Quickstart Calculator* to optimize component selection and examine predicted efficiency performance across line and load ranges.

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Trademarks

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1 High Density EVM Description

The LM25184EVM-DUAL EVM is designed to use a regulated or non-regulated input rail ranging from 6 V to 42 V to produce a tightly-regulated, isolated output voltages of 15 V and –8 V at load currents up to 500 mA. This wide V_{IN} range isolated DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The power-train passive components selected for this EVM, including transformer, rectifying diodes, and ceramic input and output capacitors, are available from multiple component vendors. Transformers with functional or basic grade isolation are available with isolation voltages of 1.5 kV or greater.

1.1 Typical Applications

- Automotive powertrain systems
- Sub-AM band automotive body electronics
- Traction inverter and motor drives: IGBT and SiC gate drive supplies
- Isolated field transmitters and field actuators
- Isolated bias power rails

1.2 Features and Electrical Performance

- Tightly-regulated, isolated output voltages of 15 V and –8 V with better than ±2% load regulation from 1% to 100% load
- Wide V_{IN} operating range of 6 V to 42 V
  – Operates down to 4.5 V after startup based on UVLO resistor divider setting
- Full load current of 500 mA, both outputs loaded, $V_{IN} \geq 18$ V
- Maximum switching frequency of 350 kHz remains below the AM band for automotive applications
- High efficiency across wide load current range
  – 88% and 90% efficiency at 400-mA load, V_{IN} = 12 V and 24 V, respectively
  – 90% efficiency at 250-mA load, V_{IN} = 12 V
- 3.3-mA and 2.8-mA no-load supply current at V_{IN} = 13.5 V and 24 V, respectively
- Ultra-low conducted and radiated EMI signatures
  – Optimized for CISPR 25 Class 5 requirements
  – Soft switching avoids diode reverse recovery
  – Input π-stage EMI filter with damping from electrolytic capacitor ESR
- Boundary conduction mode (BCM) control architecture provides fast line and load transient response
  – Peak current-mode control
  – Quasi-resonant switching for reduced power loss
  – Internal loop compensation
- Integrated 65-V flyback power MOSFET
  – Provides large headroom for input voltage transients
- Cycle-by-cycle overcurrent protection (OCP)
- Monotonic prebias output voltage start-up
- User-adjustable soft-start time set by capacitor connected between SS/BIAS and GND
  – Option for external bias using transformer auxiliary winding or voltage source connected to SS/BIAS
- Resistor-programmable input voltage UVLO with customizable hysteresis for applications with wide turn-on and turn-off voltage difference
  – Input UVLO set to turn on and off at V_{IN} of 5.9 V and 4.5 V, respectively
- Low transformer primary-to-secondary (interwinding) capacitance to accommodate high dv/dt secondary-side common-mode swings
- Fully assembled, tested, and proven PCB layout with 58-mm × 38-mm total footprint

2 EVM Performance Characteristics

Table 2. Electrical Performance Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		6	24	42	V
Input voltage turnon, $V_{IN(ON)}$	Adjusted using EN/UVLO divider resistors			5.9		V
Input voltage turnoff, $V_{IN(OFF)}$				4.5		
Input voltage hysteresis, $V_{IN(HYS)}$				1.4		
Input current, no load, $I_{IN(NL)}$	$I_{OUT1} = I_{OUT2} = 0$ A	$V_{IN} = 13.5$ V		3.3		mA
		$V_{IN} = 24$ V		2.8		
		$V_{IN} = 36$ V		2.8		
Input current, disabled, $I_{IN(OFF)}$	$V_{EN} = 0$ V	$V_{IN} = 24$ V		10		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT1}	$I_{OUT1/2} = 20$ mA to 0.4 A		14.7	15.0	15.3	V
Output voltage, V_{OUT2}			–7.8	–8	–8.2	V
Output current, I_{OUT1} , $–I_{OUT2}$ [(1)]	$V_{IN} = 6$ V		0		0.25	A
	$V_{IN} = 13.5$ V		0		0.4	
	$V_{IN} = 24$ V		0		0.55	
	$V_{IN} = 42$ V		0		0.6	
Output voltage regulation, ΔV_{OUT}	Load regulation, $V_{IN} = 24$ V	$I_{OUT1} = –I_{OUT2} = 20$ mA to 0.4 A		1.5%		
	Line regulation, $I_{OUT} = 0.2$ A	$V_{IN} = 13.5$ V to 42 V		1.5%		
Output voltage ripple, $V_{OUT(AC)}$	$V_{IN} = 24$ V, $I_{OUT1} = I_{OUT2} = 0.4$ A			100		mVrms
Output overcurrent protection, I_{OCP}	$V_{IN} = 24$ V			0.58		A
Soft-start time, t_{SS}	$C_{SS} = 47$ nF			8		ms
SYSTEM CHARACTERISTICS						
Switching frequency, $F_{SW(nom)}$	$V_{IN} = 24$ V, $I_{OUT1} = I_{OUT2} = 0.4$ A			350		kHz
Half-load efficiency, η_{HALF} [(2)]	$I_{OUT1} = I_{OUT2} = 0.2$ A	$V_{IN} = 6$ V		86.7%		
		$V_{IN} = 12$ V		89.2%		
		$V_{IN} = 24$ V		88.7%		
		$V_{IN} = 36$ V		86.5%		
Full load efficiency, η_{FULL}	$I_{OUT1} = I_{OUT2} = 0.4$ A	$V_{IN} = 12$ V		88%		
		$V_{IN} = 24$ V		90%		
		$V_{IN} = 36$ V		88.6%		
Isolation rating [(3)]	Functional insulation				1500	V
LM25184 junction temperature, T_J			–40		150	°C

(1) The output power delivered by the LM25184-Q1 PSR flyback converter increases with input voltage.
(2) The default output voltages of this EVM are 15 V and –8 V. Efficiency and other performance metrics can change based on operating input voltage, load currents, externally-connected output capacitance(s), and other parameters.
(3) The selected flyback transformer provides functional grade isolation to 1500 V DC.

3 Application Circuit Diagram

Figure 1 shows the schematic of an LM25184-based flyback converter (EMI filter stage not shown). Soft start (SS), temperature compensation (TC), and UVLO (EN/UVLO) components are shown that are configurable as required by the specific application. The transformer turns ratio is 1 : 1.5 : 0.8 and the primary-referred magnetizing inductance is 7 µH.

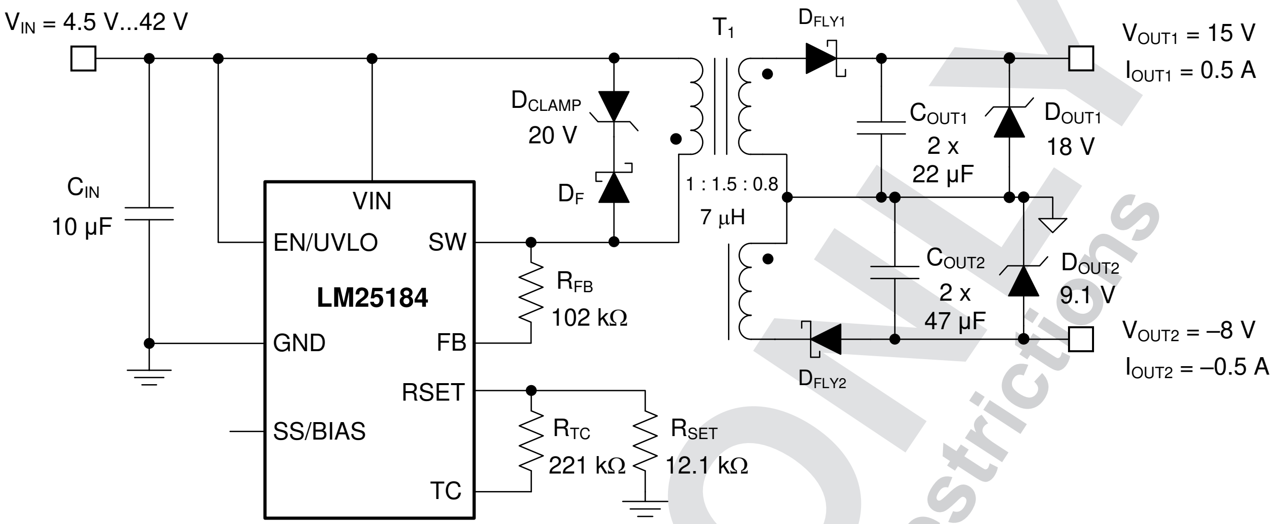

Figure 1. LM25184-Q1 PSR Flyback Dual-Output Schematic

4 Test Setup and Procedure

4.1 Test Setup

Table 3. EVM Connections

LABEL	DESCRIPTION
VIN+	Positive input voltage power and sense connection
VIN–	Negative input voltage power and sense connection
VOUT1	Output #1 power and sense connection
VOUT2	Output #2 power and sense connection
SGND	Output return and sense connection
EN	ENABLE input: tie to GND to disable converter
SS/BIAS	External BIAS input
SW	SW node connection

Referencing the EVM connections described in Table 3, the recommended test setup to evaluate the LM25184EVM-DUAL is shown in Figure 2. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before power is applied to the EVM.

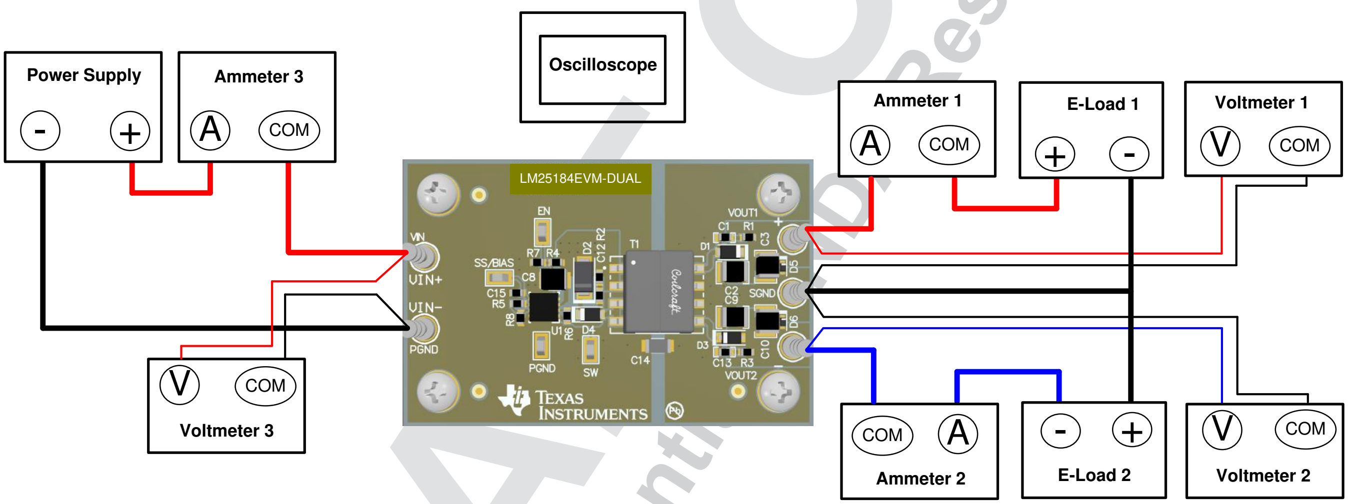

Figure 2. EVM Test Setup

CAUTION

Refer to the LM25183-Q1 and LM25184-Q1 data sheets, LM25184 Quickstart Calculator and WEBENCH® Power Designer for additional guidance pertaining to component selection and converter operation.

4.2 Test Equipment

Voltage Source: The input voltage source V_{IN} should be a 0–42-V variable DC source.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT1 to SGND. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 3:** Output voltage at VOUT2 to SGND. Set voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Load current, output #1. Set ammeter to 1-second aperture time
- **Ammeter 3:** Load current, output #2. Set ammeter to 1-second aperture time

Electronic Loads: The loads should be electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 Adc to 0.5 Adc up to 20 V. For a no-load input current measurement, disconnect the electronic load as it may draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the probe's ground barrel through the ground lead to the capacitor's negative terminal. TI does not recommend using a long-leaded ground connection because this may induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that may be live or energized.

4.3 Recommended Test Setup

4.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 100 mA maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 2. An additional input bulk capacitor is recommended to provide damping if long input lines are used.
- Connect voltmeter 3 at VIN+ and VIN– connection points to measure the input voltage.
- Connect ammeter 3 to measure the input current and set to at least 1-second aperture time.

4.3.2 Output Connections

- Connect electronic loads to VOUT1, VOUT2 and SGND connections as shown in Figure 2. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeters 1 and 2 at VOUT1, VOUT2 and SGND connection points to measure the output voltages.
- Connect ammeters 1 and 2 to measure the output currents.

4.4 Test Procedure

4.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 10 mA.
- Increase input source from 0 V to 24 V; use voltmeter 3 to measure the input voltage.
- Increase the current limit of the input supply to 2 A.
- Using voltmeters to measure the respective output voltages, vary both loads from 20 mA to 0.4 A DC; V_{OUT1} and V_{OUT2} should remain within the load regulation specification.
- Set the load currents to 0.2 A (50% rated load) and vary the input source voltage from 6 V to 42 V; V_{OUT1} and V_{OUT2} should remain within the line regulation specification.
- Decrease loads to 10 mA. Decrease input source voltage to 0 V.

5 Test Data and Performance Curves

Figure 3 through present typical performance curves for the LM25184EVM-DUAL Because actual performance data may be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency and Regulation

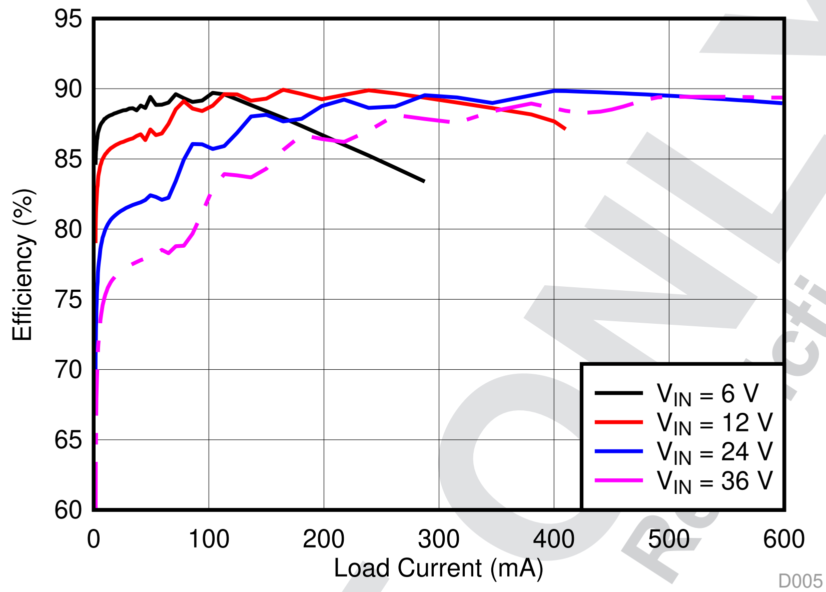

Figure 3. Conversion Efficiency (Linear Scale), Outputs Loaded Symmetrically

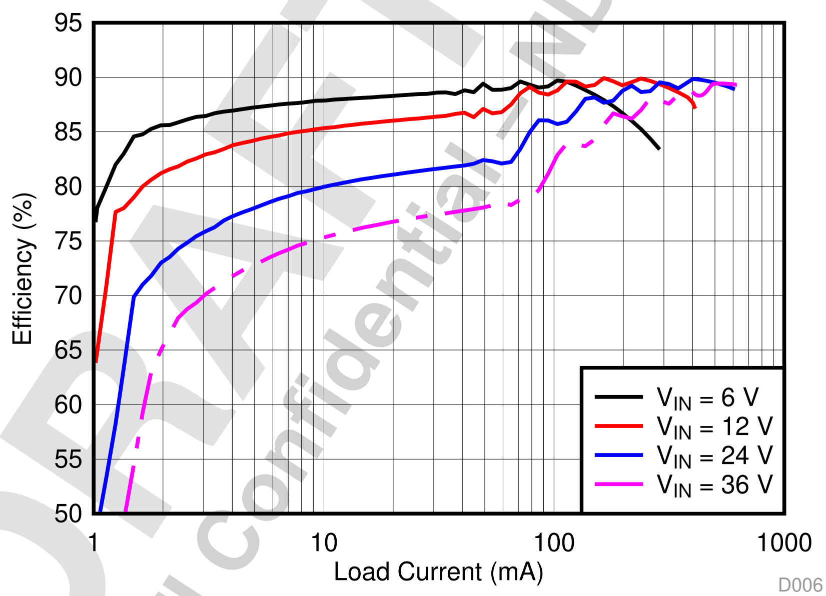

Figure 4. Conversion Efficiency (Log Scale), Outputs Loaded Symmetrically

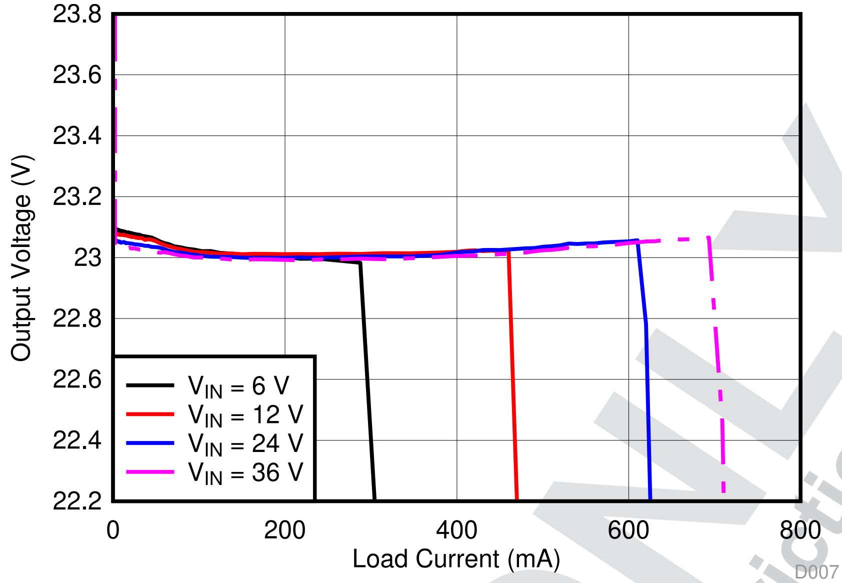

Figure 5. Load Regulation (Linear Scale), Sum of V_{OUT1} and V_{OUT2} Measured, Outputs Loaded Symmetrically

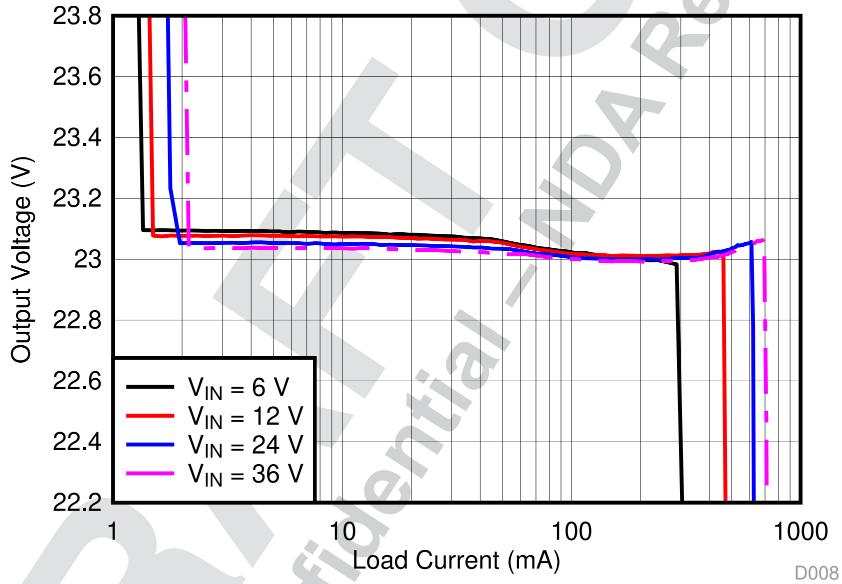

Figure 6. Load Regulation (Log Scale), Sum of V_{OUT1} and V_{OUT2} Measured, Outputs Loaded Symmetrically

5.2 Operating Waveforms

5.2.1 Switching

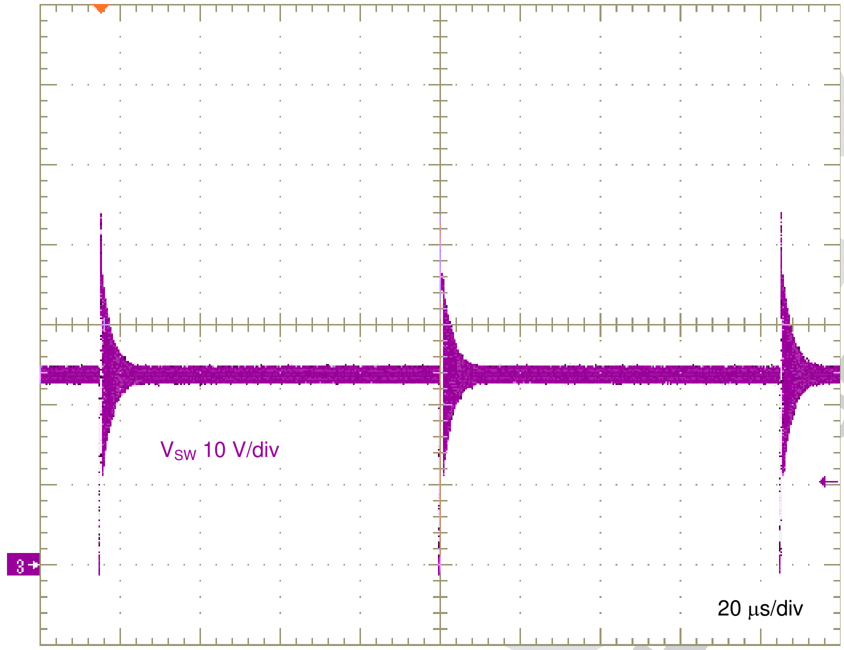

Figure 7. Switch Voltage, No Load, V_{IN} = 24 V

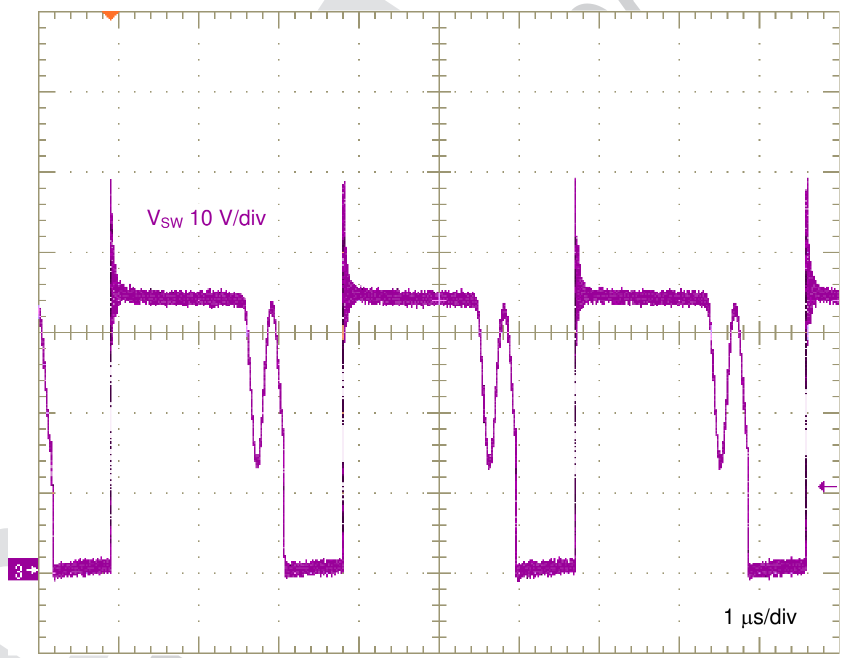

Figure 8. Switch Voltage, I_{OUT1} = –I_{OUT2} = 300 mA, V_{IN} = 24 V

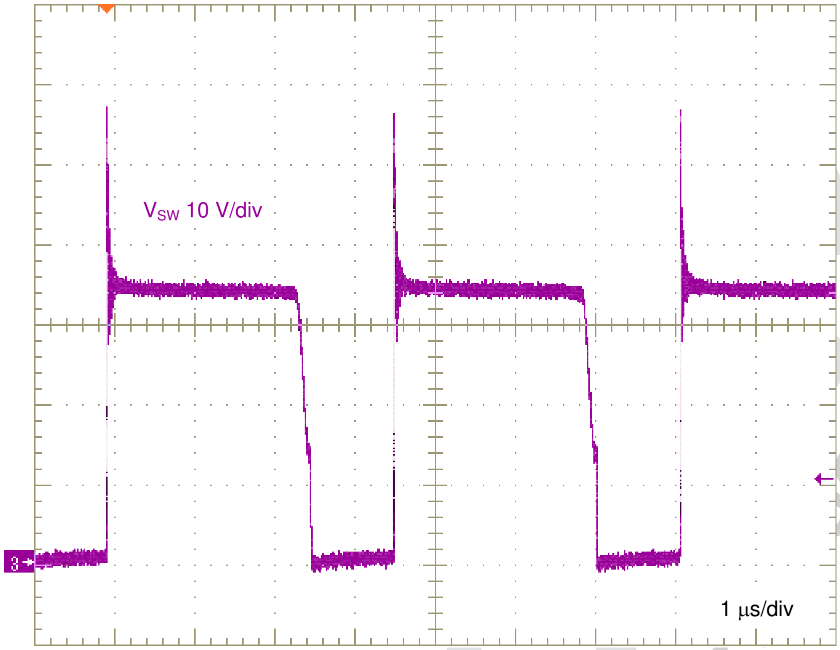

Figure 9. Switch Voltage, I_{OUT1} = $–I_{OUT2}$ = 500 mA, V_{IN} = 24 V

5.2.2 Load Transient Response

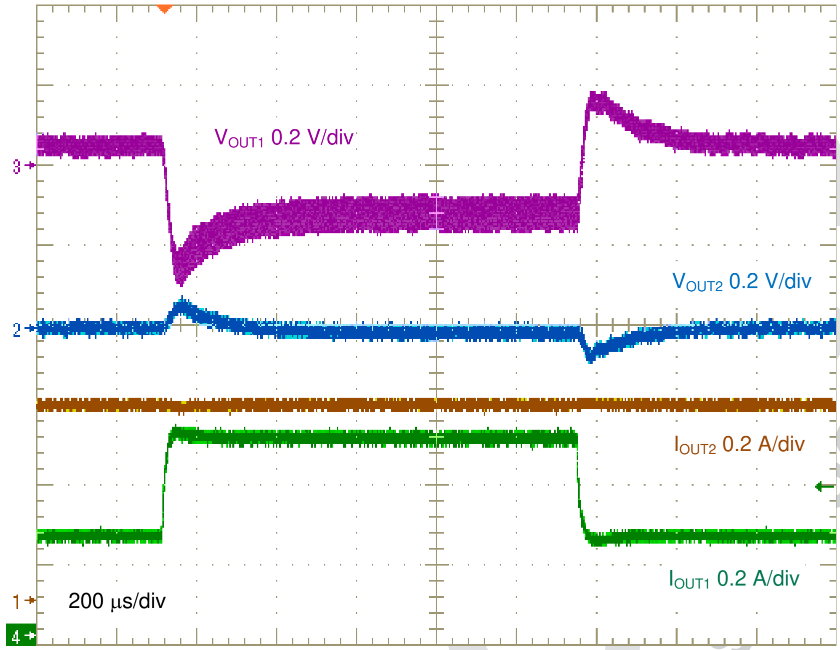

Figure 10. Output 1 Load Transient, 250 mA to 500 mA at 100 mA/µs, I_{OUT2} = –500 mA, V_{IN} = 24 V

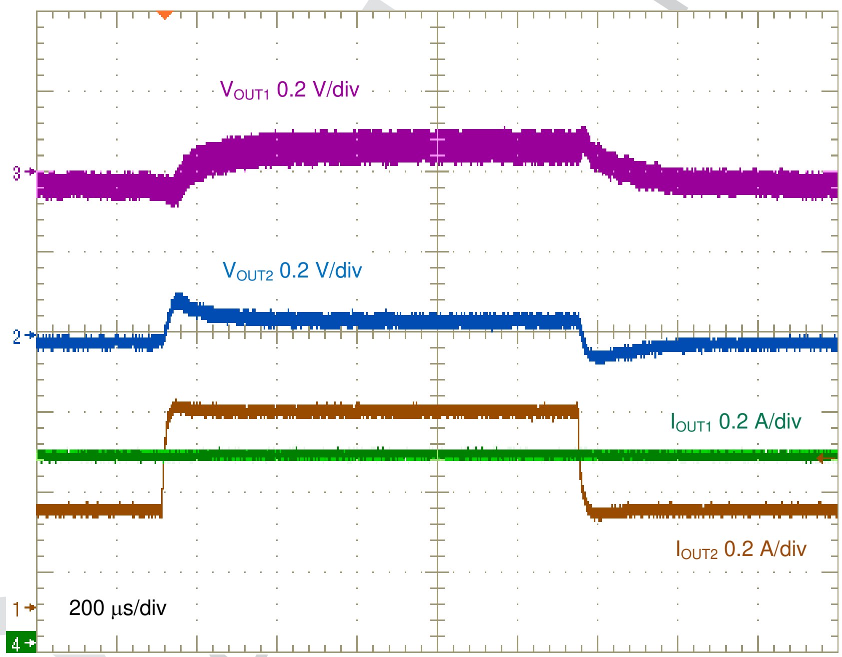

Figure 11. Output 2 Load Transient, 250 mA to 500 mA at 100 mA/µs, I_{OUT1} = 500 mA, V_{IN} = 24 V

5.2.3 Start-Up and Enable [1]

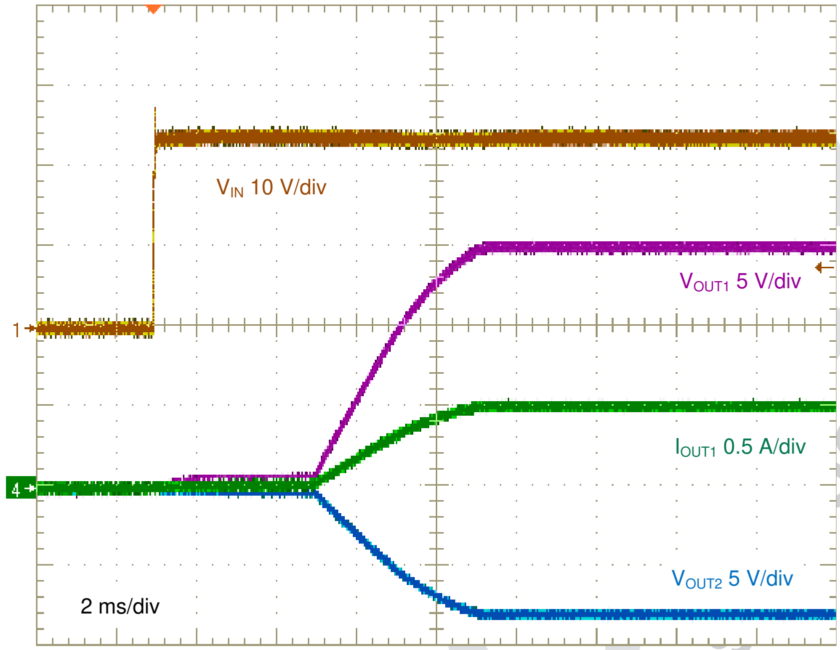

Figure 12. Start-Up, V_{IN} = 24 V, I_{OUT1} = –I_{OUT2} = 500 mA Resistive

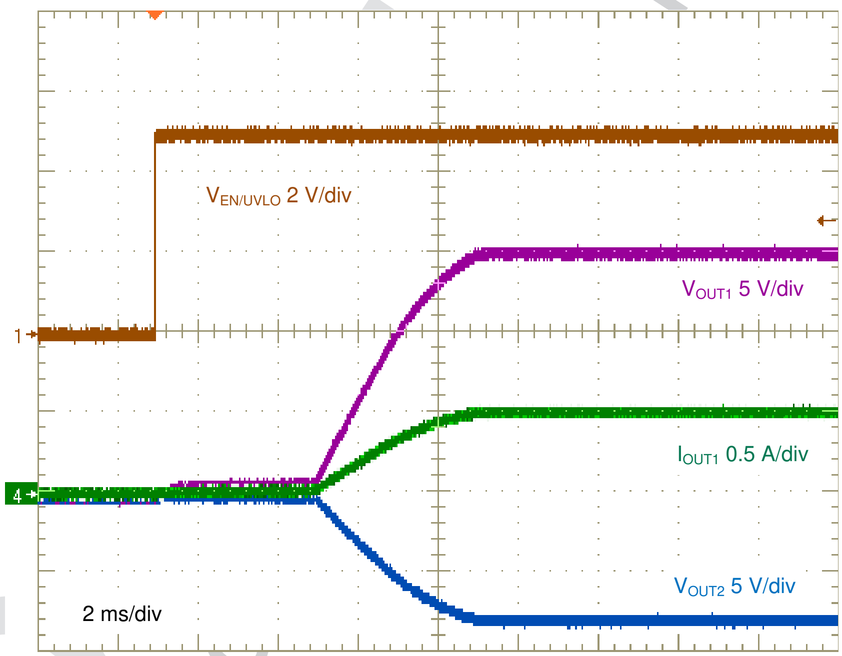

Figure 13. Enable On, V_{IN} = 24 V, I_{OUT1} = –I_{OUT2} = 500 mA Resistive

[1] The internal soft-start timer is applicable here as the SS cap was not installed during these startup tests.

6 EVM Documentation

6.1 Schematic

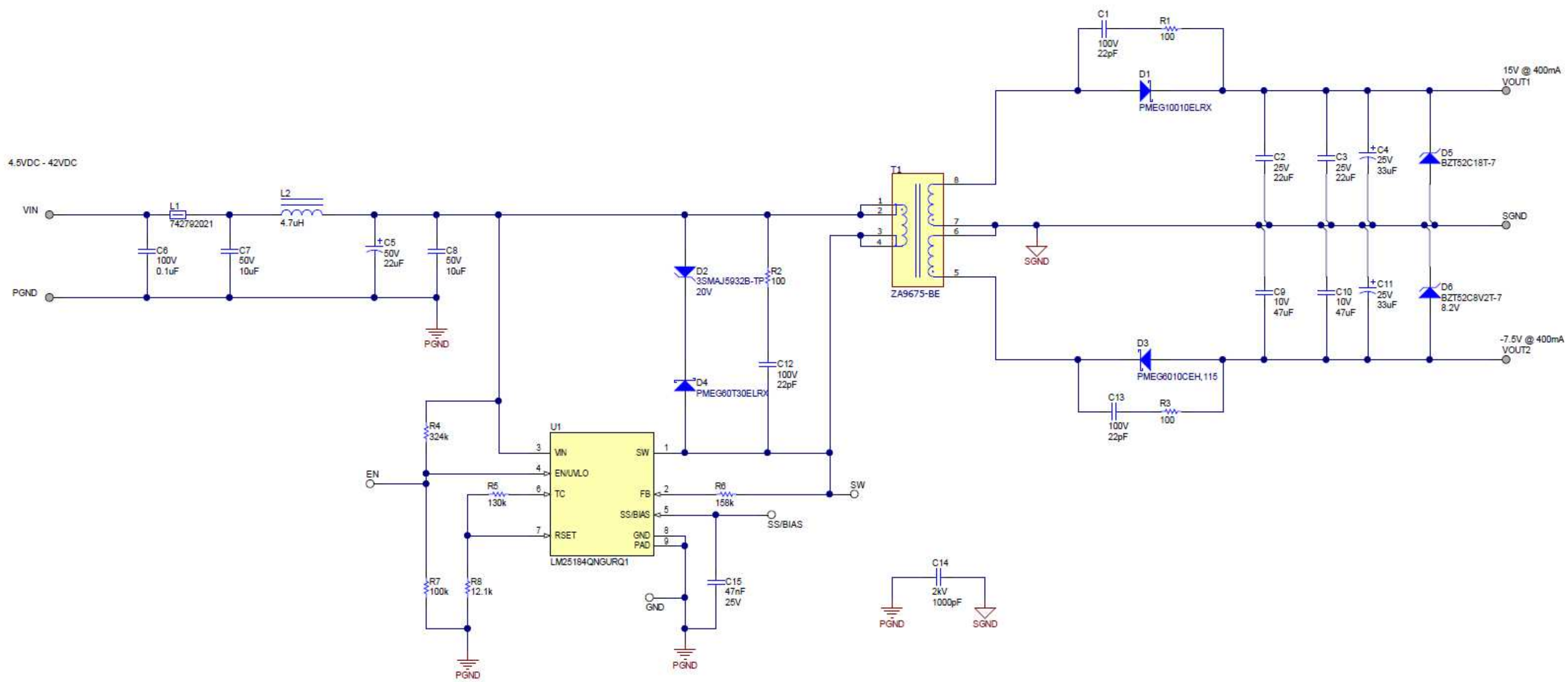

Figure 14. EVM Schematic

6.2 Bill of Materials

Table 4. Bill of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
3	C1, C12, C13	Capacitor, Ceramic, 22pF, 100V, X7R, 0603	Std	Std
2	C2, C3	Capacitor, Ceramic, 22µF, 25V, X7R, 1210, AEC-Q200	CNA6P1X7R1H106K250AE	TDK
			UMJ325KB7106KMHT	Taiyo Yuden
1	C5	Aluminum Electrolytic, 22µF, 50V, ±20%, AEC-Q200 grade 2	EEE-ZC1H220P	Panasonic
1	C6	Capacitor, Ceramic, 0.1µF, 100V, X7R, 0603	C1608X7R1A105K080AC	TDK
2	C7, C8	Capacitor, Ceramic, 10µF, 50V, X7R, 1210, AEC-Q200	CGA6P3X7R1E226M250AB	TDK
			TMK325B7226KMHT	Taiyo Yuden
2	C9, C10	Capacitor, Ceramic, 47µF, 10V, X7R, 1210	GRM32ER71A476KE15L	Murata
			LMK325B7476MM-TR	Taiyo Yuden
1	C14	Capacitor, Ceramic, 1nF, 2kV, X7R, 1206	Std	Std
1	C15	Capacitor, Ceramic, 47nF, 16V, X7R, 0603	Std	Std
1	D1	Schottky Diode, 100V, 1A, SOD-123	DFLS1100-7	Diodes Inc.
1	D2	Zener, 20V, 3W, SMA	3SMAJ5932B	Micro Commercial
1	D3	Schottky Diode, 60V, 1A, SOD-123	FSV360	OnSemi
1	D4	Schottky Diode, 60V, 3A, SOD-123	PMEG60T30	Nexperia
1	D5	Zener, 18V, SOD-523	BZT52C18VT-7	Diodes Inc.
1	D6	Zener, 9.1V, SOD-523	BZT52C9V1T-7	Diodes Inc.
1	L1	Ferrite bead, 22Ω at 100MHz, 8mΩ max, 6A	742792021	Würth Electronik
1	L2	Inductor, 4.7µH, 48.6mΩ, 3.7A, AEC-Q200	VCHA042A-4R7MS6	Cyntec
		Inductor, 4.7µH, 25mΩ, 2A, 34MHz, AEC-Q200	XFL4030-472ME	Coilcraft
1	T1	Flyback transformer, 7µH, 5A, 1 : 1.5 : 0.8 turns ratio, 9.2 × 9.8mm	750318704	Würth Electronik
		Flyback transformer, 7µH, 5A, 1 : 1.5 : 0.8 turns ratio, 13 × 11mm	ZA9675-BE	Coilcraft
3	R1, R2, R3	Resistor, Chip, 100Ω, 1/10W, 1%, 0603	Std	Std
1	R4	Resistor, Chip, 243kΩ, 1/16W, 1%, 0603	Std	Std
1	R5	Resistor, Chip, 249kΩ, 1/16W, 1%, 0603	Std	Std
1	R6	Resistor, Chip, 102kΩ, 1/16W, 1%, 0603	Std	Std
1	R7	Resistor, Chip, 82.5kΩ, 1/16W, 1%, 0603	Std	Std
1	R8	Resistor, Chip, 12.1kΩ, 1/16W, 1%, 0603	Std	Std
1	U1	IC, LM25184-Q1, wide V_{IN} PSR flyback converter, WSON-8	LM25184QNGURQ1	TI
1	PCB1	PCB, FR4, 4 layer, 1 oz, 58 mm x 38 mm	PCB	–
5	J1, J2, J3, J4, J5	Turret, PTH, 4.72mm, VIN+, VIN–, VOUT1, VOUT2, SGND	1573-2	Keystone Electronics
4	TP1, TP2, TP3, TP4	Test points for EN, SW, SS/BIAS, GND	5015	Keystone Electronics

6.3 PCB Layout

Figure 15 through Figure 18 show the design of the LM25184-Q1 4-layer PCB with 1-oz copper thickness. The EVM is a two-sided design with post connections for VIN+, VIN–, VOUT1+, VOUT2+ and SGND.

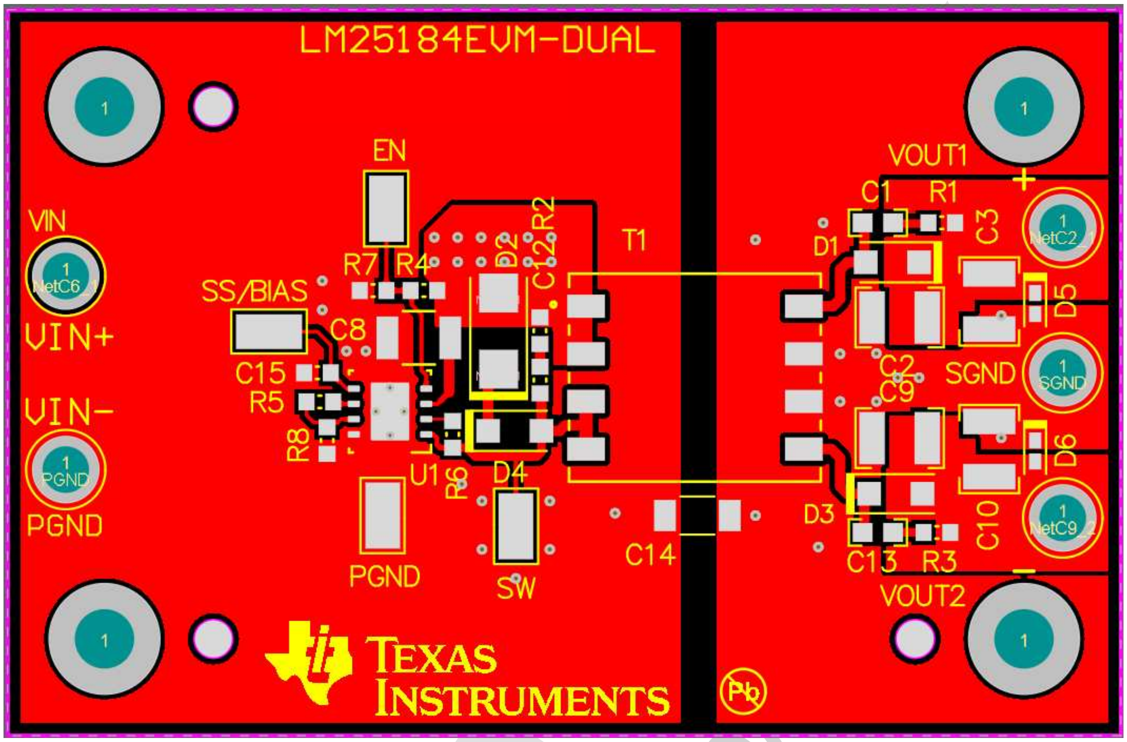

Figure 15. Top Copper (Top View)

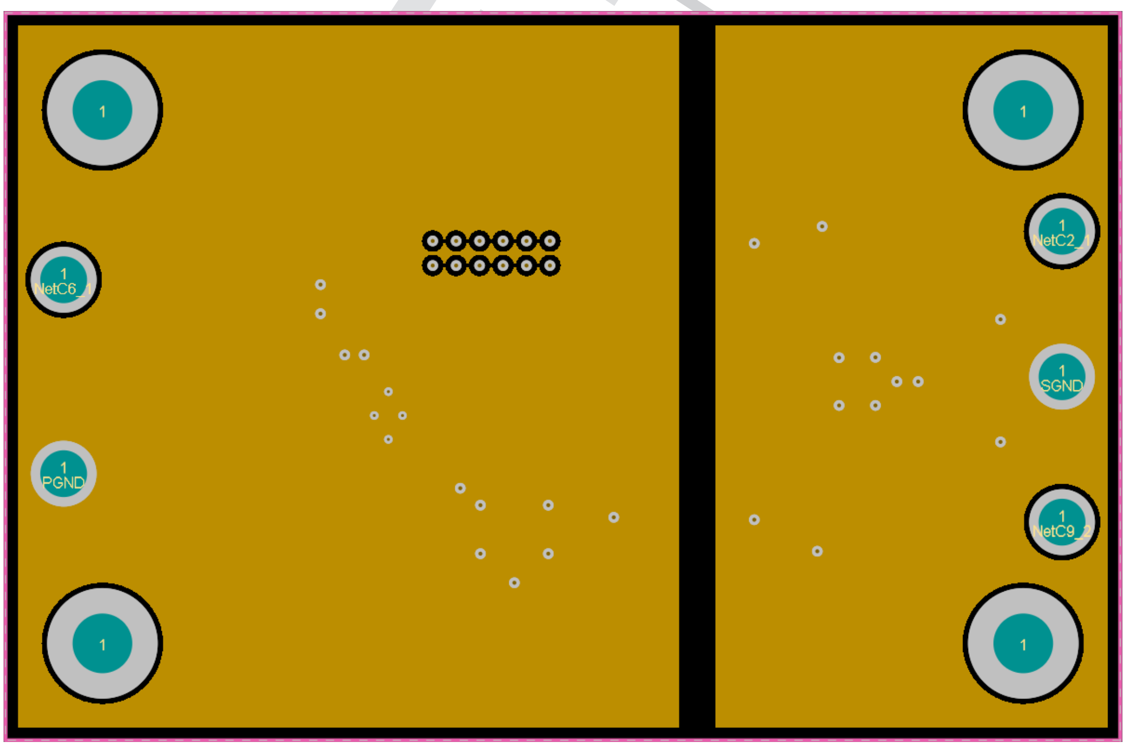

Figure 16. Layer 2 Copper (Top View)

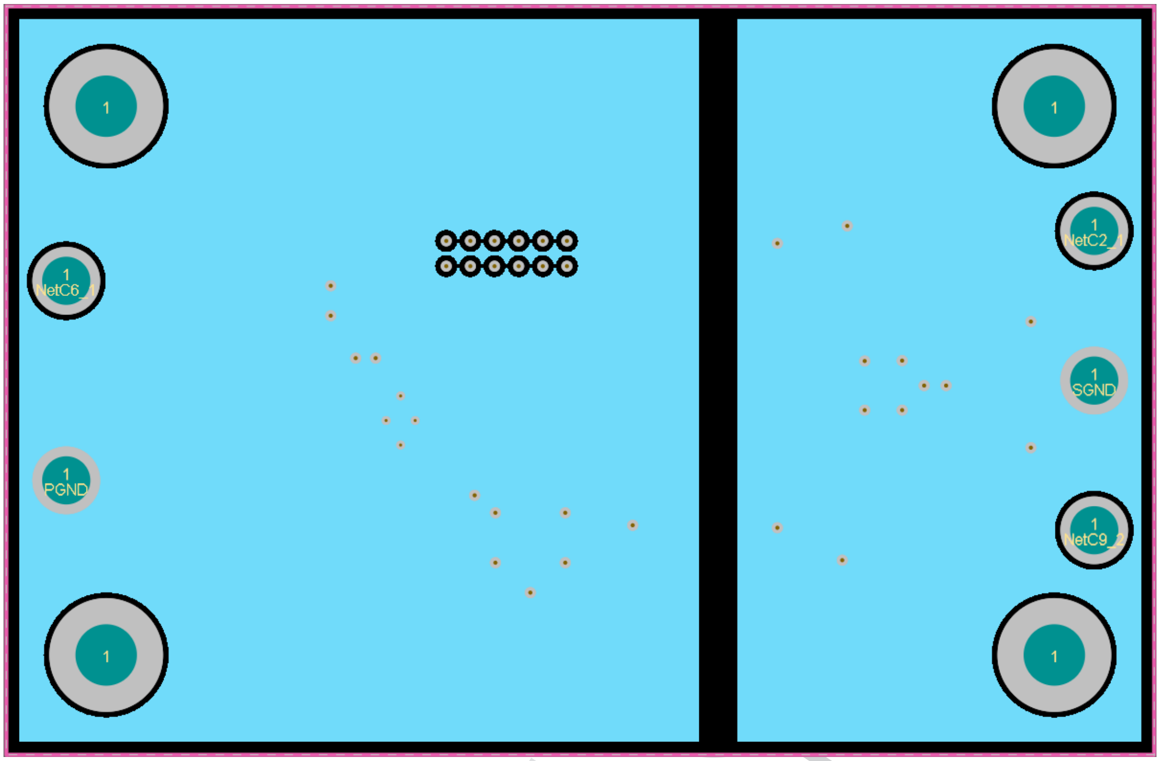

Figure 17. Layer 3 Copper (Top View)

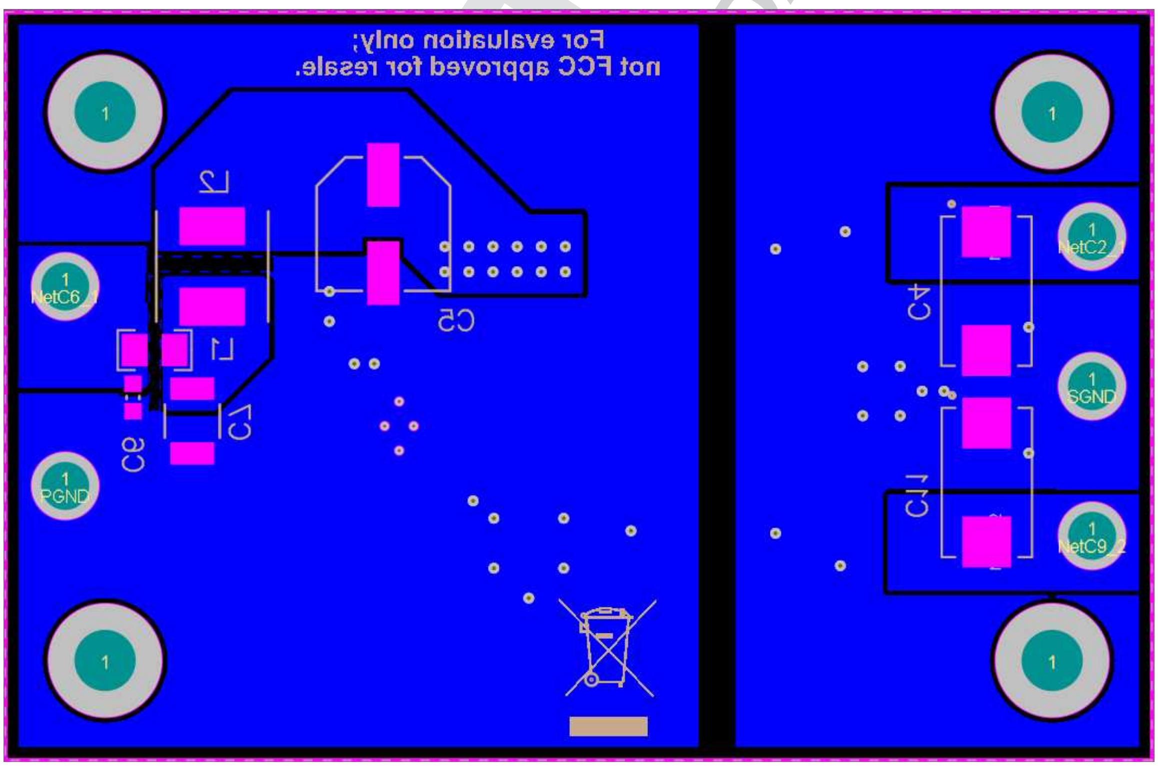

Figure 18. Bottom Copper (Top View)

6.3.1 PCB Layout Tips

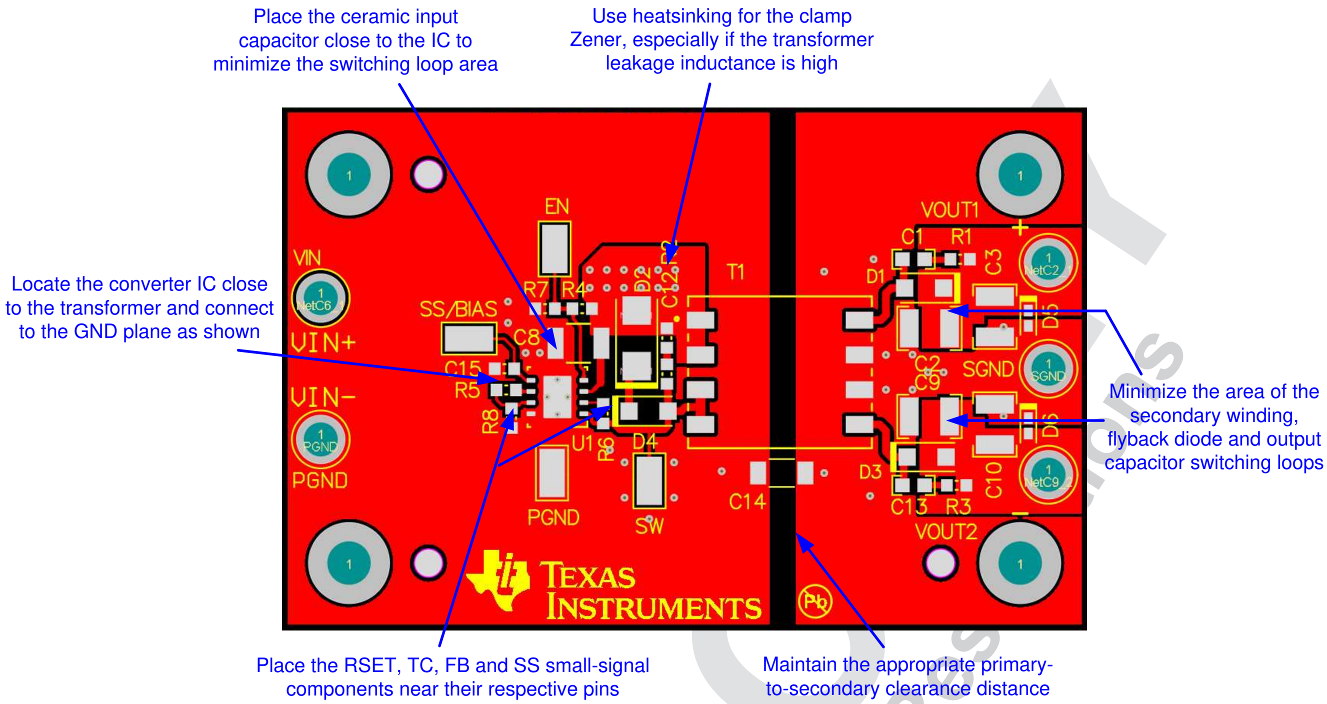

Figure 19. PCB Layout Design Tips for a Dual-output PSR Flyback Converter

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

For development support see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
- LM25184-Q1 PSR Flyback Converter Quickstart Calculator and PSPICE simulation models

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- *LM25184EVM-S12 EVM User's Guide* (SNVU680)
- *LM5180EVM-DUAL Dual-Output EVM User's Guide* (SNVU609)
- *IC Package Features Lead to Higher Reliability in Demanding Automotive and Communications Equipment Systems* (SNVA804)
- *PSR Flyback Transformer Design for mHEV Applications* (SNVA805)
- *How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density* (SLYT779)
- TI Designs:
  - *Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller*
  - *Compact, Efficient, 24-V Input Auxiliary Power Supply Reference Design for Servo Drives*
  - *Reference Design for Power-Isolated Ultra-Compact Analog Output Module*
  - *HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design*
  - *4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers*
  - *Channel-to-Channel Isolated Analog Input Module Reference Design*
- TI Technical Articles:
  - *Flyback Converters: Two Outputs are Better Than One*
  - *Common Challenges When Choosing the Auxiliary Power Supply for Your Server PSU*
  - *Maximizing PoE PD Efficiency on a Budget*
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications* (SLYY104)
  - *An Overview of Conducted EMI Specifications for Power Supplies* (SLYY136)
  - *An Overview of Radiated EMI Specifications for Power Supplies* (SLYY142)
- *Under the Hood of Flyback SMPS Designs* (SLUP261)
- *Flyback Transformer Design Considerations for Efficiency and EMI* (SLUP338)

7.2.1.1 PCB Layout Resources

- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply – Layout Considerations* (SLUP230)
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x* (SNVA721)

- TI Technical Articles:
  - *High-Density PCB Layout of DC-DC Converters*

7.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design by Insight, Not Hindsight* (SNVA419)
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* (SNVA183)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Thermal Design Made Simple with LM43603 and LM43602* (SNVA719)
- *PowerPAD Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)
- *Using New Thermal Metrics* (SBVA025)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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