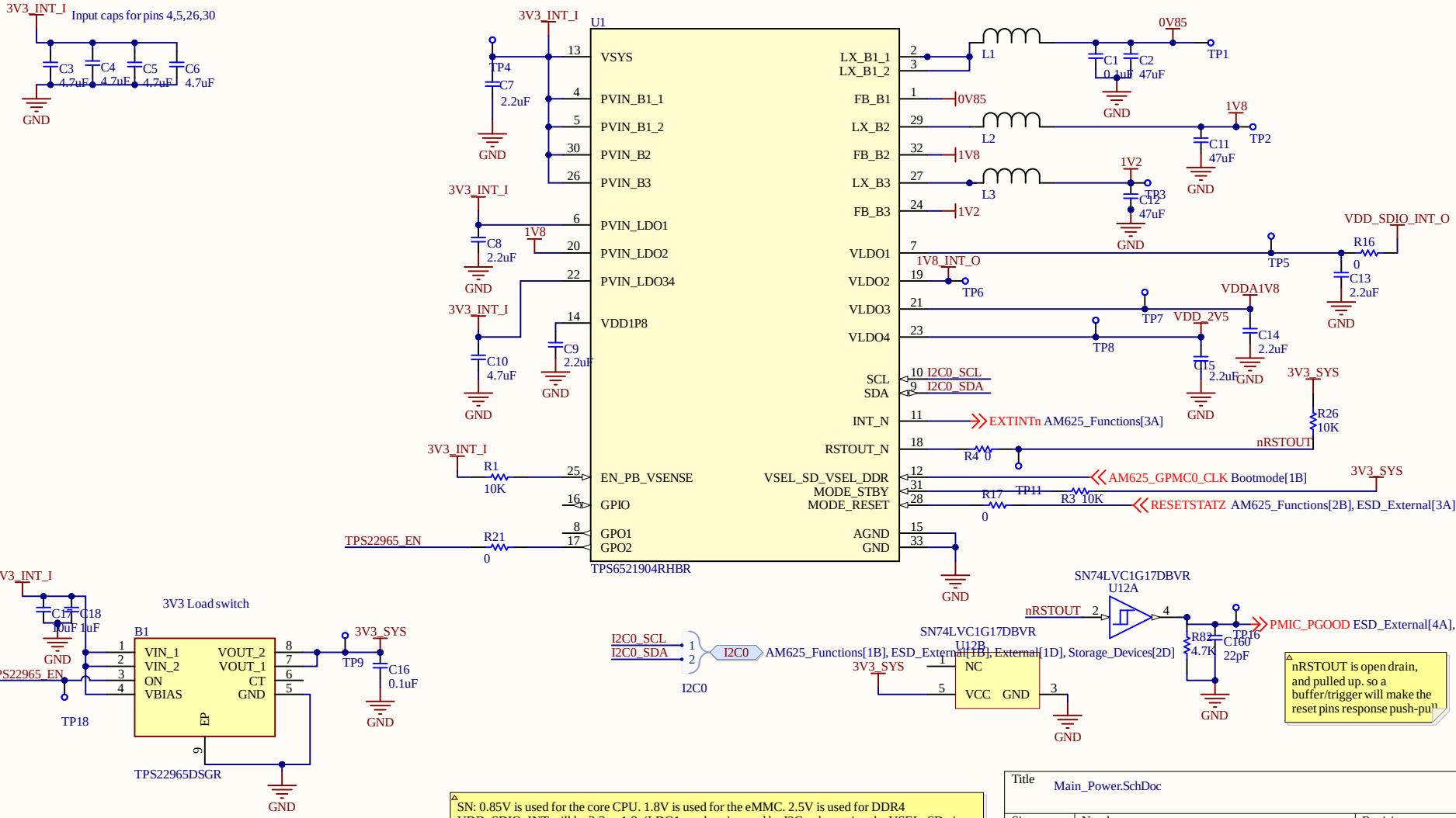
SN: Schematic specific notes
DN: Design/Decision Notes
PN: Notes for PCB layout

SN: 3V3_INT_I comes from the attached interface board as an inbound signal.
VDD_SDIO_INT_O goes to the attached interface board as an output signal for SD card operations
1V8_INT_O goes to the attacvhed interface board as an output signal for peripherals



SN: 0.85V is used for the core CPU. 1.8V is used for the eMMC. 2.5V is used for DDR4
VDD_SDIO_INT will be 3.3 or 1.8. (LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V).)

Title	Main_Power.SchDoc	
Size: A4	Number	Revision
Date: 2/06/2026		Sheet of
File: C:\Users\..\Main_Power.SchDoc		Drawn By:

PN: Decouple caps for VDD_CORE signals. 0.1uF go near SOC pins

VDD_CORE

C19 10uF, C20 4.7uF, C21 1uF, C22 0.1uF, C23 0.1uF, C24 0.1uF, C25 0.1uF, C26 0.1uF, C27 0.1uF, C28 0.1uF, C29 0.1uF, C30 0.1uF, C31 0.1uF, C32 0.1uF, C33 0.1uF, C34 0.1uF, C35 0.1uF, C36 0.1uF, C37 0.1uF, C38 0.1uF

GND

PN: Decouple caps for VDDR_CORE signals.0.1uF go near SOC pins

VDDR_CORE

C47 1uF, C48 4.7uF, C49 0.1uF, C50 0.1uF, C51 0.1uF, C52 0.1uF, C53 0.1uF, C54 0.1uF

GND

PN: Decouple caps for VDD_DDR4 signals.0.1uF go near SOC pins

VDD_DDR4

C39 10uF, C40 4.7uF, C41 1uF, C42 0.1uF, C43 0.1uF, C44 0.1uF, C45 0.1uF, C46 0.1uF

GND

VDDA_1V8

C55 0.1uF

GND

U2A

A1	VSS	VSS	R13
A24	VSS	VSS	R15
A25	VSS	VSS	R18
B25	VSS	VSS	R20
F13	VSS	VSS	T8
G13	VSS	VSS	T13
G19	VSS	VSS	T14
H13	VSS	VSS	T16
H16	VSS	VSS	T17
H18	VSS	VSS	T18
H20	VSS	VSS	U8
J7	VSS	VSS	U19
J13	VSS	VSS	V9
K7	VSS	VSS	V10
K13	VSS	VSS	V11
K15	VSS	VSS	V13
K19	VSS	VSS	V16
L20	VSS	VSS	V18
M7	VSS	VSS	W7
M8	VSS	VSS	Y2
M10	VSS	VSS	AA11
M12	VSS	VSS	AB9
M13	VSS	VSS	AD1
M17	VSS	VSS	AD9
M18	VSS	VSS	AD12
N15	VSS	VSS	AD16
P7	VSS	VSS	AD25
P10	VSS	VSS	AE1
P13	VSS	VSS	AE8
AE25	VSS	VSS	AE12
AE24	VSS	VSS	AE16

XAM6254ATCGGAALW

GND

GND

PN: Decouple caps. 0.1uF go near SOC pins

VDD_3V3

C71 4.7uF, C72 1uF, C73 0.1uF, C74 0.1uF, C75 0.1uF, C76 0.1uF, C77 0.1uF, C78 0.1uF, C79 0.1uF, C80 0.1uF, C82 0.1uF, C83 0.1uF, C84 0.1uF

GND

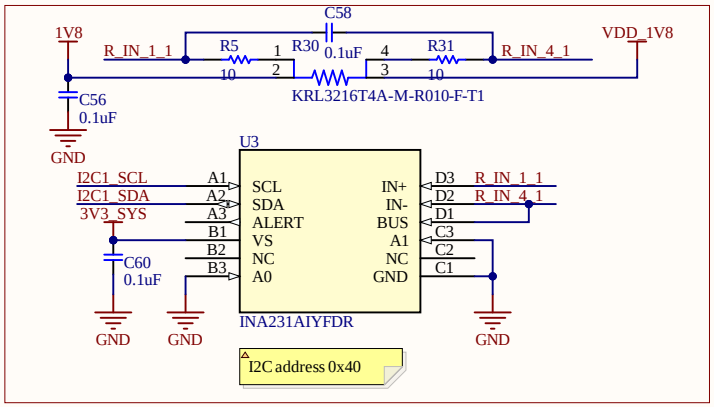
PN: Decouple caps. 0.1uF go near SOC pins

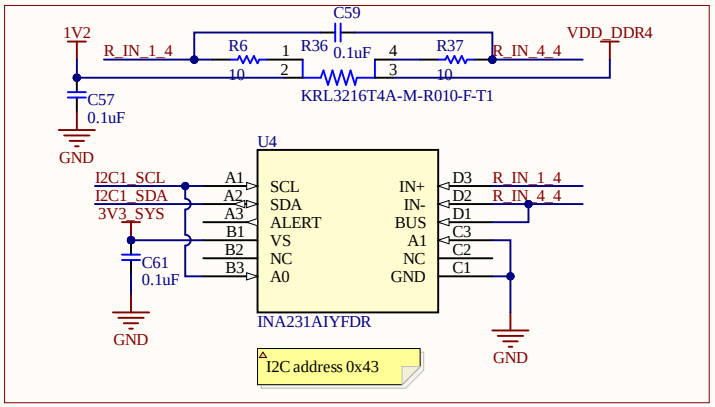
VDD_1V8

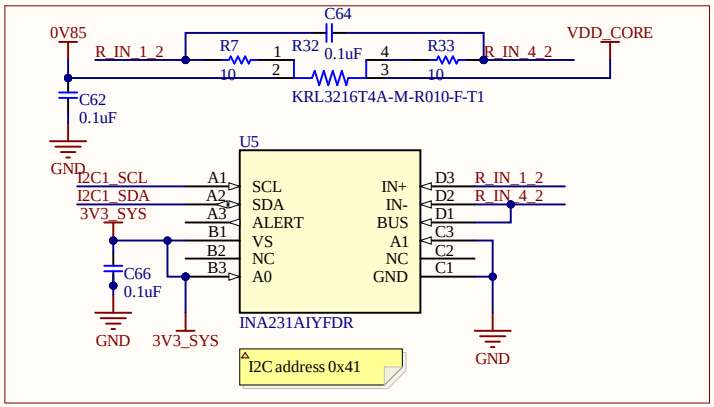
C86 4.7uF, C87 1uF, C88 0.1uF, C89 0.1uF, C90 0.1uF, C91 0.1uF

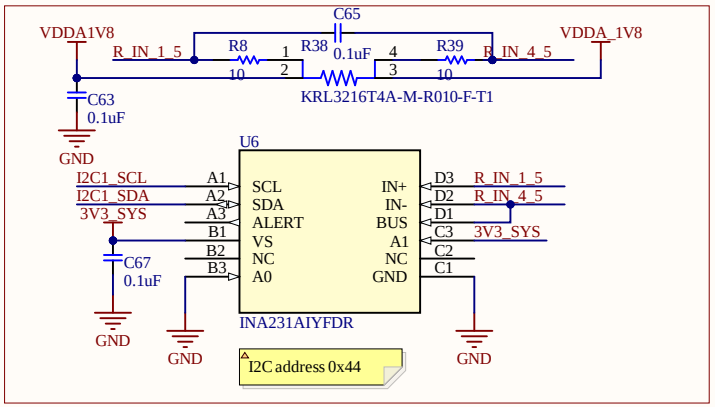
GND

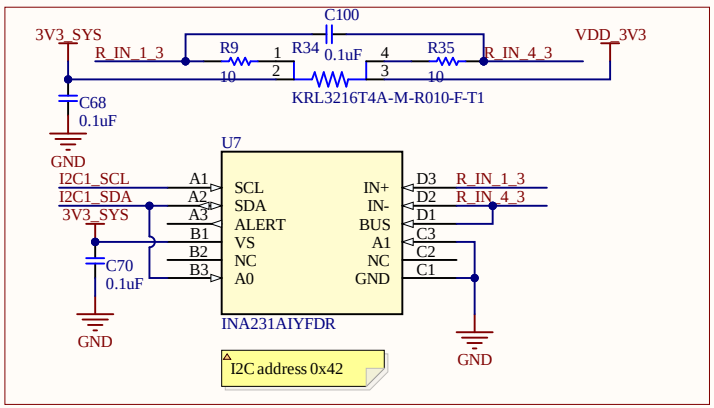
Title	AM625_Power.SchDoc		
Size	Number		Revision
A4			
Date:	2/06/2026	Sheet of	
File:	C:\Users\..\AM625_Power.SchDoc	Drawn By:	

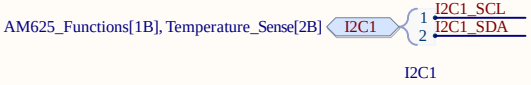








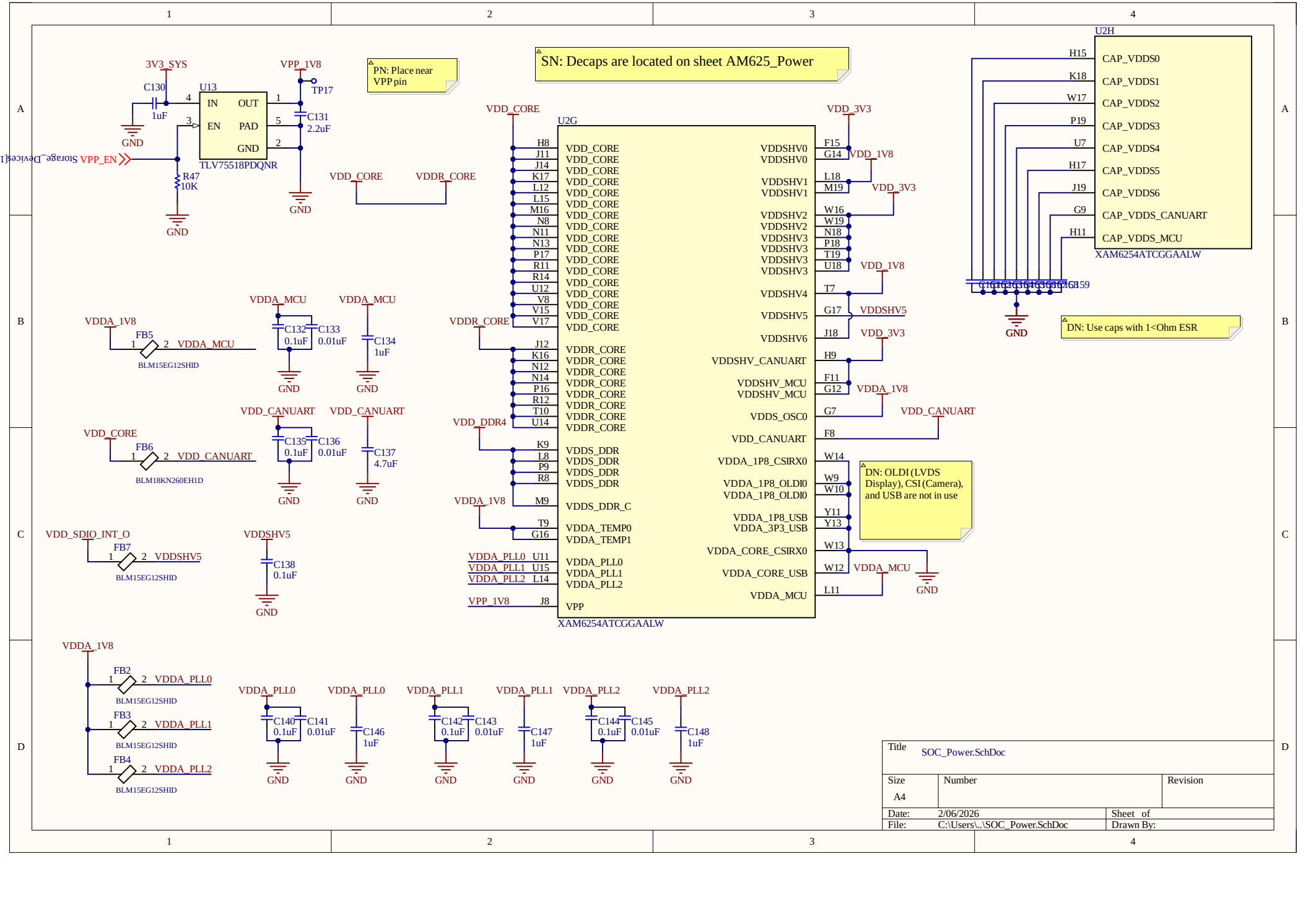


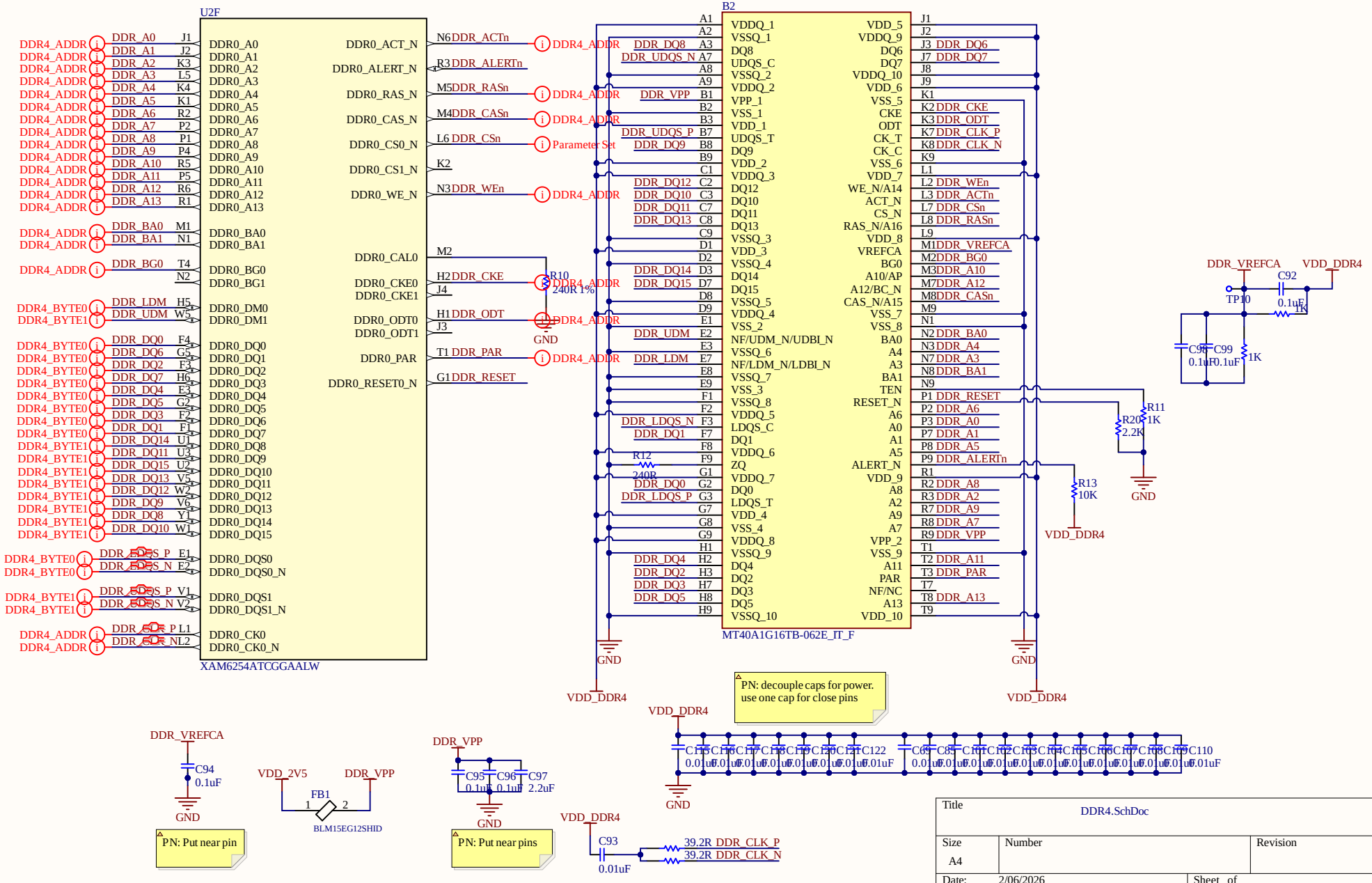


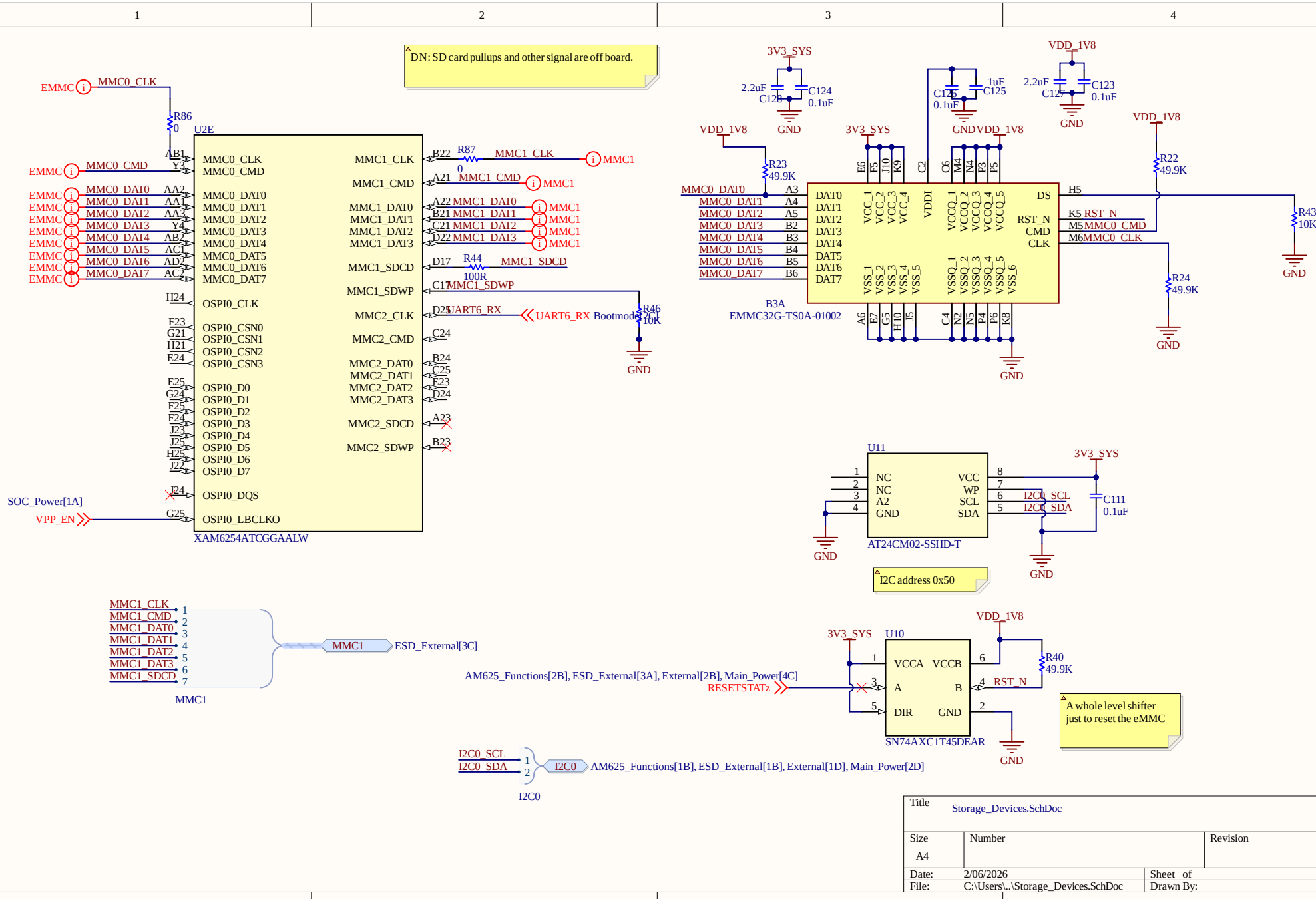
See datasheet table 8-2 for address configurations

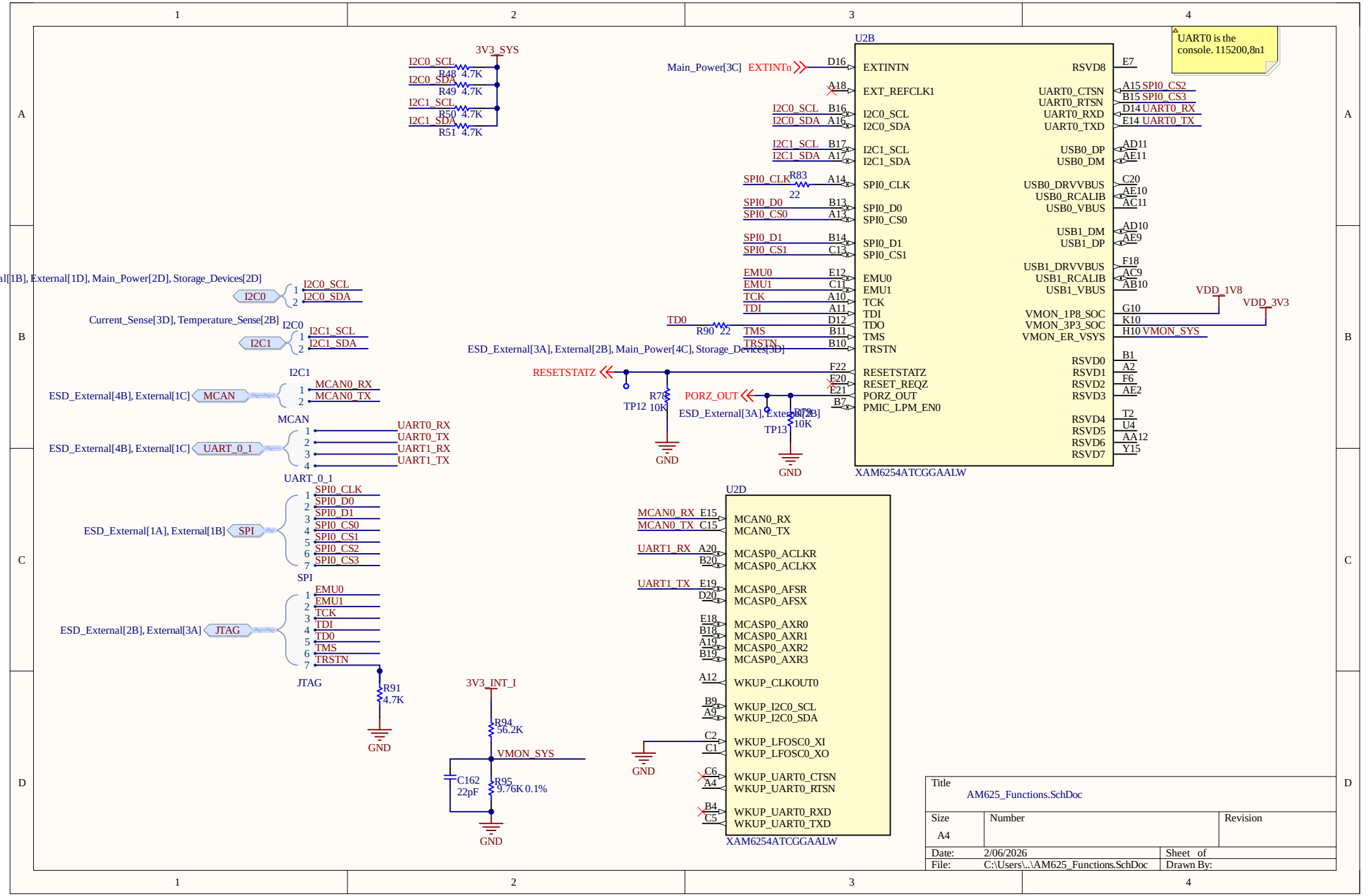
DN: I2C is tied to VDDSHV0 volatge levels

Title: Current_Sense.SchDoc		
Size: A4	Number:	Revision:
Date: 2/06/2026		Sheet of
File: C:\Users\..\Current_Sense.SchDoc		Drawn By:


3V3_SYS
VPP_1V8
C130
1uF
U13
IN
OUT
EN
PAD
GND
TLV75518PDQNR
TP17
C131
2.2uF
R47
10K
VPP_EN
Storage_Devices1
PN: Place near VPP pin
SN: Decaps are located on sheet AM625_Power
VDD_CORE
VDDR_CORE
U2G
XAM6254ATCGGAALW
VDD_3V3
VDD_1V8
VDDSHV5
VDD_CANUART
VDDA_1V8
VDDA_MCU
VDD_DDR4
VDDA_PLL0
VDDA_PLL1
VDDA_PLL2
VPP_1V8
U2H
CAP_VDDS0
CAP_VDDS1
CAP_VDDS2
CAP_VDDS3
CAP_VDDS4
CAP_VDDS5
CAP_VDDS6
CAP_VDDS_CANUART
CAP_VDDS_MCU
XAM6254ATCGGAALW
DN: Use caps with 1<Ohm ESR
DN: OLDI (LVDS Display), CSI (Camera), and USB are not in use
FB5
BLM15EG12SHID
FB6
BLM18KN260EH1D
FB7
FB2
FB3
FB4
C132
0.1uF
C133
0.01uF
C134
1uF
C135
C136
C137
4.7uF
C138
C140
C141
C142
C143
C144
C145
C146
C147
C148
Title
SOC_Power.SchDoc
Size
A4
Number
Revision
Date:
2/06/2026
Sheet of
File:
C:\Users\..\SOC_Power.SchDoc
Drawn By:


U2F
XAM6254ATCGGAALW
B2
MT40A1G16TB-062E_IT_F
DDR_VREFCA
VDD_DDR4
PN: decouple caps for power.
use one cap for close pins
PN: Put near pin
PN: Put near pins
BLM15EG12SHID
GND
Title
DDR4.SchDoc
Size
A4
Number
Revision
Date: 2/06/2026
File: C:\Users\..\DDR4.SchDoc
Sheet of
Drawn By:


DN: SD card pullups and other signal are off board.
XAM6254ATCGGAALW
B3A
EMMC32G-TS0A-01002
AT24CM02-SSHD-T
I2C address 0x50
SN74AXC1T45DEAR
A whole level shifter
just to reset the eMMC
Title
Storage_Devices.SchDoc
Size
A4
Number
Revision
Date:
2/06/2026
Sheet of
File:
C:\Users\..\Storage_Devices.SchDoc
Drawn By:


UART0 is the console. 115200,8n1
U2B
XAM6254ATCGGAALW
U2D
XAM6254ATCGGAALW
3V3_SYS
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
R48 4.7K
R49 4.7K
R50 4.7K
R51 4.7K
Main_Power[3C]
EXTINTn
D16
EXTINTN
A18
EXT_REFCLK1
B16
A16
I2C0_SCL
I2C0_SDA
B17
A17
I2C1_SCL
I2C1_SDA
SPI0_CLK
R83
22
A14
SPI0_CLK
SPI0_D0
SPI0_CS0
B13
A13
SPI0_D0
SPI0_CS0
SPI0_D1
SPI0_CS1
B14
C13
SPI0_D1
SPI0_CS1
EMU0
EMU1
TCK
TDI
TDO
TMS
TRSTN
E12
C11
A10
A11
D12
B11
B10
TD0
R90 22
ESD_External[3A], External[2B], Main_Power[4C], Storage_Devices[3D]
RESETSTATZ
F22
F20
E21
B7
RESETSTATZ
RESET_REQZ
PORZ_OUT
PMIC_LPM_EN0
R78
10K
TP12
GND
PORZ_OUT
ESD_External[3A], External[2B]
R79
10K
TP13
GND
RSVD8
E7
UART0_CTSN
UART0_RTSN
UART0_RXD
UART0_TXD
A15 SPI0_CS2
B15 SPI0_CS3
D14 UART0_RX
E14 UART0_TX
USB0_DP
USB0_DM
AD11
AE11
USB0_DRVVBUS
USB0_RCALIB
USB0_VBUS
C20
AE10
AC11
USB1_DM
USB1_DP
AD10
AE9
USB1_DRVVBUS
USB1_RCALIB
USB1_VBUS
F18
AC9
AB10
VMON_1P8_SOC
VMON_3P3_SOC
VMON_ER_VSYS
G10
K10
H10 VMON_SYS
VDD_1V8
VDD_3V3
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
B1
A2
F6
AE2
T2
U4
AA12
Y15
al[1B], External[1D], Main_Power[2D], Storage_Devices[2D]
I2C0
I2C0_SCL
I2C0_SDA
Current_Sense[3D], Temperature_Sense[2B]
I2C0
I2C1
I2C1_SCL
I2C1_SDA
I2C1
ESD_External[4B], External[1C]
MCAN
MCAN0_RX
MCAN0_TX
MCAN
ESD_External[4B], External[1C]
UART_0_1
UART0_RX
UART0_TX
UART1_RX
UART1_TX
UART_0_1
ESD_External[1A], External[1B]
SPI
SPI0_CLK
SPI0_D0
SPI0_D1
SPI0_CS0
SPI0_CS1
SPI0_CS2
SPI0_CS3
SPI
ESD_External[2B], External[3A]
JTAG
EMU0
EMU1
TCK
TDI
TD0
TMS
TRSTN
JTAG
R91
4.7K
GND
3V3_INT_I
R94
56.2K
VMON_SYS
C162
22pF
R95
9.76K 0.1%
GND
MCAN0_RX E15
MCAN0_TX C15
MCAN0_RX
MCAN0_TX
UART1_RX A20
B20
MCASP0_ACLKR
MCASP0_ACLKX
UART1_TX E19
D20
MCASP0_AFSR
MCASP0_AFSX
E18
B18
A19
B19
MCASP0_AXR0
MCASP0_AXR1
MCASP0_AXR2
MCASP0_AXR3
A12
WKUP_CLKOUT0
B9
A9
WKUP_I2C0_SCL
WKUP_I2C0_SDA
C2
C1
WKUP_LFOSC0_XI
WKUP_LFOSC0_XO
GND
C6
A4
WKUP_UART0_CTSN
WKUP_UART0_RTSN
B4
C5
WKUP_UART0_RXD
WKUP_UART0_TXD
Title
AM625_Functions.SchDoc
Size
A4
Number
Revision
Date: 2/06/2026
Sheet of
File: C:\Users\..\AM625_Functions.SchDoc
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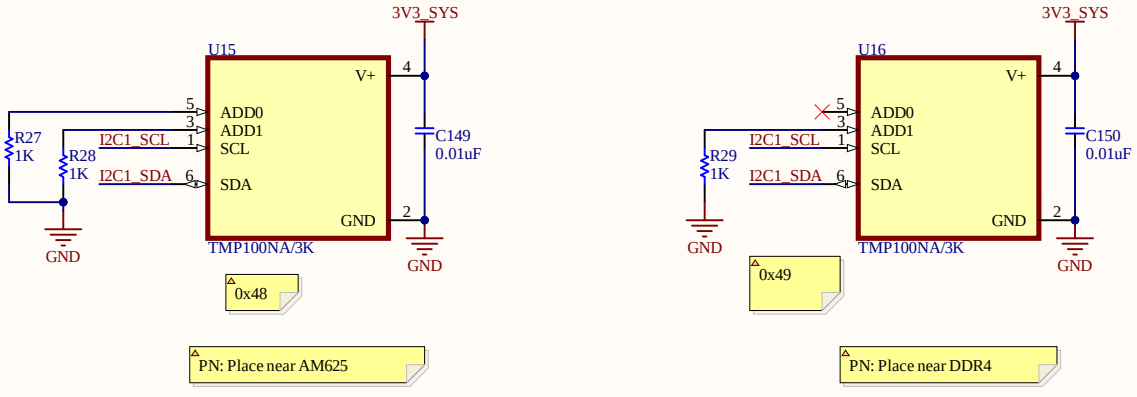

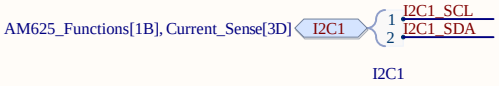

Table 2. Address Pins and Slave Addresses for the TMP100

ADD1	ADD0	SLAVE ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111

Title: Temperature_Sense.SchDoc		
Size: A4	Number:	Revision:
Date: 2/06/2026		Sheet of
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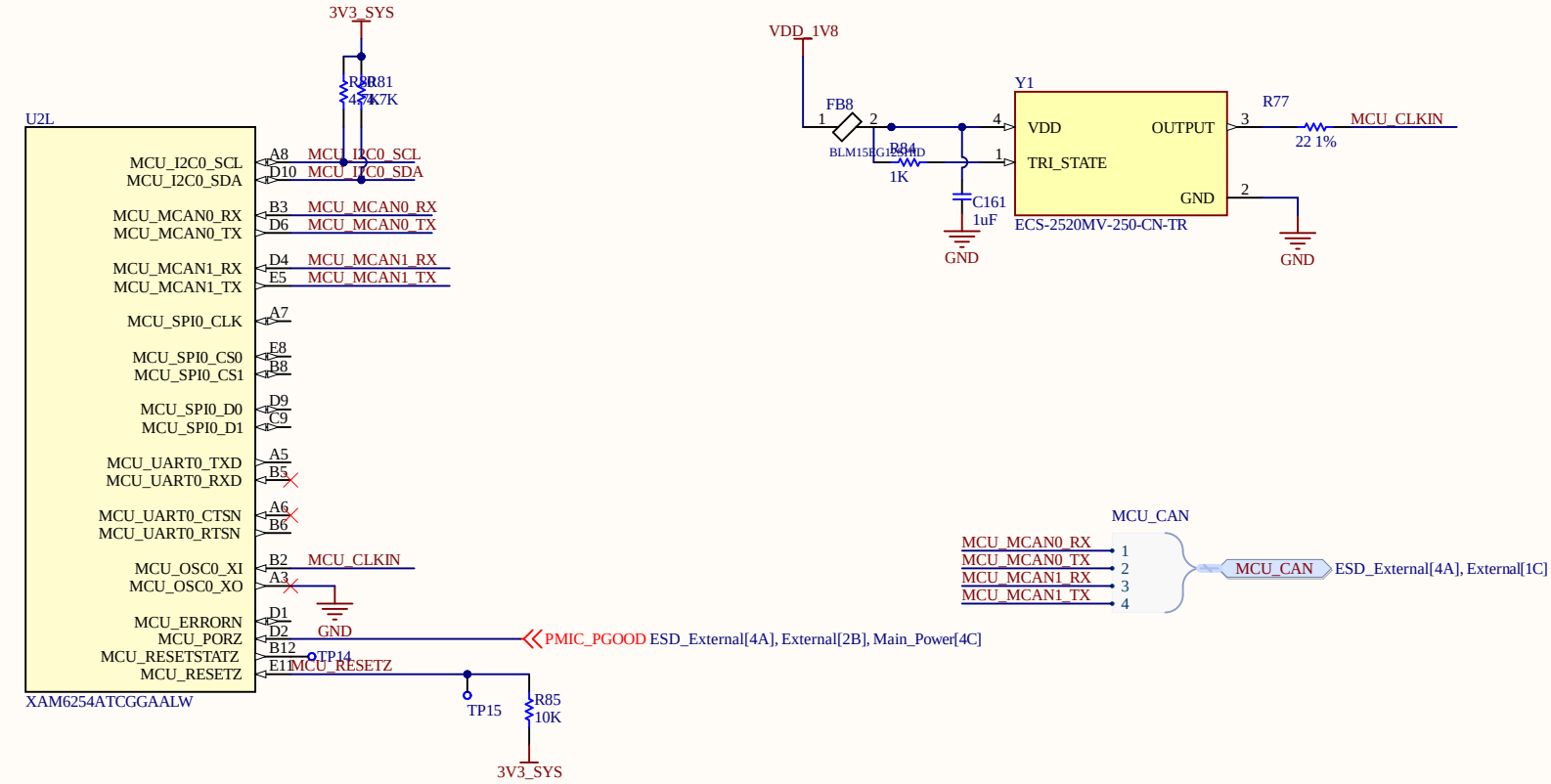

Title	MCU_Domain.SchDoc	
Size: A4	Number	Revision
Date: 2/06/2026		Sheet of
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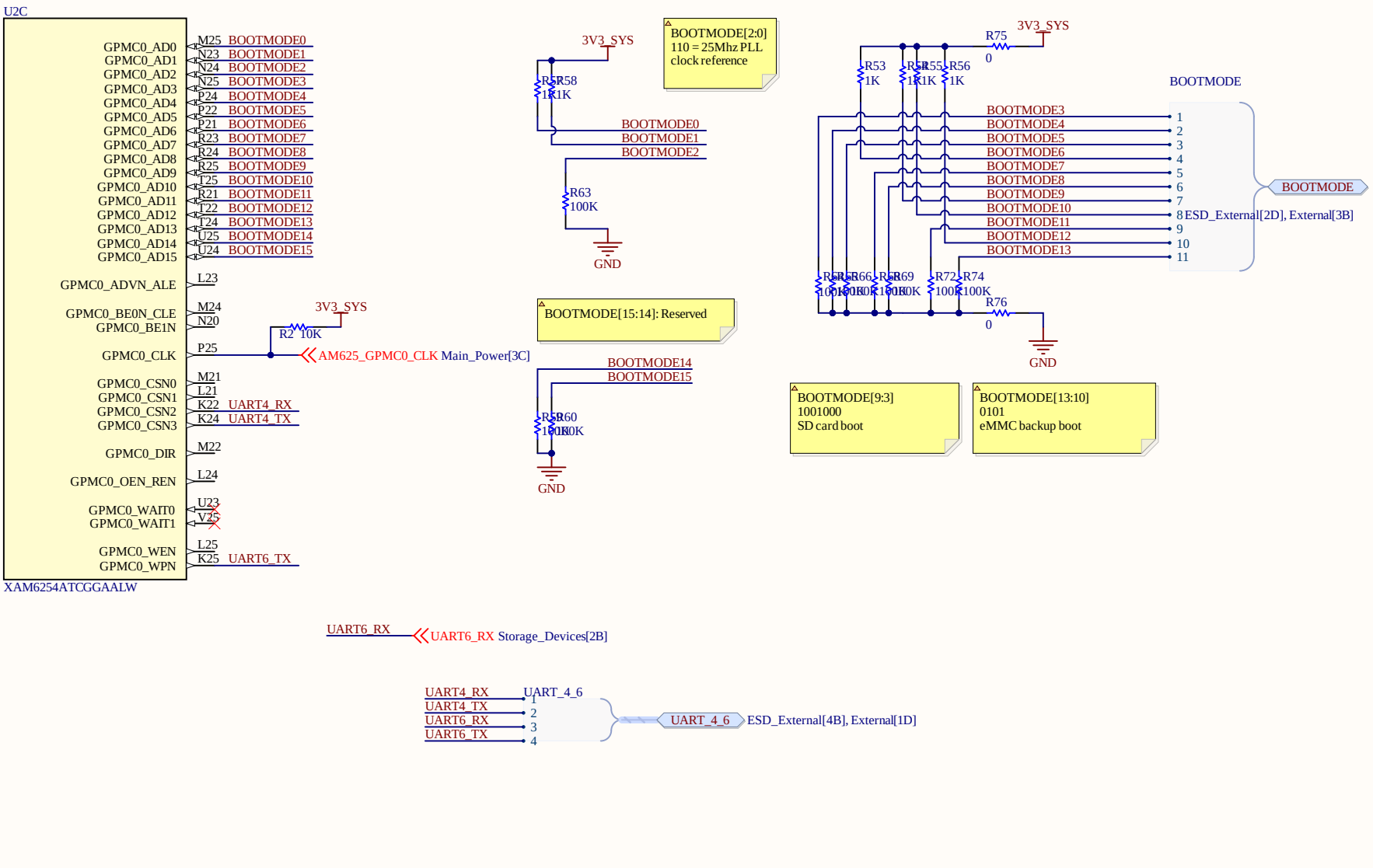
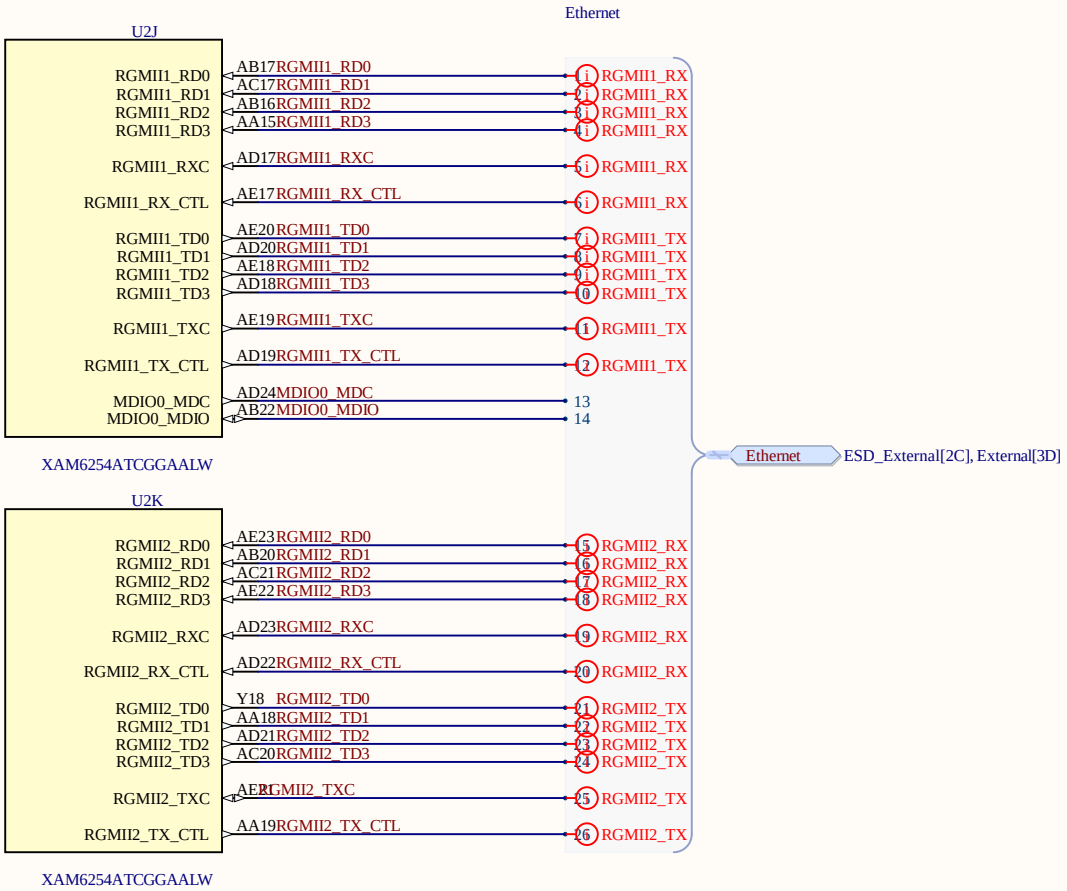

U2C
GPMC0_AD0 M25 BOOTMODE0
GPMC0_AD1 N23 BOOTMODE1
GPMC0_AD2 N24 BOOTMODE2
GPMC0_AD3 N25 BOOTMODE3
GPMC0_AD4 P24 BOOTMODE4
GPMC0_AD5 P22 BOOTMODE5
GPMC0_AD6 P21 BOOTMODE6
GPMC0_AD7 R23 BOOTMODE7
GPMC0_AD8 R24 BOOTMODE8
GPMC0_AD9 R25 BOOTMODE9
GPMC0_AD10 T25 BOOTMODE10
GPMC0_AD11 R21 BOOTMODE11
GPMC0_AD12 T22 BOOTMODE12
GPMC0_AD13 T24 BOOTMODE13
GPMC0_AD14 U25 BOOTMODE14
GPMC0_AD15 U24 BOOTMODE15
GPMC0_ADVN_ALE L23
GPMC0_BE0N_CLE M24
GPMC0_BE1N N20
GPMC0_CLK P25
GPMC0_CSN0 M21
GPMC0_CSN1 L21
GPMC0_CSN2 K22 UART4_RX
GPMC0_CSN3 K24 UART4_TX
GPMC0_DIR M22
GPMC0_OEN_REN L24
GPMC0_WAIT0 U23
GPMC0_WAIT1 V25
GPMC0_WEN L25
GPMC0_WPN K25 UART6_TX
XAM6254ATCGGAALW
3V3_SYS
R2 10K
AM625_GPMC0_CLK Main_Power[3C]
BOOTMODE[2:0]
110 = 25Mhz PLL
clock reference
R58 1K
R63 100K
BOOTMODE[15:14]: Reserved
R60 100K
R75 0
R53 1K
R54 1K
R55 1K
R56 1K
R76 0
BOOTMODE
BOOTMODE3
BOOTMODE4
BOOTMODE5
BOOTMODE6
BOOTMODE7
BOOTMODE8
BOOTMODE9
BOOTMODE10
BOOTMODE11
BOOTMODE12
BOOTMODE13
ESD_External[2D], External[3B]
R65 R66 R67 R68 R69 R72 R74 100K
BOOTMODE[9:3]
1001000
SD card boot
BOOTMODE[13:10]
0101
eMMC backup boot
UART6_RX
UART6_RX Storage_Devices[2B]
UART4_RX
UART4_TX
UART6_RX
UART6_TX
UART_4_6
UART_4_6 ESD_External[4B], External[1D]
Title Bootmode.SchDoc
Size A4
Number
Revision
Date: 2/06/2026
Sheet of
File: C:\Users\..\Bootmode.SchDoc
Drawn By:



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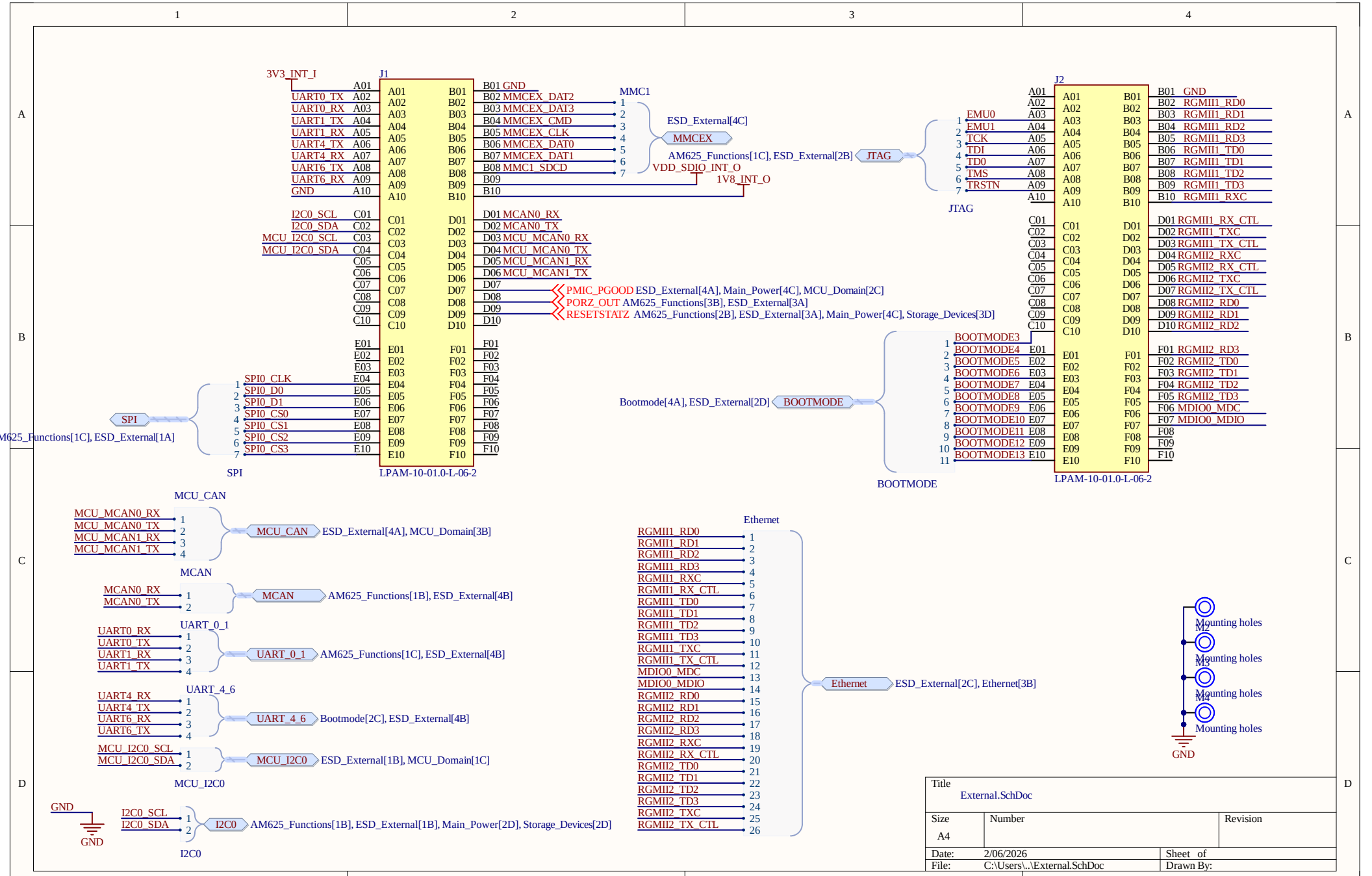

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Date: 2/06/2026	Sheet of	
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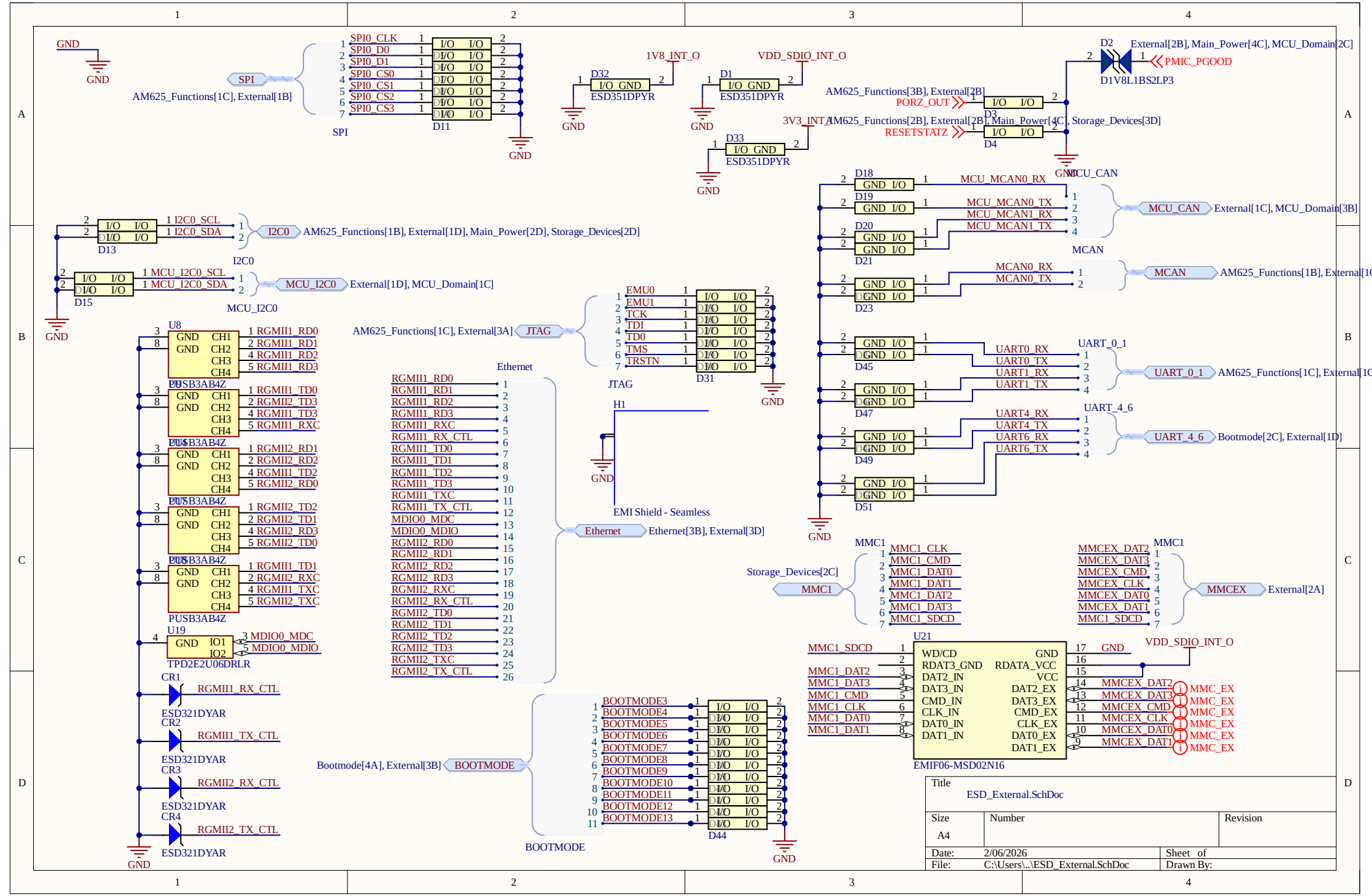
SPI
SPI0_CLK
SPI0_D0
SPI0_D1
SPI0_CS0
SPI0_CS1
SPI0_CS2
SPI0_CS3
AM625_Functions[1C], External[1B]
D11
D32
D1
D33
ESD351DPYR
1V8_INT_O
VDD_SDIO_INT_O
3V3_INT_O
PORZ_OUT
RESETSTATZ
AM625_Functions[3B], External[2B]
AM625_Functions[2B], External[2B], Main_Power[4C], Storage_Devices[3D]
D2
D1V8L1BS2LP3
External[2B], Main_Power[4C], MCU_Domain[2C]
PMIC_PGOOD
D3
D4
I2C0
I2C0_SCL
I2C0_SDA
AM625_Functions[1B], External[1D], Main_Power[2D], Storage_Devices[2D]
D13
MCU_I2C0
MCU_I2C0_SCL
MCU_I2C0_SDA
External[1D], MCU_Domain[1C]
D15
MCU_CAN
MCU_MCAN0_RX
MCU_MCAN0_TX
MCU_MCAN1_RX
MCU_MCAN1_TX
External[1C], MCU_Domain[3B]
D18
D19
D20
D21
MCAN
MCAN0_RX
MCAN0_TX
AM625_Functions[1B], External[1C]
D23
JTAG
AM625_Functions[1C], External[3A]
EMU0
EMU1
TCK
TDI
TDO
TMS
TRSTN
D31
UART_0_1
UART0_RX
UART0_TX
UART1_RX
UART1_TX
AM625_Functions[1C], External[1C]
D45
UART_4_6
UART4_RX
UART4_TX
UART6_RX
UART6_TX
Bootmode[2C], External[1D]
D47
D49
D51
U8
PUSB3AB4Z
RGMII1_RD0
RGMII1_RD1
RGMII1_RD2
RGMII1_RD3
RGMII1_TD0
RGMII1_TD1
RGMII1_TD2
RGMII1_TD3
RGMII1_RXC
RGMII1_RX_CTL
RGMII1_TXC
RGMII1_TX_CTL
RGMII2_RD0
RGMII2_RD1
RGMII2_RD2
RGMII2_RD3
RGMII2_TD0
RGMII2_TD1
RGMII2_TD2
RGMII2_TD3
RGMII2_RXC
RGMII2_RX_CTL
RGMII2_TXC
RGMII2_TX_CTL
U19
TPD2E2U06DRLR
MDIO0_MDC
MDIO0_MDIO
CR1
CR2
CR3
CR4
ESD321DYAR
Ethernet
Ethernet[3B], External[3D]
H1
EMI Shield - Seamless
Storage_Devices[2C]
MMC1
MMC1_CLK
MMC1_CMD
MMC1_DAT0
MMC1_DAT1
MMC1_DAT2
MMC1_DAT3
MMC1_SDCD
MMCEX
External[2A]
MMCEX_DAT2
MMCEX_DAT3
MMCEX_CMD
MMCEX_CLK
MMCEX_DAT0
MMCEX_DAT1
U21
EMIF06-MSD02N16
WD/CD
RDAT3_GND
DAT2_IN
DAT3_IN
CMD_IN
CLK_IN
DAT0_IN
DAT1_IN
GND
RDATA_VCC
VCC
DAT2_EX
DAT3_EX
CMD_EX
CLK_EX
DAT0_EX
DAT1_EX
MMC_EX
BOOTMODE
Bootmode[4A], External[3B]
BOOTMODE3
BOOTMODE4
BOOTMODE5
BOOTMODE6
BOOTMODE7
BOOTMODE8
BOOTMODE9
BOOTMODE10
BOOTMODE11
BOOTMODE12
BOOTMODE13
D44
GND
Title
ESD_External.SchDoc
Size
A4
Number
Revision
Date:
2/06/2026
Sheet of
File:
C:\Users\..\ESD_External.SchDoc
Drawn By: