Application Report
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# Comparing the Performance and Thermal Properties of a DC/DC Converter in the SOT23 and new SOT563 Packaging Technologies

*Sabrina Ramalingam*

**ABSTRACT**

This application report compares the thermal performance of flip-chip on lead (FCOL) SOT563 package with the conventional wire-bond SOT23 packages and FCOL SOT23 package. It summarizes the packages thermal results and explains the advantages and disadvantages for electronic board design. The results show that FCOL packages have better thermal dissipation capabilities, with the SOT563 being on top a 65% smaller package than SOT23.

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## Trademarks



# 1 Introduction

There is a strong trend towards smaller form factors in electronic board designs. At the same time, there is also an increasing need for more power rails and, in some cases, higher currents to supply digital cores like Micro-Controller Units (MCU), field-programmable Gate Arrays (FPGA), or other embedded processors. In terms of power design, this translates into the need for integrated circuits (ICs) with higher power density where thermal design becomes critical to achieve the required performance without compromising cost. This application report focuses on DC/DC converters in SOT23 and the new, 65% smaller, SOT563 packages. More specifically on the performance differences of a same non-isolated 5-V/2-A buck converter (TLV62569) in three different packages: SOT 23-5, SOT23-6, and SOT563.

After an overview of the SOT23 and SOT563 packaging technology, this application report shows the thermal performances of the TLV62569 in different packages and discusses the impact in specific power designs. Finally, it summarizes the advantages of each package in order to help the designer choose the right package for addressing key challenges in his/her end equipment.

# 2 Describing the TLV62569 Package Technologies: SOT23-5, SOT23-6, and SOT563

The TLV62569 device is a synchronous step-down converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 2 A. As shown in Table 1, this device is available in three different packages: SOT23-5, SOT23-6, and SOT563. In the three packages, the die area remains the same for this device.

**Table 1. Device Information**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV62569DBV | SOT23 (5) | 2.90-mm × 2.80-mm |
| TLV62569PDDC | SOT23 (6) | |
| TLV62569DRL | SOT563 (6) | 1.60-mm × 1.60-mm |
| TLV62569PDRL | SOT563 (6) | |

As of today, SOT23 packages are widely used in several applications because of their ease of use.

Even though the SOT23-5 (DBV) and SOT23-6 (DDC) share the same package appearance with the same footprint dimensions, these two packages use different interconnection between silicon and package itself. The SOT23-5 (DBV) is designed with a bonding wire interconnection structure whereas the SOT23-6 uses the Flip Chip On Lead (FCOL) approach. Connecting the IC with wire bonds using copper, gold, or aluminum wires inside the package has the advantage of being flexible and cost effective. However, it requires space and the bonding wires add parasitic inductance and resistance on the pins. On the contrary, with the FCOL package technology, copper bumps are used as interconnection and they are directly located on the die. Therefore there is no additional parasitic inductance and resistance added due to the interconnection structure. For more details on SOT23-5 and SOT23-6 packages, see the *SOT23 Package Thermal Consideration Application Report*.

Similar to the SOT23-6, the new SOT563 (DRL) package is also based on FCOL bonding structure. Thanks to innovations in packaging structures and lead frame designs, it is possible to achieve a 65% smaller IC package compared to SOT23-5 and SOT23-6 for the same die area without compromising thermal performance. Table 4 shows that the junction to top and junction to board thermal characteristics $\psi_{JT}$ and $\psi_{JB}$ are the smallest for the DRL package, translating directly in a better heat dissipation of the junction to top and junction to board.

# 3 Understanding Thermal Performance and Junction Temperature Estimation

## *3.1 Understanding Thermal Performance*

Having good thermal performances could have various meanings depending on the end equipment (EE).

Some systems, like Industrial PCs, have a specified board temperature you cannot exceed. In this case, the board designer has to ensure that the heat dissipation of the IC is optimized through a good layout and cooling system. In other end equipment, like security cameras, a defined operating ambient temperature is required and the designer needs to ensure that the IC stays within the specified recommended operating junction temperature for reliable operation. In other systems, like Solid State Drive (SSD) Memories, the board heats up mainly from other ICs, like the SSD controller. In such cases, the heat dissipation through the board is limited due to its restricted size and form factor. The system designer needs to make sure the power IC package is able to support a good board to top heat dissipation in oder to stay within the recommended junction temperature and avoid unwanted behavior like thermal shutdown.

## 3.2 Estimating Junction Temperature

The junction temperature of the IC is a crucial parameter for good thermal design. For further details on thermal parameters of ICs, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

The reliable method to estimate the junction temperature of a DC/DC converter is to use the junction-to-board characterization parameter of the IC, $\psi_{JT}$ , specified in table 2 of the *TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package Data Sheet* with equation 1.

$$T_j = \psi_{JT} \times P_{IC,\ diss} + T_{case} \quad (1)$$

**Table 2. Variables Description for Junction Temperature Calculation**

| PARAMETER | DESCRIPTION | COMMENTS |
|---|---|---|
| $T_j$ | IC junction temperature | Target value to calculate |
| $T_{case}$ | IC case temperature | Can be easily measured for given operating condition with a thermal camera as shown on figure 1. |
| $\psi_{JT}$ | Junction-to-top characterization parameter | Specified in the *TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package Data Sheet*. See table 1. |
| $P_{IC,\ diss}$ | Dissipated power in the IC for the given operating conditions | This parameter needs to be estimated carefully to have more reliable results (see below). |

There are two ways to estimate the IC power dissipation $P_{IC,diss}$. The first and easiest way to estimate $P_{IC,diss}$ is the WEBENCH® Power Designer Tool for the required operating conditions. The second way is to use Equation 2:

$$P_{IC,diss} = P_{diss} - P_{ind} \quad (2)$$

**Table 3. Variables Description for IC Power Dissipation Calculation**

| PARAMETER | DESCRIPTION | COMMENTS |
|---|---|---|
| $P_{IC,\ diss}$ | IC power dissipation | |
| $P_{diss}$ | Total dissipated power<br>$P_{diss} = (1 - n) \times (P_{out} / \eta)$ | $P_{out}$: Output power |
| | | $\eta$ : Efficiency of the power stage – can be found in the *TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package Data Sheet* or modeled in WEBENCH® |
| $P_{ind}$ | DC power losses in inductor<br>$P_{ind} = DCR \times I_{out}^2$ | DCR: inductor series resistor |
| | | This parameter can be simulated in some manufacturer's website or in WEBENCH® |

It is important to model the dissipated power in the inductor in order to have a more reliable estimation of the junction temperature. As rule of thumb, it is good enough to model only the DC losses of the inductor.

**Table 4. IC Thermal Information**

| THERMAL METRIC | DEV (5 PINS) | DDC (6 PINS) | DRL (6 PINS) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | 188.2 | 106.2 | 146.3 | °C/W |
| $R_{\theta JC(top)}$ | 137.5 | 52.9 | 51.0 | °C/W |
| $R_{\theta JB}$ | 41.2 | 31.2 | 27.0 | °C/W |
| $\psi_{JT}$ | 31.4 | 11.3 | 2.2 | °C/W |
| $\psi_{JB}$ | 40.6 | 31.6 | 27.6 | °C/W |
| $R_{\theta JC(bot)}$ | N/A | N/A | N/A | °C/W |

In this section, the different relevance of thermal performance across EE applications were explained and the important parameters for good thermal performance evaluation were introduced. The next section focuses on the specific thermal performance of the TLV62569 across the three different packages: SOT23-5, SOT23-6, and SOT563.

## 4 Measurement Setup and Test Results

This section shows a comparison of the performances of the TLV62569 which has the same die area in the three packages: SOT23-5 (DBV), SOT23-6 (DDC), and SOT563 (DRL).

For analyzing the thermal performance across the three different packages, the efficiency is measured on the three different Evaluation Modules (EVM) shown in Table 5. The case temperature is measured with a thermal camera as shown in Figure 1 and the junction temperature is estimated using Equation 1 as explained in the previous section.

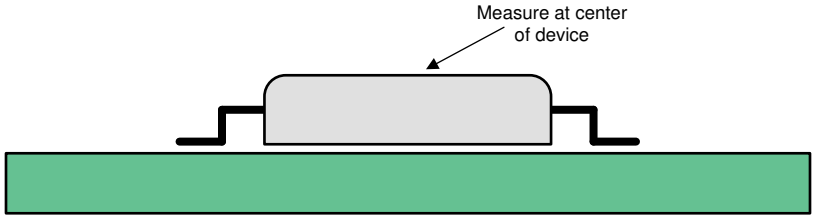
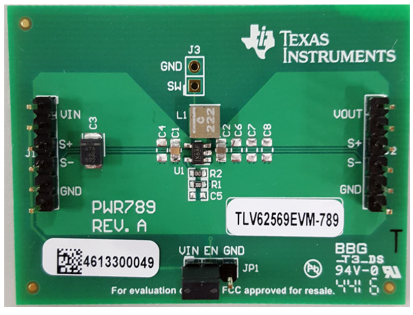
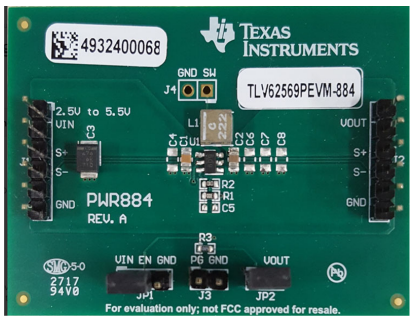
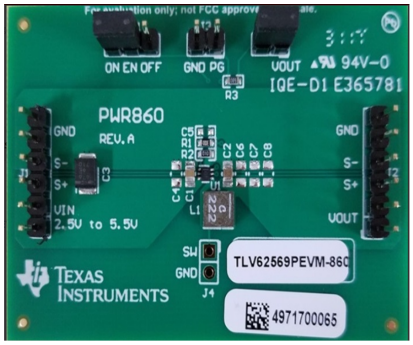



**Figure 1. Case Temperature Measurement with a Thermal Camera**

**Table 5. EVMs Used for Measurements**

| SOT23-5 PACKAGE (DBV) TLV62569EVM-789 | SOT23-6 PACKAGE (DDC) TLV62569EVM-884 | SOT563 PACKAGE (DRL) TLV62569EVM-860 |
|---|---|---|
|  |  |  |

## 4.1 Efficiency Measurements

For all the EVM boards using the same Bill of Materials (BOM) excluding the TLV62569 ICs, the efficiency is measured for an input voltage of Vin = 5.0 V and an output voltage of Vout = 3.3 V.

Figure 2 shows the results and the following two key points can be derived:

| OUTPUT CURRENT < 1 A | OUTPUT CURRENT > 1 A |
|---|---|
| SOT23-5 and SOT23-6 packages have similar efficiency up to 1A | Difference between SOT23-5, SOT23-6 and SOT563 is less significant than for light loads |
| SOT563 has the best efficiency up to 96.5%. | SOT23-6 has the best efficiency for loads above 1.5A |

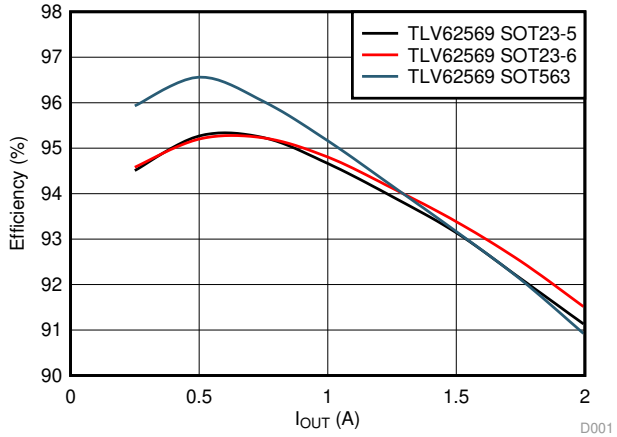
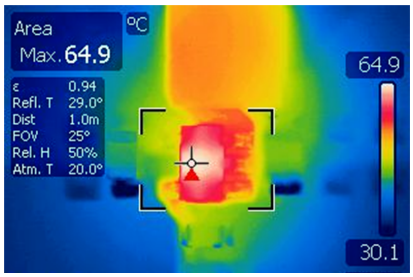
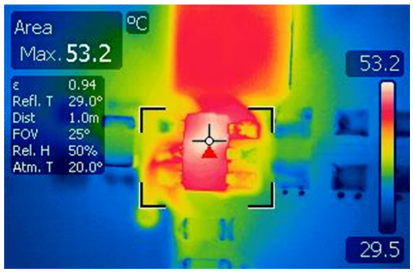
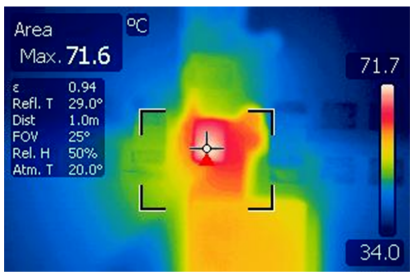



**Figure 2. Efficiency Measurements on TLV62569 EVMs for Vin = 5 V and Vout = 3.3 V**

## 4.2 Thermal Measurements

As a first step to evaluate the thermal performances on all three EVM boards, the case temperature of the IC is measured using a thermal camera for Vin = 5 V, Vout = 3.3 V over a load range of 250 mA to 2 A. Table 6 show an example of thermal pictures captured for Iout = 2A.

**Table 6. Thermal Picture on TLV62569 EVMs at Vin = 5 V, Vout = 3.3 V, and Iout = 2 A**

| SOT23-5 PACKAGE | SOT23-6 PACKAGE | SOT563 PACKAGE (DRL) |
|---|---|---|
|  |  |  |
| Case temperature: $T_{case}$ = 65°C | Case temperature: $T_{case}$ = 53°C | Case temperature $T_{case}$ = 72°C |



The results of IC case temperature measurements over the entire load range up to 2 A are compiled in Figure 3. As a next step, the junction temperatures of the IC in the three different packages are deducted using Equation 1. Figure 4 shows the results.

The thermal measurements are represented versus output current and IC power dissipation to demonstrate the linear relation between IC temperature and IC power dissipation on each of the EVMs.

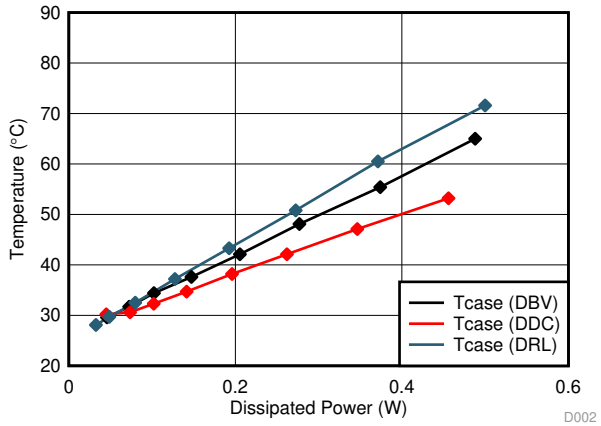



**Figure 3. Case Temperature vs. Dissipated Power**

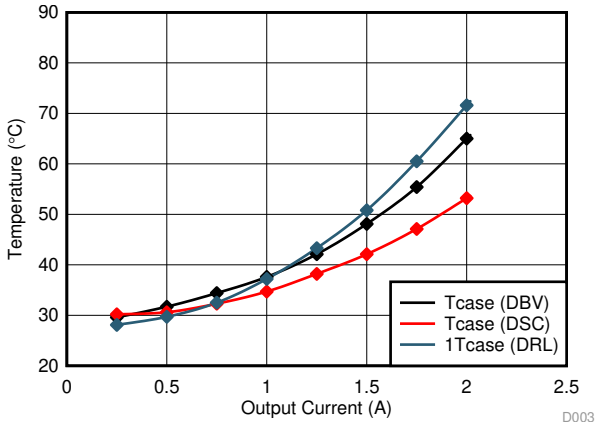



**Figure 4. Case Temperature vs. Output Current**

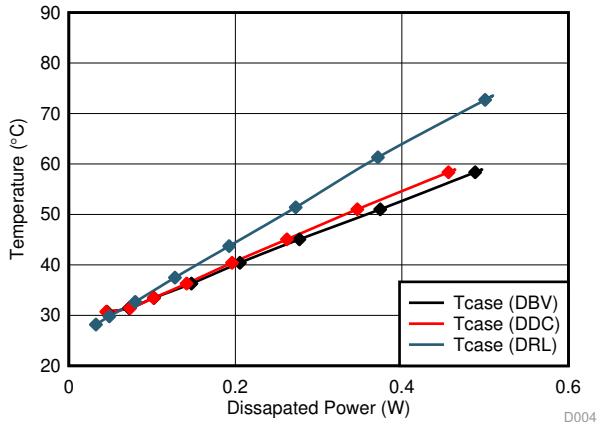



**Figure 5. Calculated Junction Temperature vs. Dissipated Power**

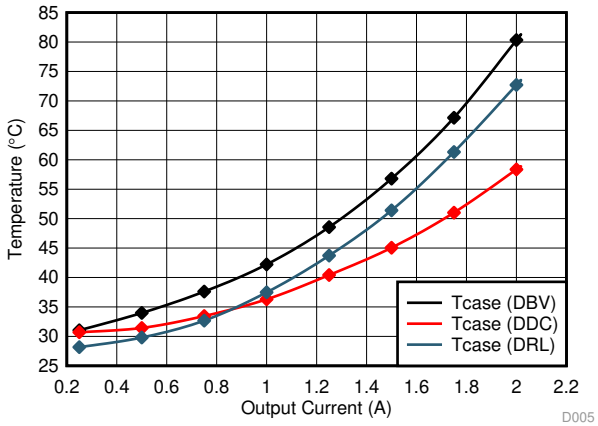



**Figure 6. Calculated Junction Temperature vs. Output current**

Thermal performances are critical for higher load current as power dissipation becomes a challenge with conduction losses increasing.

**Table 7. Thermal Performance at Vin = 5 V, Vout = 3.3 V, and Iout = 2 A**

| DEVICE | CASE TEMPERATURE | JUNCTION TEMPERATURE | TEMPERATURE RAISE |
|---|---|---|---|
| SOT23-5 (DBV) | 65°C | 80°C | ~15°C |
| SOT23-6 (DDC) | 53°C | 58°C | ~5°C |
| SOT563 (DRL) | 71.6°C | 72°C | ≤1°C |

From graphs on Figure 2, Figure 3, and Table 7, three main observations can be made:

- SOT23-5 has the highest junction temperature.
- SOT23-6 has the lowest Junction and case temperature.
- SOT563 has the lowest junction to top temperature raise.

This section concentrated on the method to measure and estimate IC temperature and tangible results were shown for the TLV62569. Moving forward, the focus is set on the analysis of these measurement results and the meaning in terms of IC packaging.

# 5 Thermal Performance Analysis for SOT23-5, SOT23-6, and SOT563 Packages

Measurements done in the previous section show the performance of a same device TLV62569, with a same die area in three different packages. In other words, the measurements show just the difference in packages, excluding impact of the standalone die. This section focuses on analyzing the impact of each package on the performance of the device and understanding which package is more suitable to address a specific key requirement of the end equipment.

## 5.1 Comparing SOT563 (DRL) and SOT23-6 (DDC)

As observed in the previous section, with a lower junction and case temperature, SOT23-6 package offers improved thermal performances over the SOT563. Although both packages use FCOL technology, SOT23-6 package leadframe design has a bigger copper area which reduces the parasitic impedance and allows more power dissipation, which translates into higher efficiency at heavy loads and improved thermal performances respectively.

On the other side, the SOT563 offer better efficiency at light loads. Also SOT563 (DRL) package is 65% smaller than the SOT23-6 (DDC), enabling much smaller design for space critical designs.

## 5.2 Comparing SOT23-6 (DDC) and SOT23-5 (DBV)

Compared to SOT23-5, the SOT23-6 has better thermal performances with 10°C lower junction temperature and 12°C lower case temperature for the 2-A load. In addition, the SOT23-6 (DDC) package offers better efficiency at heavy loads as shown in Figure 4. For further detailed comparison between these two packages, see the *SOT23 Package Thermal Consideration Application Report*.

## 5.3 Comparing SOT563 (DRL) and SOT23-5 (DBV)

Compared to SOT563 (DRL), the SOT23-5 (DBV) package seems to have a better thermal performance with a lower case temperature, with $T_{case}$ = 65°C, than SOT563, $T_{case}$ = 71°C (see Table 7). However, SOT23-5 package has the highest junction temperature, $T_{junction}$ = 80°C, for the same operating conditions over the three packages. The system designer has to be careful and take in account this aspect when deciding upon which package option to choose. With the SOT563 package, the junction temperature is almost equal to the case temperature, (lower than for SOT23-5 package), which allows easier control of junction temperature. This aspect is reflected in the $\psi_{JT}$ parameter of the *TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package Data Sheet*.

The SOT563 package also offers higher light load efficiency than SOT23-5, thanks to FCOL technology where there are no losses through the internal bond wires. The third biggest advantage of the SOT563 (DRL) over the SOT23-5 (DBV) and SOT23-6 (DBV) is the package size (-65%). SOT563 (DRL) is a more recent package technology innovation that allows a smaller package size (see Figure 7), higher power density, and improved thermal dissipation.

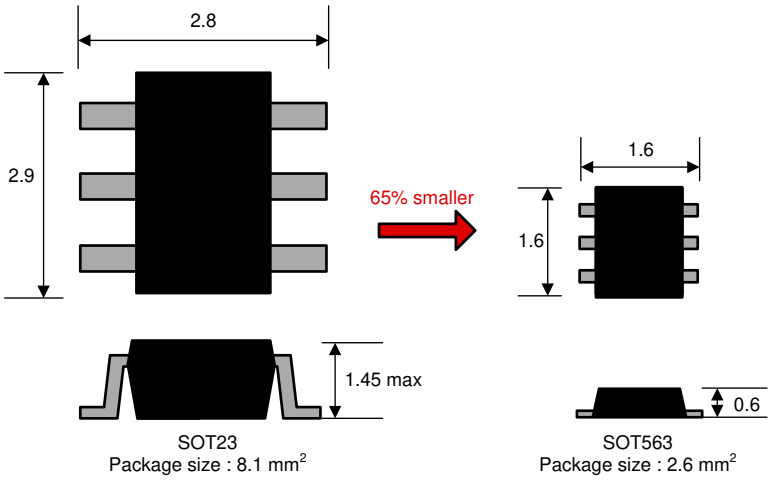



**Figure 7. SOT23 and SOT563 Package Size**

For applications like Motor Drives Control Modules where thermal performance is a key concern, the SOT23-6 (DDC) package offers the lower junction and case temperature. For applications like Industrial PC, Security Cameras, or SSD Memory Modules where size and temperature are critical for the system design SOT563 (DRL) offers the smallest IC size, 65% smaller than SOT23 (DBV, DDC) with very good thermal performance.

## 6 Summary

This application report compared the performance of a 5-V/2-A DC/DC converter (TLV62569) in three different packages: SOT23-5 (DBV), SOT23-6 (DDC), and SOT563 (DRL).

While SOT23-5 (DBV) is widely used since many years, newer packages using FCOL technologies like SOT23-6 (DDC) and SOT563 (DRL) offer multiple advantages depending on the key requirements of the application. For thermal critical applications where the solution size is not the key limiting factor, the SOT23-6 (DDC) package offers the coolest solution between the three packages. For applications where solution size matters the most, the SOT563 (DRL) package offers the smallest size with best light load efficiency among the three packages, without compromising thermal performances and cost.

## 7 References


- *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953)
- *SOT23 Package Thermal Consideration Application Report* (SLVA937)
- *How To Use Psi Jt User Guide* (SLUU484)
- *TI's Journey to High-volume Copper Wire Bonding Production White Paper* (SSZY003)
- *TLV62569 2-A High Efficiency Synchronous Buck Converter in SOT Package Data Sheet* (SLVSDG1)

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