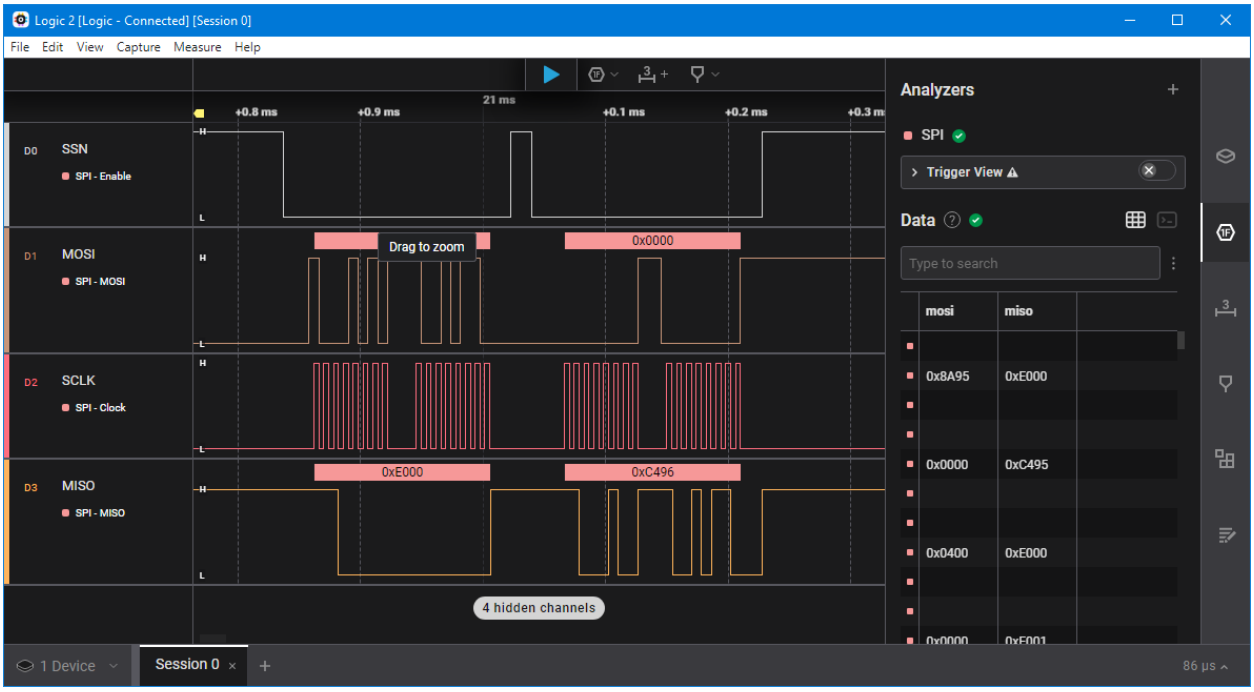
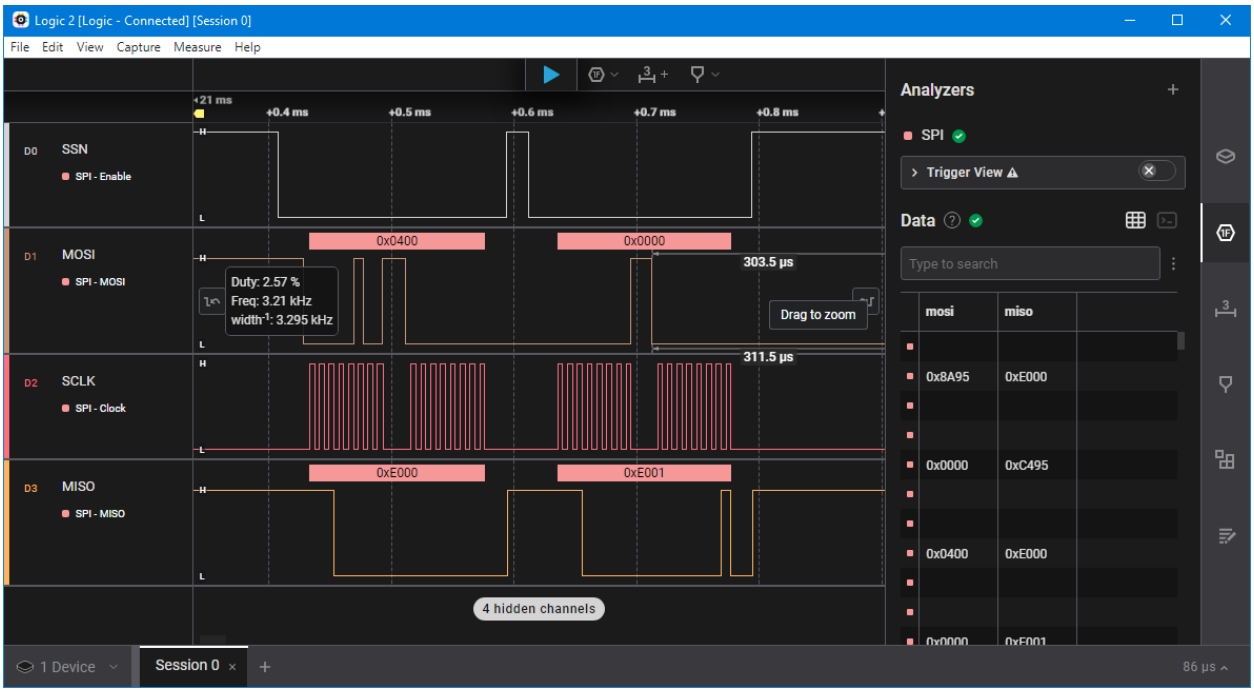
RMW test program w/ logic analyzer traces

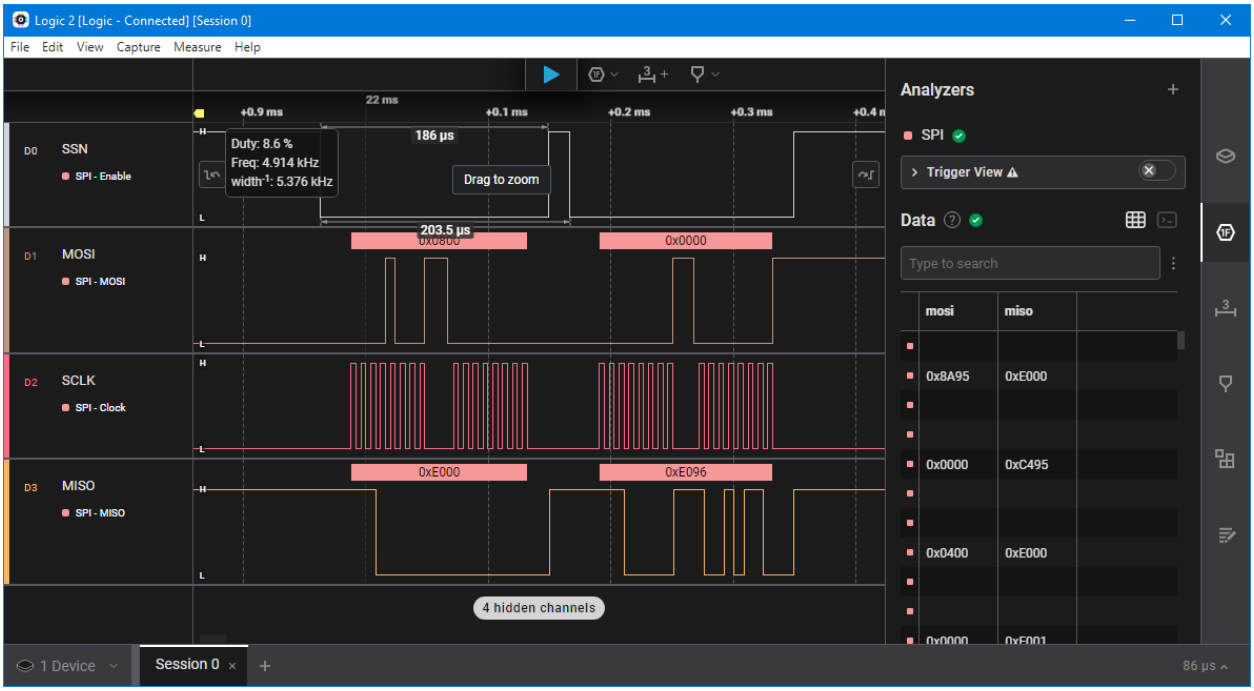
Step 1. Write 0x96 to ThermWarnLimit register (Address = 0x02). Write command is followed by another 16 bit transfer to collect the response frame.



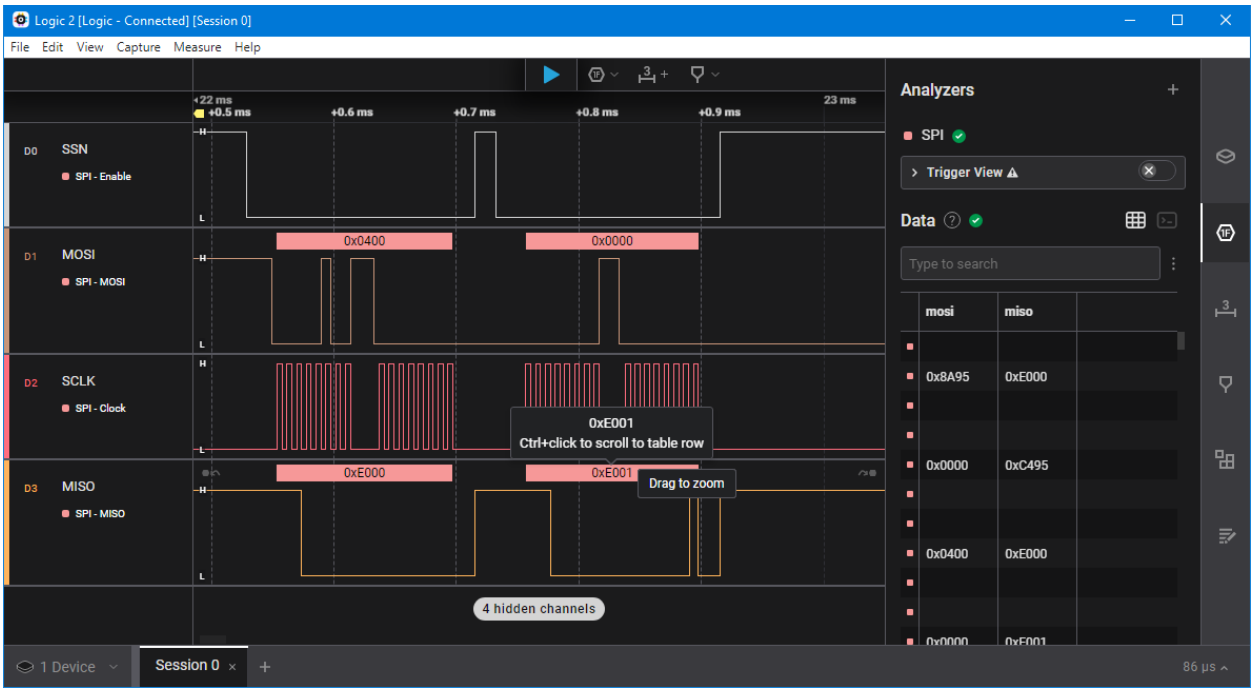
Step 2: Read STATUS register (Address = 0x01). According to datasheet this should clear SPE.



Step 3: Read ThermWarnLimit register (Address = 0x02). If the previous write operation was successful we should get back 0x96 in the datafield of the response frame.



Step 4: Read STATUS register again ...the response frame is 0xE001 so the SPE flag is set in the response frame and the data portion also indicates and active SPI error condition.



Things which seem inconsistent w/ the part datasheet description.

a) Read STATUS register does not seem to clear the SPE condition?

b) TPS92518 should ignore writes w/ SPI errors but they seem to be accepted even though SPE is set in the write response frame. Datasheet says we should receive an Write Error response frame (0x8000).