



SPN72T10

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN72T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

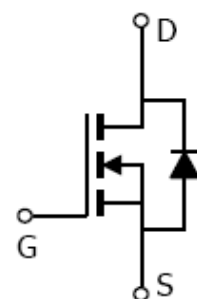
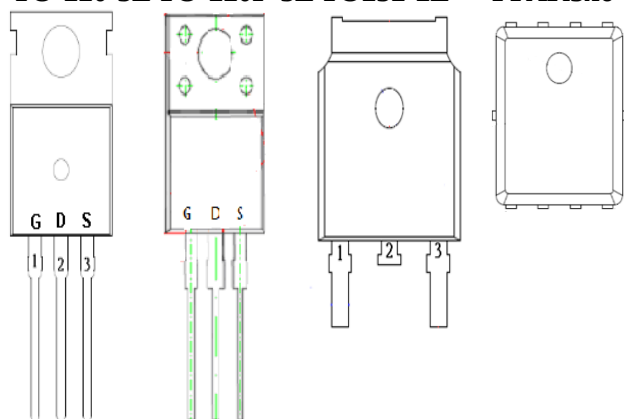
- ◆ 100V/72A, $R_{DS(ON)}=9.8m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-252-2L/PPAK5x6-8L package design

APPLICATIONS

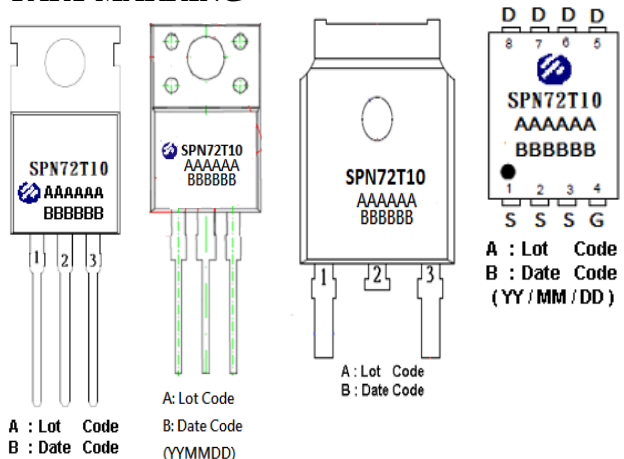
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

PIN CONFIGURATION

TO-220-3L TO-220F-3L TO252-2L PPAK5x6



PART MARKING





SPN72T10

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN72T10T220TGB	TO-220-3L	SPN72T10
SPN72T10T220FTGB	TO-220F-3L	SPN72T10
SPN72T10T252RGB	TO-252-2L	SPN72T10
SPN72T10DN8RGB	PPAK5x6-8L	SPN72T10

- ※ SPN72T10T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN72T10T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN72T10T252RGB : Tape&Reel ; Pb – Free ; Halogen – Free
- ※ SPN72T10DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free



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ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	100	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T _C =25°C	I _D	72	A
	T _C =100°C		50	
Continuous Drain Current (Silicon Limited) (PPAK5x6)	T _C =25°C	I _D	63	A
	T _C =100°C		40	
Pulsed Drain Current		I _{DM}	160	A
Avalanche Energy, Single Pulse @ L=0.1mH, T _C =25°C		E _{AS}	31	mJ
Power Dissipation @ T _C =25°C	TO-220	P _D	104	W
Power Dissipation @ T _C =25°C	TO-220F/TO-252		93	
Power Dissipation @ T _C =25°C	PPAK5x6		83	
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case (TO-220/TO-220F)		R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252)		R _{θJC}	1.35	°C/W
Thermal Resistance-Junction to Case (PPAK5x6)		R _{θJC}	1.5	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V T _J =25°C			1	μA
		V _{DS} =80V, V _{GS} =0V T _J =100°C			100	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		8.0	9.8	mΩ
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =10A		80		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		1.4		Ω
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =50V, V _{GS} =10V I _D =20A		24		nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			6		
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V f=1MHz		1450		pF
Output Capacitance	C _{oss}			273		
Reverse Transfer Capacitance	C _{rss}			5		
Turn-On Time	t _{d(on)}	V _{DD} =50V, V _{GS} =10V I _D =20A, R _G =10Ω		6		nS
	t _r			4		
Turn-Off Time	t _{d(off)}			18		
	t _f			3		
Reverse Recovery Time	t _{rr}	V _R =50V, I _F =20A, d I _F /dt=500A/μS		52		nS
Reverse Recovery Charge	Q _{rr}			176		nC



SPN72T10

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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

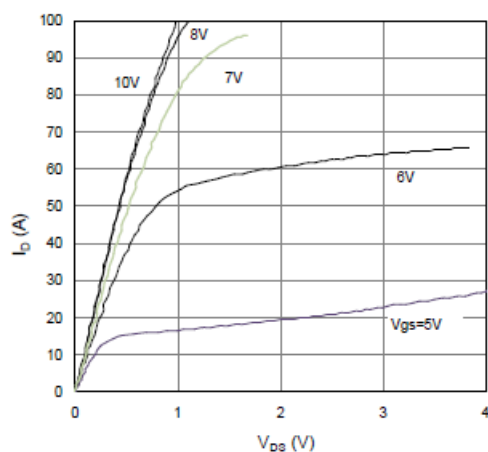


Figure 2. On-Resistance vs. Gate-Source Voltage

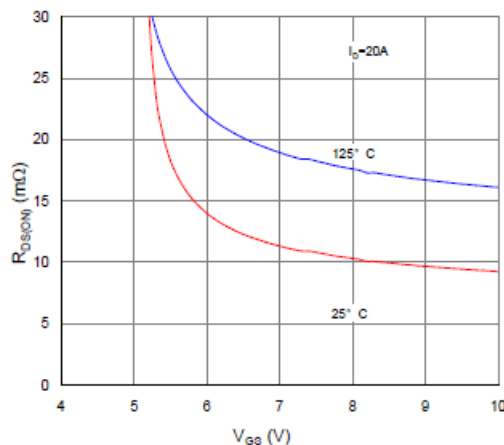


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

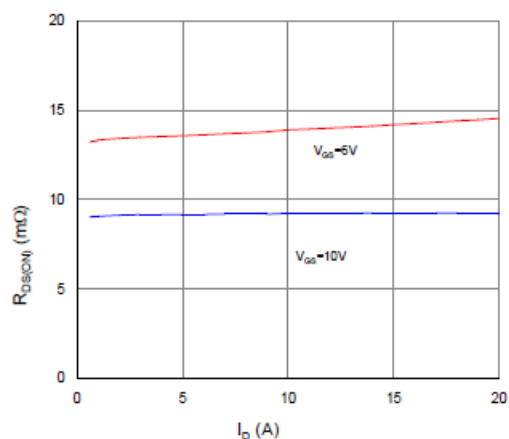


Figure 4. Normalized On-Resistance vs. Junction Temperature

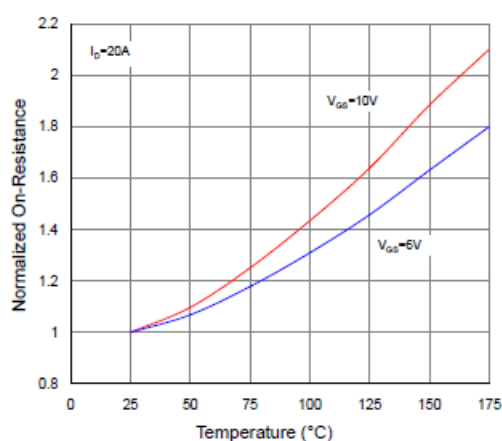


Figure 5. Typical Transfer Characteristics

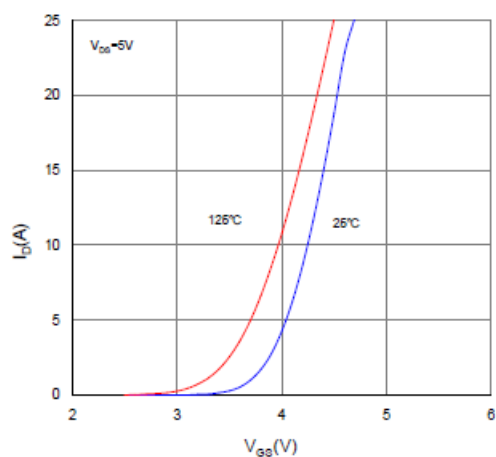
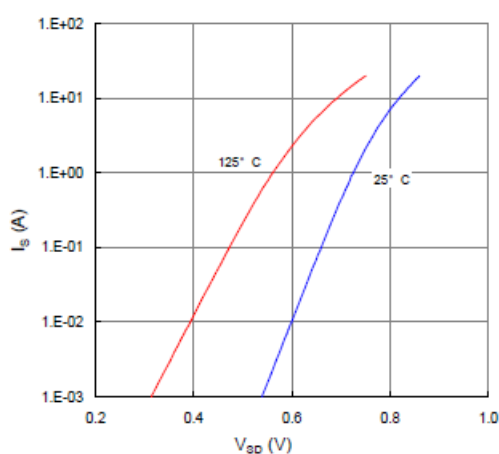


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

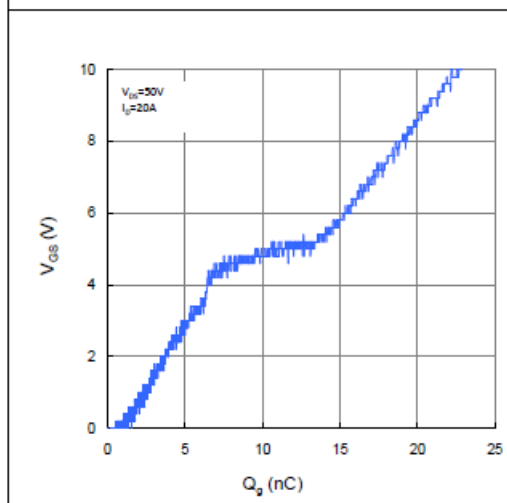


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

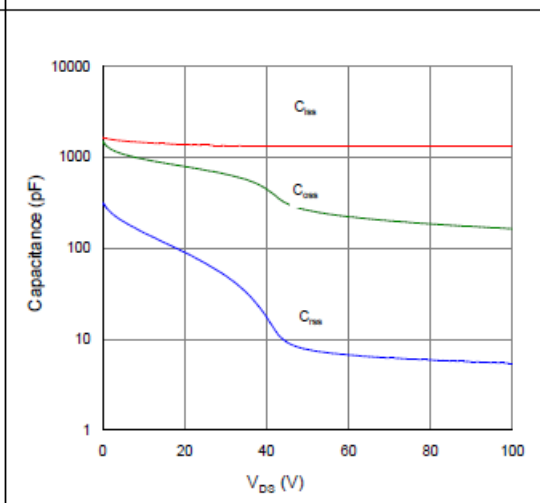


Figure 9. Maximum Safe Operating Area

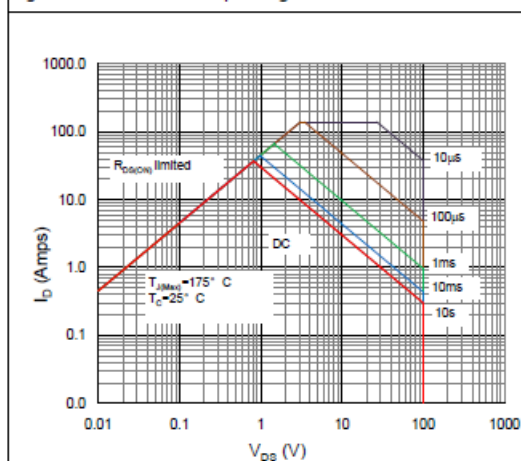


Figure 10. Maximum Drain Current vs. Case Temperature

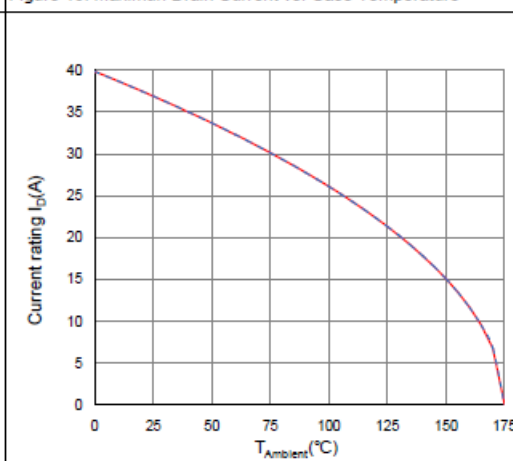
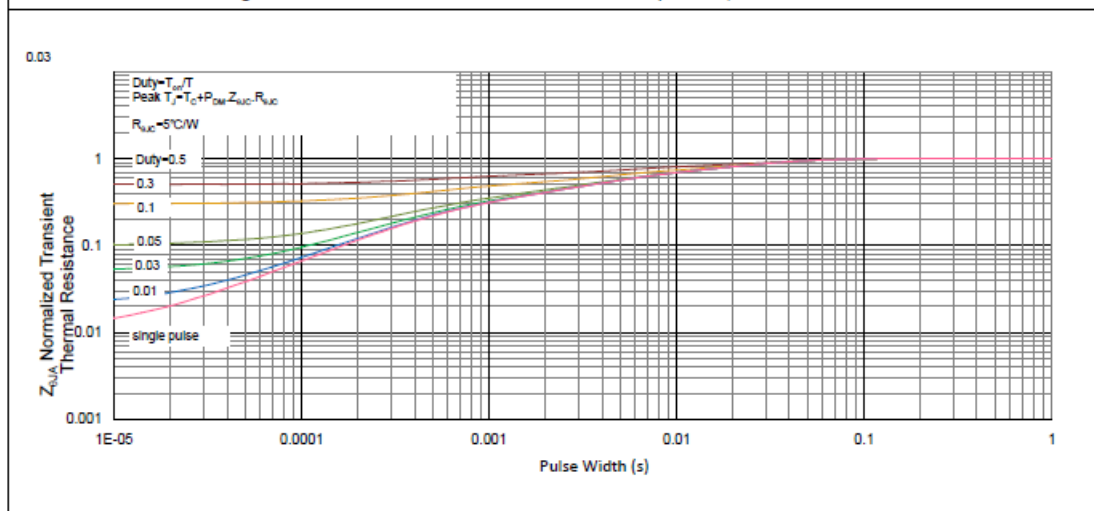


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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