

Layer	Name	Material	Thickness	Constant	Board Layer	Stack
	Top Overlay					
	Top Solder	Solder Resist	0.40mil	3.5		
1	Top Layer		2.80mil			
	Dielectric 1	FR-4 High Tg	10.00mil	4.2		
2	Signal Layer 1		1.42mil			
	Dielectric2	FR-4 High Tg	32.00mil	4.2		
3	Signal Layer 2		1.42mil			
	Dielectric 3	FR-4 High Tg	10.00mil	4.2		
4	Bottom Layer		2.80mil			
	Bottom Solder	Solder Resist	0.40mil	3.5		
	Bottom Overlay					

Total board thickness:

61.23mH

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL; HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 μ m ☐ OTHER _____

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATT ☐ SEMI-GLOSS

SURFACE FINISH:

IMM. TIN/SILVER OR EQUIV ☐ OTHER ☐

ARRAY/PANEL:

CERTIFICATION: ☐ N.C. ROUTE ☒ V. SCORE

MATERIALS AND WORKMANSHIP FOR ALL PCBs
TO MEET OR EXCEED THE REQUIREMENTS OF:

☐ Yes ☐ No☒ ANSIPPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS

MICROSECTION: ☐ YES

BASE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

☐ TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
LMR60460EVM

DESIGNED FOR:
Public Release

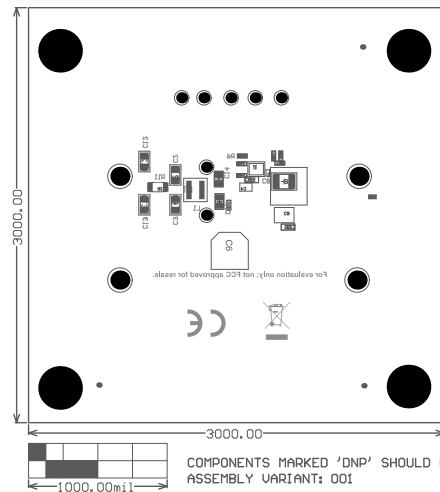
FILE NAME:
SR147.PcbDoc

ENGINEER:	Rahil Ajani
-----------	-------------

LAYOUT BY:
Rahil Ajani

SCALE: 0.72

ALTIUM DESIGNER VERSION:	25.2.1.25
--------------------------	-----------



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38 TON DUOHS 'DNP' COMPONENTS SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001 001 :VARIANT YJBM322A

ABB-ABB-CBCE-NETWORKEDP-0000109192DE						A	BOARD	#:	SRI47IAR	:	DART	:	A	SUN 300: NORTON MONS16A86H166E
LAYER NAME = <u>MANAGE-TOOL-CONTROL</u> pdaOption						TID #:	N/A	:N	:	#	QIT			
PLANT NAME: /BIOSon Layer Assembly Duration						GENERATED On : 6/13/2025 13:12:48 PM msa24jw6J TEXAS INSTRUMENTS J9								

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification, or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.