1. INTRODUCTION

ST9902 is an integrated circuit for liquid-crystal shutter glasses driver. It combines a DC/DC converter that generates a specified voltage level as the output voltage source to the four-channel analog switches. Each analog switch has a dedicated input control pin and a dedicated output analog pin. The analog switches can be used as the lens driver in a 3D glasses system application. 16K-byte EEPROM is suitable for the MCU-based system, which can use EEPROM as a code or data storage unit. ST9902 chip is integrated into a 16-pin QFN package and only a few external passive components are required.

2. FEATURES

DC/DC Converter

- Input voltage: 2.5V to 4.2V
- High efficiency (max output current =100uA)
- Output voltage is 10V

Package and Operating Temperature Range

- 3mm x 3mm 16Pin QFN package
- Operating temperature range: 0~70℃

Analog Switch

- On-resistance match between four channels
- Low ON/OFF leakage current
- Vop support voltage = 10V

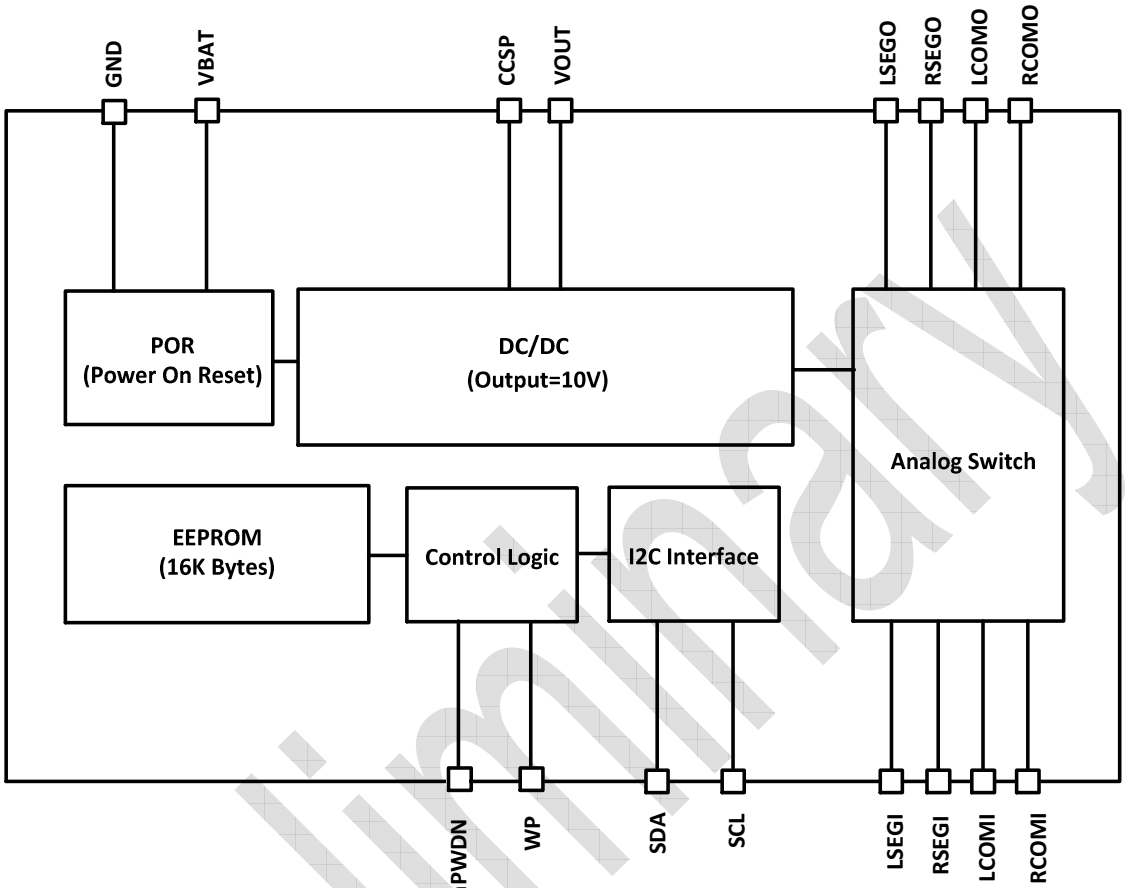
Control Interface

- I2C serial interface
- Up to 400KHz I2C bus compatibility
- Support power down control pin

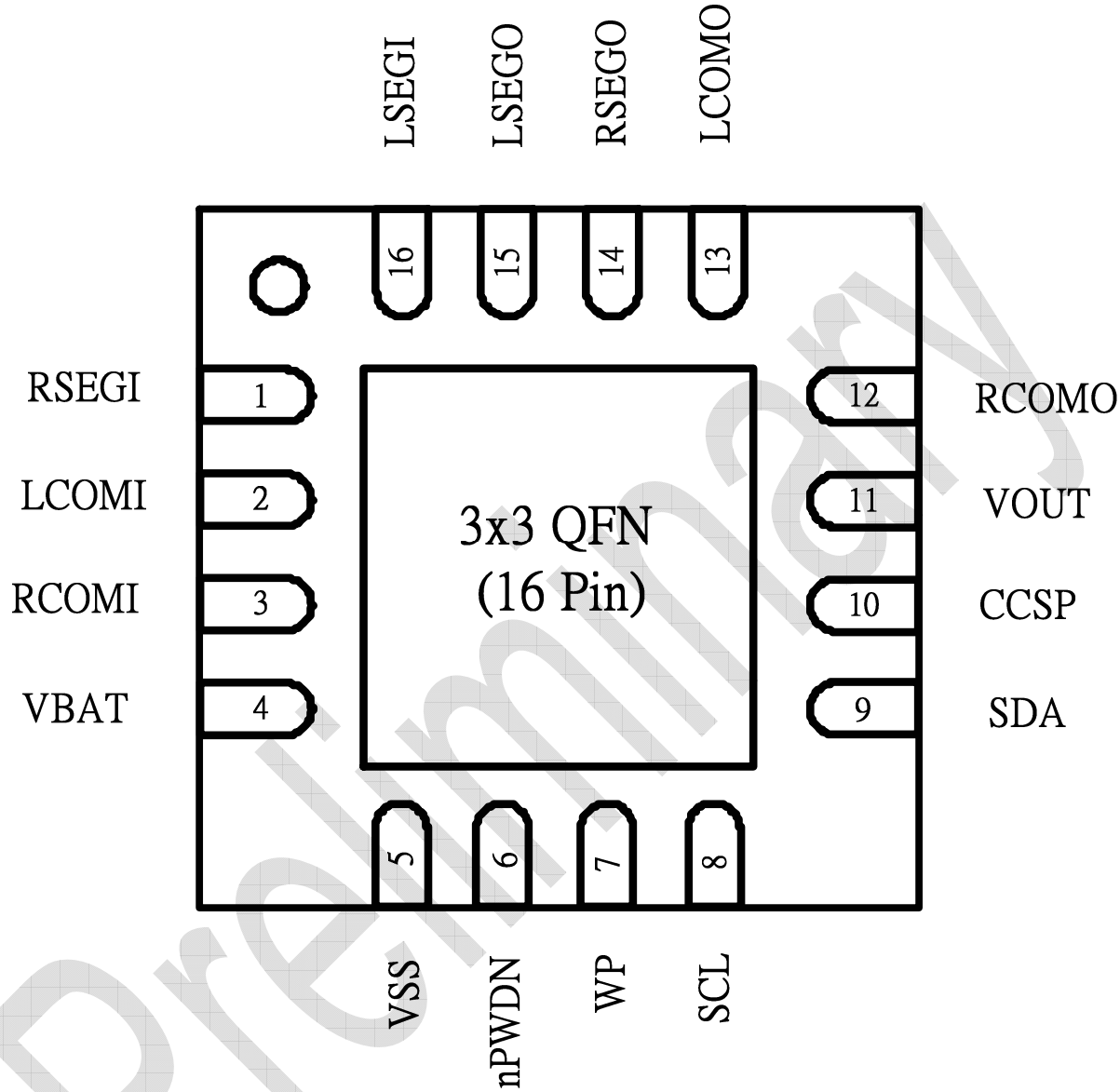
16K-byte EEPROM

- Support byte program and page program
- 32 byte page buffer
- Self-timed programming cycle (6m sec max.)
- Endurance：300K write cycle
- Data retention time：more than 10 years

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PINNING DESCRIPTIONS

System Wide Pins

Pin Name	Type	Description	No. of Pins
VBAT	**P**	Battery power supply input pin.	**4**
VSS (GND)	**P**	System ground pin.	**5**
SCL	**I**	I2C serial clock input pin.	**8**
SDA	**I/O**	I2C serial data input/output pin.	**9**
WP	**I**	Write protection of EEPROM pin.	**7**
nPWDN (SHUTDOWN)	**I**	Power down control pin. (0=system power down；1=system normal mode)	**6**

Analog Switch interface Pins

Pin Name	Type	Description	No. of Pins
RCOMO (LO0), LCOMO (LO1), RSEGO (LO2), LSEGO (LO3)	**O**	Lens drive output pins.	**12, 13, 14, 15**
RCOMI (LIN0), LCOMI (LIN1), RSEGI (LIN2), LSEGI (LIN3)	**I**	Lens control input pins.	**1, 2, 3, 16**

DC/DC Pins

Pin Name	Type	Description	No. of Pins
CCSP (DCAP0)	**P**	Terminal of holding capacitor. (Connect to a capacitor)	**10**
VOUT (DCAP1)	**P**	Charge pump output voltage for liquid crystal driving. (Connect to a capacitor)	**11**

6. FUNCTIONS DESCRIPTION

DC/DC Converter

The device adopts the charge pump architecture because the power efficiency of the charge pump is suitable for 100uA current loading application.

Capacitor Selection

For best performance, it is recommended that low ESR capacitors (ceramic or tantalum) be used for both VOUT and CCSP to reduce noise and ripple. Increasing the size of VOUT capacitor will reduce output voltage ripple. The recommended capacitors specification is illustrated in application circuit.

Layout Considerations

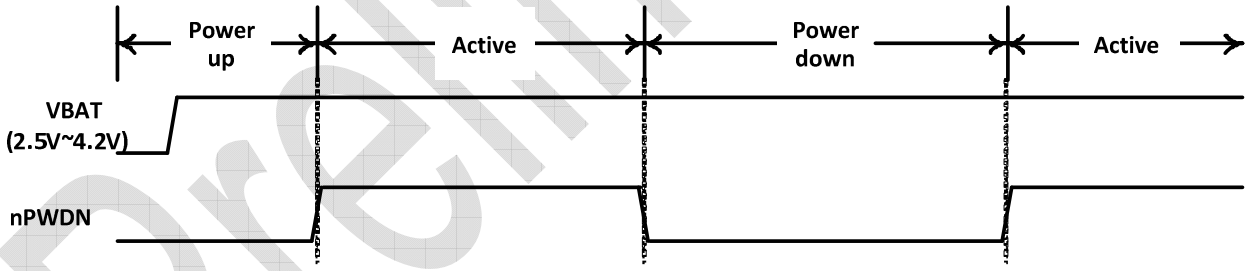
Careful of board layout is a must. For best performance, use very short path connections to all capacitors.

Analog Switch

The analog switch is a 4-output high-voltage liquid crystal lens driver. The VOUT support voltage is 10V. With the devices, data transfers are done through the 4 parallel data bus. Please refer application circuit.

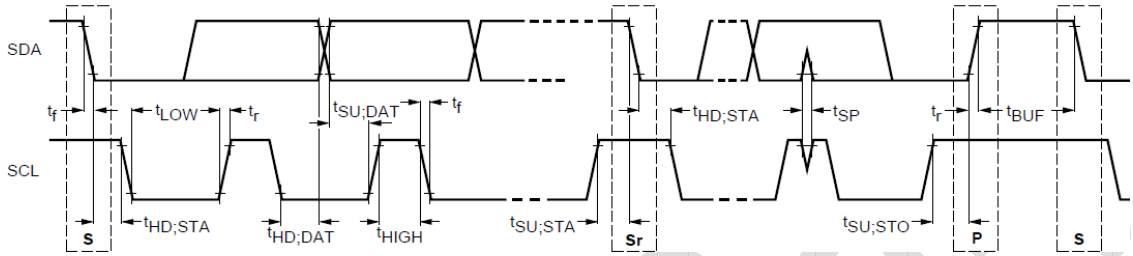
Power Management (nPWDN)

Sitronix recommends the following power control sequence to be implemented by MCU by using GPIO pin to control nPWDN (SHUTDOWN). When nPWDN pin sets to low level means ST9902 in the power down mode for power saving, nPWDN pin sets to high level for normal operation.



I²C Serial Interface

The two-wire bus provides a channel for the I²C master to access the on-chip register and 16K Bytes EEPROM via I²C protocols. The I²C Interface is a bi-directional, two-line communication interface. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected with a pull-up resistor, which drives SDA and SCL to high when the bus is idle. Data transfer can be initiated only when the bus is in idle state. A clock pulse on SCL line transfers one data bit. The data on the SDA line must remain stable during the high period of the clock pulse. A high-to-low transition of SDA, while SCL is high, is defined as the START (S) condition. A low-to-high transition of SDA, while SCL is high, is defined as the STOP (P) condition. An 8-bit transfer is always followed by an acknowledge bit. The first transaction on I²C bus is the slave device identification phase. The 7-bit slave address of this device is defined to **50H**. (8bit one byte is equal to **A0H**)



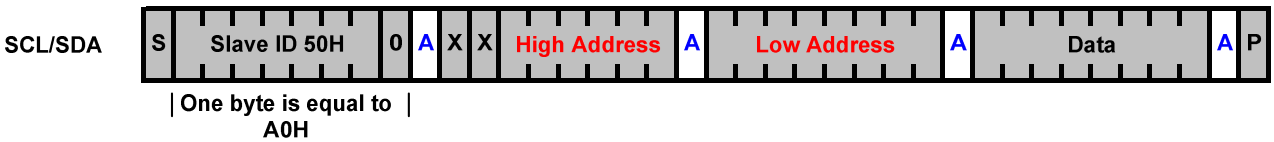
For accessing the on-chip register and read/erase/program 16K Bytes EEPROM, please use the operation protocol described as follow.

EEPROM Read/Erase/Program Operation

This device provides a serial electrically erasable and programmable read only memory (EEPROM), which organized in 16384 words of 8 bits each. The serial EEPROM requires 14 serial bits as its memory address. The address space of the EEPROM is from 0000H to 3FFFH. It contains a 32-byte page buffer, which can be used for page program operation. This device also supports the byte program operation. The erase operation will be automatically performed internally by hardware after external MCU completes data writes to the EEPROM. During internal program cycle, the external MCU needs to check if the EEPROM internal program cycle is complete or not by polling RDY bit in EERPOM Control register.

Byte Write Operation

A write operation requires two 8-bit data word address following the device address word and ACKNOWLEDGE signal. Upon receipt of this address, the EEPROM will respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will again output a “0”. The addressing device, such as a microcontroller, must terminate the write sequence with a STOP condition. At this time the EEPROM enters into an internally-timed write cycle state. All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed



Page Write Operation

The EEPROM are capable of 32-byte page write.

A page write is initiated the same way as a byte write, but the microcontroller does not send a STOP condition after the first data word is clocked in. The microcontroller can transmit up to 31 more data words after the EEPROM acknowledges receipt of the first data word. The EEPROM will respond with a “0” after each data word is received. The microcontroller must terminate the page write sequence with a STOP condition.

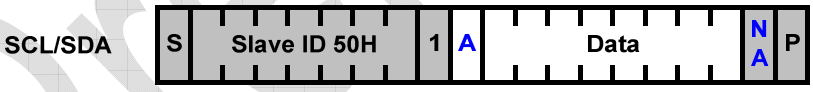
The lower six bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and the previous data will be overwritten.

ACKNOWLEDGE POLLING

ACKNOWLEDGE polling is used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

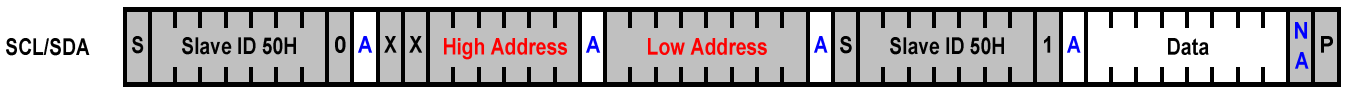
CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit set to “1”. The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. A data byte will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the microcontroller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode



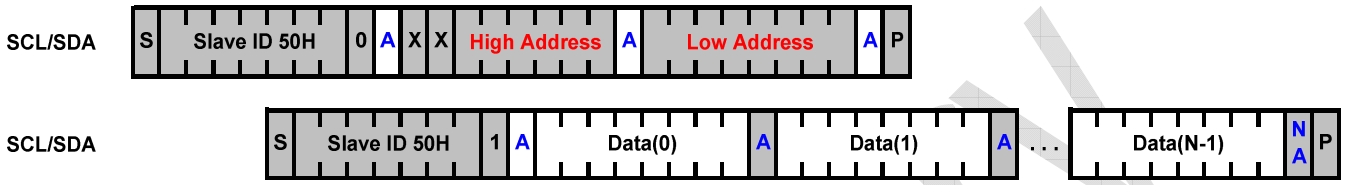
Random Read Operation

A random read operation firstly requires an I^2C write sequence to load the 14 bits memory address into the EEPROM. Once the memory address clocked in and acknowledged by EEPROM, the MCU have to initiate another I^2C read sequence to have the EEPROM serially clock out the data byte. The I^2C protocol format of a random read operation is illustrated as below:



Sequential Read Operation

The I^{2}C protocol format of a sequential read operation is initiated the same way as random read operation. After the MCU receives the first data byte, it has to respond with an 'ACK'. As long as an 'ACK' received by the EEPROM, it will continue to increment the internal address pointer and serially clock out the next data byte. When the address pointer reaches 3FFFH, it will roll over to 0000H and the sequential read will still continues. To terminate the sequential read operation, the MCU simply respond a 'NAK' to the EEPROM and followed by a STOP condition. The I^{2}C protocol format of a sequential read operation is illustrated as below:



7. ELECTRICAL CHARACTERISTICS

DC Characteristics

(Condition: Bare dice; Room temperature 25℃)

Item	Symbol	Conditions	Min	TYP	Max	Unit
System Operating Voltage Range	VBAT	External VDD	2.5	-	4.2	V
Input High Voltage	VIH	-	0.8xVBAT	-	VBAT	V
Input Low Voltage	VIL	-	GND	-	0.2xVBAT	V
High-level Output Voltage	VOH	IOH=1mA	0.8xVBAT	-	VBAT	V
Low-level Output Voltage	VOL	IOL=1mA	GND	-	0.2xVBAT	V
Input Leakage Current	ILI	-	–1.0	-	1.0	uA
Output leakage current	ILO	-	–3.0	-	3.0	uA
Power Supply Current	Is	Power Down Mode	-	-	10	uA
Operation Temperature	TEMP	-	0	-	70	℃

DC/DC Characteristic

(Condition: Bare dice; Room temperature 25℃)

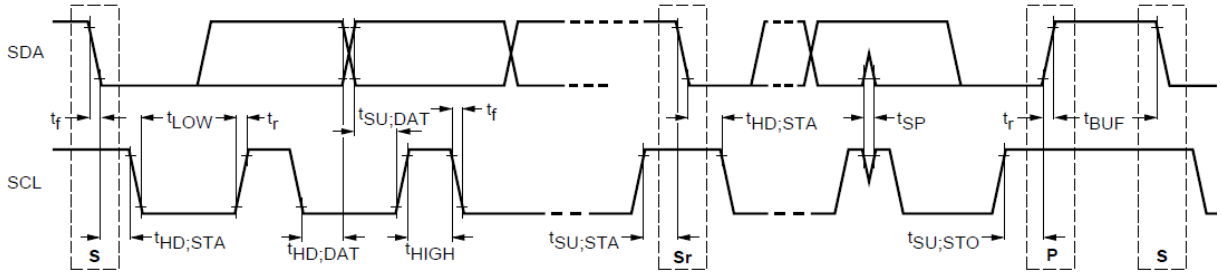
Symbol	Parameter	Conditions	Min	TYP	Max	Unit
VBAT	Input Voltage Range	External VDD	2.5	-	4.2	V
VOUT	Output Voltage for liquid crystal	-	-	10	-	V
		Accuracy	-	5	-	%
Iload	Load Current	VOUT=10V	-	-	100	μA
Tstart	Start up time	-	50	-	-	ms

Analog Switch Characteristic

(Condition: Bare dice; Room temperature 25℃)

Symbol	Parameter	Conditions	Min	TYP	Max	Unit
VBAT	Input Voltage Range	External VDD	2.5	-	4.2	V
Rds(on)	Switch on-resistance	-	-	200	-	Ohm

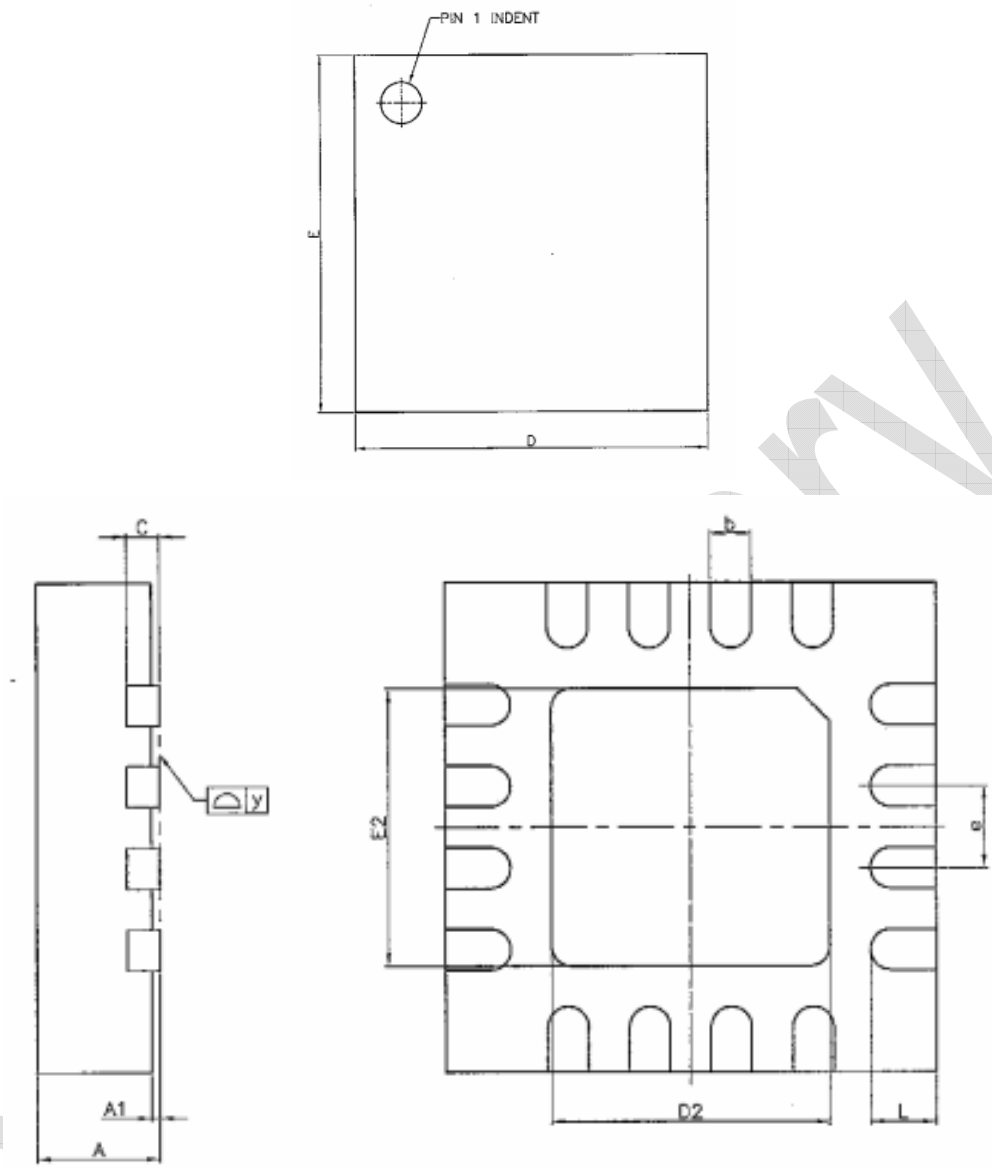
8. Timing Characteristics



(Condition: Bare dice; Room temperature 25℃)

Symbol	Parameter	Conditions	Min	TYP	Max	Unit
f_{SCL}	SCL clock frequency	-	100	-	400	KHz
t_{LOW}	LOW period of the SCL clock	-	1.3	-	-	us
t_{HIGH}	HIGH period of the SCL clock	-	0.6	-	-	us
$t_{SU;STA}$	Setup time for a repeated START condition	-	0.6	-	-	us
$t_{HD;DAT}$	Data hold time	-	0	-	-	us
$t_{SU;DAT}$	Data set-up time	-	100	-	-	ns
$t_{HD;STA}$	Hold time (repeated) Start condition	-	0.6	-	-	us
$t_{SU;STO}$	Setup time for STOP condition	-	0.6	-	-	us
t_r	Rise time of both SCL and SDA signals	-	$20+0.1C_b$	-	300	ns
t_f	Fall time of both SCL and SDA signals	-	$20+0.1C_b$	-	300	ns
t_{BUF}	Bus free time between a STOP and START condition	-	1.3	-	-	us
C_b	Capacitive load for each bus line	-	-	-	400	pf

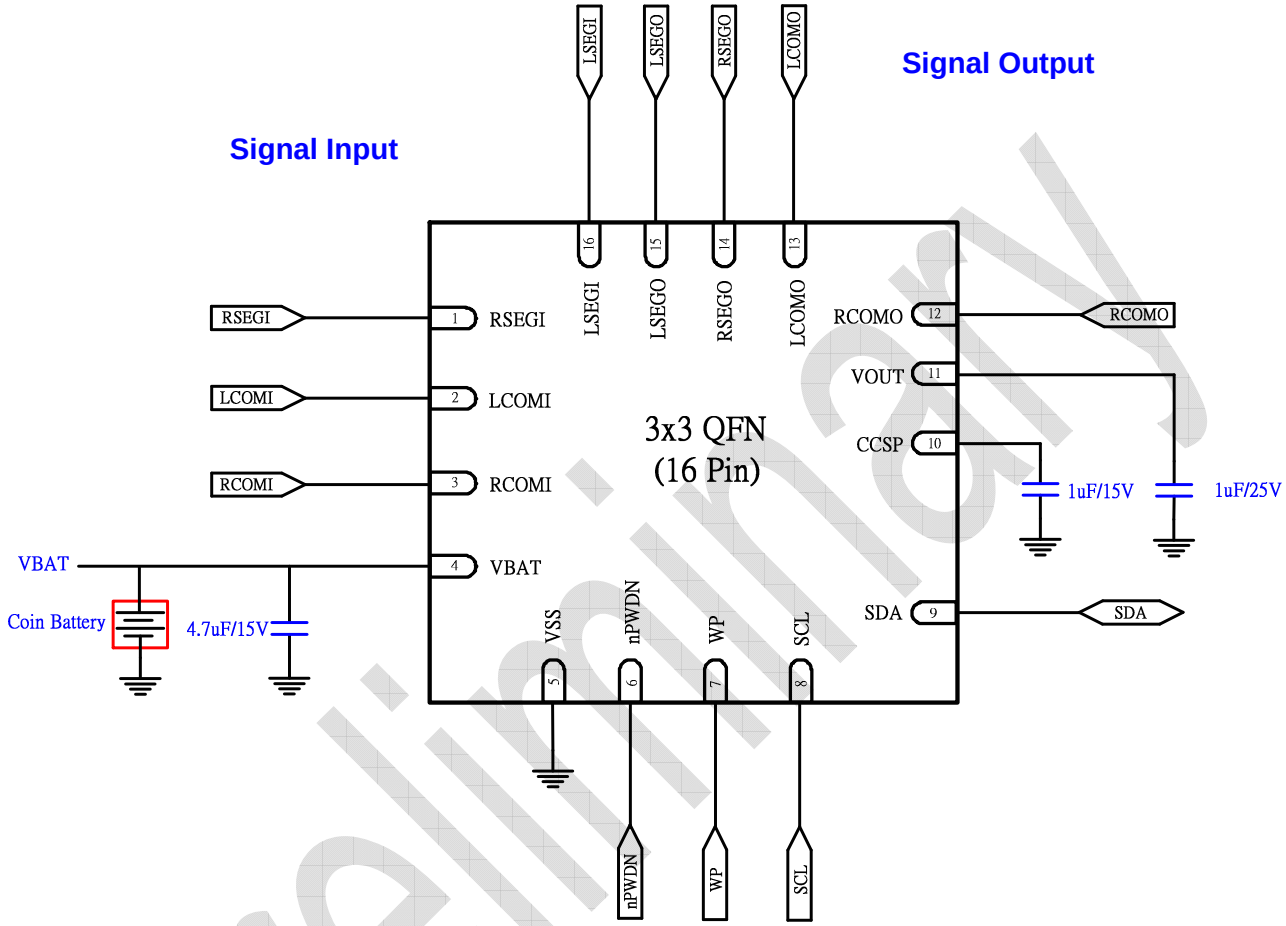
9. Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	——	0.20 REF.	——
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.65	1.70	1.75
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

10. Application Circuitry

Coin Battery (2.5V~4.2V)



Note:

For I2C bus (SDA and SCL) read/write operation, needs pull high resistor, recommend value is 4.7kΩ.

11. Reversion History

Version	Date	Description
0.0	2011/09/22	Preliminary Version.
0.1	2011/11/22	Modify Application Circuit.
0.2	2012/01/10	Modify Application Circuit.
0.3	2012/03/02	Modify page buffer size.
0.4	2012/03/27	1. Modify Features. 2. Modify Application Circuit.
0.5	2012/05/03	Modify package pin number to 16Pin.