Schematic Review, March 31, 2020.docx

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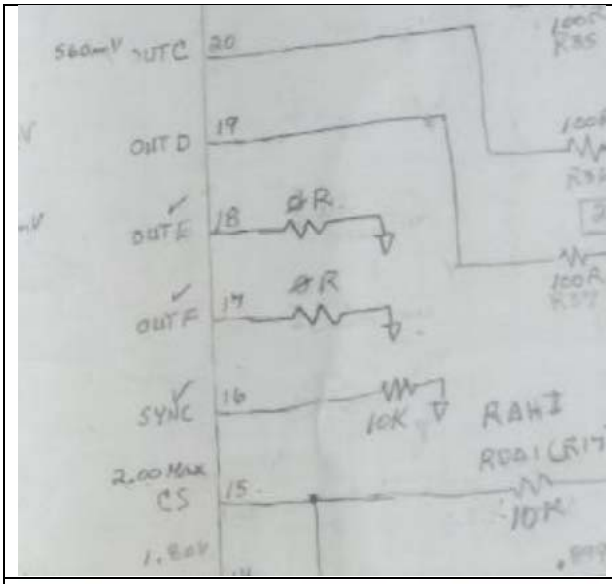
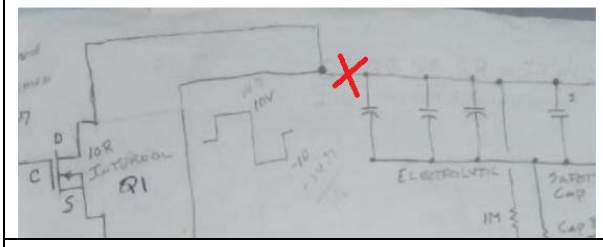
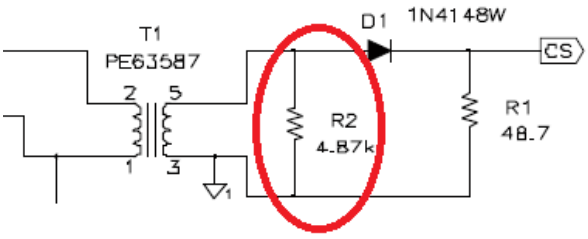
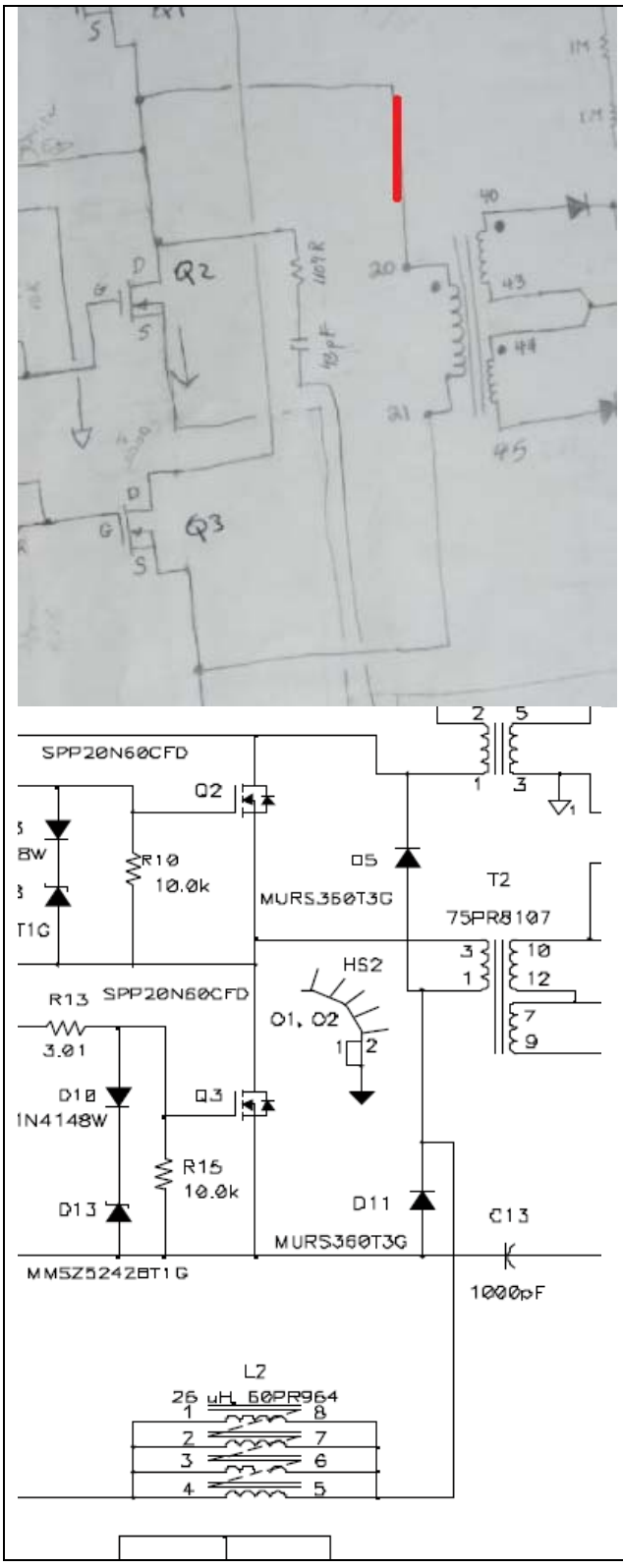
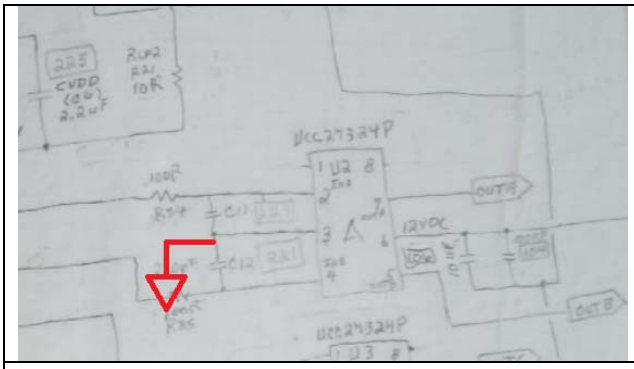
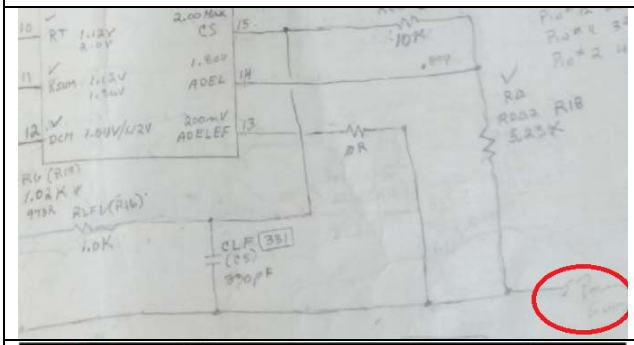
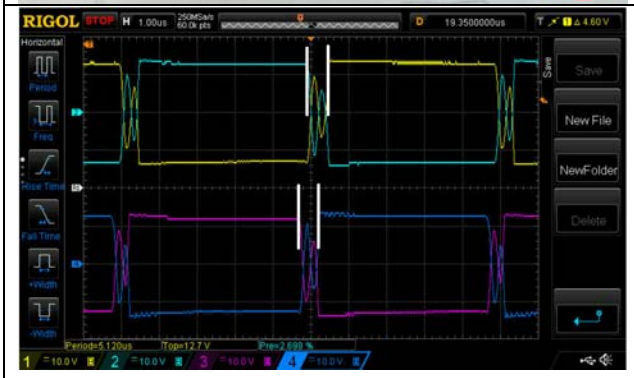
Hi Eddie.

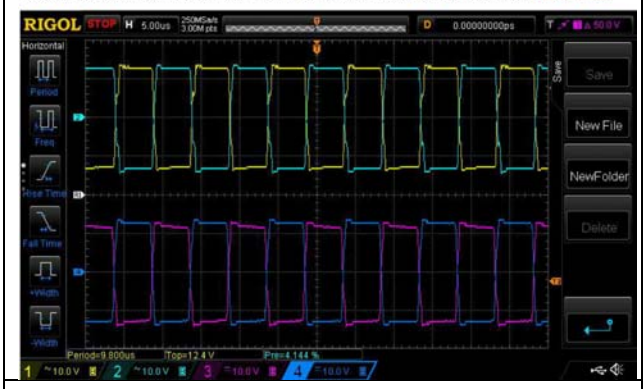
Please check that the GND connection to the gate driver is correct (Pin 3)

	You are not using OUTE or OUTF so you should leave these pins open circuit. You can also tie the DCM pin to VREF to disable the OUTE and OUTF signals. This may slightly reduce the amount of noise in the system. Shorting the DCM pin to GND, as you have done, is OK but the OUTE and OUTF signals will remain enabled.
	I was not able to find of the Current Transformer primary. It should be at the location marked here. Double check the phasing of the primary / secondary.
	You don't have a reset network for the current transformer. This is needed so that the core flux can reset during the interval between switching cycles. There are a number of ways to do this but a resistor is usually sufficient. I'd use a reset resistor (R2) which is 100 times larger than the burden resistor (R1). http://www.ti.com/lit/ds/symlink/ucc28951-q1.pdf Section 8.2.2.10 has some details of a typical calculation.



You don't have a separate shim inductor and clamp diodes. The shim inductance + Leakage inductance ensures enough energy is stored to force ZVS. For now – I'd leave it alone but you might want to review the calculations for the shim/leakage inductance. They are included in the Excel calculator for the controller which you can find on the product page. The shim inductor is L2 and the clamp diodes are D5 and D11 in the EVM schematic.

	I don't see a GND connection at pin 3 of the driver ICs – I'm sure it's there but please double check. You should not need the RC time constant at the inputs to the driver – the dead times are generated by the controller.
	GND, VDD, OUTA OUTB, OUTC,OUTD, CS, ADEL, ADELEF, RSUM, RT, TMIN, DELEF, DELCD, DELAB, SS/EN, COMP, EA-, EA+, REF pins are all ok. SYNC has 10k to GND, this is ok but you may leave the pin O/C too if you wish. OUTE and OUTF should be left open circuit. DCM may be left connected to GND but later you can connect it to VREF and that will disable the OUTE, OUTF signals.
	The red node should be connected to the GND pin of the IC through a VERY low impedance connection. It's not clear from the schematic.
	These are the signals at the output of the GDT. Please check the OUTx signals at the pins of the controller and again at the input to the gate driver IC and at the output of the gate driver IC. I expect that all the signals will be nice square waves. The ringing is due to the transformer secondary inductances being resonant with the transformer stray capacitance. The dead times are those marked by white lines – they look ok for now although they may need adjusting a bit.
IS IT MY DELAY TIME, DEAD TIME? WHAT EVER IT IS, IT IS CHANGING THE SIGNAL COMING FROM THE UCC28950 IC. THIS TELS ME IT IS EITHER THE FEEDBACK PIN 4, CURRENT SENSE PIN 15, VDD RAIL?	The feedback loop will have a bandwidth less than 15kHz so it cannot be responsible for changes at MHz frequencies. I believe the ringing is due to the GDT inductance ringing with its self capacitance. Once the secondary is loaded by the MOSFET gate the ringing should disappear.

WHATS HAPPENING TO THE OUTA, B, C, D SIGNALS ARE NOT BECAUSE OF THE LOAD, BECAUSE WHAT HAPPENS TO THE LOAD CAN NOT GO BACKWARDS THRU THE GDT AND CAUSE IT TO CHANGE.	I expect that the OUTx signals are ok.
FIGURE 2. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE NO DC LINK 	These waveforms look ok for now.