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Selecting output capacitors to optimize voltage ripple and loop stability in PSR flyback DC/DC converters

Introduction

Primary-side regulation (PSR) is an observer-based approach to estimate the output voltage of a flyback converter using the reflected voltage on a primary-referenced winding. Previous ADJ articles [1-2] describe the operation and switching behavior of an auxless PSR flyback DC/DC converter for automotive and industrial applications where appropriately-timed sensing of the primary switch voltage at its resonant knee position provides a suitable proxy for the output voltage. This magnetically sensed regulation technique supports sub-1% output voltage accuracy across load, line and temperature ranges [1]. Moreover, it avoids the secondary-side optocoupler and error amplifier normally used for isolated feedback, thereby eliminating a component crossing the isolation barrier and enabling a cost-effective, high-reliability design with low component count.

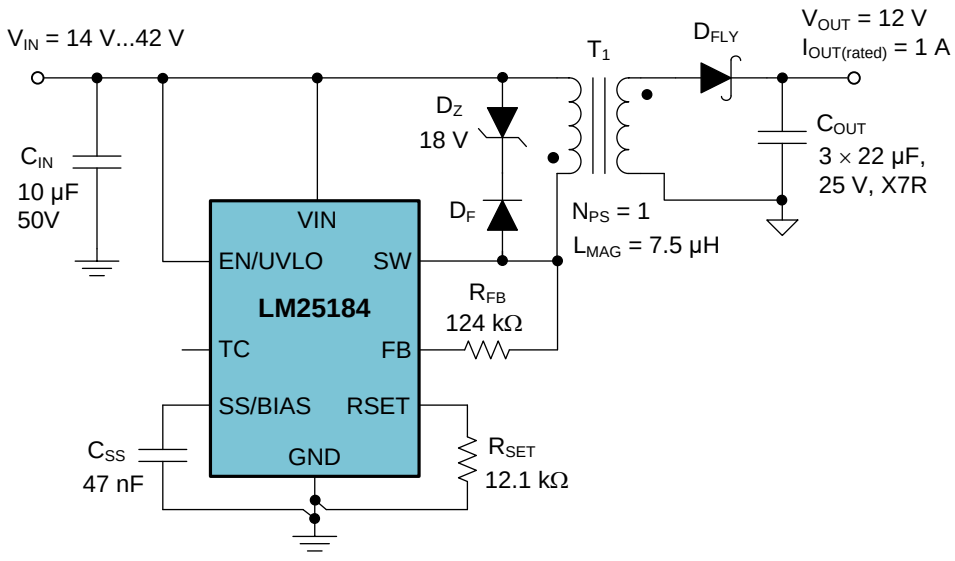
Within this context, this article reviews the modes of operation and salient characteristics of a PSR flyback DC/DC converter, and specifically examines output capacitor selection to meet system specifications for output voltage ripple and small-signal stability.

PSR flyback dc/dc converter with multi-mode control

Figure 1 exemplarily shows the schematic of a PSR flyback converter [3] with integrated primary switch and loop compensation components. The device supports magnetically-sensed output voltage regulation via the transformer primary winding. Equation 1 gives the output voltage setpoint, where N_{PS} is the primary-to-secondary transformer turns ratio, V_{REF} is the internal bandgap reference voltage, and V_D is the flyback diode drop (at close to zero current).

$$V_{OUT} = \frac{V_{REF}}{N_{PS}} \frac{R_{FB}}{R_{SET}} - V_D \quad (1)$$

Figure 1. Typical schematic of an auxless PSR flyback converter



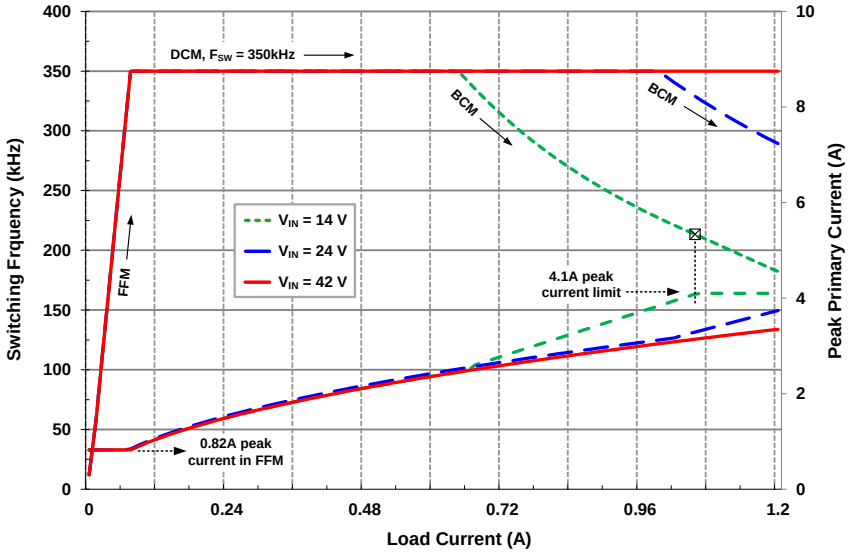
Using a variable switching frequency control law with peak current-mode control (VFPCM), the converter operates in boundary (BCM) or discontinuous (DCM) conduction mode depending on the load current, as depicted in Figure 2 [4]. Modulation of the switching frequency (FM) and peak primary current amplitude (AM) are used to maintain high efficiency across wide operating ranges of load and line.

More specifically, the converter operates in BCM at heavy loads, and the primary switch turns on with a resonant-half-period delay after switch voltage knee detection (core reset) to achieve a quasi-resonant switching transition. As shown in Figure 2, the switching frequency in BCM increases as the load current decreases. To prevent high-frequency operation at medium load, the mode changes from BCM to DCM such that the switching frequency remains constant at its maximum value (350 kHz in this example). Equation 2 gives the critical output current at the DCM-BCM boundary:

$$I_{OUT(DCM\text{-}BCM)} = \frac{V_{OUT} N_{PS}^{2}}{2 L_{MAG} F_{SW\text{-}DCM}} \left(\frac{V_{IN}}{V_{IN} + V_{OUT} N_{PS}} \right)^{2} \quad (2)$$

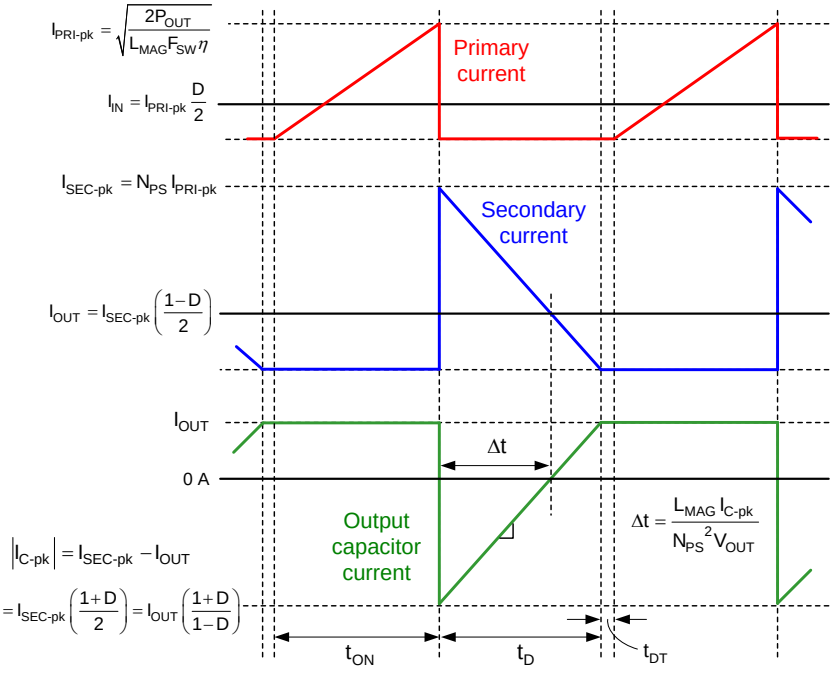
Operation at light load changes to frequency-foldback mode (FFM), which is effectively DCM with variable switching frequency and constant peak current. As magnetic regulation relies on sensing the output voltage during switching cycles, it is necessary to maintain a certain minimum switching frequency at no load to continue sensing the output voltage (12 kHz in this example).

Figure 2. Switching frequency and primary peak current vs. load current for the converter in Figure 1



Clearly, BCM has a lower switching frequency and a higher peak current than DCM. As such, BCM dictates the output capacitor sizing for a given ripple voltage specification. Figure 3 shows the current waveforms in BCM.

Figure 3. Idealized current waveforms of a flyback converter in BCM



Output capacitor sizing for voltage ripple

Based on the waveforms in Figure 3, Equation 3 expresses the output capacitor peak-to-peak ripple voltage, ΔV_{OUT}, in BCM:

$$\Delta V_{OUT} = \frac{I_{C\text{-}pk}\,\Delta t}{2C_{OUT}} = \frac{I_{C\text{-}pk}}{2C_{OUT}}\frac{L_{MAG\text{-}sec}\,I_{C\text{-}pk}}{V_{OUT}} \approx \frac{L_{MAG}\,I_{PRI\text{-}pk}^{\,2}}{2C_{OUT}V_{OUT}}\left(\frac{1+D}{2}\right)^2 = \frac{L_{MAG}\,I_{OUT}^{\,2}}{2C_{OUT}V_{OUT}\,N_{PS}^{\,2}}\left(\frac{1+D}{1-D}\right)^2 \quad (3)$$

Using the circuit values in Figure 1, Equation 4 gives the required capacitance for 1% ripple on a 12-V output:

$$C_{OUT} \geq \frac{7.5\mu H\times(1A)^2}{2\times 120mV\times 12V\times 1^2}\times\left(\frac{1+0.47}{1-0.47}\right)^2 = 20\mu F \quad (4)$$

while Equation 5 defines the worst-case condition at maximum duty cycle (corresponding to the minimum input voltage):

$$D = \frac{N_{PS}\left(V_{OUT}+V_D\right)}{V_{IN(min)}+N_{PS}\left(V_{OUT}+V_D\right)} = \frac{1\times(12V+0.4V)}{14V+1\times(12V+0.4V)} = 0.47 \quad (5)$$

Equation 6 gives the output capacitor RMS current:

$$I_{COUT\text{-}RMS} = I_{SEC\text{-}pk}\sqrt{\frac{1-D}{3}} = \sqrt{\frac{2I_{OUT}\,I_{SEC\text{-}pk}}{3}} = \sqrt{\frac{2\times 1A\times 4A}{3}} = 1.6A \quad (6)$$

Figure 4 shows the effective capacitance vs. voltage and temperature of a 22-µF, 25-V multi-layer ceramic capacitor (MLCC) from Murata [5]. Even though the nameplate capacitance is 22 µF, the effective value is 9.1 µF at 25°C and 7.2 µF at -40°C when a DC bias of 12 V is applied. Three such capacitors in parallel are therefore required to meet the ripple voltage specification. The equivalent series resistance (ESR) of each MLCC is approximately 3 mΩ within the frequency range of interest and hence represents a negligible contribution to output ripple.

Figure 4. Plots of MLCC effective capacitance vs. voltage (a) and temperature (b) for a 22 µF/25 V/1210/X7R

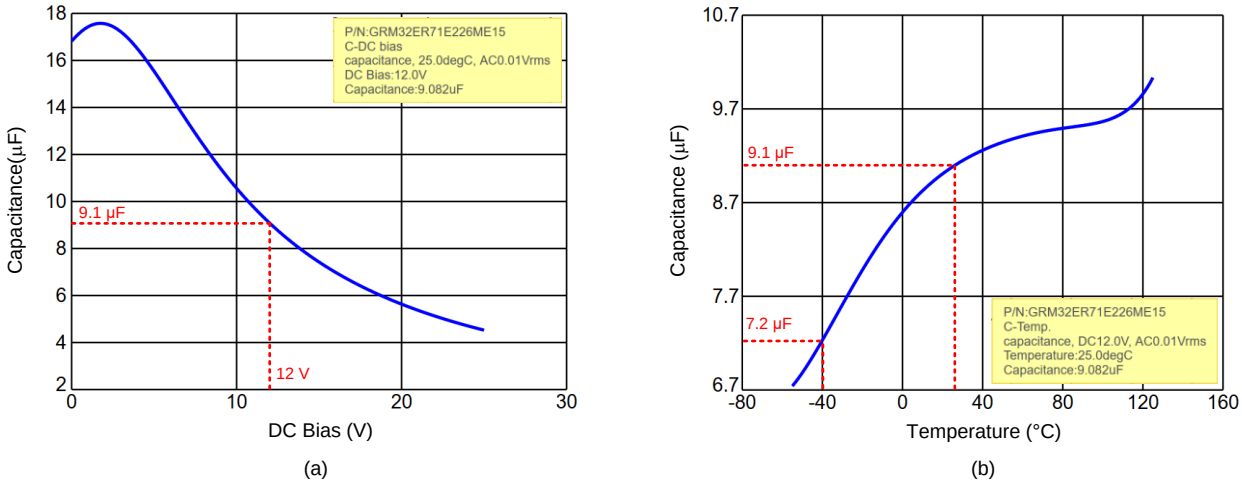
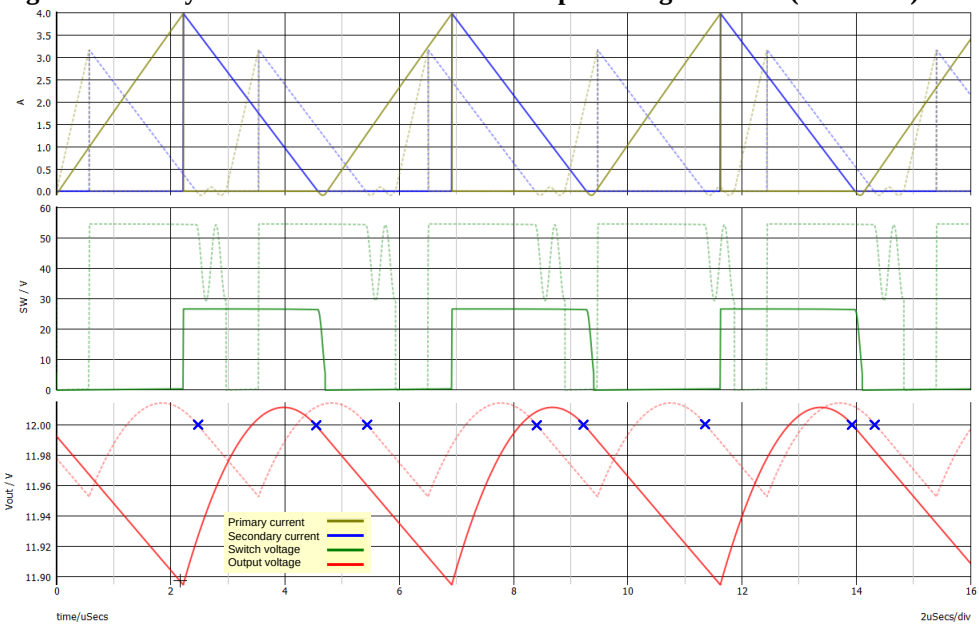


Figure 5 shows the simulated primary and secondary currents, primary switch voltage, and output capacitor ripple voltage at input voltages of 14 V (BCM) and 42 V (DCM) with an effective output capacitance of 22 µF. For simplicity, the oscillatory effects of transformer parasitic leakage inductance are not included here.

The × symbols mark the sampling instants on the output voltage waveform – note that sampling occurs at an instantaneous output voltage of 12 V close to the peak of the ripple waveform, but the DC output voltage is slightly lower given the total ripple amplitude.

Figure 5. PSR flyback converter waveforms at input voltages of 14 V (solid lines) and 42 V (dotted lines).



Small-signal stability review

As shown by the waveforms in Figure 3, the flyback converter delivers the entire magnetizing energy stored during the on-time t_{ON} to the output during the diode conduction time t_D. And unlike DCM where the control variable is the duty cycle, a converter in BCM regulates the output voltage by varying the on-time of the primary switch, which then controls the average diode current I_D. As a result, the duty cycle remains approximately constant, and I_D through the effective impedance of the output filter and load establishes the output voltage.

Neglecting high-frequency phase delays related to current-mode control and PSR sample-and-hold, Equation 7 gives the overall loop gain as a product of the control-to output (modulator and power stage), feedback, and compensator transfer functions:

$$T_V(s) = G_{VC}(s)G_C(s)G_{FB}(s) = \begin{cases} \left[\frac{N_{PS}R_L}{2R_i}\left(\frac{1-D}{1+D}\right)\frac{1-s/\omega_{zRHP}}{1+s/\omega_p}\right]\left[g_mR_{EA}\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right]\frac{V_{REF}}{V_{OUT}}, & \text{BCM} \\ \left[\frac{1}{R_i}\sqrt{\frac{L_{mag}F_{SW}R_L}{2}}\left(\frac{1-s/\omega_{zRHP}}{1+s/\omega_p}\right)\right]\left[g_mR_{EA}\left(\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right)\right]\frac{V_{REF}}{V_{OUT}}, & \text{DCM} \\ \left[\frac{K_{VCO}}{R_i}\left(\frac{N_{PS}V_{OUT}}{2F_{SW}}\right)\left(\frac{1-s/\omega_{RHPZ}}{1+s/\omega_p}\right)\right]\left[g_mR_{EA}\left(\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right)\right]\frac{V_{REF}}{V_{OUT}}, & \text{FFM} \end{cases} \quad (7)$$

where R_L is the load resistance; R_i is the effective current-sense resistance; ω_p is the power-stage load pole; ω_{p1} and ω_{z1} are the pole and zero of a type-2 compensator; and g_mR_{EA} is the DC gain of the transconductance error amplifier. K_{VCO} is the VCO gain from control voltage to switching frequency in FFM. ω_{zRHP} is the right-half-plane zero (RHPZ) of the flyback power stage (related to the phase shift delay of the secondary current when the primary current changes). The RHPZ, however, locates at sufficiently high frequency that it can be ignored for analysis in DCM.

Equation 8 gives the power stage dominant pole:

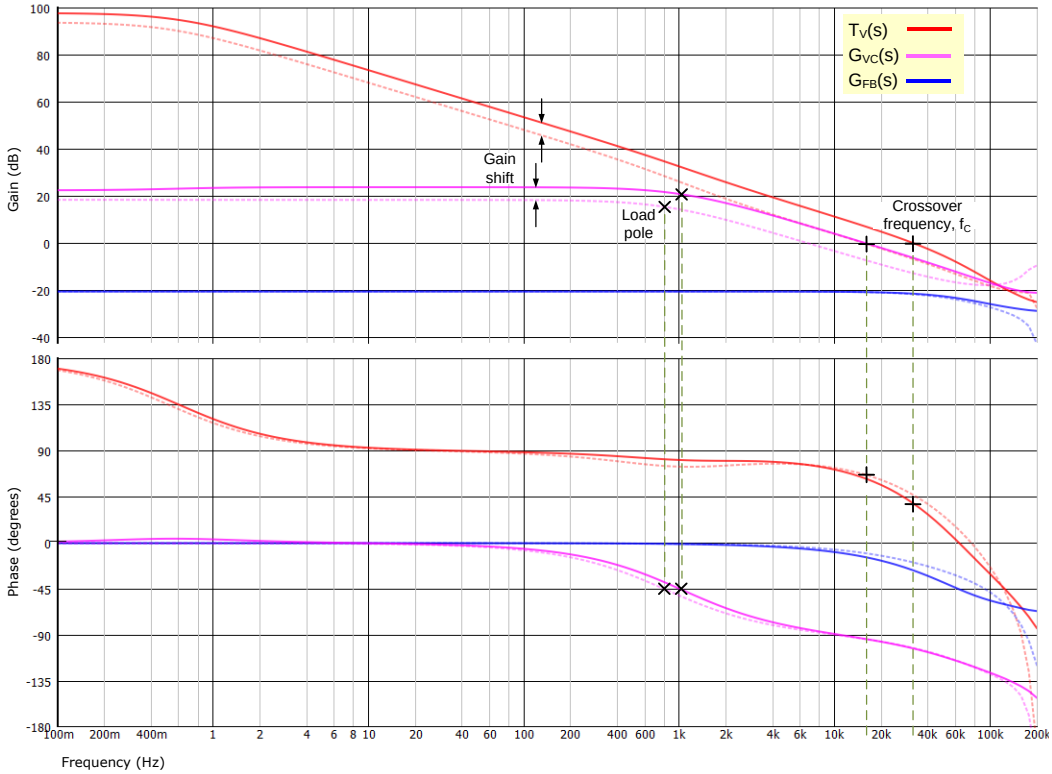
$$\omega_p = \begin{cases} (1+D)/R_LC_{OUT}, & \text{BCM} \\ 2/R_LC_{OUT}, & \text{DCM and FFM} \end{cases} \quad (8)$$

Interestingly, as the PSR sample-and-hold occurs at an instantaneous secondary current of zero, the left-half-plane zero evident in the control-to-output transfer function – normally associated with the output capacitor and its equivalent series resistance

(ESR) – shows no impact on the overall loop gain transfer function and thus is not included here. In fact, the ESR zero is offset by a corresponding pole in the feedback-sampler transfer function.

Figure 6 shows bode plot simulations of the overall loop gain for the converter circuit in Figure 1 at input voltages of 14 V and 42 V, assuming a total effective output capacitance of 22 µF. Simulation is mandatory here as practical measurements are not feasible given the integrated compensation design. Besides, the feedback (FB) node sees AC current based on the switch-voltage swing, making it unsuitable as an oscillator signal injection point for loop response measurements.

Figure 6. Simulated bode plots at input voltages of 14 V (dotted lines, BCM) and 42 V (solid lines, DCM)



Clearly evident from the plot in Figure 6, the frequency of the load pole is higher in DCM than BCM, and the gain of $G_{VC}(s)$ in DCM is generally higher. These two factors result in an increased loop gain in DCM and thus a higher crossover frequency, f_C. Accordingly, the operating condition in DCM at full load sets the output capacitance requirement apropos loop stability. If the switching frequency in DCM is 350 kHz, a good target for maximum f_C is 35 kHz (10% of switching frequency).

Output capacitor sizing for small-signal stability

From Figure 6, the loop gain generally presents as a slope of -20 dB per decade up to and beyond f_C, simplifying the determination of required output capacitance. From Equation 7, Equation 9 gives a simplified loop gain expression in DCM:

$$T_V(s)\big|_{s\to j2\pi f_c} \approx \frac{1}{R_i}\sqrt{\frac{L_{MAG}F_{SW}R_L}{2}}\left(\frac{2}{sR_L C_{OUT}}\right)\left(g_m R_{EA}\frac{sR_C C_C}{sR_{EA}C_C}\right)\frac{V_{REF}}{V_{OUT}} \tag{9}$$

where R_C and C_C denote the compensation resistance and capacitance, respectively. This further simplifies to yield an expression for C_{OUT} based on a target crossover frequency at unity gain:

$$C_{OUT} \approx \frac{1}{f_C}\frac{g_m R_C V_{REF}}{\pi R_i V_{OUT}}\sqrt{\frac{L_{MAG}F_{SW}}{2R_L}} \tag{10}$$

Collating parameters from the LM25184 circuit shown in Figure 1, Equation 11 gives the output capacitance for a target crossover frequency of 35 kHz (10% of switching frequency):

$$C_{OUT}(\mu F) = \frac{1}{f_C\,(kHz)}\frac{15}{V_{OUT}}\sqrt{\frac{L_{MAG}}{R_L}} = \frac{1}{35\,kHz}\times\frac{15}{12\,V}\times\sqrt{\frac{7.5\,\mu H}{12\,\Omega}} = 28\,\mu F \tag{11}$$

The capacitance result is a slight overestimation given the attenuating contributions from the PSR sampler and the current-mode control high-frequency pole (although offset by the RHPZ zero gain) that may exist at high f_C. The result also aligns with generally satisfactory load transient response.

Summary

Proper selection of components for a flyback converter requires an understanding of mode behaviors and operating characteristics. This article examines the output capacitance requirement for a PSR flyback DC/DC converter as it pertains to peak-to-peak output ripple and small-signal stability. Worst case for output ripple is at minimum input voltage and full load, which normally corresponds to operation in BCM. Distinctly, the capacitance requirement for loop stability occurs at high input voltage and full load when operating in DCM.

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Related Websites

Product information:
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