Designed with TPSM82813SILR

3.6V input,

1.0V, 3A output.

1.Input supply

Input is supplied from TPSM84824MOLR.

Parameter	min		tyo	max	
Vin	-1.833%	3.534V	3.600V	3.666V	1.833%

The output of the TPSM84824MOLR is also supplied to other power sources.

2.Output required for TPSM82813 SILR

The output of the TPSM82813 SILR is supplied to the FPGA.

Parameter	min		typ	max	
Vout	-3.000%	0.970V	1.000V	1.030V	3.000%
Iout	-	-	-	2.000A	-

3.Designed material

The following materials are available.

- ・Schematic
- ・Bills of materials
- ・Cin/Cout Part data
- ・WEBNCH Summary Report

4. What I care about

4-1.Output accuracy

DC output accuracy	±1.081%	: Use a 0.1% resistor.
Load Regulation	±0.15%	: 0.05%/A×2A+α=0.1%+α α=0.05%
Line Regulation	±0.04%	: 0.02%/V×1V+α=0.02%+α α=0.02%
Vout Ripple	±0.5%	: ±5mV
Total output accuracy	±1.771%	

Satisfy the required output accuracy ± 3%

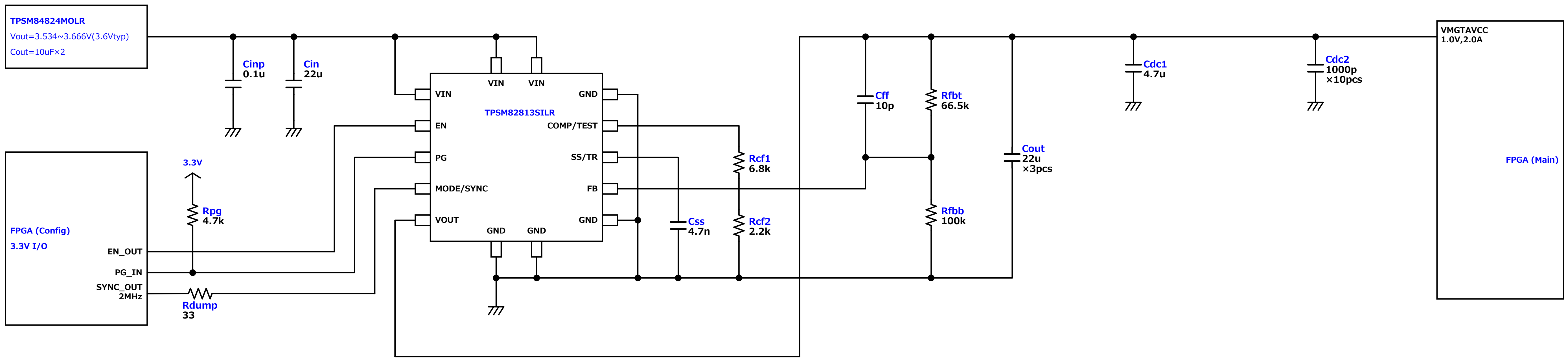
Is my output accuracy calculation correct?

4-2.External sync signal

I use an external sync signal.The frequency was designed at 2MHz.
Enter as shown in Schematic.
What kind of problem do you expect?

4-3.Cin/Cout

It was designed to use Murata's GRM21BR61E226ME44L for Cin and Cout.
Please tell me if there is any problem from the characteristic data.



TPSM84824MOLR
Vout=3.534~3.666V(3.6Vtyp)
Cout=10uF×2
Cinp
0.1u
Cin
22u
VIN
VIN
VIN
GND
TPSM82813SILR
EN
COMP/TEST
PG
SS/TR
MODE/SYNC
FB
VOUT
GND
GND
GND
Rcf1
6.8k
Rcf2
2.2k
Css
4.7n
Cff
10p
Rfbt
66.5k
Rfbb
100k
Cout
22u
×3pcs
Cdc1
4.7u
Cdc2
1000p
×10pcs
VMGTAVCC
1.0V,2.0A
FPGA (Main)
3.3V
Rpg
4.7k
FPGA (Config)
3.3V I/O
EN_OUT
PG_IN
SYNC_OUT
2MHz
Rdump
33

Part	Manufacturer	Part Number	Quantity	Description
Css	MuRata	GRM1555C1H472JE01D	1	Cap: 4.7 nF Total Derated Cap: 4.7 nF VDC: 50 V ESR: 4 mΩ Package: 0402
Rfbb	KOA	RN73R1ETTP1003B25	1	Resistance: 100 kΩ Tolerance: 0.1% Power: 63 mW Package: 0402
Rfbt	KOA	RN73R1ETTP6652B25	1	Resistance: 66.5 kΩ Tolerance: 0.1% Power: 63 mW Package: 0402
Rpg	KOA	RK73H1ETTP4701F	1	Resistance: 4.7 kΩ Tolerance: 1.0% Power: 0.1 W Package: 0402
U1	Texas Instruments	TPSM82813SILR	1	
Cin	MuRata	GRM21BR61E226ME44L	1	Cap: 22 µF Total Derated Cap: 13.5 µF VDC: 25 V ESR: 2 mΩ Package: 0805
Cout	MuRata	GRM21BR61E226ME44L	3	Cap: 22 µF Total Derated Cap: 64.2 µF VDC: 25 V ESR: 2 mΩ Package: 0805
Rcf1	KOA	RK73H1ETTP6801F	1	Resistance: 6.8 kΩ Tolerance: 1.0% Power: 0.1 W Package: 0402
Rcf2	KOA	RK73H1ETTP2201F	1	Resistance: 2.2 kΩ Tolerance: 1.0% Power: 0.1 W Package: 0402
Cff	MuRata	GRM0335C1H100JA01D	1	Cap: 10 pF Total Derated Cap: 10 pF VDC: 50 V ESR: 200 mΩ Package: 0201
Rdump	KOA	RK73H1ETTP33R0F	1	Resistance: 33 Ω Tolerance: 1.0% Power: 0.1 W Package: 0402
Cinp	MuRata	GRM033R61E104KE14D	1	Cap: 0.1 µF Total Derated Cap: 0.07 µF VDC: 25 V ESR: 30 mΩ Package: 0201
Cdc1	MuRata	GRM188R61E475KE11D	1	Cap: 4.7 µF Total Derated Cap: 4.5 µF VDC: 25 V ESR: 4 mΩ Package: 0603
Cdc2	MuRata	GRM0335C1E102JA01D	10	Cap: 1000 pF Total Derated Cap: 1000 pF VDC: 25 V ESR: 9 mΩ Package: 0201

ホーム　製品情報　製品詳細

コンデンサ 〉 セラミックコンデンサ(キャパシタ) 〉 セラミックコンデンサ(SMD)

一般用チップ積層セラミックコンデンサ

製品をご使用になる前にこちらを必ずお読みください
模倣品に関するご注意

GRM21BR61E226ME44#

「＃」には包装コードが入ります。

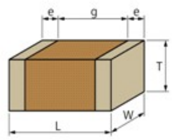
生産中

一般用　RoHS　REACH　85℃ max.　リフローOK　フローOK

＜包装コード有り品番一覧＞

GRM21BR61E226ME44L　GRM21BR61E226ME44K

外観および形状



スペック

近い仕様の製品を検索

L寸法	2.0±0.2mm
W寸法	1.25±0.2mm
T寸法	1.25±0.2mm
静電容量	22μF ±20%
外部電極間距離g	0.7mm min.
外部電極寸法e	0.2～0.7mm
使用温度範囲	-55℃ ～ 85℃
定格電圧	25Vdc
サイズコード mm	2012M
静電容量変化率	±15.0%
温度特性 (準拠規格)	X5R(EIA)
温度特性の温度範囲	-55℃ ～ 85℃

製品検索アシスタント

同サイズ又は小型サイズで近い仕様の候補製品をご提案いたします

■小型　■高容量　■高耐電圧　■高温対応　■DCバイアス特性重視　■近い容量のシリコンキャパシタを探す

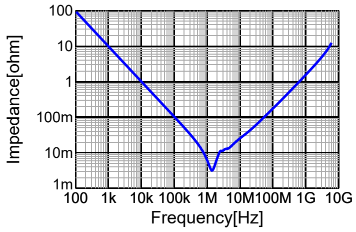
参考情報

包装コード	仕様	最小受注単位
L	180mmエンボステーピング	3000
K	330mmエンボステーピング	10000

質量 (代表値)	
1個	23.0mg
φ180mmリール	118g

特性データ

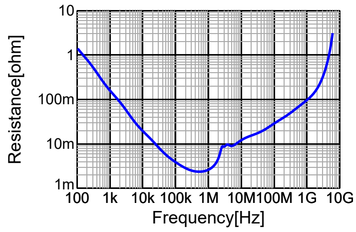
周波数特性|Z|



GRM21BR61E226ME44,DC0V,25degC

画像保存 ?

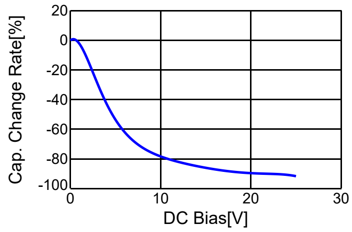
周波数特性R



GRM21BR61E226ME44,DC0V,25degC

画像保存 ?

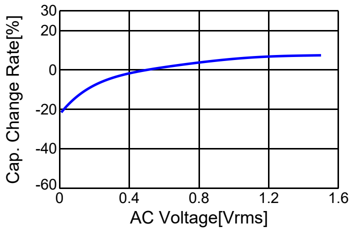
DCバイアス特性



GRM21BR61E226ME44,capchange, 25.0degC, AC0.5Vrms

画像保存 ?

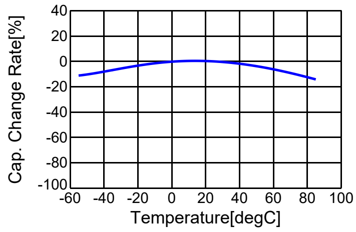
AC電圧特性



GRM21BR61E226ME44,capchange, DC0V, 25.0degC

画像保存 ?

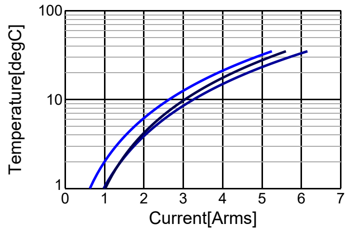
温度特性



GRM21BR61E226ME44,capchange, DC0.0V, AC0.2Vrms

画像保存 ?

リップル発熱特性



GRM21BR61E226ME44(☑80kHz ☑400kHz ☑800kHz)

画像保存 ?

(Simsurfing)さらに詳しいグラフ ?

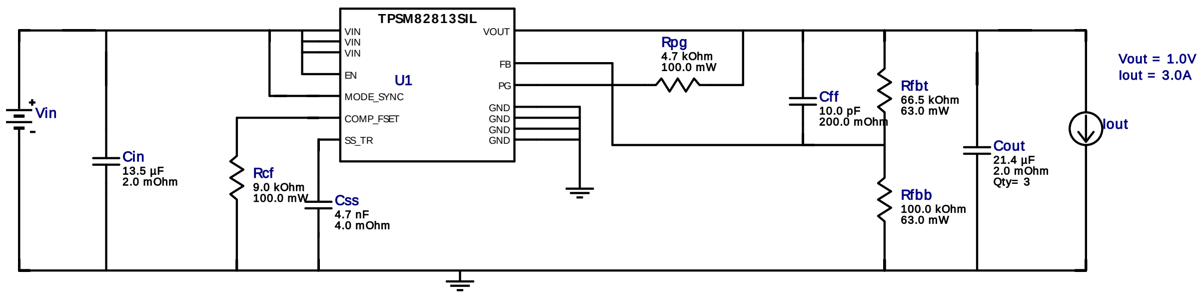
TEXAS INSTRUMENTS

WEBENCH ® Design Report

VinMin = 3.5V
VinMax = 3.7V
Vout = 1.0V
Iout = 3.0A

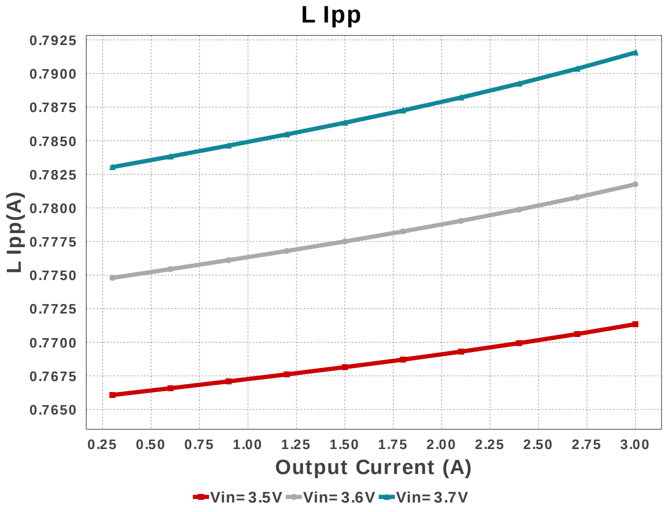
Device = TPSM82813SILR
Topology = Buck
Created = 2020-09-14 00:55:36.970
BOM Cost = $2.84
BOM Count = 11
Total Pd = 0.58W

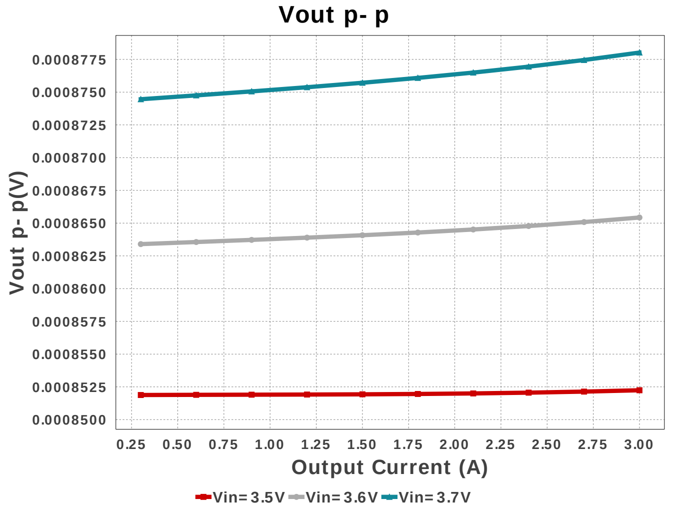
Design : 58 TPSM82813SILR
TPSM82813SILR 3.5V-3.7V to 1.00V @ 3A

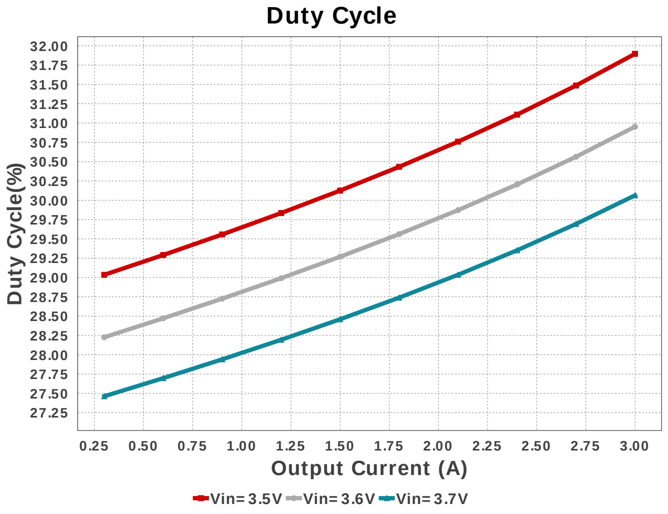


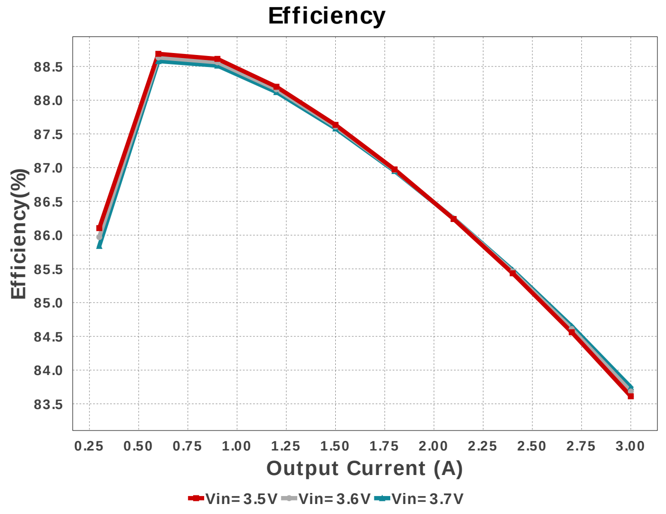
Electrical BOM

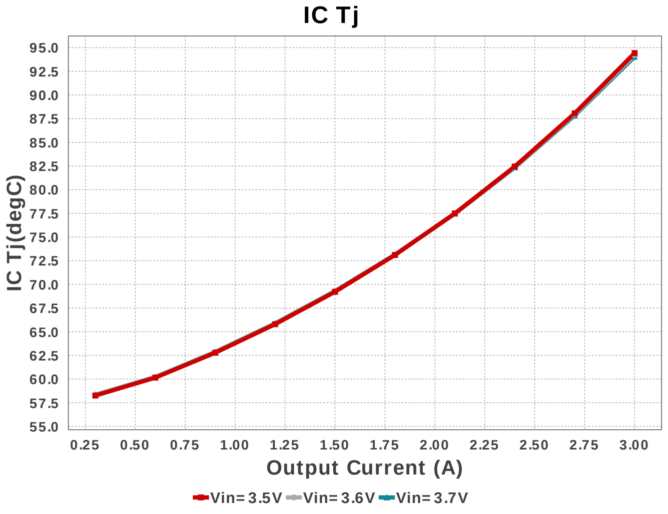
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cff	MuRata	GRM0335C1H100JA01D Series= C0G/NP0	Cap= 10.0 pF ESR= 200.0 mOhm VDC= 50.0 V IRMS= 0.0 A	1	$0.10	0201 2 mm²
Cin	MuRata	GRM21BR61E226ME44L Series= X5R	Cap= 13.5 uF ESR= 2.0 mOhm VDC= 25.0 V IRMS= 2.8 A	1	$0.10	0805 7 mm²
Cout	Murata	GRM21BR61E226ME44L Series= X5R	Cap= 21.4 uF ESR= 2.0 mOhm VDC= 25.0 V IRMS= 2.8 A	3	$0.10	0805 7 mm²
Css	MuRata	GRM1555C1H472JE01D Series= X5R	Cap= 4.7 nF ESR= 4.0 mOhm VDC= 50.0 V IRMS= 0.0 A	1	$0.10	0402 3 mm²
Rcf	KOA	RK73H1ETTP6801F Series= CRCW..e3	Res= 9.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	$0.10	0402 6 mm²
Rfbb	KOA	RN73R1ETTP1003B25 Series= CRCW..e3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 0.1%	1	$0.10	0402 3 mm²
Rfbt	KOA	RN73R1ETTP6652B25 Series= CRCW..e3	Res= 66.5 kOhm Power= 63.0 mW Tolerance= 0.1%	1	$0.10	0402 3 mm²
Rpg	KOA	RK73H1ETTP4701F Series= CRCW..e3	Res= 4.7 kOhm Power= 100.0 mW Tolerance= 1.0%	1	$0.10	0402 3 mm²
U1	Texas Instruments	TPSM82813SILR	Switcher	1	$1.84	SIL0014B 20 mm²

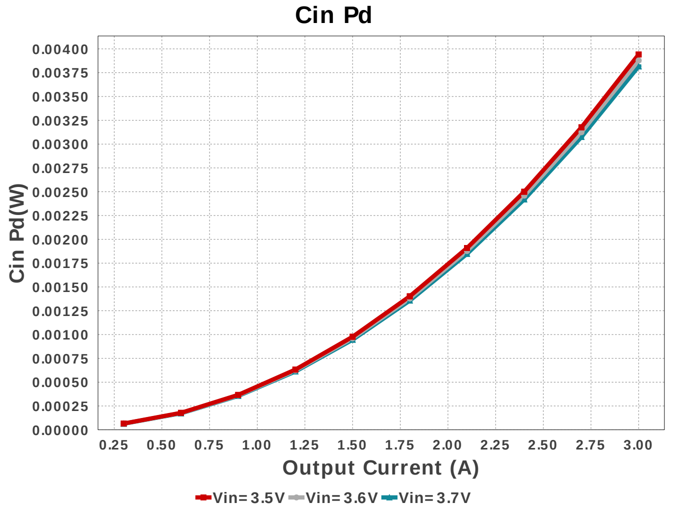

L Ipp
L Ipp(A)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V


Vout p- p
Vout p- p(V)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V

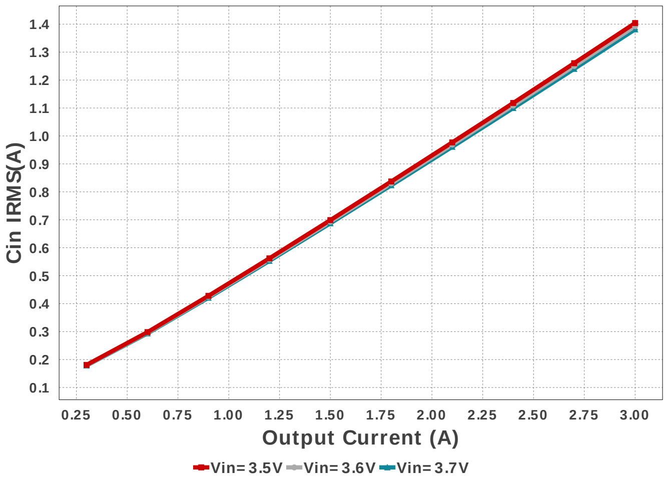

Duty Cycle
Duty Cycle(%)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V


Efficiency
Efficiency(%)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V

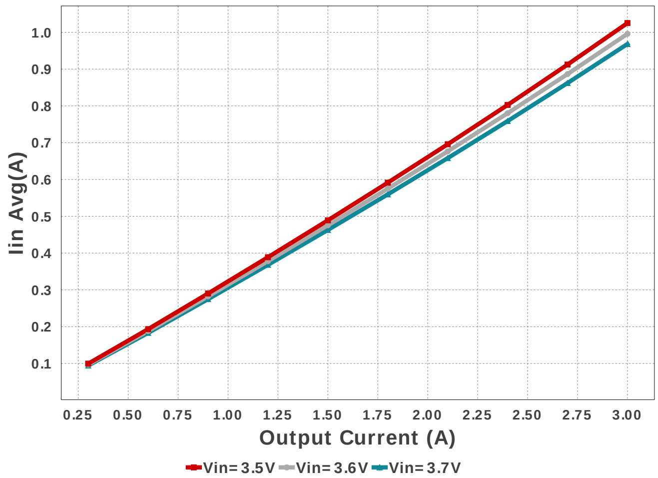

IC Tj
IC Tj(degC)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V


Cin Pd
Cin Pd(W)
Output Current (A)
Vin=3.5V Vin=3.6V Vin=3.7V

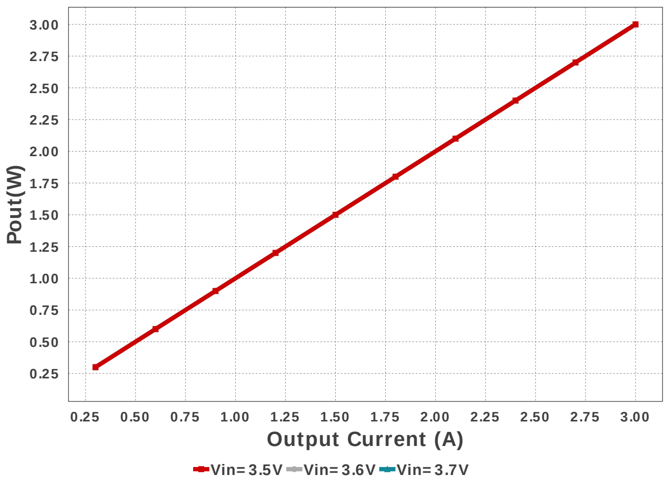
Cin IRMS



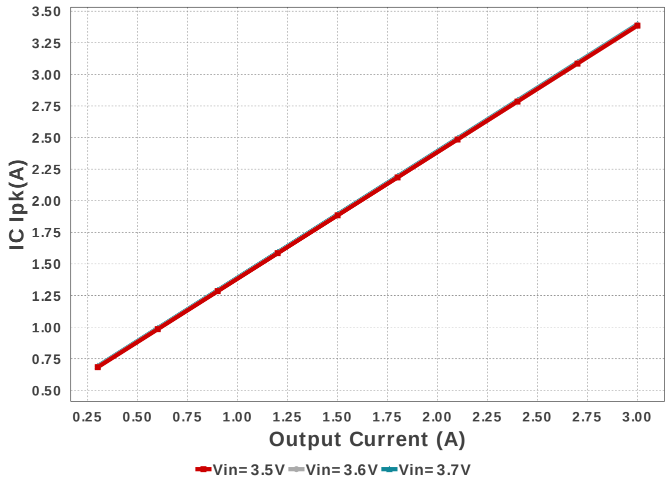
Iin Avg



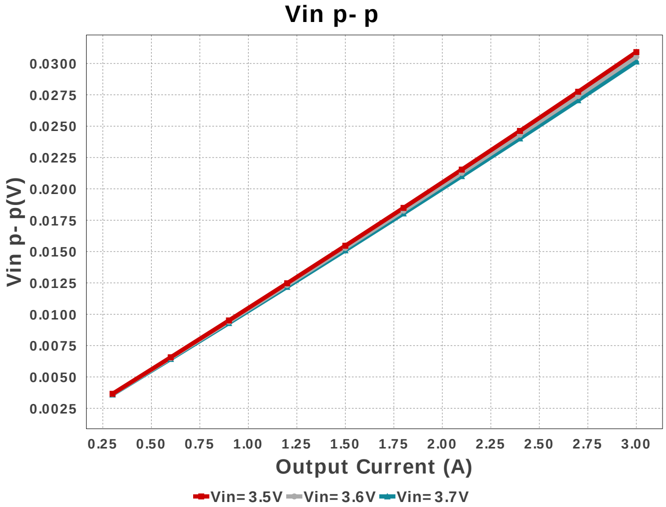
Pout



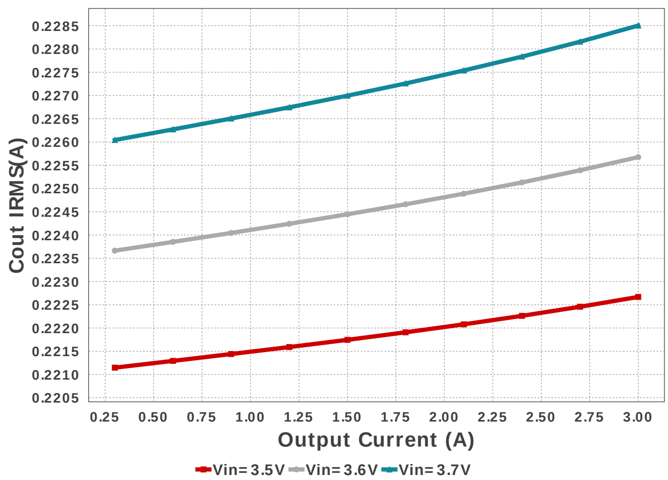
IC Ipk

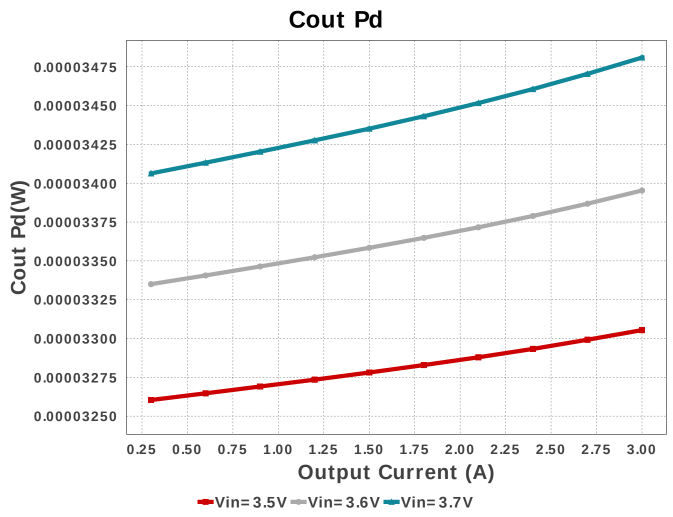


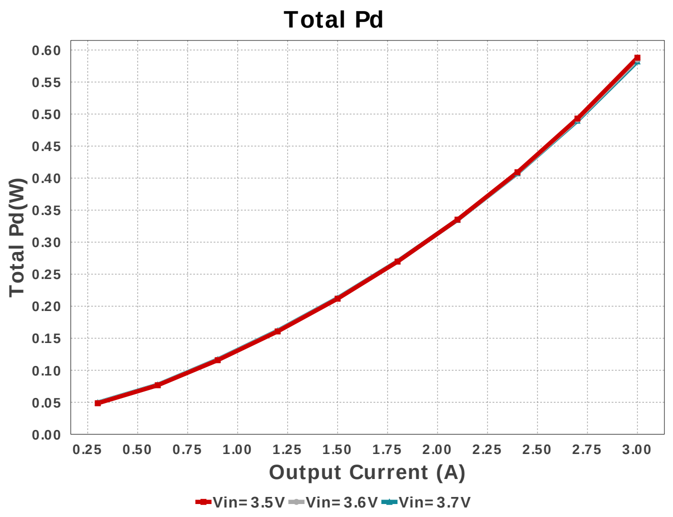
Vin p- p

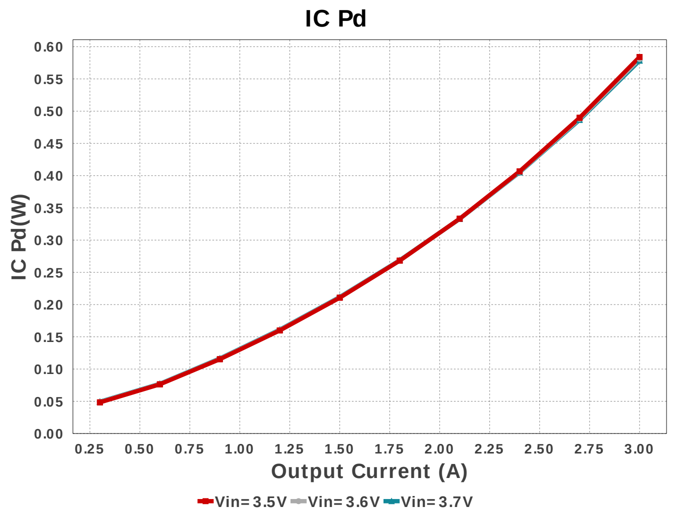


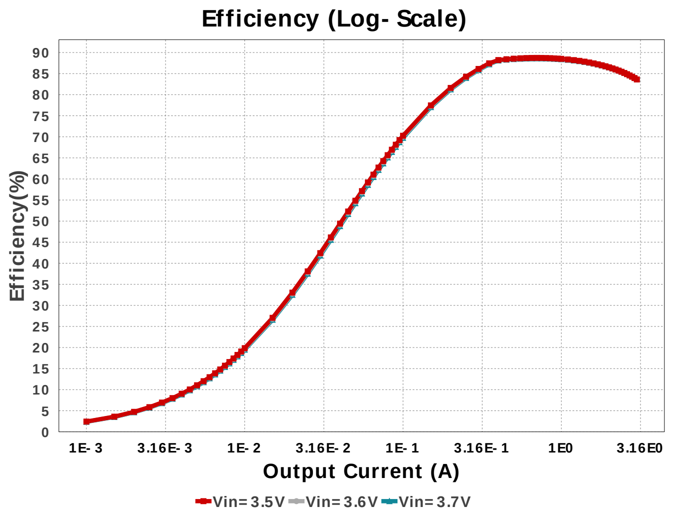
Cout IRMS











Operating Values

#	Name	Value	Category	Description
1.	BOM Count	11		Total Design BOM count
2.	Total BOM	$2.84		Total BOM Cost
3.	Cin IRMS	1.381 A	Capacitor	Input capacitor RMS ripple current
4.	Cin Pd	3.816 mW	Capacitor	Input capacitor power dissipation
5.	Cout IRMS	228.503 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	34.809 µW	Capacitor	Output capacitor power dissipation
7.	IC Ipk	3.396 A	IC	Peak switch current in IC
8.	IC Pd	578.36 mW	IC	IC power dissipation
9.	IC Tj	94.04 degC	IC	IC junction temperature
10.	IC Tolerance	6.0 mV	IC	IC Feedback Tolerance
11.	ICThetaJA	67.5 degC/W	IC	IC junction-to-ambient thermal resistance
12.	Iin Avg	968.17 mA	IC	Average input current
13.	Cin Pd	3.816 mW	Power	Input capacitor power dissipation
14.	Cout Pd	34.809 µW	Power	Output capacitor power dissipation
15.	IC Pd	578.36 mW	Power	IC power dissipation
16.	Total Pd	582.22 mW	Power	Total Power Dissipation
17.	Duty Cycle	30.063 %	System Information	Duty cycle
18.	Efficiency	83.747 %	System Information	Steady state efficiency
19.	FootPrint	64.0 mm^2	System Information	Total Foot Print Area of BOM components
20.	Frequency	2.0 MHz	System Information	Switching frequency
21.	Iout	3.0 A	System Information	Iout operating point
22.	L Ipp	791.559 mA	System Information	Peak-to-peak inductor ripple current
23.	Mode	FCCM	System Information	Conduction Mode
24.	Pout	3.0 W	System Information	Total output power

#	Name	Value	Category	Description
25.	Vin	3.7 V	System Information	Vin operating point
26.	Vin p-p	30.153 mV	System Information	Peak-to-peak input voltage
27.	Vout	1.0 V	System Information	Operational Output Voltage
28.	Vout Actual	999.0 mV	System Information	Vout Actual calculated based on selected voltage divider resistors
29.	Vout Tolerance	1.081 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
30.	Vout p-p	878.021 µV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	3.0	Maximum Output Current
SoftStart	1.0 ms	Soft Start Time (ms)
VinMax	3.7	Maximum input voltage
VinMin	3.5	Minimum input voltage
Vout	1.0	Output Voltage
base_pn	TPSM82813	Base Product Number
source	DC	Input Source Type
Ta	55.0	Ambient temperature
UserFsw	2.0 M	Customer Selected Frequency

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

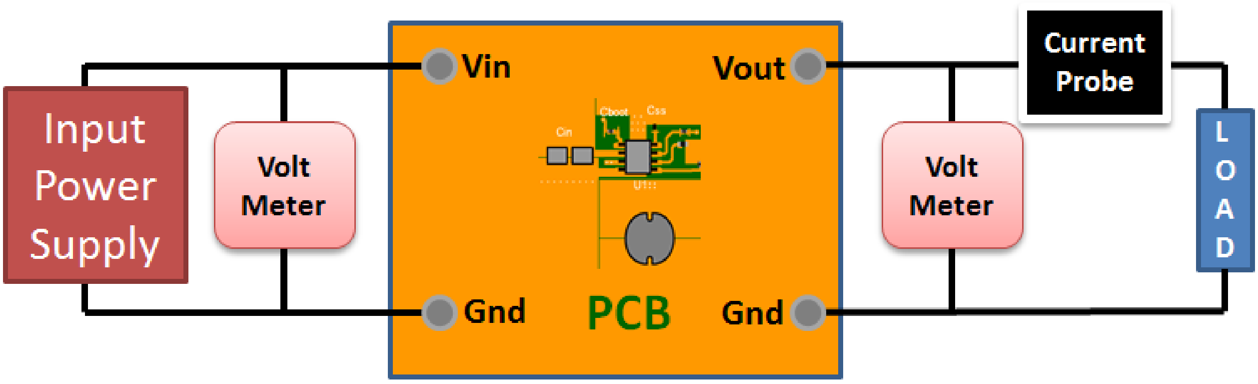
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 3.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : 4B22EECAC03607DD[v1]

2. **TPSM82813** Product Folder : http://www.ti.com/product/TPSM82813 : contains the data sheet and other resources.

Important Notice and Disclaimer

TI provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources AS IS and with all faults, and disclaims all warranties. These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Providing these resources does not expand or otherwise alter TI's applicable Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with TI products.