Understanding non-linear slope-compensation: a graphical analysis

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While current-mode control (CMC) remains the much preferred PWM scheme for switchmode power supplies, its advantages aren't automatic. Indeed, ensuring stability in a switchmode supply involves such factors as the right type of slope compensation, a subject that's not too easy to grasp without a cadre of mathematical formulae that, although necessary to successful modelling and design, more often than not keeps the typical system designer from appreciating the underlying issues. We address that issue in this article by turning to graphical representations derived from the basic CMC circuit equations to provide you with an intuitive understanding of what proper CMC and slope-compensation design are all about.

Overview

The primary advantage of CMC is simplified system-loop compensation. In the very simplest form, a single compensation capacitor, C_o, and resistor, R_o, are selected that cancel the predictable pole created by the RC pair. The resul-
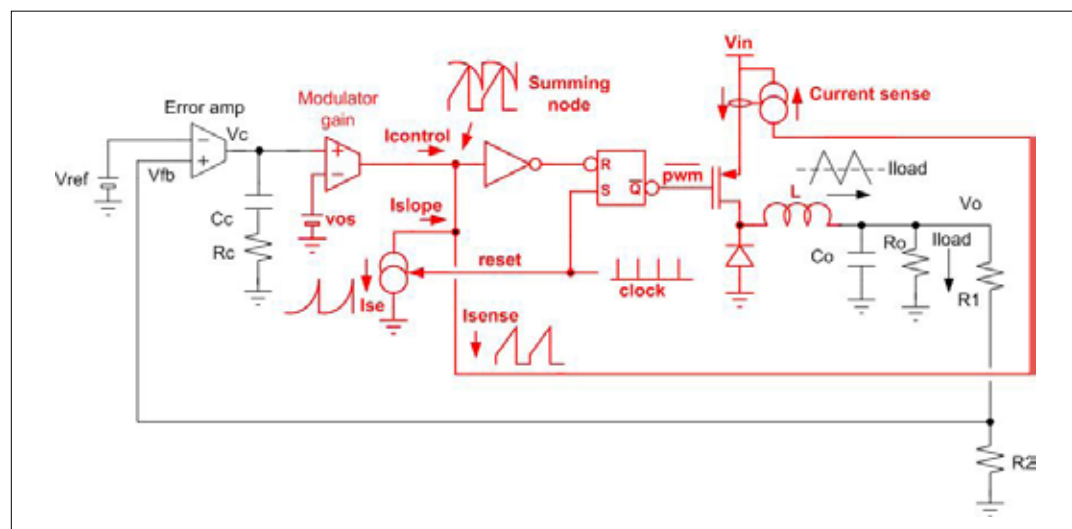

Fig. 1: Current-mode buck converter, CMC loop highlighted

tant loop acts as a single-pole system. Also, line regulation is inherently better, as is immunity from audio effects.

But there's more to it. For PWM duty cycles above 50 per cent, all current-mode control buck converters require a linear ramp (i.e., slope-compensation) to avoid sub-harmonic oscillation. And higher duty cycles require greater slope compensation. Using non-linear compensation circuitry (such as found in National's LM20xxx series, for instance) offers a better solution because it optimises the stability

of the regulator device over the entire output voltage range.

Basic current-mode operation

In the typical fixed-frequency DC/DC converter, a PWM pulse controls the time during which the inductor is energised within each switch period. CMC, in the simplest terms, compares a slow moving output-voltage error signal to the relatively fast changing inductor current. The inductor current sense signal can be converted to a 'sense' voltage signal for a voltage comparator based

CMC design, a method commonly described in the literature. Alternatively, the error signal can also be converted to a current so that the regulator's three signal currents (error or control, current sense, and slope compensation) can be summed at a common node for comparison. The two approaches are equivalent. Let's look at current-summing as shown in Fig. 1, which illustrates the entire control loop for a CMC buck DC/DC converter.

The CMC circuitry is highlighted in red. The RS flip-flop is central to the CMC timing. A fixed frequency clock sets the flip-flop, which then turns on the power FET and energises the inductor. This is the start of the PWM pulse. A current-sense feedback signal terminates the PWM when the energizing current in the inductor, reflected to the summing node via the sense circuit, reaches a peak control level, $I_{control} - I_{slope}$.

$I_{control}$ is directly related to the V_{out} error signal, V_c. During the PWM 'on' pulse time, the power FET conducts and inductor current increases. The rate of increase for the inductor current during this period is defined as S_u. It's controlled by the differ-
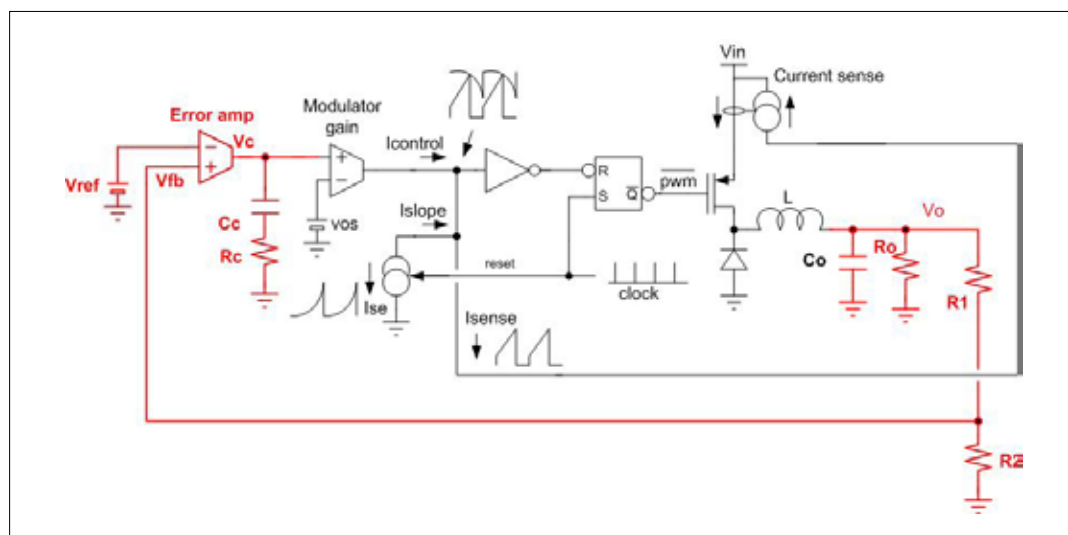

Fig. 2: Buck converter, voltage regulation loop highlighted

ence between V_{in} and V_{out}, the voltage drop in the FET switch, and the value of the inductor, L. More specifically, S_u increases with increasing (V_{in} - Vout) and decreases with increasing L. When the PWM pulse is terminated and the FET turns off, inductor current flows from the diode. The inductor current decreases linearly until the next cycle.

The rate of inductor current change during this 'off' time is defined as S_d. The waveform diagrams that follow assume the voltage drop in the FET switch and the diode has negligible effect on the shape of the waveforms. The diode is often replaced with a low-loss synchronous FET switch.

A p-channel MOSFET is used in this circuit, but the switch could be an n-channel MOSFET. In the steady state condition, the starting and ending inductor currents within a switching period, T_s, are identical. The average inductor current is the DC/DC converter load current.

Only the peak inductor current needs to be sensed. For this reason sensing the current in the power FET is equally effective as sensing the actual inductor current. I_{sense} is typically 10 microamps to 100 microamps per ampere of inductor current.

Current-mode control is desirable because the CMC loop in effect forces the peak current to be the same for each switch cycle as long as V_c is constant. Thus, the inductor in combina-
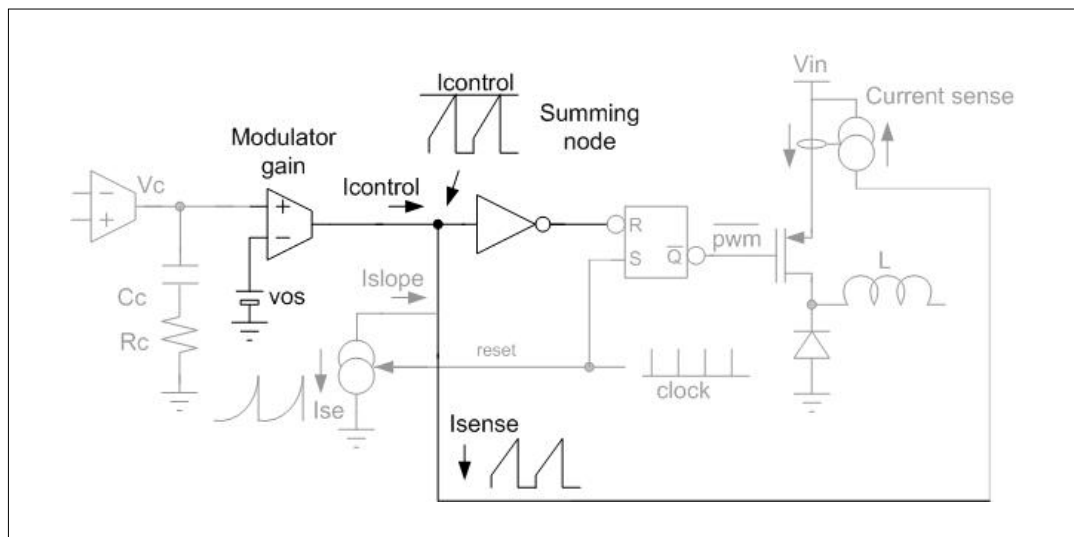

Fig. 3: CMC summing node without slope compensation

tion with the CMC loop can be thought of as a current source. Unlike voltage-mode control, the inductor L and output filter capacitor, C_o, do not contribute a complex pole pair to the overall system loop. The removal of a power pole due to L in the CMC system loop removes the need for a corresponding zero in the overall system compensation network. A single RC network is adequate for optimal CMC system compensation, a significant reduction in complexity for tuning system performance.

The non-CMC portion of the system loop, highlighted in Fig. 2, generates the control voltage, V_c. In operation, this "outside" loop regulates V_{out} by providing the control signal to the CMC circuitry. In turn, the CMC provides the PWM value that generates the desired output

voltage, which in turn satisfies the requirement for balance at the error amplifier's input.

Now consider the basic summing node signals at the core of the CMC loop (Fig. 3). The waveforms shown at the summing node excludes the slope compensation current, I_{slope}. I_{sense} is representative of the inductor current during PWM high, and returns to zero once I_{sense} exceeds $I_{control}$ and the PWM is terminated.

The peak current in the inductor is limited by the $I_{control}$ signal, which is directly controlled by the output of the error signal, V_c. The CMC also requires the addition of I_{slope} to the control signal. This additional signal is shown in Fig. 4.

The effect of I_{slope} is to modify the slow moving $I_{control}$ signal so that it has a downward slope for

the duration of each switching cycle. Notice the change of the two summing node waveforms with the addition of I_{slope}. This example illustrates a non-linear I_{slope} signal. I_{slope} is often a sawtooth waveform with linear ramp. But as we will see, there's a great difference between linear and non-linear slope compensation.

Evaluating the transient responses

What role does I_{slope} play in the operation of the CMC loop? To find out, let's observe the settling of the inductor current loop in response to a theoretical disruption of the inductor current.

The loop's recovery to a hypothetical disruption in inductor current, under certain regions of CMC operation, can take excessive time to settle. Sometimes, settling is never achieved and the circuit falls into the sub-harmonic oscillation seen in improperly compensated CMC circuits.

The first three sets of plots in Figs. 5-7 show current settling for duty cycles of 25, 50, and 66 per cent, respectively, for a CMC loop that has no I_{slope}. In each case the load current or average inductor current is arbitrarily selected to be 2.5 amps and the inductor ripple current is adjusted to be 30 per cent of the load current. The desired value of switching frequency, duty cycle, V_{out}, and ripple current specify the value of inductor for each case. These three examples represent the
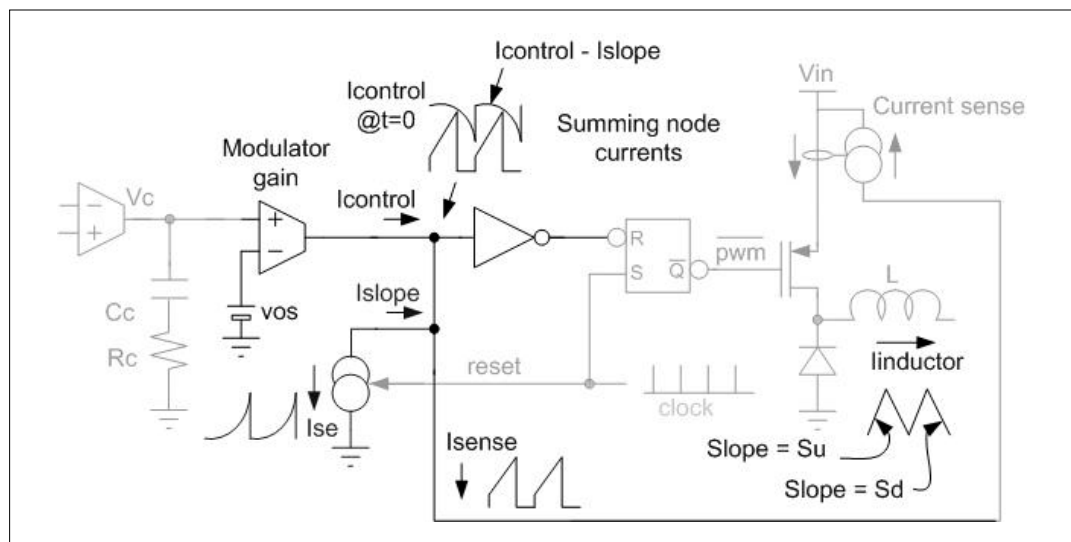

Fig. 4: CMC summing node with slope compensation

same control circuit and input supply operating with three different feedback attenuation resistor settings that provide three different values of V_{out}.

See Fig. 5. For all the waveforms in this section, the green dashed triangle waveform is the expected steady state inductor current for the specific application's duty cycle. The duty cycle is 25 per cent; therefore the power FET is conducting energizing current from V_{in} to the load via the inductor for approximately the first 25 per cent of each switching cycle.

The solid black lines are the CMC control currents referenced to the inductor current. The control current determines the peak value of the sensed inductor current, so it is convenient to refer the control signal to the level of the inductor current in order to plot the two signals on the same scale. The third (solid red) waveform is a hypothetical perturbed inductor current which at time t=0 is one half of the steady state inductor current. The perturbed inductor current is still constrained by V_{in} and V_{out} to have 'on' and 'off' period slopes of S_u and S_d. For 25 per cent duty cycle, the perturbation to the inductor current is able to converge to the desired steady state pattern within several switching cycles. Now consider a 50 per cent duty cycle (Fig. 6) without slope compensation, and where the instability can become even more significant. The effective control current and the steady state current are the same as in Figs. 5 and 6. Again, the load and ripple current are adjusted to the same target of 2.5 amps and 30 per cent. The value of V_{in} and V_{out} are adjusted for a duty cycle of 50 per cent and the value of S_u and S_d change accordingly.

There is now a significant change in the ability of the perturbed inductor current to converge to the desired steady state inductor current. The resulting inductor current and PWM appear to be locked into alternating between two values of duty cycle, with the average being 50 percent.

This operation is commonly described as sub-harmonic oscillation because the pattern is often repeated at one half of the switching frequency. A 50 per cent duty cycle is the theoretical limit for stable CMC operation without any slope compensation.

Figure 7 has the same load and ripple current as before. Here, V_{out} is set to 2/3 V_{in}. Without any slope compensation in this example, we see that perturbed inductor current is unable to converge to the desired steady state pattern and its variation in PWM is even more erratic than in the 50 per cent example. The math says that this waveform will eventually settle to a sub-harmonic oscillation as well.

Adding slope compensation
The next series of plots (Figs. 8-10) show the same power converter applications (fixed Vin, Vout, L, and load) with the addition of an artificial slope compensation signal, I-slope, to the summing node of the CMC circuit. How does this additional time dependent bias signal help avoid the runaway condition seen in Figs. 6 and 7?

Notice that without slope compensation for duty cycles greater than 50 per cent, S_d has a greater magnitude than S_u. This means that for perturbed currents, and for higher duty cycles, the downward current moves away from the control signal at a greater rate. The rate of divergence of the downward inductor current from the control signal becomes greater than the rate of convergence of the upward inductor current to the control current in this region of high duty cycle. Intuitively, the higher rate of divergence during the 'off' time leads to overall divergence of the inductor current and therefore instability.

The up and down slopes of the inductor current can not be changed for a fixed application, but the apparent rate of convergence and divergence can be artificially modified. The solution for stability at higher values of duty cycle is to change the slope
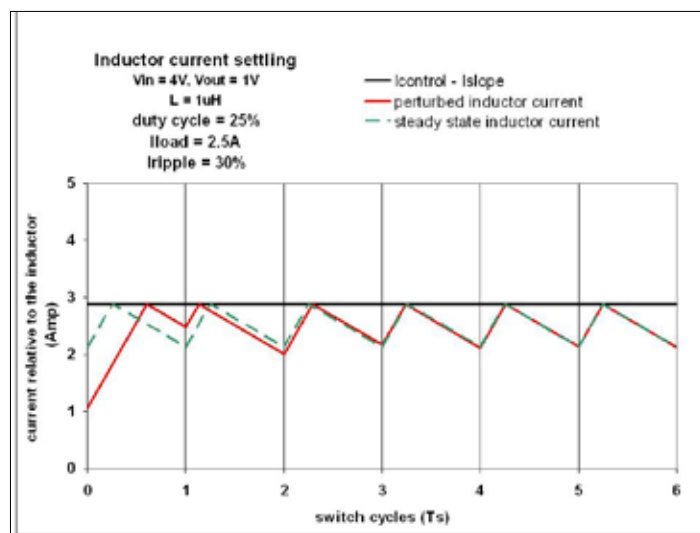

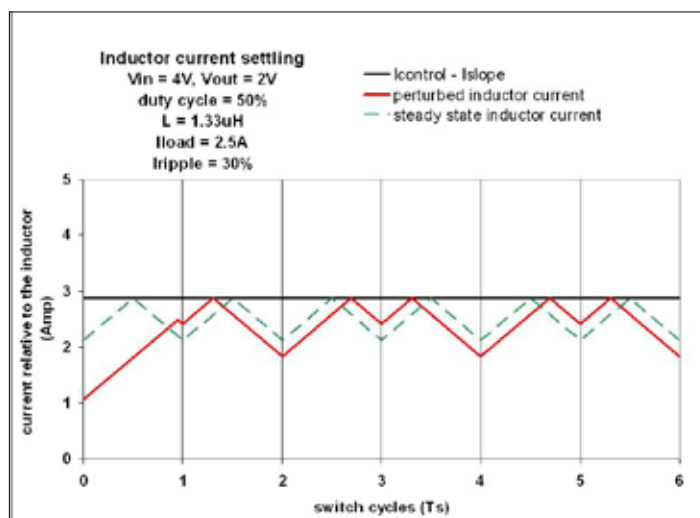Fig. 5: Perturbed inductor current; duty cycle = 25, Islope = 0.
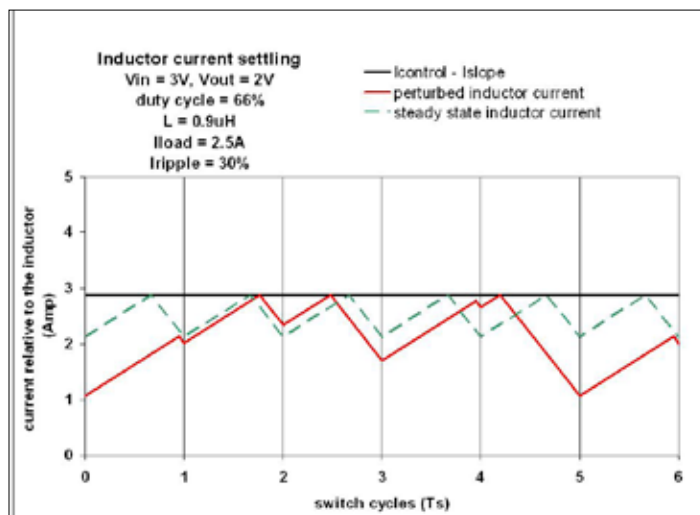

Fig. 6: Inductor current; duty cycle = 50, Islope = 0.

Fig. 7: Inductor current; duty cycle = 66, Islope = 0.

of the control signal to favour a lesser rate of divergence for the downward inductor current from the control signal.

We modify the control signal by the addition of a linear I_{slope} signal, as shown in Fig. 8. I_{slope} is subtracted from the $I_{control}$ (see $I_{control}$ - I_{slope} waveform). We define the slope of I_{slope} as S_e. Even this minor modification provides for a substantial improvement in the recovery time of the perturbed inductor current for a 50 per cent duty cycle. The question becomes how much slope
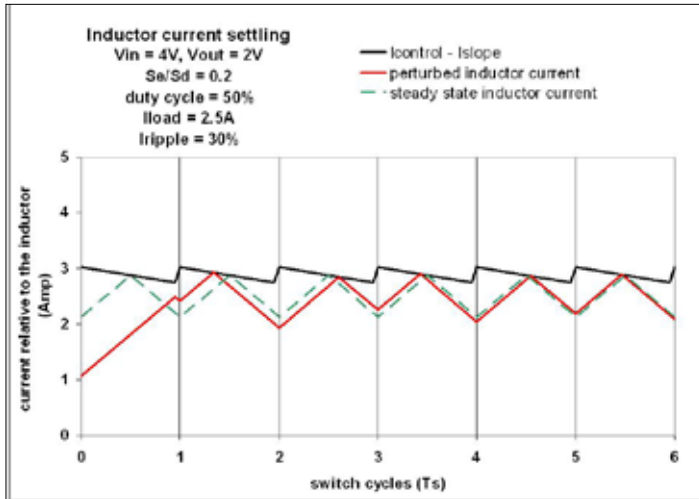
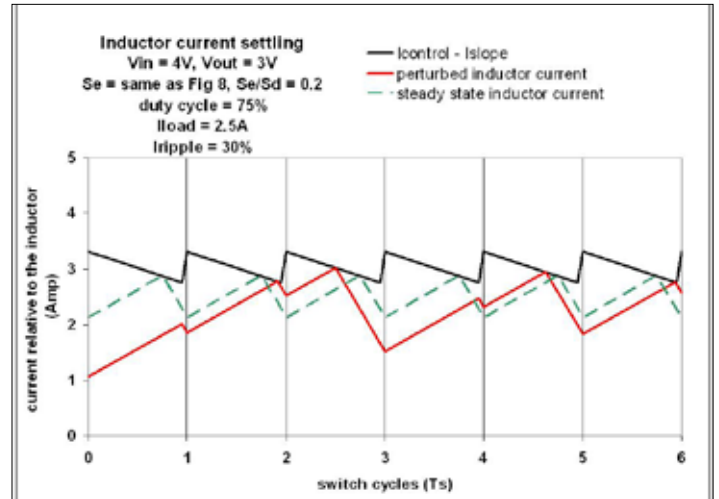Fig. 8: Inductor current; duty cycle = 50, Islope = 0.2 Isense.

Fig. 9: Inductor current; duty cycle = 75, Islope = 0.2 Isense.

Fig. 10: Inductor current; duty cycle = 50, Islope = Isense.

compensation is required for stability in all applications?

The relative ratio of I_{slope} to inductor current needs to increase for higher duty cycles to have the same stabilising effect. To illustrate this point, the value of I_{slope} in Fig. 8 is not acceptable at 75 per cent duty cycle.

See Fig. 9. Clearly, differing contributions of slope compensation are needed for different duty cycle applications, (different values of V_{out}). This leads us to the next level: non-linear slope compensation. This technique will increases I_{slope} as the duty cycle increases. This concept is illustrated by the same perturbed inductor current versus time plots.

First it is necessary to consider what the proper ratio of I_{slope} to I_{sense} is for a given duty cycle. Figure 10 illustrates a very special value of I_{slope}, the case where I_{slope} is the same as the downward slope of the inductor current, or $S_e = S_d$.

The result of the special case is that the perturbed inductor current settles in one switching cycle. This condition is often called 'deadbeat.' With *linear* slope compensation and a fixed value of S_e, this condition can only occur with one value of V_{out} and one value of inductor. With *non-linear* slope compensation, deadbeat can be secured for a wide range of V_{out} settings.

In part 2 of this article, we'll introduce non-linear slope compensation with time plots of inductor current for three values of V_{in} for a fixed V_{out} value. We'll wind up by highlighting the relative strengths of linear and non-linear slope compensation.

References

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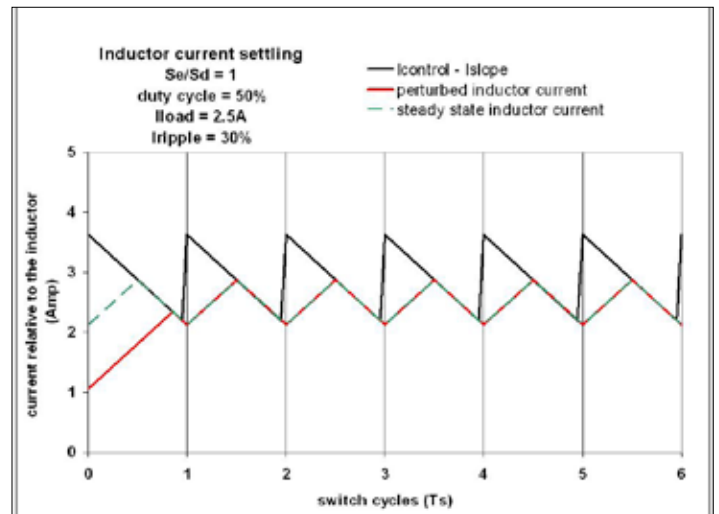2. Raymond B. Ridley, "A New, Continuous Time Model for Current Mode Control," IEEE Transactions on Power Electronics, Vol 6, No 2, 1991 pp. 271-280.
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