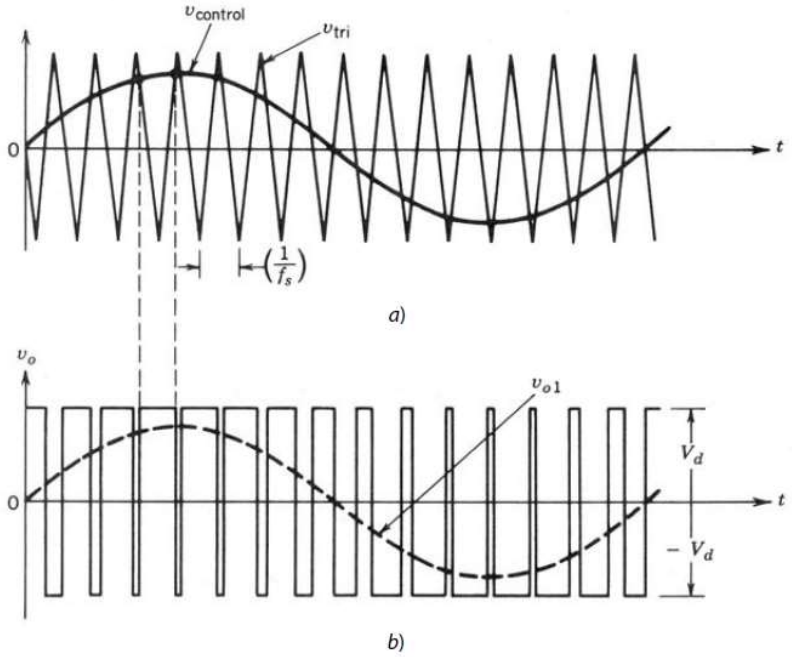
Some details of the design:

- Switching frequency: 20KHz.
- Duty cycle: being an inverter, the control of the UCC27282 is by PWMS. So, the duty cycle is variable. But I can give you the amplitude modulation ratio which is ma = 0.9. and the frequency modulation ratio is mf = 50.




- Regarding the Rgate value, I just followed the example in the UCC27282 datasheet.

**Figure 8-1. Typical Application**

**8.2.1 Design Requirements**

Table below lists the system parameters. UCC27282 needs to operate satisfactorily in conjunction with them.

**Table 8-1. Design Requirements**

| Parameter | Value |
|---|---|
| MOSFET | CSD19535KTT |
| Maximum Bus/Input Voltage, $V_{in}$ | 75V |
| Operating Bias Votage, $V_{DD}$ | 7V |
| Switching Frequency, Fsw | 300kHz |
| Total Gate Charge of FET at given VDD, $Q_G$ | 52nC |
| MOSFET Internal Gate Resistance, $R_{GFET\_Int}$ | 1.4 |
| Maximum Duty Cycle, $D_{Max}$ | 0.5 |
| Gate Driver | UCC27282 |

In the case of the inverter, I am using the CSD19536KCS.

Use Equation 9 to calculate the driver high-side pull-up current.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}}$$

Vdd= 7V; Vdh=0.85V;
Rhoh= 0.13/100mA=1.3ohm

Iohh= 6.15V/(1.3+3.3+1.4)= 1.025A.

where

- $I_{OHH}$ is the high-side, peak pull-up current
- $V_{DH}$ is the bootstrap diode forward voltage drop
- $R_{HOH}$ is the gate driver internal high-side pull-up resistor. Value either directly provided in datasheet or can be calculated from test conditions ($R_{HOH} = V_{HOH}/I_{HO}$)
- $R_{GATE}$ is the external gate resistance connected between driver output and power MOSFET gate
- $R_{GFET(int)}$ is the MOSFET internal gate resistance provided by MOSFET datasheet

Use Equation 10 to calculate the driver high-side sink current.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}}$$

Vdd= 7V; Vdh=1V;
Rhol= 0.1/100mA=1ohm

Iolh= 6.15V/(1+1.2+1)= 1.92A.

where

- $R_{HOL}$ is the gate driver internal high-side pull-down resistance

Use Equation 11 to calculate the driver low-side source current.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}}$$

Vdd= 7V; Vdh=1V;
Rloh= 0.13/100mA=1.3ohm

Iohh= 7V/(1.3+3.3+1.4)= 1.18A.

where

- $R_{LOH}$ is the gate driver internal low-side pull-up resistance

Use Equation 12 to calculate the driver low-side sink current.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}}$$

Vdd= 7V; Vdh=1V;
Rhol= 0.1/100mA=1ohm

Iolh= 7V/(1+1.2+1)= 2.18A.

where

- The LO, HO-HS and HS images will be sent to you in these days.

Finally, I attach a pdf file with the PCB design.