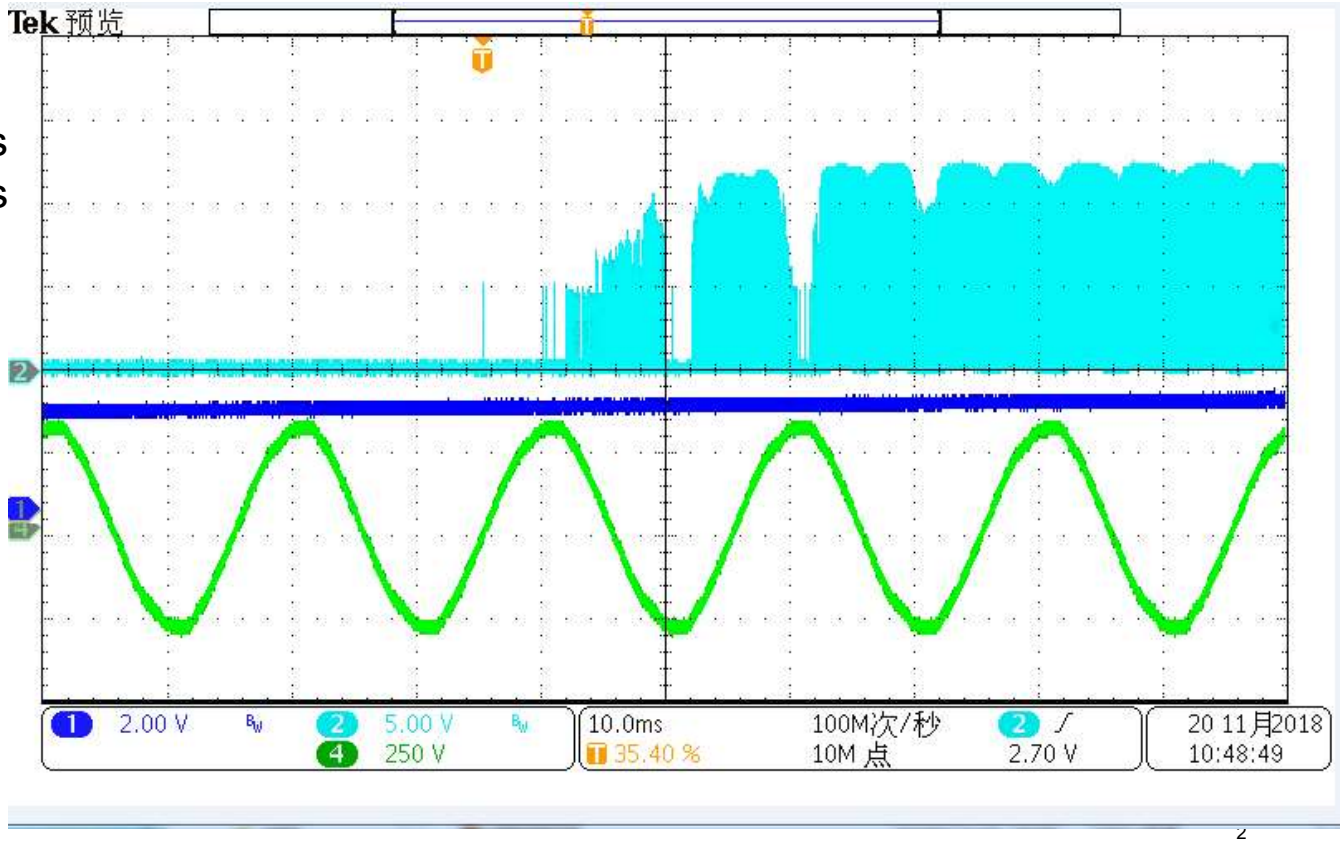
UCC28070

StartUp behaviour

Design Root Cause Analysis

Introduction

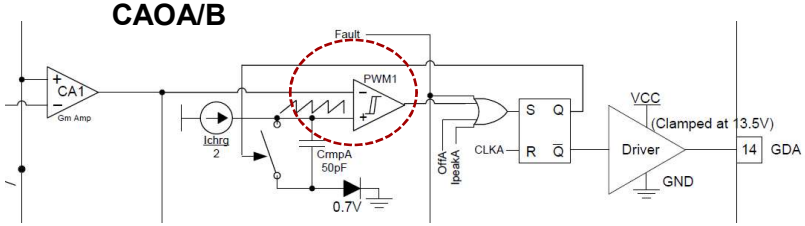
- Observe spurious PWM signal at Startup.
- There is a delay of some ms before normal operation starts
- The behavior was confirmed on the TI evm.
- TI Design
  - Ran simulations to reproduce the behavior.
  - Analyzed the design implementation to confirm the IC behavior.

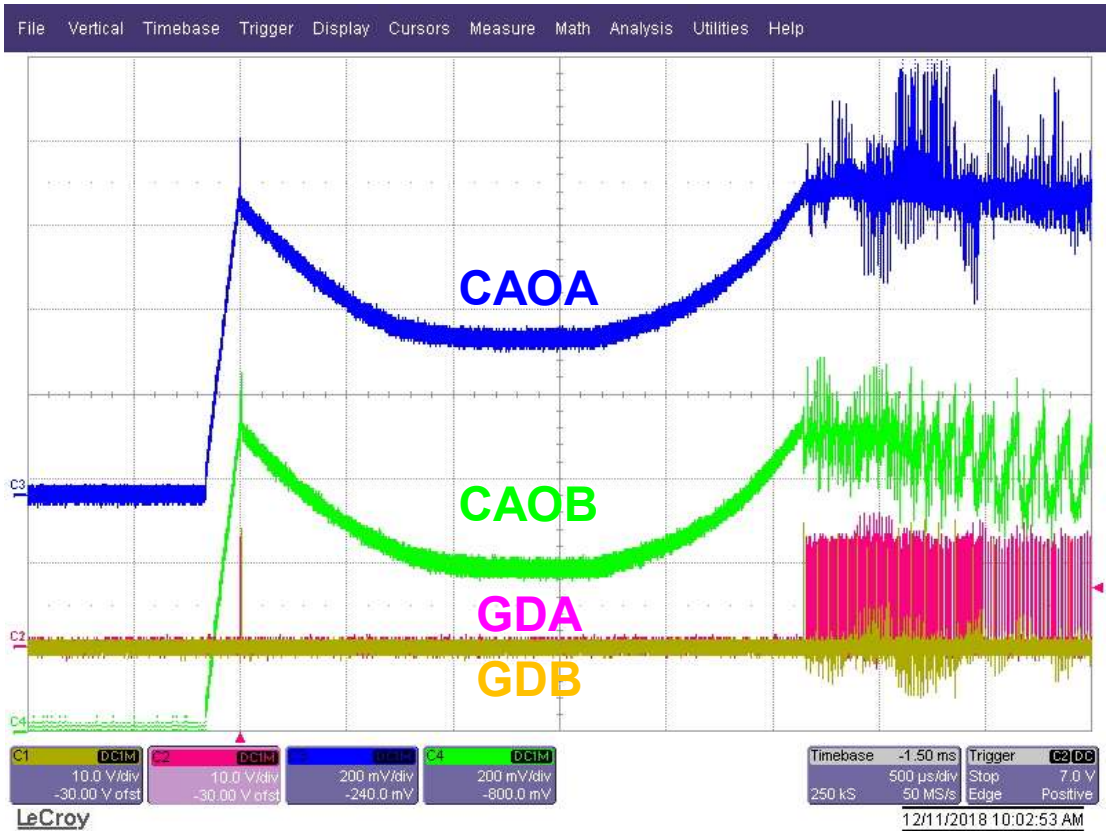


Root Cause Analysis - silicon

- The waveforms on Current Amplifier Output A (CAOA) and CAOB explain the behavior:
  - The switching is inhibit until CAOA/B < 0.7V, see circuit below
  - Once CAOA/B rises above 0.7V, at the first rising/falling edge of the clock GDA/GDB are turned on
  - After the first switching cycle CAOA/B decrease going below 0.7V, inhibiting any other switching cycle
  - The switching will restart again once CAOA/B goes again above 0.7V

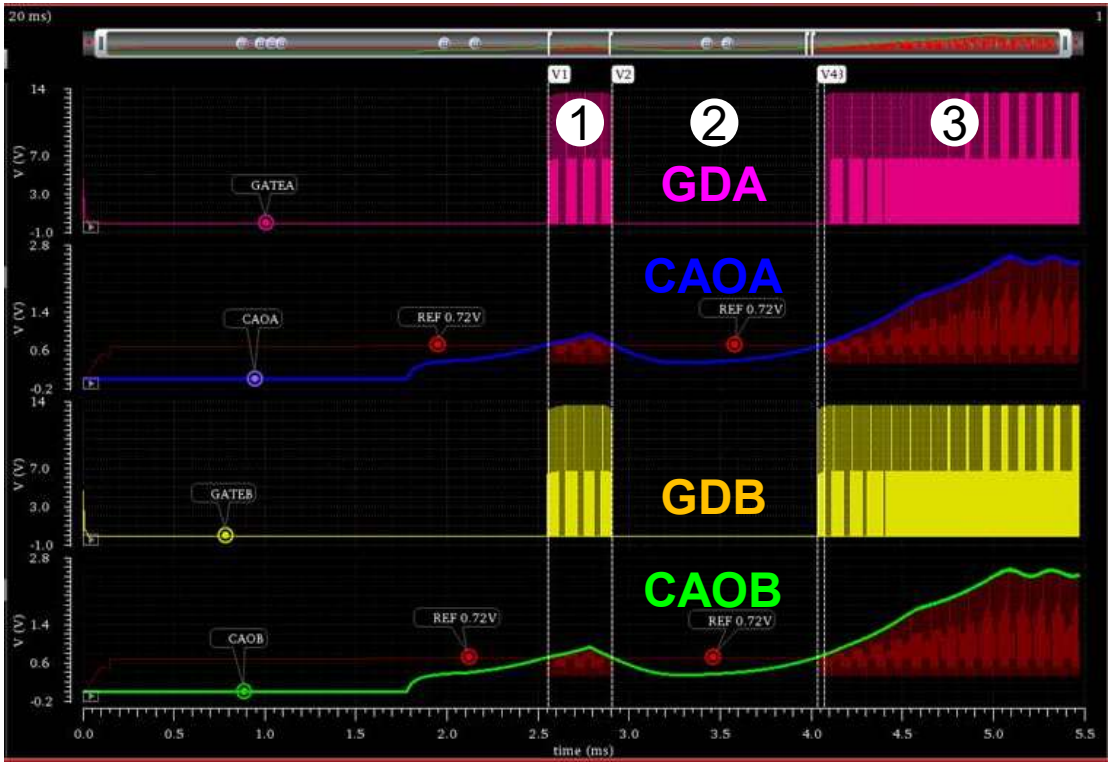
CAOA/B





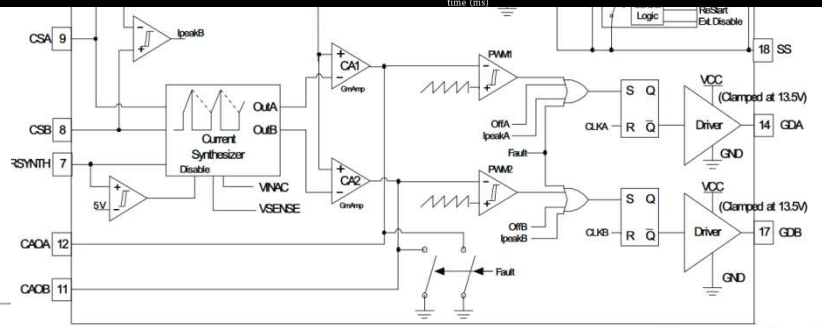
Root Cause Analysis - simulation

- Simulation confirmed the analysis:
  1. A first packet of switching cycle is observed
  2. Then there is no switching for few ms
  3. The switching starts again later
  - The first packet of switching cycles starts when CAOA and CAOB rise above 0.7V
  - Around the middle of this packet of switching cycles CAOA and CAOB start to fall
  - When CAOA and CAOB goes below 0.7V the switching stops
  - The switching restarts when CAOA and CAOB go again above 0.7V



Why do CAOA/B change Slope

- Simulation shows that a negative shift on the positive input (IN+) of the current error amplifier occurs, on both phases, after some switching cycles
  - When IN+ is above IN- , CAO rises
  - When the negative shift occurs, IN+ drops below IN- and CAO changes slope starting to decrease
  - IN+ has an increasing trend that will take some time to compensate for the negative step and move IN+ again above IN-, to make CAO rise again
  - This negative shift occurs in IN+ signal due to a change in bias current when the Current Synthesizer circuit is enabled. This is part of the normal startup process.



Root Cause Analysis – conclusion

- At power-up the switching is determined by the CAOA/B level:
  - V(CAOA/B) > 0.7V switching allowed
  - V(CAOA/B) < 0.7V switching inhibited
- CAOA/B initially rises but after the first switching cycles it starts to fall
- The change in the slope is due to a shift on one input of the current error amplifier, that will cause the plus input to become lower than the minus input
- The negative shift occurs when the Current Synthesizer circuit starts to work
- The behavior is in line with the IC design implementation