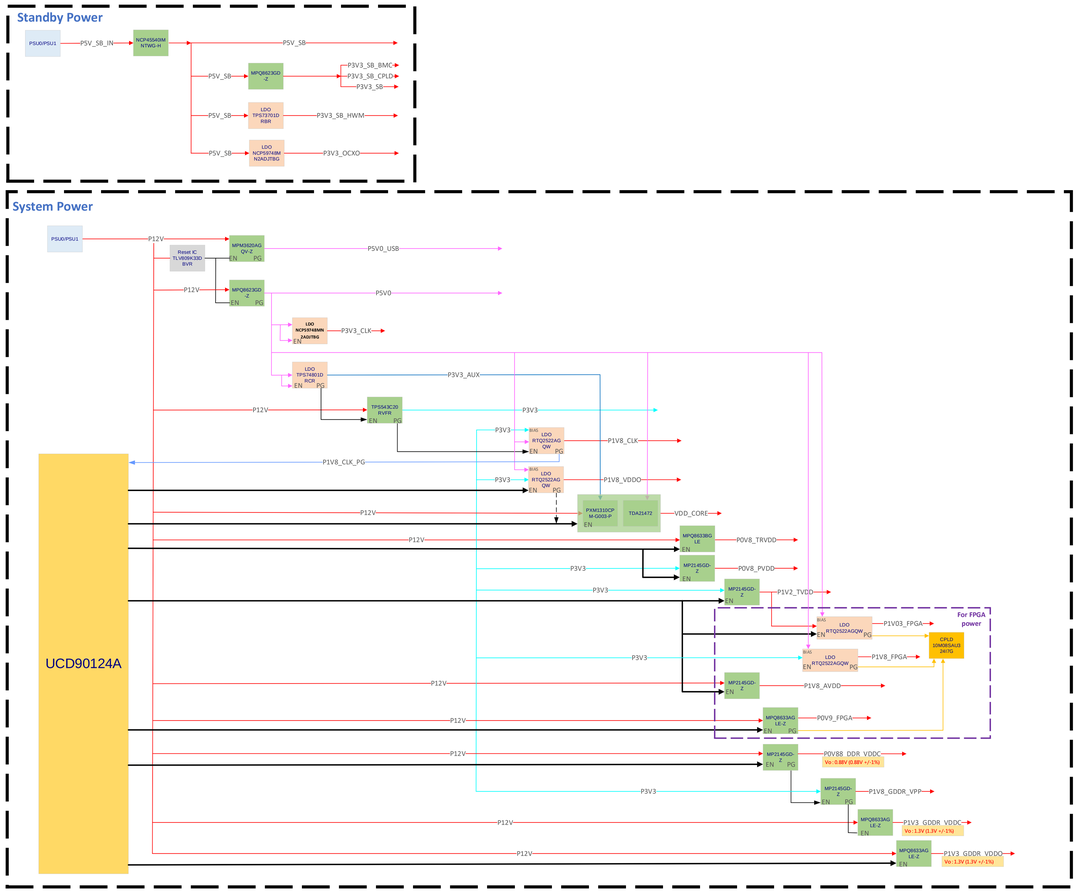
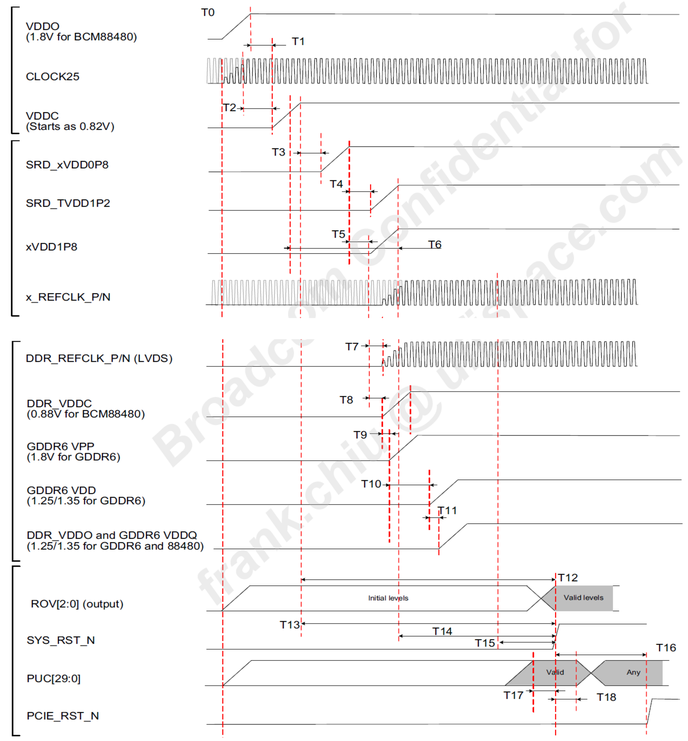




NOTE: The power-up sequence can be easily met for voltage ramp-ups as slow as 1V/3 ms.

Table 12: Power-Up Sequence Timing

T Number	Description	Min.	Max.	Unit
T0	Initial condition: ■ All voltage rails are below 100 mV. ■ SCAN_MODE, TEST[4:0], and JTAG_TCE are 0. ■ SYS_RST_N and PCIE_RST_N are 0.			
Vramp	Voltage ramp-up time for 1V. The rise time of 1V should be longer than 50 µs and shorter than 5 ms.	50	5000	µs
T1	(VDDO > 95%) to (VDDC start).	0	5	ms
T2	(CLOCK25 Valid) to (VDDC start).	0	—	ms
T3	(VDDC > 95%) to (SRD_xVDD0P8 start).	0	3	ms
T4[a,b]	(SRD_xVDD0P8 > 95%) to (SRD_TVDD1P2 start).	0	3	ms
T5[a,c]	(SRD_xVDD0P8 > 95%) to (xVDD1P8 start).	0	3	ms
T6	(VDDC = 0.55V) to (xVDD1P8 > 95%).	—	10	ms
T7	(xVDD1P8 start) to (DDR_REFCLK_P/N start).	0	—	ms
T8	(xVDD1P8 start) to (DDR_VDDC start).	0	—	ms
T9	(DDR_VDDC start) to (GDDR6 VPP 1.8V start).	0	—	ms
T10[d]	(GDDR6 VPP 1.8V start) to (GDDR6 VDD start).	0	10	ms
T11[e]	(GDDR6 VDD start) to (DDR_VDDO and GDDR6 VDDQ start).	0	—	ms
T12	(VDDC > 95%) to ROV valid.	—	60	ms
T13	(VDDC > 95%) to SYS_RST_N de-assertion (rising from 0 to 1).	60	—	ms
T14[f]	(Last power to reach 95%) to SYS_RST_N de-assertion (rising from 0 to 1).	10	—	ms
T15	x_REFCLK_P/N valid to SYS_RST_N de-assertion.	10	—	ms
T16	SYS_RST_N =1 to PCIE_RST_N de-assertion (rising from 0 to 1).	100	—	ms
T17	PUC set-up time to SYS_RST_N de-assertion.	160	—	ns
T18	PUC hold time after SYS_RST_N de-assertion.	160	—	ns

a. There is no required timing between xVDD1P8 and SRD_TVDD1P2.
b. SRD_TVDD1P2 should *not* exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).
c. xVDD1P8 should *not* exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 – SRD_xVDD0P8 < 1.2V).
d. VPP must be equal to or greater than VDD and VDDQ at all times the device is powered up.
e. VDD and VDDQ must be within 300 mV of each other at all times the device is powered up.
f. The last power rail out of xVDD1P8, SRD_TVDD1P2, or DDR_VDDC.

SRD_xVDD0P8 represents the following rails:
- PCI_PVDD0P8
- PCI_TRVDD0P8
- NIF50_[1:0]_PLL[1:0]_PVDD0P8, NIF50_[1:0]_RVDD0P8, and NIF50_[1:0]_TVDD0P8
- NIF25_[10:2]_PVDD0P8 and NIF25_RTVDD0P8

SRD_TVDD1P2 represents the following rails:
- NIF50_[1:0]_TVDD1P2 and NIF25_TVDD1P2

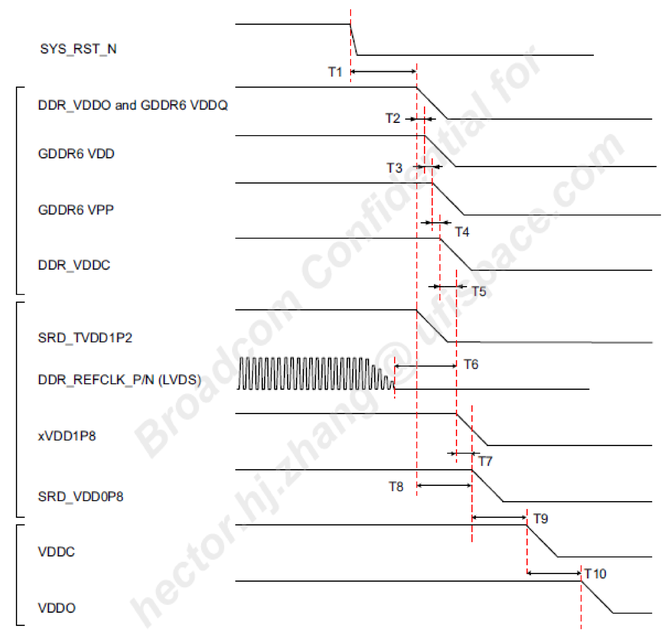
xVDD1P8 represents the following rails:
- TS_PLL_VDD1P8
- DDR[1:0]_AVDD1P8 and DDR#_V_ANALOG
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- NIF_[4:0]_PVDD1P8
- FLEXE_PLL_AVDD1P8

x_REFCLK_P/N represents the differential reference clocks:
- PCIE_REFCLK_P/N
- TS_PLL_REFCLK_P/N
- C_PLL_REFCLK_P/N
- U_PLL_REFCLK_P/N
- NIF_PLL_REFCLK_P/N
- NIF_[3:0]_REFCLK_P/N
- FLEXE_REFCLK

5.5.2 Power-Down Sequence

The following figure illustrates the power-down sequence.

Figure 10: Power-Down Sequence



SRD_xVDD0P8 represent the following rails:
- PCI_PVDD0P8 and PCI_TRVDD0P8
- NIF50_[1:0]_PLL[1:0]_PVDD0P8, NIF50_[1:0]_RVDD0P8, and NIF50_[1:0]_TVDD0P8
- NIF25_[10:2]_PVDD0P8 and NIF25_RTVDD0P8

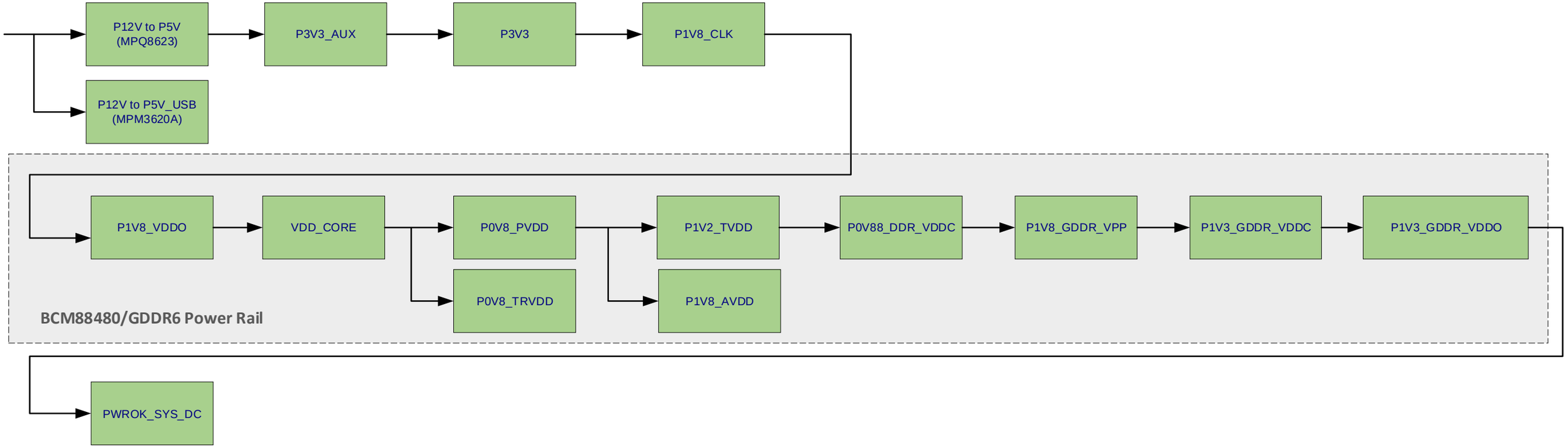
SRD_TVDD1P2 represents the following rails:
- NIF50_[1:0]_TVDD1P2 and NIF25_TVDD1P2

xVDD1P8 represents the following rails:
- TS_PLL_VDD1P8
- SYNCE_PLL_AVDD1P8
- DDR[1:0]_AVDD1P8
- and DDR#_V_ANALOG
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- NIF_[4:0]_PVDD1P8
- FLEXE_PLL_AVDD1P8

Table 13: Power-Down Sequence Timing

T Number	Description[a]	Min.	Max.	Unit
T1	SYS_RST_N asserted to first power drop start. (DDR_VDDO and GDDR6_VDDQ, or SRD_TVDD1P2). This period is optional and is needed to minimize the number of packets with errors during reset.	5	—	µs
T2[b]	DDR_VDDO (+ GDDR6 VDDQ) drop start to GDDR6_VDD drop start.	0	—	ms
T3[c]	GDDR6_VDD drop start to GDDR6_VPP drop start.	0	—	ms
T4	GDDR6_VPP drop start DDR_VDDC drop start.	0	—	ms
T5	DDR_VDDC drop start to xVDD1P8 drop start.	0	—	ms
T6	DDR_REFCLK_P/N drop start to xVDD1P8 drop start.	0	—	ms
T7[d,e]	xVDD1P8 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T8[d,f]	SRD_TVDD1P2 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T9	SRD_xVDD0P8 drop start to VDDC drop start.	0	—	ms
T10	VDDC drop start to VDDO drop start.	0	—	ms

a. Power rails can start drop without delay; however, the requirements in the following footnotes must be met.
b. VDD and VDDQ must be within 300 mV of each other at all times the device is powered up.
c. VPP must be equal to or greater than VDD and VDDQ at all times the device is powered up.
d. Timing is not required between xVDD1P8 and SRD_TVDD1P2.
e. xVDD1P8 should not exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 – SRD_xVDD0P8 < 1.2V).
f. SRD_TVDD1P2 should not exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).


P12V to P5V
(MPQ8623)
P3V3_AUX
P3V3
P1V8_CLK
P12V to P5V_USB
(MPM3620A)
P1V8_VDDO
VDD_CORE
P0V8_PVDD
P1V2_TVDD
P0V88_DDR_VDDC
P1V8_GDDR_VPP
P1V3_GDDR_VDDC
P1V3_GDDR_VDDO
P0V8_TRVDD
P1V8_AVDD
BCM88480/GDDR6 Power Rail
PWROK_SYS_DC