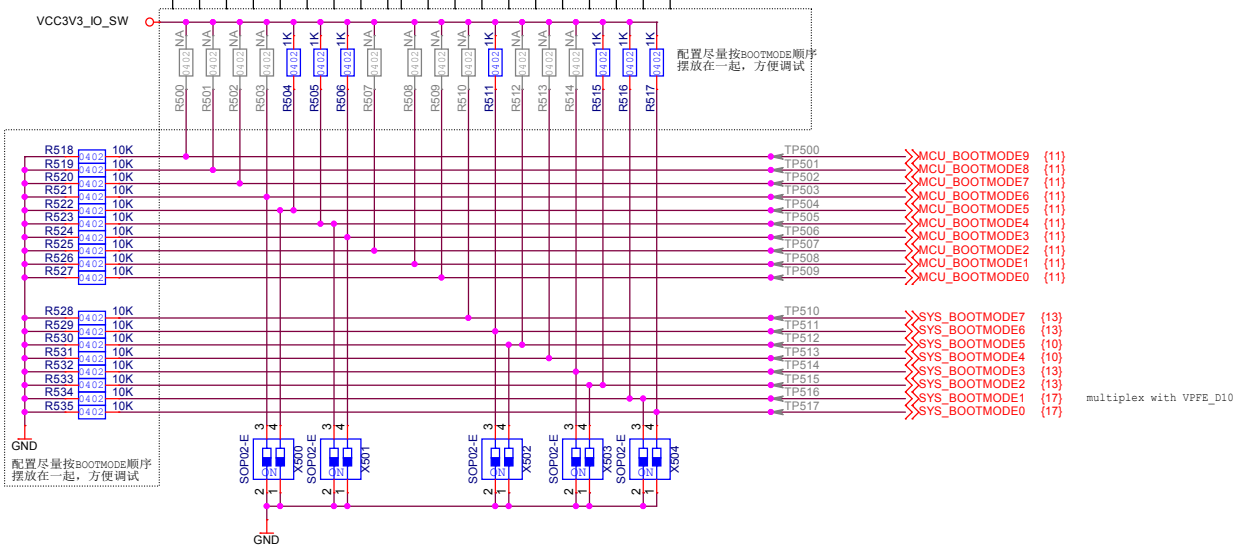
	MCU_BOOTMODE9	MCU_BOOTMODE8	MCU_BOOTMODE7	MCU_BOOTMODE6	MCU_BOOTMODE5	MCU_BOOTMODE4	MCU_BOOTMODE3	MCU_BOOTMODE2	MCU_BOOTMODE1	MCU_BOOTMODE0	SYS_BOOTMODE7	SYS_BOOTMODE6	SYS_BOOTMODE5	SYS_BOOTMODE4	SYS_BOOTMODE3	SYS_BOOTMODE2	SYS_BOOTMODE1	SYS_BOOTMODE0
UART	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0
USB	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
EMMC	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
OSPI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0
DEBUG	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	1	1	1
	NP	NP	NP	NP				NP	NP	NP	NP		NP	NP	NP			



BOOT PIN	VDDIO	MUX NETWORK	Description			UART	USB	EMMC	OSPI	DEBUG
MCU_BOOTMODE9			POST Config Pins:							
MCU_BOOTMODE8			MCU[9:8]=00-DMSC LBIST followed by MCU LBIST followed by PBIST MCU[9:8]=01-DMSC LBIST and MCU LBIST in parallel followed by PBIST MCU[9:8]=10-DMSC LBIST MCU[9:8]=11-POST bypass			0	0	0	0	0
MCU_BOOTMODE7			Reserved Set to 0			0	0	0	0	0
MCU_BOOTMODE6			MCU Only Pin: MCU[6]=0-Normal boot mode MCU[6]=1-MCU Only boot mode			0	0	0	0	0
MCU_BOOTMODE5			Primary Boot Mode A Pins:	Primary Boot	Backup Boot	1	0	0	0	1
MCU_BOOTMODE4			SYS[0]MCU[5:3]=0001	OSPI	UART	1	1	0	0	1
MCU_BOOTMODE3			SYS[0]MCU[5:3]=0010	QSPI	UART	1	0	1	1	1
			SYS[0]MCU[5:3]=0011	SPI	UART					
			SYS[0]MCU[5:3]=0100	RGMII	I2C					
			SYS[0]MCU[5:3]=0101	RMII	I2C					
			SYS[0]MCU[5:3]=0110	I2C	UART					
			SYS[0]MCU[5:3]=0111	UART	I2C					
			SYS[0]MCU[5:3]=1000	MMC/SD						
			SYS[0]MCU[5:3]=1001	EMMC						
			SYS[0]MCU[5:3]=1010	USB						
			SYS[0]MCU[5:3]=1100	GPMC NOR						
			SYS[0]MCU[5:3]=1101	PCIe						
MCU_BOOTMODE2			PLL Config Pins: Ref Clock(MHz)			0	0	0	0	0
MCU_BOOTMODE1			MCU[2:0]=000 19.2			0	0	0	0	0
MCU_BOOTMODE0			MCU[2:0]=001 20 MCU[2:0]=010 24 MCU[2:0]=011 25 MCU[2:0]=100 26 MCU[2:0]=101 27(not supported USB DFU boot) MCU[2:0]=110 Reserved MCU[2:0]=111 No PLL setup			0	0	0	0	0
SYS_BOOTMODE7			Backup Boot Mode Config			0	0	0	0	0
SYS_BOOTMODE6			Primary Boot Mode Configuration			0	0	0	1	1
SYS_BOOTMODE5						0	0	0	0	0
SYS_BOOTMODE4						0	0	0	0	0
SYS_BOOTMODE3			Backup Boot Mode Pins:	Backup Boot		0	0	0	0	0
SYS_BOOTMODE2			SYS[3:1]=000	NONE		1	1	1	1	1
SYS_BOOTMODE1			SYS[3:1]=001	USB		1	1	1	1	1
			SYS[3:1]=010	Reserved						
			SYS[3:1]=011	UART						
			SYS[3:1]=100	Ethernet						
			SYS[3:1]=101	MMC/SD						
			SYS[3:1]=110	SPI						
			SYS[3:1]=111	I2C						
SYS_BOOTMODE0			Primary Boot Mode B Pin			0	1	1	0	1

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Design NO.	Rev	Sheet Name
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Custom	ZEHUI.LI	mingyu.gong	jianmin.yang

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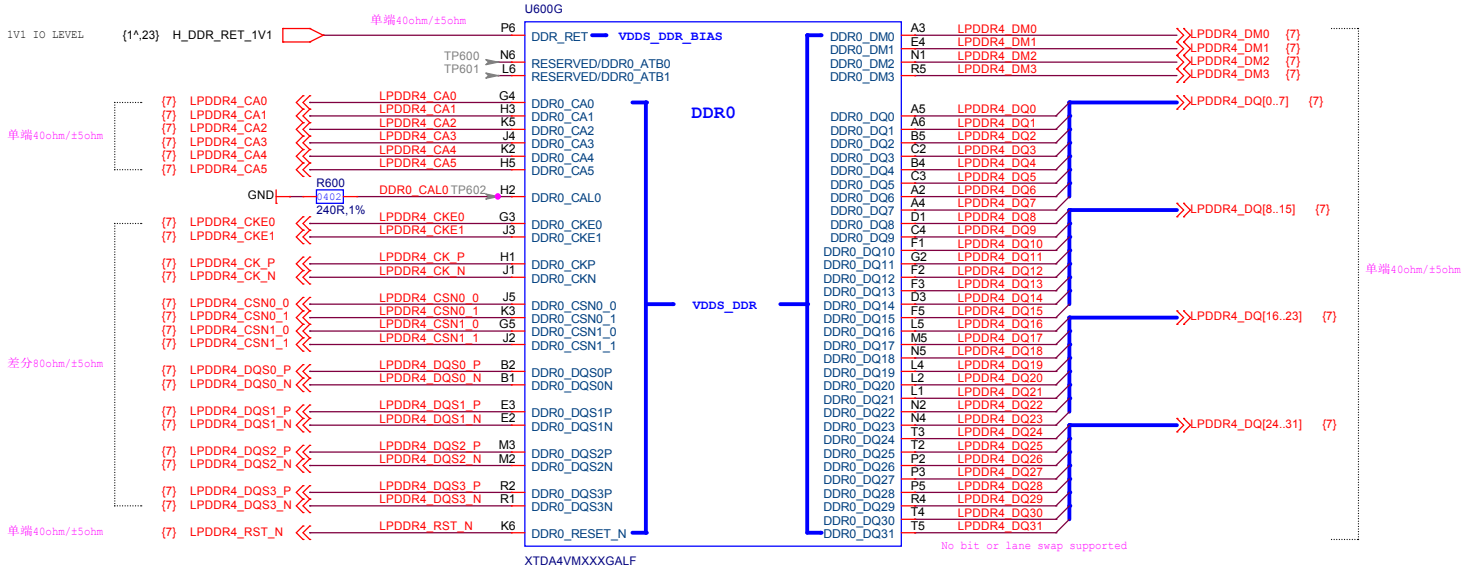


```
LPDDR4 layout routing spec:
Impedance control:
1.point-to-point diff impedance 80ohm/±5ohm
2.point-to-point single-ended impedance 40ohm/±5ohm

ADDR_CTRL control:
1.CK max trace length < 250ps or 1375mils (Vp=5.5mil/ps,Er=4.6)
2.1.ADDR_CTRL max trace length < 250ps or 1375mil (Vp=5.5mil/ps,Er=4.6)
3.skew within CK diff pair < 0.25ps or 1.375mils (Vp=5.5mil/ps,Er=4.6)
4.skew within ADDR_CTRL net group < 3ps or 16.5mils (Vp=5.5mil/ps,Er=4.6)
5.skew between each T-branch signal pair < 0.1ps or 0.55mils (Vp=5.5mil/ps,Er=4.6)
6.skew between ADDR_CTRL net group refer to CK < 3ps or 16.5mils (Vp=5.5mil/ps,Er=4.6)
7.no stubs allowed on traces
8.max vias on each trace < 4
9.via count difference < 0
10.via stub length typical is 20 mils
11.Center-to-center CK to other LPDDR4 trace spacing > 4W
12.Center-to-center ADDR_CTRL to other LPDDR4 trace spacing >3W
13.Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing > 3W
14.CK spacing to other net > 4W

DATA group control:
1.DQSx max trace length < 250ps or 1375mils (Vp=5.5mil/ps,Er=4.6)
2.DATA max trace length < 250ps or 1375mil (Vp=5.5mil/ps,Er=4.6)
3.DQSx pair length must be less than CK pair (include trace length to die in the package)
4.skew within DQSx diff pair < 0.1ps or 0.55mils (Vp=5.5mil/ps,Er=4.6)
5.skew between DATA net group refer to DQSx < 0.5ps or 2.75mils (Vp=5.5mil/ps,Er=4.6)
6.DQSx pair length must be less than DQ/DM (include trace length to die in the package)
7.no stubs allowed on traces
8.max vias on each trace < 2
9.via count difference < 0
10.via stub length typical is 40 mils
11.center-to-center spacing (between clock net class) > 4W
12.center-to-center spacing (between signal net class) > 4W
13.center-to-center spacing (within signal net class) > 3W
```

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Design NO. 825501036_ADAS_SCH		Rev V1.1	Sheet Name EMIF1
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
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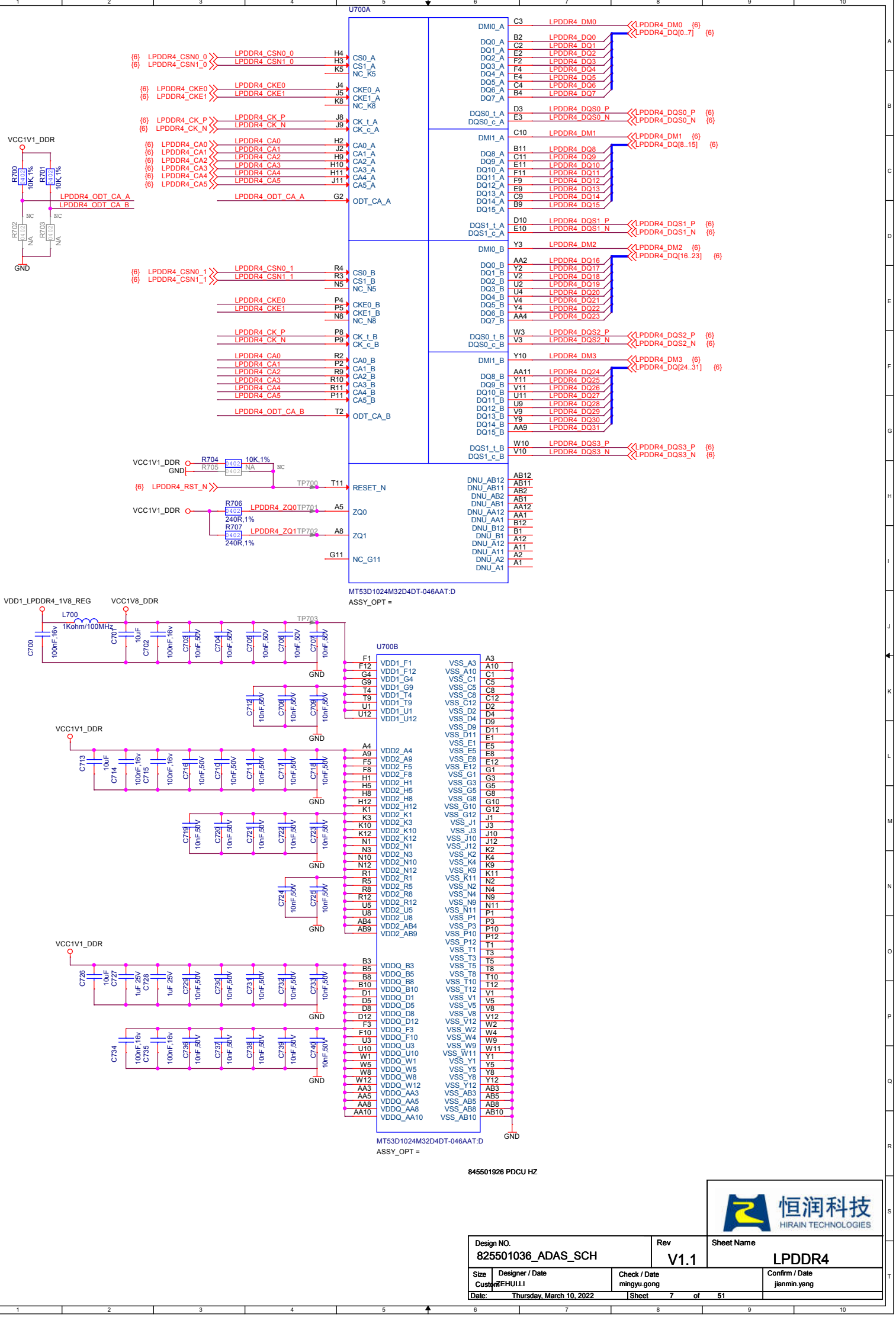
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VCC1V1_DDR
R700 0402 10K,1%
R701 0402 10K,1%
R702 0402 NA
R703 0402 NA
NC
GND
LPDDR4_ODT_CA_A
LPDDR4_ODT_CA_B
{6} LPDDR4_CSN0_0
{6} LPDDR4_CSN1_0
LPDDR4_CSN0_0
LPDDR4_CSN1_0
H4 H3 K5
CS0_A CS1_A NC_K5
{6} LPDDR4_CKE0
{6} LPDDR4_CKE1
LPDDR4_CKE0
LPDDR4_CKE1
J4 J5 K8
CKE0_A CKE1_A NC_K8
{6} LPDDR4_CK_P
{6} LPDDR4_CK_N
LPDDR4_CK_P
LPDDR4_CK_N
J8 J9
CK_t_A CK_c_A
{6} LPDDR4_CA0
{6} LPDDR4_CA1
{6} LPDDR4_CA2
{6} LPDDR4_CA3
{6} LPDDR4_CA4
{6} LPDDR4_CA5
H2 J2 H9 H10 H11 J11
CA0_A CA1_A CA2_A CA3_A CA4_A CA5_A
LPDDR4_ODT_CA_A
G2
ODT_CA_A
DMI0_A C3 LPDDR4_DM0
DQ0_A B2 LPDDR4_DQ0
DQ1_A C2 LPDDR4_DQ1
DQ2_A E2 LPDDR4_DQ2
DQ3_A F2 LPDDR4_DQ3
DQ4_A F4 LPDDR4_DQ4
DQ5_A E4 LPDDR4_DQ5
DQ6_A C4 LPDDR4_DQ6
DQ7_A B4 LPDDR4_DQ7
DQS0_t_A D3 LPDDR4_DQS0_P
DQS0_c_A E3 LPDDR4_DQS0_N
DMI1_A C10 LPDDR4_DM1
DQ8_A B11 LPDDR4_DQ8
DQ9_A C11 LPDDR4_DQ9
DQ10_A E11 LPDDR4_DQ10
DQ11_A F11 LPDDR4_DQ11
DQ12_A F9 LPDDR4_DQ12
DQ13_A E9 LPDDR4_DQ13
DQ14_A C9 LPDDR4_DQ14
DQ15_A B9 LPDDR4_DQ15
DQS1_t_A D10 LPDDR4_DQS1_P
DQS1_c_A E10 LPDDR4_DQS1_N
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LPDDR4_DQS0_N {6}
LPDDR4_DM0 {6}
LPDDR4_DQ[0..7] {6}
LPDDR4_DM1 {6}
LPDDR4_DQ[8..15] {6}
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{6} LPDDR4_CSN1_1
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LPDDR4_CSN1_1
R4 R3 N5
CS0_B CS1_B NC_N5
LPDDR4_CKE0
LPDDR4_CKE1
P4 P5 N8
CKE0_B CKE1_B NC_N8
LPDDR4_CK_P
LPDDR4_CK_N
P8 P9
CK_t_B CK_c_B
LPDDR4_CA0
LPDDR4_CA1
LPDDR4_CA2
LPDDR4_CA3
LPDDR4_CA4
LPDDR4_CA5
R2 P2 R9 R10 R11 P11
CA0_B CA1_B CA2_B CA3_B CA4_B CA5_B
LPDDR4_ODT_CA_B
T2
ODT_CA_B
DMI0_B Y3 LPDDR4_DM2
DQ0_B AA2 LPDDR4_DQ16
DQ1_B Y2 LPDDR4_DQ17
DQ2_B V2 LPDDR4_DQ18
DQ3_B U2 LPDDR4_DQ19
DQ4_B U4 LPDDR4_DQ20
DQ5_B V4 LPDDR4_DQ21
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DQ7_B AA4 LPDDR4_DQ23
DQS0_t_B W3 LPDDR4_DQS2_P
DQS0_c_B V3 LPDDR4_DQS2_N
DMI1_B Y10 LPDDR4_DM3
DQ8_B AA11 LPDDR4_DQ24
DQ9_B Y11 LPDDR4_DQ25
DQ10_B V11 LPDDR4_DQ26
DQ11_B U11 LPDDR4_DQ27
DQ12_B U9 LPDDR4_DQ28
DQ13_B V9 LPDDR4_DQ29
DQ14_B Y9 LPDDR4_DQ30
DQ15_B AA9 LPDDR4_DQ31
DQS1_t_B W10 LPDDR4_DQS3_P
DQS1_c_B V10 LPDDR4_DQS3_N
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LPDDR4_DQS2_N {6}
LPDDR4_DM2 {6}
LPDDR4_DQ[16..23] {6}
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LPDDR4_DQS3_N {6}
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GND
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R705 0402 NA
NC
{6} LPDDR4_RST_N
TP700
T11
RESET_N
VCC1V1_DDR
R706 0402 240R,1%
R707 0402 240R,1%
LPDDR4_ZQ0
LPDDR4_ZQ1
TP701
TP702
A5
A8
ZQ0
ZQ1
G11
NC_G11
DNU_AB12 AB12
DNU_AB11 AB11
DNU_AB2 AB2
DNU_AB1 AB1
DNU_AA12 AA12
DNU_AA1 AA1
DNU_B12 B12
DNU_B1 B1
DNU_A12 A12
DNU_A11 A11
DNU_A2 A2
DNU_A1 A1
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VCC1V8_DDR
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C700 100nF,16v
C701 10uF
C702 100nF,16v
C703 10nF,50v
C704 10nF,50v
C705 10nF,50v
C706 10nF,50v
C707 10nF,50v
TP703
GND
U700B
F1 F12 G4 G9 T4 T9 U1 U12
VDD1_F1 VDD1_F12 VDD1_G4 VDD1_G9 VDD1_T4 VDD1_T9 VDD1_U1 VDD1_U12
C712 10nF,50v
C708 10nF,50v
C709 10nF,50v
A4 A9 F5 F8 H1 H5 H8 H12 K1 K3 K10 K12 N1 N3 N10 N12 R1 R5 R8 R12 U5 U8 AB4 AB9
VDD2_A4 VDD2_A9 VDD2_F5 VDD2_F8 VDD2_H1 VDD2_H5 VDD2_H8 VDD2_H12 VDD2_K1 VDD2_K3 VDD2_K10 VDD2_K12 VDD2_N1 VDD2_N3 VDD2_N10 VDD2_N12 VDD2_R1 VDD2_R5 VDD2_R8 VDD2_R12 VDD2_U5 VDD2_U8 VDD2_AB4 VDD2_AB9
C713 10uF
C714 10nF,16v
C715 100nF,16v
C716 10nF,50v
C710 10nF,50v
C711 10nF,50v
C717 10nF,50v
C718 10nF,50v
C719 10nF,50v
C720 10nF,50v
C721 10nF,50v
C722 10nF,50v
C723 10nF,50v
C724 10nF,50v
C725 10nF,50v
B3 B5 B8 B10 D1 D5 D8 D12 F3 F10 U3 U10 W1 W5 W8 W12 AA3 AA5 AA8 AA10
VDDQ_B3 VDDQ_B5 VDDQ_B8 VDDQ_B10 VDDQ_D1 VDDQ_D5 VDDQ_D8 VDDQ_D12 VDDQ_F3 VDDQ_F10 VDDQ_U3 VDDQ_U10 VDDQ_W1 VDDQ_W5 VDDQ_W8 VDDQ_W12 VDDQ_AA3 VDDQ_AA5 VDDQ_AA8 VDDQ_AA10
C726 10uF
C727 1uF,25V
C728 1uF,25V
C729 10nF,50v
C730 10nF,50v
C731 10nF,50v
C732 10nF,50v
C733 10nF,50v
C734 100nF,16v
C735 100nF,16v
C736 10nF,50v
C737 10nF,50v
C738 10nF,50v
C739 10nF,50v
C740 10nF,50v
A3 A10 C1 C5 C8 C12 D2 D4 D9 D11 E1 E5 E8 E12 G1 G3 G5 G8 G10 G12 J1 J3 J10 J12 K2 K4 K9 K11 N2 N4 N9 N11 P1 P3 P10 P12 T1 T3 T5 T8 T10 T12 V1 V5 V6 V12 W2 W4 W9 W11 Y1 Y5 Y8 Y12 AB3 AB5 AB8 AB10
VSS_A3 VSS_A10 VSS_C1 VSS_C5 VSS_C8 VSS_C12 VSS_D2 VSS_D4 VSS_D9 VSS_D11 VSS_E1 VSS_E5 VSS_E8 VSS_E12 VSS_G1 VSS_G3 VSS_G5 VSS_G8 VSS_G10 VSS_G12 VSS_J1 VSS_J3 VSS_J10 VSS_J12 VSS_K2 VSS_K4 VSS_K9 VSS_K11 VSS_N2 VSS_N4 VSS_N9 VSS_N11 VSS_P1 VSS_P3 VSS_P10 VSS_P12 VSS_T1 VSS_T3 VSS_T5 VSS_T8 VSS_T10 VSS_T12 VSS_V1 VSS_V5 VSS_V8 VSS_V12 VSS_W2 VSS_W4 VSS_W9 VSS_W11 VSS_Y1 VSS_Y5 VSS_Y8 VSS_Y12 VSS_AB3 VSS_AB5 VSS_AB8 VSS_AB10
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845501926 PDCU HZ
恒润科技
HIRAIN TECHNOLOGIES
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Rev V1.1
Sheet Name LPDDR4
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Designer / Date ZEHUI.LI
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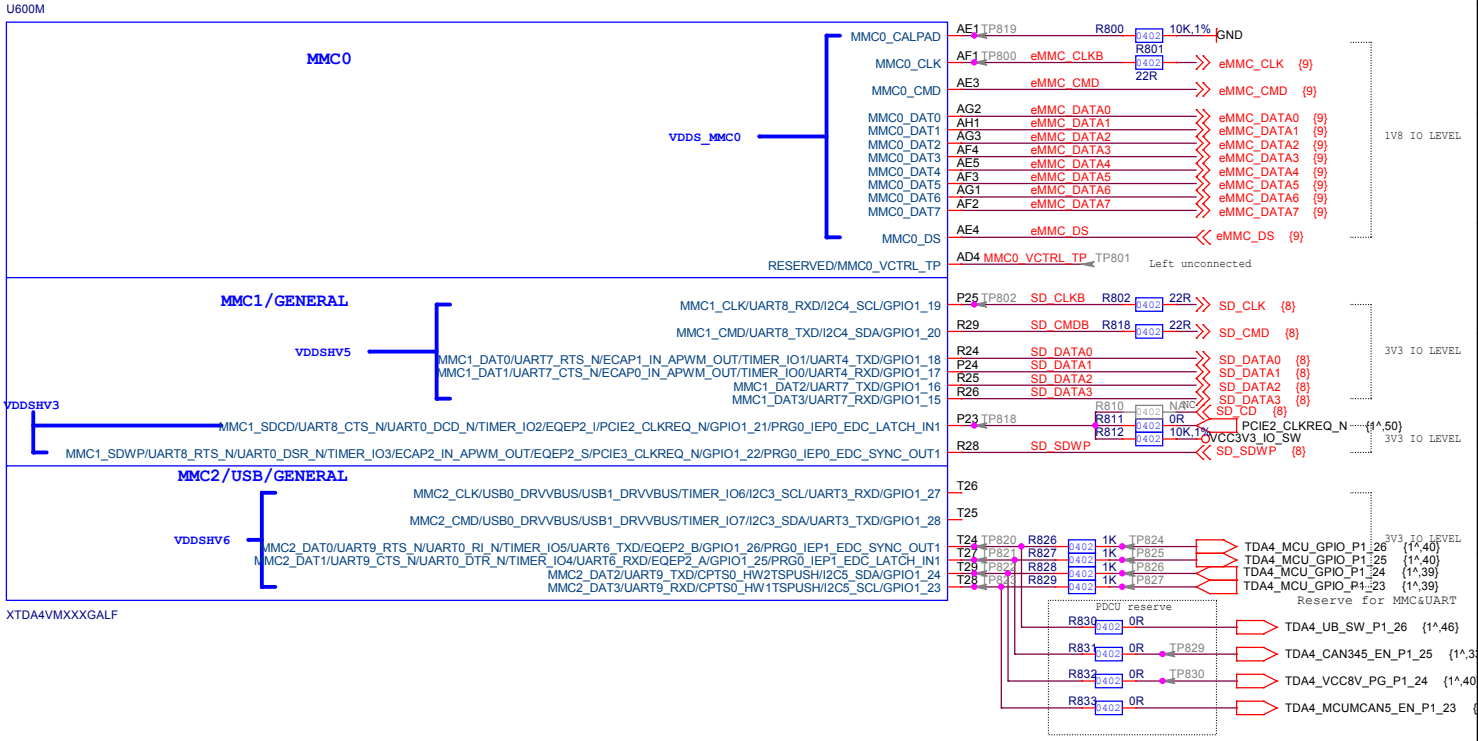

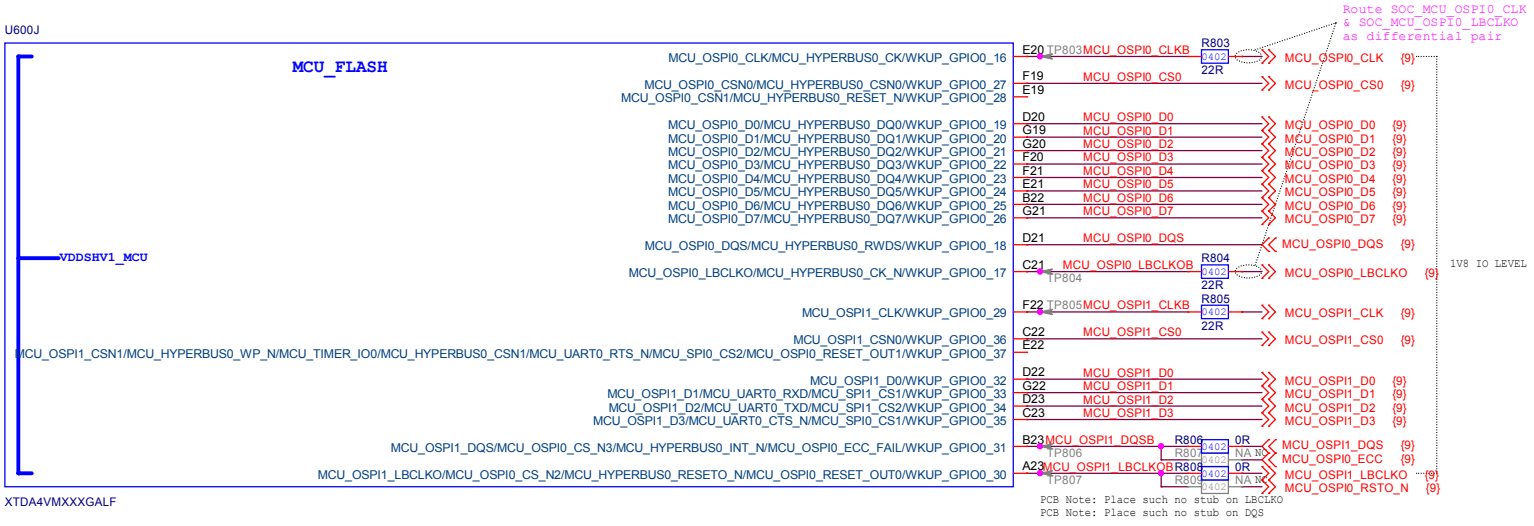

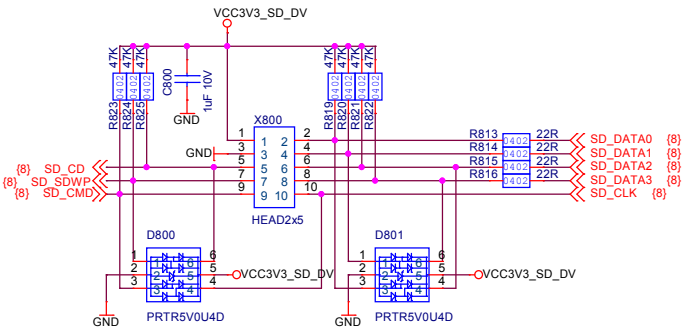

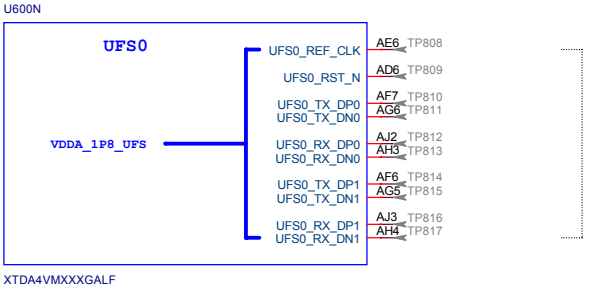

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Design NO.	Rev	Sheet Name
825501036_ADAS_SCH	V1.1	MMC_QSPI_SPI_UFS

Size	Designer / Date	Check / Date	Confirm / Date
Custom	ZEHUI.LI	mingyu.gong	jianmin.yang

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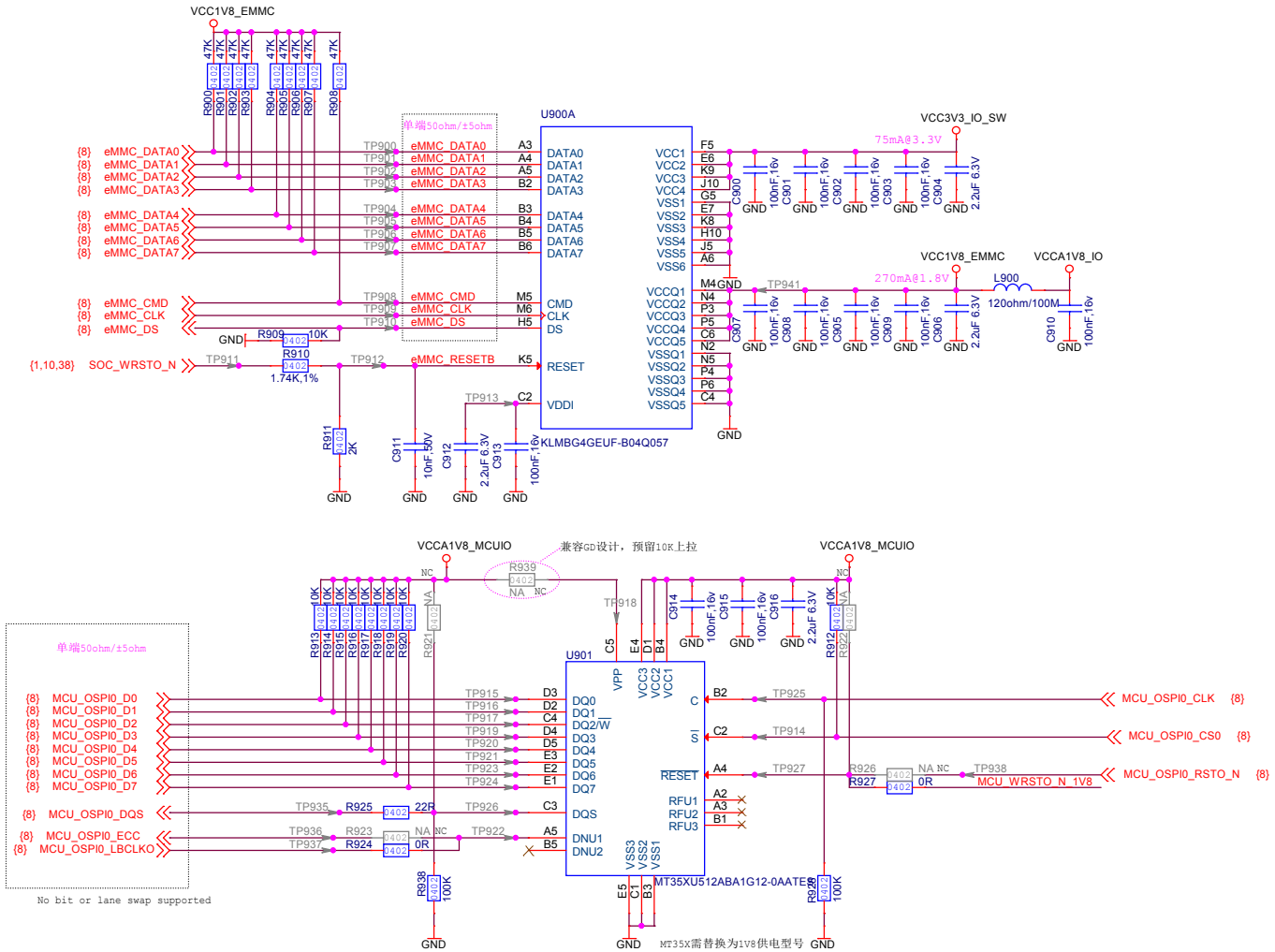

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Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
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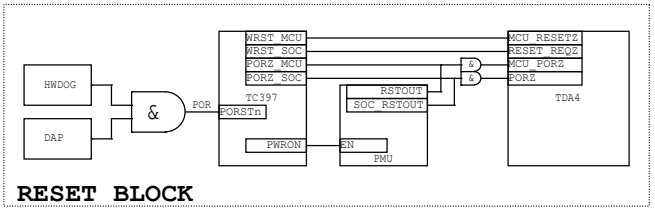
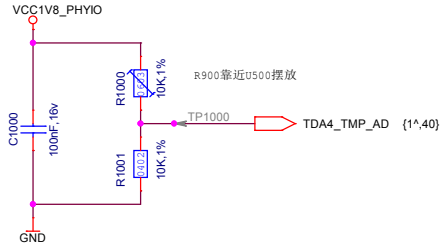


RESET BLOCK



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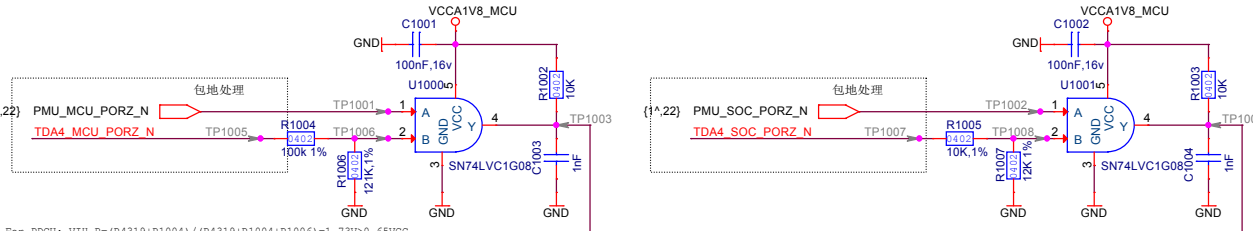
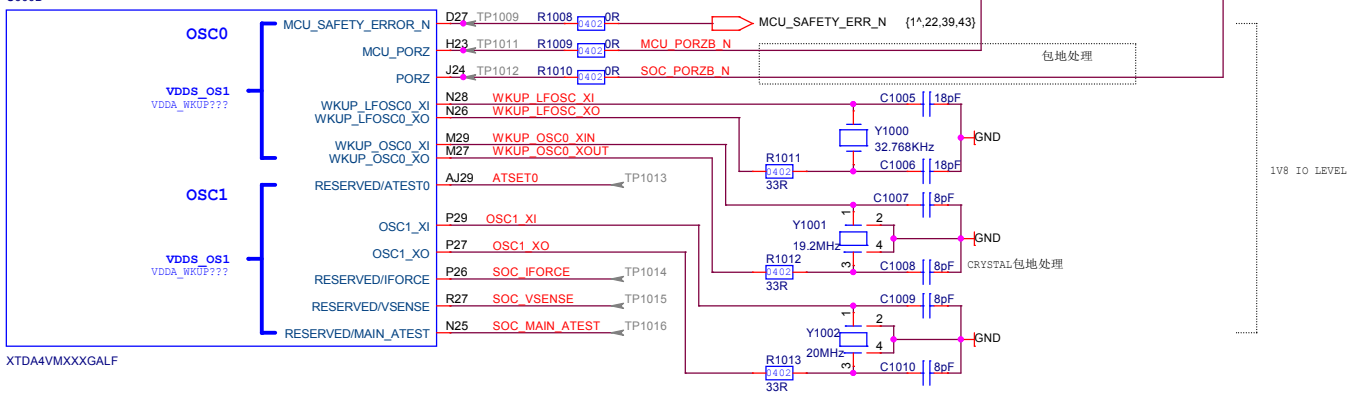


For PDCU: VIH_B=(R4319+R1004)/(R4319+R1004+R1006)=1.73V>0.65VCC

U600D



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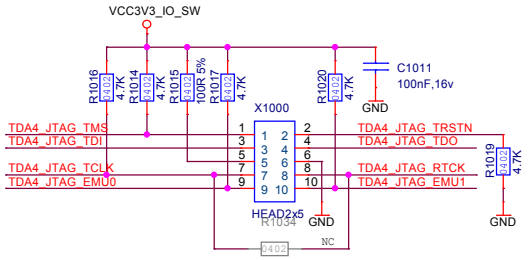

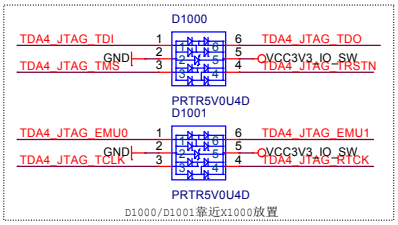

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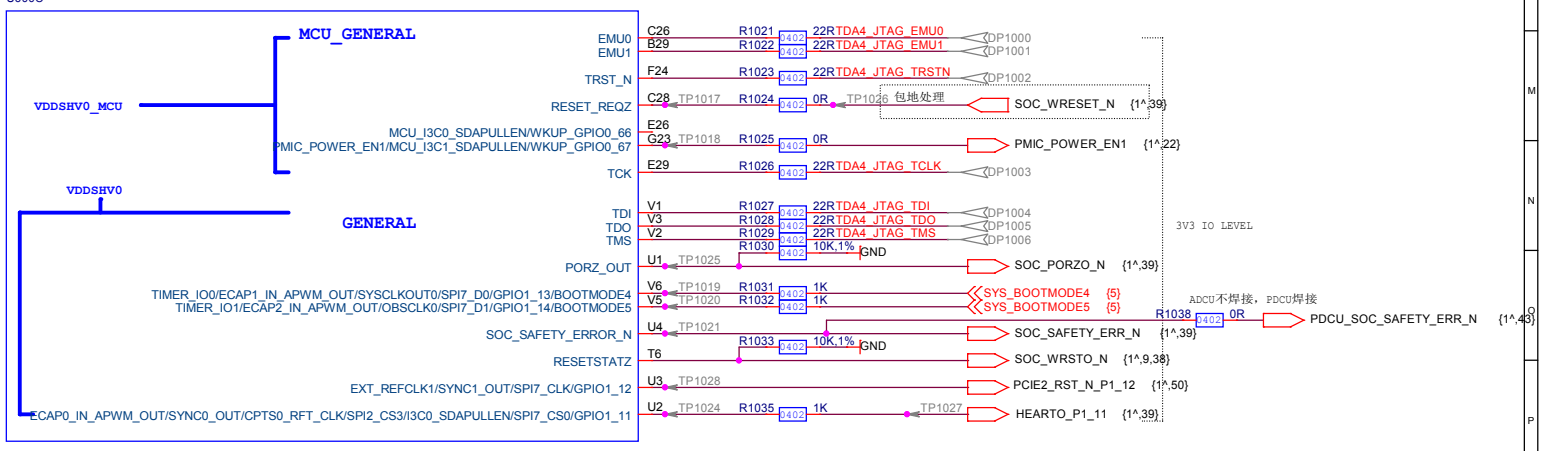

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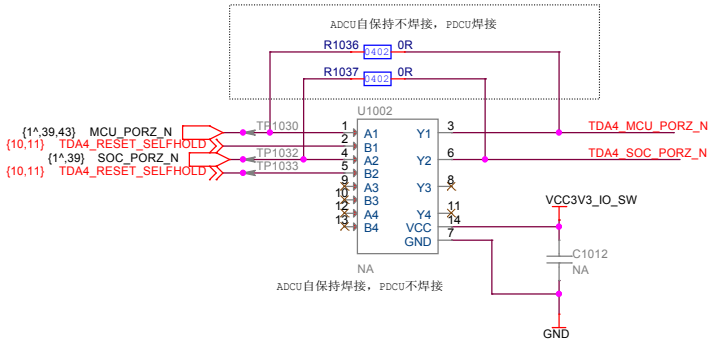

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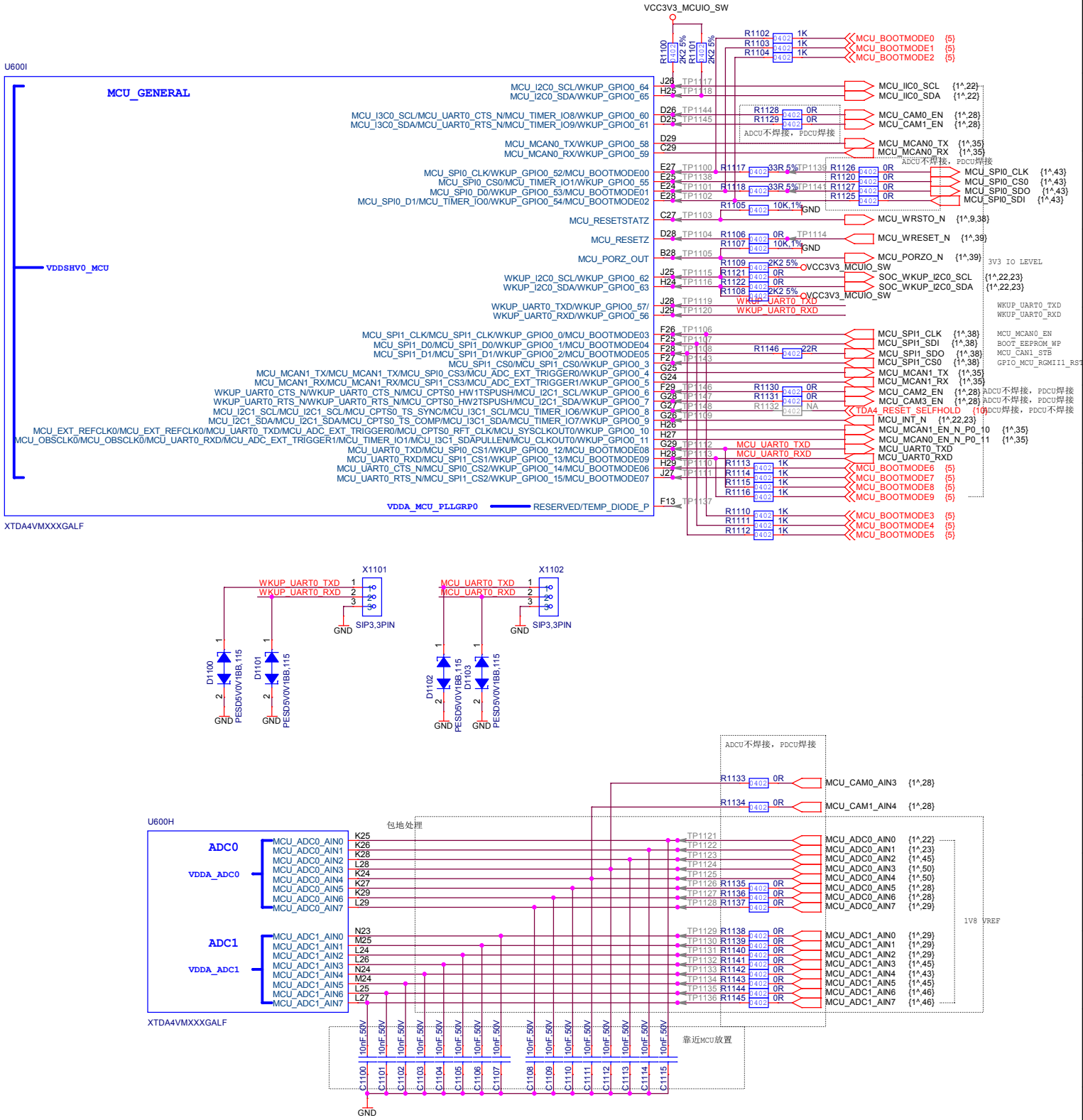
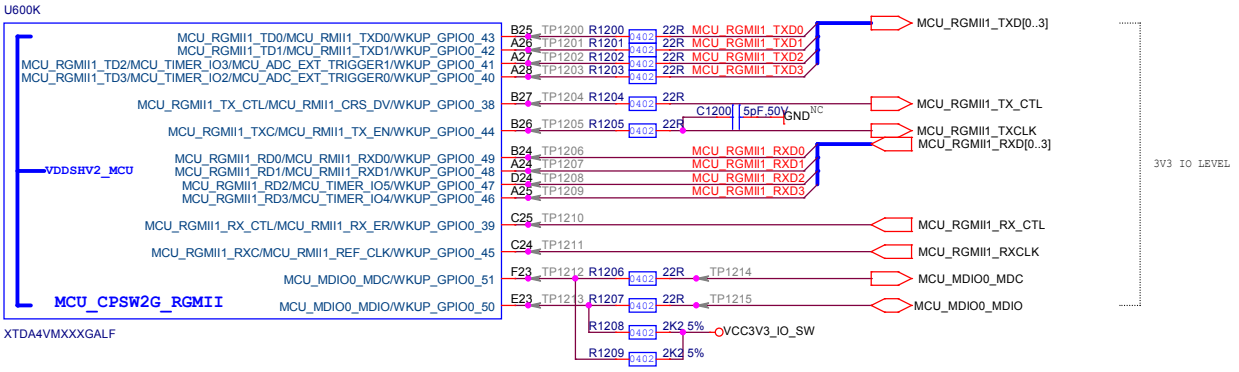
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022	Sheet 10 of 51		



845501926 PDCU HZ

Design NO. 825501036_ADAS_SCH		Rev V1.1	Sheet Name MCU_SPI_IIC
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022		Sheet 11 of 51	

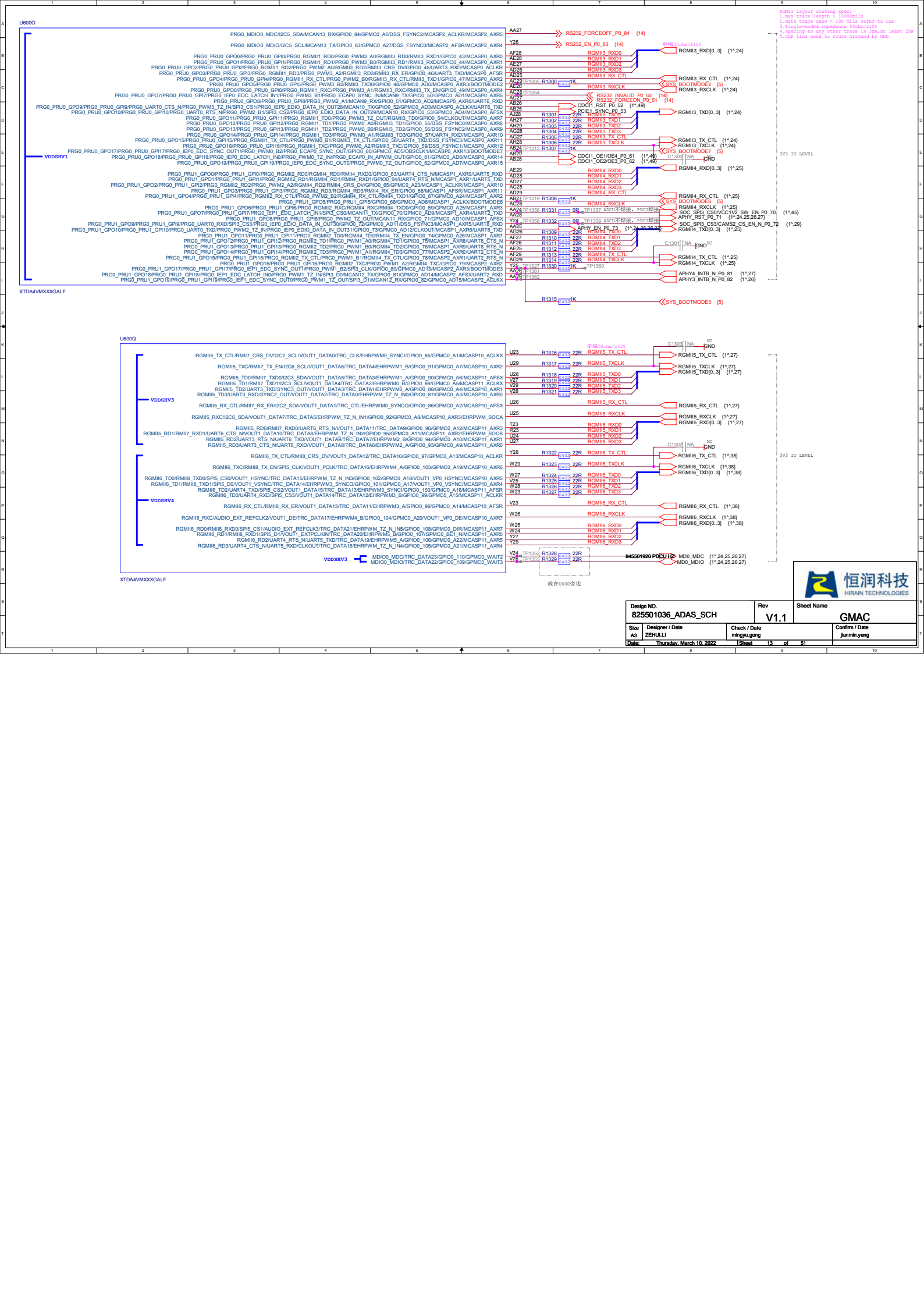
恒润科技 HIRAIN TECHNOLOGIES

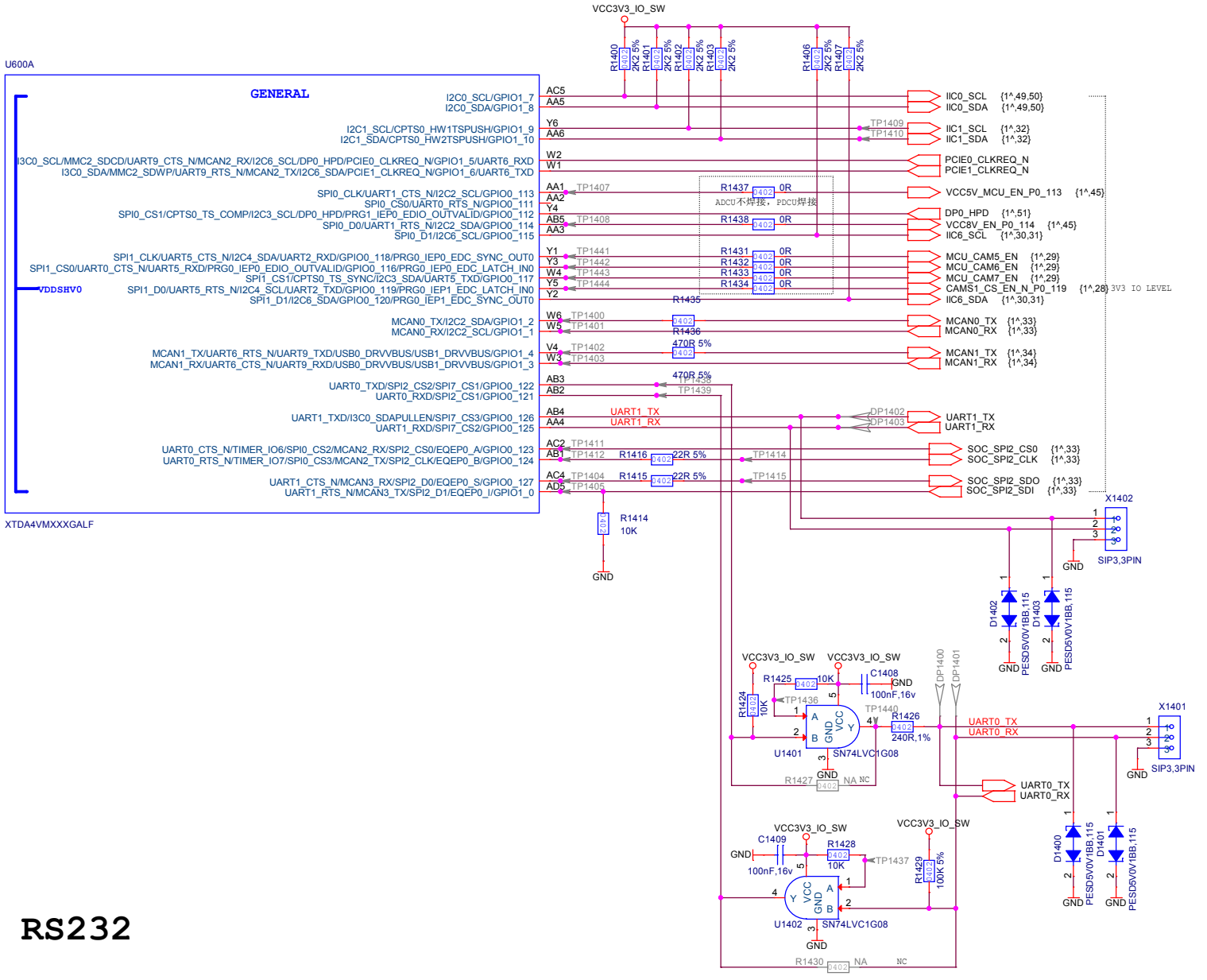


845501926 PDCU HZ

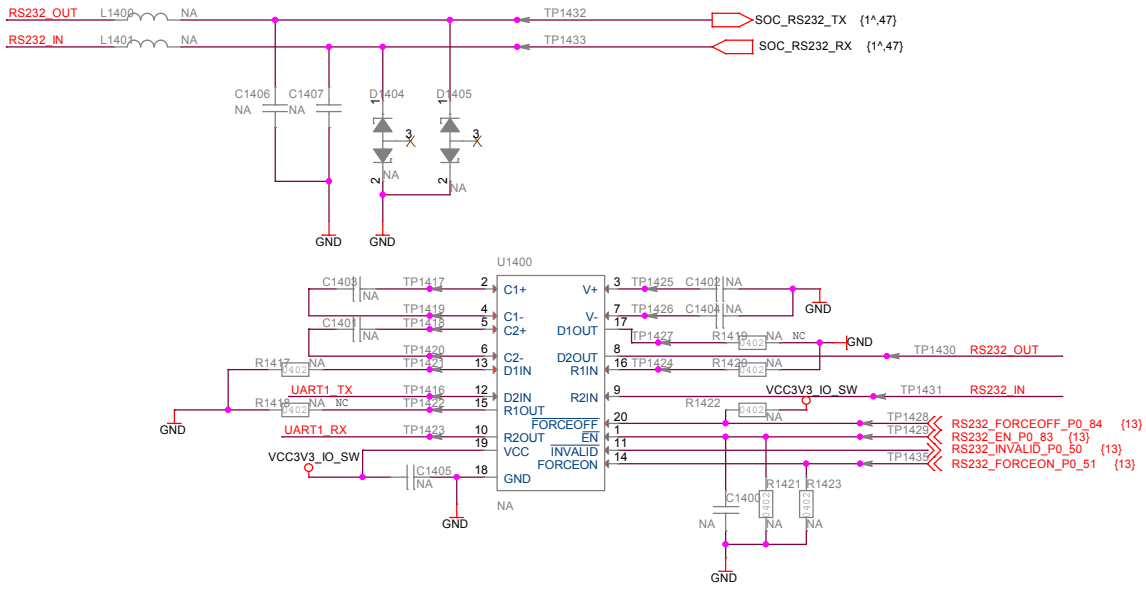
恒润科技 HIRAIN TECHNOLOGIES

Design NO. 825501036_ADAS_SCH		Rev V1.1	Sheet Name MCU_GMAC
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022	Sheet 12 of 51		


RGMII layout routing spec:
1.max trace length < 10000mils
2.data trace skew < 100 mils refer to CLK
3.Single-ended impedance 50ohm/±10%
4.spacing to any other trace is 3xW,at least 2xW
5.CLK line need to route arround by GND
U600O
XTDA4VMXXXGALF
VDDSHV1
3V3 IO LEVEL
U600Q
XTDA4VMXXXGALF
VDDSHV3
VDDSHV4
放在U600旁边
恒润科技
HIRAIN TECHNOLOGIES
Design NO.
825501036_ADAS_SCH
Rev
V1.1
Sheet Name
GMAC
Size
A3
Designer / Date
ZEHULI
Check / Date
mingyu.gong
Confirm / Date
jianmin.yang
Date:
Thursday, March 10, 2022
Sheet
13
of
51



RS232



INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

H = high level, L = low level, X = irrelevant, Z = high impedance

845501926 PDCU HZ

恒润科技 HIRAIN TECHNOLOGIES

Design NO.	Rev	Sheet Name
825501036_ADAS_SCH	V1.1	SOC_IIC_CAN

Size	Designer / Date	Check / Date	Confirm / Date
Custom	ZEHUI.LI	mingyu.gong	jianmin.yang

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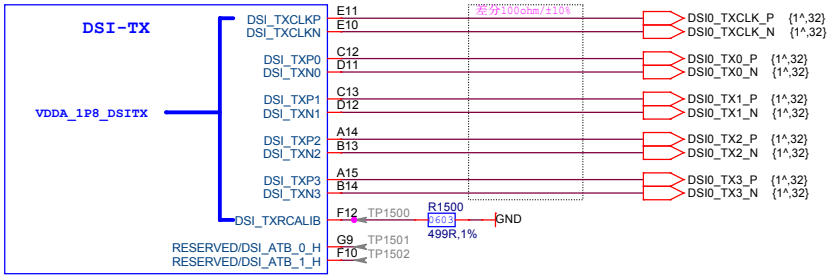
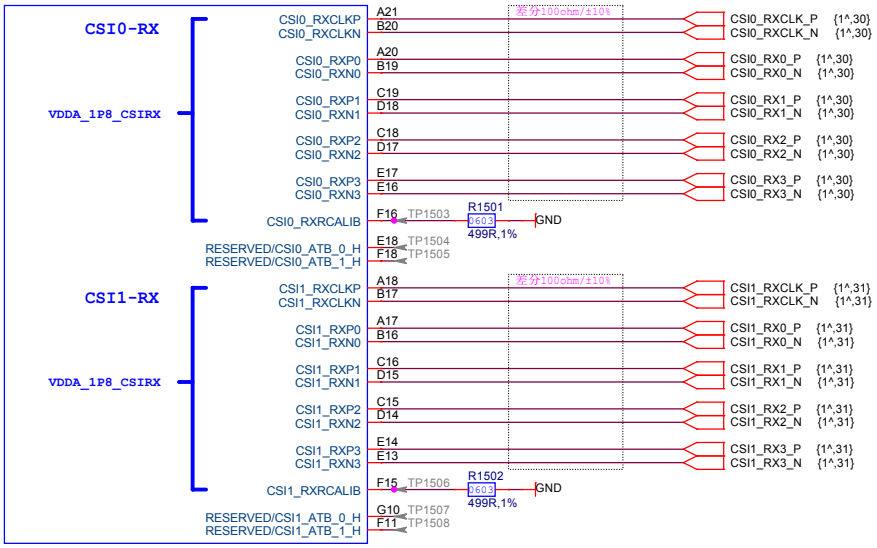
MIPI layout routing spec:
1.max trace length < 10000mils
2.diff pair skew < 8ps or 44mil (Vp=5.5mil/ps,Er=4.6)
3.diff lane skew < 50 mils refer to CLK
4.diff impedance 100ohm/±10%
5.Single-ended impedance 50ohm/±10%
6.no stubs allowed on traces
7.max vias on each trace < 2
8.via stub length typical is 20 mils
9.spacing to any other trace is 3xDS,at least 2xDS
DS = differential spacing of the traces

U600E



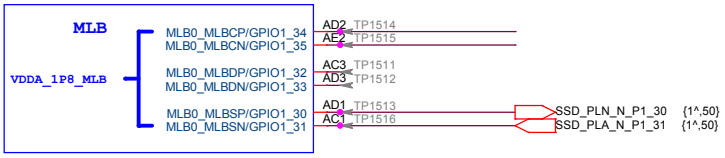
XTDA4VMXXXGALF

U600F



XTDA4VMXXXGALF

U600L

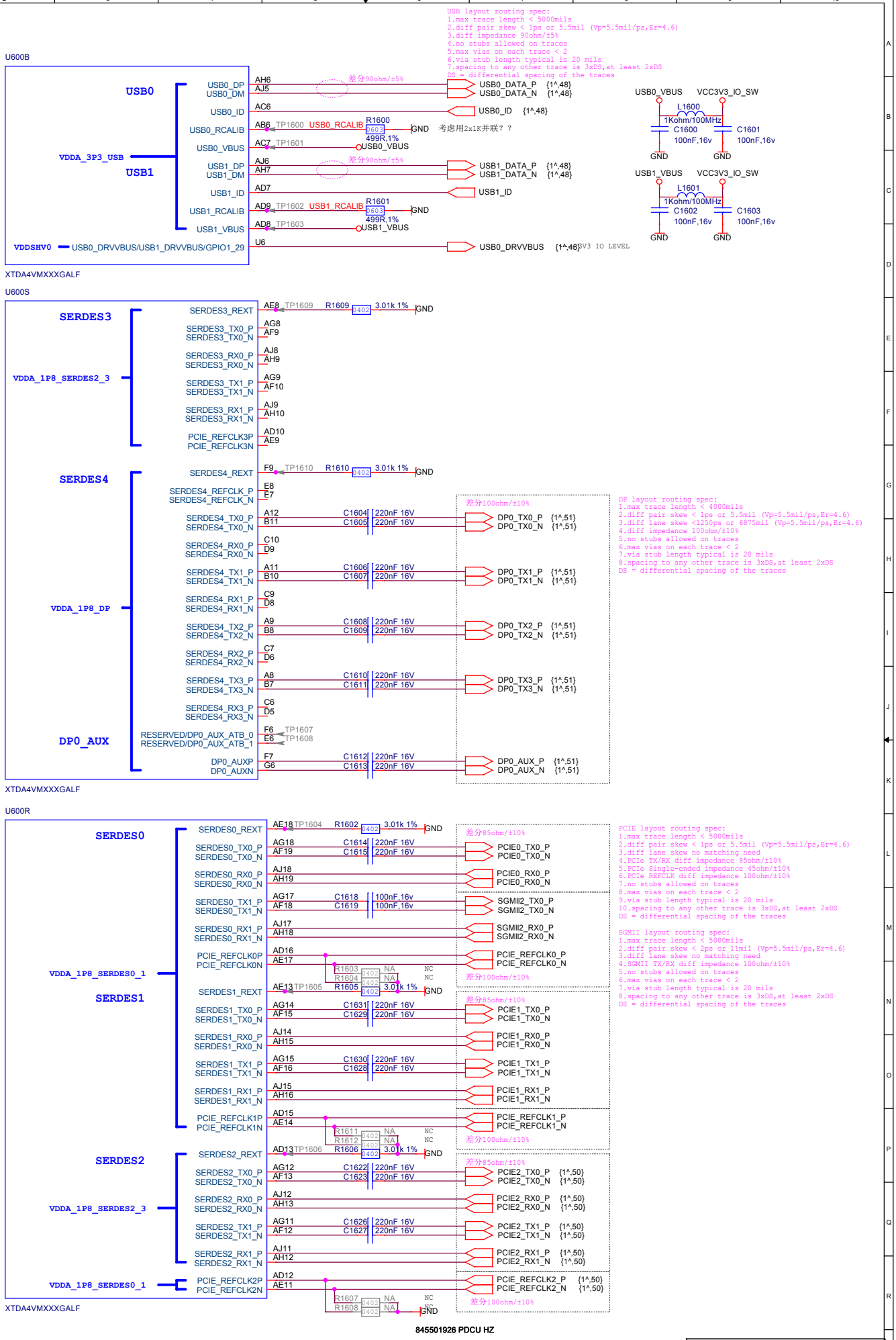


XTDA4VMXXXGALF

845501926 PDCU HZ

恒润科技 HIRAIN TECHNOLOGIES

Design NO. 825501036_ADAS_SCH		Rev V1.1	Sheet Name CSI_DSI_MLB
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022	Sheet 15 of 51		


USB layout routing spec:
1.max trace length < 5000mils
2.diff pair skew < 1ps or 5.5mil (Vp=5.5mil/ps,Er=4.6)
3.diff impedance 90ohm/±5%
4.no stubs allowed on traces
5.max vias on each trace < 2
6.via stub length typical is 20 mils
7.spacing to any other trace is 3xDS,at least 2xDS
DS = differential spacing of the traces
U600B
USB0
USB1
VDDA_3P3_USB
VDDSHV0
USB0_DP
USB0_DM
USB0_ID
USB0_RCALIB
USB0_VBUS
USB1_DP
USB1_DM
USB1_ID
USB1_RCALIB
USB1_VBUS
USB0_DRVVBUS/USB1_DRVVBUS/GPIO1_29
差分90ohm/±5%
USB0_DATA_P
USB0_DATA_N
USB1_DATA_P
USB1_DATA_N
USB0_RCALIB
USB1_RCALIB
R1600
R1601
499R,1%
考虑用2x1K并联？？
USB0_VBUS
USB1_VBUS
USB0_DRVVBUS
3V3 IO LEVEL
L1600
L1601
1Kohm/100MHz
C1600
C1601
C1602
C1603
100nF,16v
GND
XTDA4VMXXXGALF
U600S
SERDES3
SERDES4
DP0_AUX
VDDA_1P8_SERDES2_3
VDDA_1P8_DP
SERDES3_REXT
SERDES3_TX0_P
SERDES3_TX0_N
SERDES3_RX0_P
SERDES3_RX0_N
SERDES3_TX1_P
SERDES3_TX1_N
SERDES3_RX1_P
SERDES3_RX1_N
PCIE_REFCLK3P
PCIE_REFCLK3N
SERDES4_REXT
SERDES4_REFCLK_P
SERDES4_REFCLK_N
SERDES4_TX0_P
SERDES4_TX0_N
SERDES4_RX0_P
SERDES4_RX0_N
SERDES4_TX1_P
SERDES4_TX1_N
SERDES4_RX1_P
SERDES4_RX1_N
SERDES4_TX2_P
SERDES4_TX2_N
SERDES4_RX2_P
SERDES4_RX2_N
SERDES4_TX3_P
SERDES4_TX3_N
SERDES4_RX3_P
SERDES4_RX3_N
RESERVED/DP0_AUX_ATB_0
RESERVED/DP0_AUX_ATB_1
DP0_AUXP
DP0_AUXN
3.01k 1%
差分100ohm/±10%
DP0_TX0_P
DP0_TX0_N
DP0_TX1_P
DP0_TX1_N
DP0_TX2_P
DP0_TX2_N
DP0_TX3_P
DP0_TX3_N
DP0_AUX_P
DP0_AUX_N
DP layout routing spec:
1.max trace length < 4000mils
2.diff pair skew < 1ps or 5.5mil (Vp=5.5mil/ps,Er=4.6)
3.diff lane skew <1250ps or 6875mil (Vp=5.5mil/ps,Er=4.6)
4.diff impedance 100ohm/±10%
5.no stubs allowed on traces
6.max vias on each trace < 2
7.via stub length typical is 20 mils
8.spacing to any other trace is 3xDS,at least 2xDS
DS = differential spacing of the traces
XTDA4VMXXXGALF
U600R
SERDES0
SERDES1
SERDES2
VDDA_1P8_SERDES0_1
VDDA_1P8_SERDES2_3
SERDES0_REXT
SERDES0_TX0_P
SERDES0_TX0_N
SERDES0_RX0_P
SERDES0_RX0_N
SERDES0_TX1_P
SERDES0_TX1_N
SERDES0_RX1_P
SERDES0_RX1_N
PCIE_REFCLK0P
PCIE_REFCLK0N
SERDES1_REXT
SERDES1_TX0_P
SERDES1_TX0_N
SERDES1_RX0_P
SERDES1_RX0_N
SERDES1_TX1_P
SERDES1_TX1_N
SERDES1_RX1_P
SERDES1_RX1_N
PCIE_REFCLK1P
PCIE_REFCLK1N
SERDES2_REXT
SERDES2_TX0_P
SERDES2_TX0_N
SERDES2_RX0_P
SERDES2_RX0_N
SERDES2_TX1_P
SERDES2_TX1_N
SERDES2_RX1_P
SERDES2_RX1_N
PCIE_REFCLK2P
PCIE_REFCLK2N
3.01k 1%
差分85ohm/±10%
PCIE0_TX0_P
PCIE0_TX0_N
PCIE0_RX0_P
PCIE0_RX0_N
SGMII2_TX0_P
SGMII2_TX0_N
SGMII2_RX0_P
SGMII2_RX0_N
PCIE_REFCLK0_P
PCIE_REFCLK0_N
差分100ohm/±10%
PCIE1_TX0_P
PCIE1_TX0_N
PCIE1_RX0_P
PCIE1_RX0_N
PCIE1_TX1_P
PCIE1_TX1_N
PCIE1_RX1_P
PCIE1_RX1_N
PCIE_REFCLK1_P
PCIE_REFCLK1_N
PCIE2_TX0_P
PCIE2_TX0_N
PCIE2_RX0_P
PCIE2_RX0_N
PCIE2_TX1_P
PCIE2_TX1_N
PCIE2_RX1_P
PCIE2_RX1_N
PCIE_REFCLK2_P
PCIE_REFCLK2_N
PCIE layout routing spec:
1.max trace length < 5000mils
2.diff pair skew < 1ps or 5.5mil (Vp=5.5mil/ps,Er=4.6)
3.diff lane skew no matching need
4.PCIe TX/RX diff impedance 85ohm/±10%
5.PCIe Single-ended impedance 45ohm/±10%
6.PCIe REFCLK diff impedance 100ohm/±10%
7.no stubs allowed on traces
8.max vias on each trace < 2
9.via stub length typical is 20 mils
10.spacing to any other trace is 3xDS,at least 2xDS
DS = differential spacing of the traces
SGMII layout routing spec:
1.max trace length < 5000mils
2.diff pair skew < 2ps or 11mil (Vp=5.5mil/ps,Er=4.6)
3.diff lane skew no matching need
4.SGMII TX/RX diff impedance 100ohm/±10%
5.no stubs allowed on traces
6.max vias on each trace < 2
7.via stub length typical is 20 mils
8.spacing to any other trace is 3xDS,at least 2xDS
DS = differential spacing of the traces
XTDA4VMXXXGALF
845501926 PDCU HZ
恒润科技
HIRAIN TECHNOLOGIES
Design NO.
825501036_ADAS_SCH
Rev
V1.1
Sheet Name
USB_DP_PCIE_SGMII
Size
Custom
Designer / Date
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jianmin.yang
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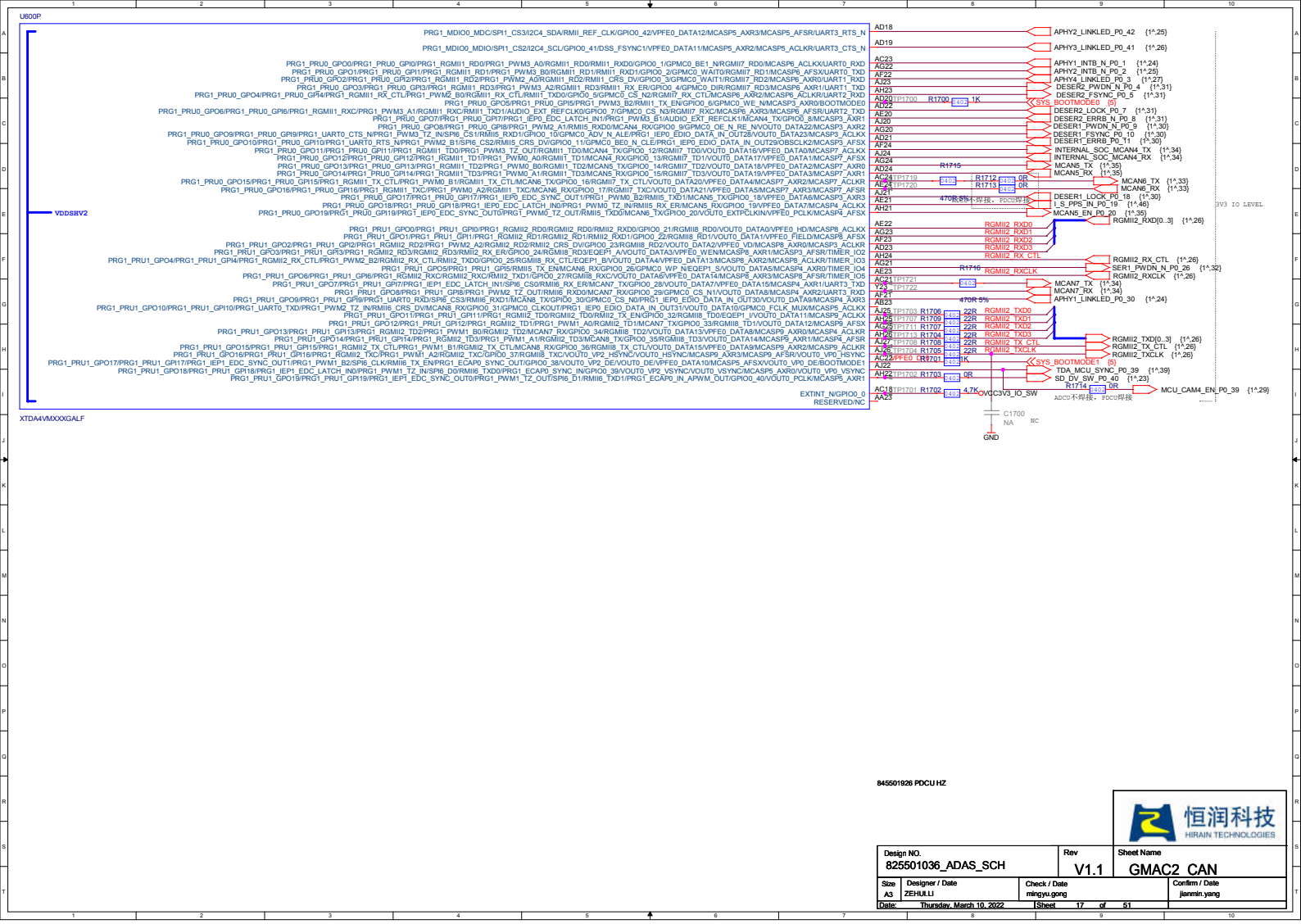
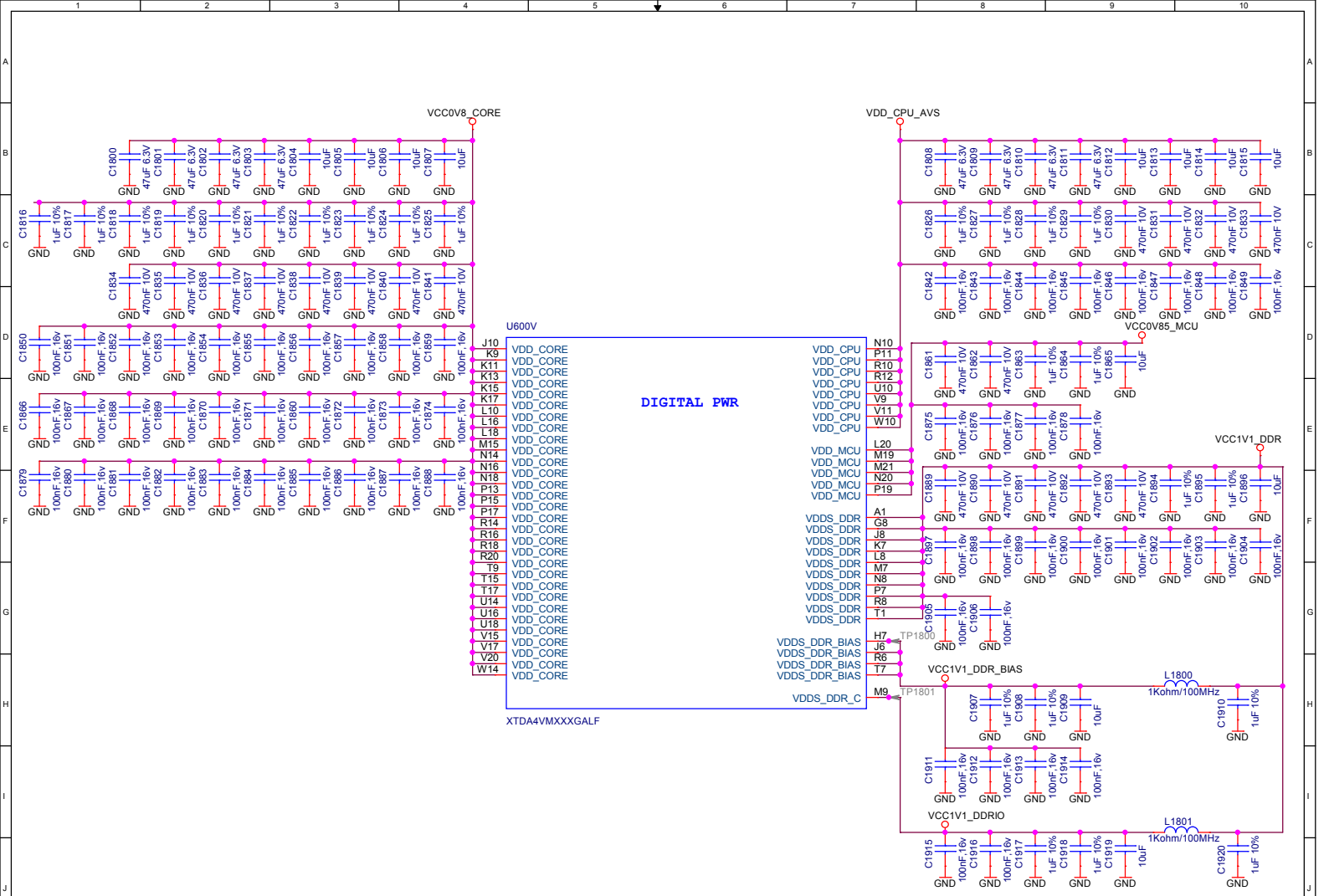

U600P
PRG1_MDIO0_MDC/SPI1_CS3/I2C4_SDA/RMII_REF_CLK/GPIO0_42/VPFE0_DATA12/MCASP5_AXR3/MCASP5_AFSR/UART3_RTS_N
PRG1_MDIO0_MDIO/SPI1_CS2/I2C4_SCL/GPIO0_41/DSS_FSYNC1/VPFE0_DATA11/MCASP5_AXR2/MCASP5_ACLKR/UART3_CTS_N
PRG1_PRU0_GPO0/PRG1_PRU0_GPI0/PRG1_RGMII1_RD0/PRG1_PWM3_A0/RGMII1_RD0/RMII1_RXD0/GPIO0_1/GPMC0_BE1_N/RGMII7_RD0/MCASP6_ACLKX/UART0_RXD
PRG1_PRU0_GPO1/PRG1_PRU0_GPI1/PRG1_RGMII1_RD1/PRG1_PWM3_B0/RGMII1_RD1/RMII1_RXD1/GPIO0_2/GPMC0_WAIT0/RGMII7_RD1/MCASP6_AFSX/UART0_TXD
PRG1_PRU0_GPO2/PRG1_PRU0_GPI2/PRG1_RGMII1_RD2/PRG1_PWM2_A0/RGMII1_RD2/RMII1_CRS_DV/GPIO0_3/GPMC0_WAIT1/RGMII7_RD2/MCASP6_AXR0/UART1_RXD
PRG1_PRU0_GPO3/PRG1_PRU0_GPI3/PRG1_RGMII1_RD3/PRG1_PWM2_A0/RGMII1_RD3/RMII1_RX_ER/GPIO0_4/GPMC0_DIR/RGMII7_RD3/MCASP6_AXR1/UART1_TXD
PRG1_PRU0_GPO4/PRG1_PRU0_GPI4/PRG1_RGMII1_RX_CTL/PRG1_PWM2_B0/RGMII1_RX_CTL/RMII1_TXD0/GPIO0_5/GPMC0_CS_N2/RGMII7_RX_CTL/MCASP6_AXR2/MCASP6_ACLKR/UART2_RXD
PRG1_PRU0_GPO5/PRG1_PRU0_GPI5/PRG1_PWM3_B2/RMII1_TX_EN/GPIO0_6/GPMC0_WE_N/MCASP3_AXR0/BOOTMODE0
PRG1_PRU0_GPO6/PRG1_PRU0_GPI6/PRG1_RGMII1_RXC/PRG1_PWM3_A1/RGMII1_RXC/RMII1_TXD1/AUDIO_EXT_REFCLK0/GPIO0_7/GPMC0_CS_N3/RGMII7_RXC/MCASP6_AXR3/MCASP6_AFSR/UART2_TXD
PRG1_PRU0_GPO7/PRG1_PRU0_GPI7/PRG1_IEP0_EDC_LATCH_IN1/PRG1_PWM3_B1/AUDIO_EXT_REFCLK1/MCAN4_TX/GPIO0_8/MCASP3_AXR1
PRG1_PRU0_GPO8/PRG1_PRU0_GPI8/PRG1_PWM2_A1/RMII1_RXD0/MCAN4_RX/GPIO0_9/GPMC0_OE_N_RE_N/VOUT0_DATA22/MCASP3_AXR2
PRG1_PRU0_GPO9/PRG1_PRU0_GPI9/PRG1_UART0_CTS_N/PRG1_PWM3_TZ_IN/SPI6_CS1/RMII1_RXD1/GPIO0_10/GPMC0_ADV_N_ALE/PRG1_IEP0_EDIO_DATA_IN_OUT28/VOUT0_DATA23/MCASP3_ACLKX
PRG1_PRU0_GPO10/PRG1_PRU0_GPI10/PRG1_UART0_RTS_N/PRG1_PWM2_B1/SPI6_CS2/RMII1_CRS_DV/GPIO0_11/GPMC0_BE0_N_CLE/PRG1_IEP0_EDIO_DATA_IN_OUT29/OBSCLK2/MCASP3_AFSX
PRG1_PRU0_GPO11/PRG1_PRU0_GPI11/PRG1_RGMII1_TD0/PRG1_PWM3_TZ_OUT/RGMII1_TD0/MCAN4_TX/GPIO0_12/RGMII7_TD0/VOUT0_DATA16/VPFE0_DATA0/MCASP7_ACLKX
PRG1_PRU0_GPO12/PRG1_PRU0_GPI12/PRG1_RGMII1_TD1/PRG1_PWM0_A0/RGMII1_TD1/MCAN4_RX/GPIO0_13/RGMII7_TD1/VOUT0_DATA17/VPFE0_DATA1/MCASP7_AFSX
PRG1_PRU0_GPO13/PRG1_PRU0_GPI13/PRG1_RGMII1_TD2/PRG1_PWM0_B0/RGMII1_TD2/MCAN5_TX/GPIO0_14/RGMII7_TD2/VOUT0_DATA18/VPFE0_DATA2/MCASP7_AXR0
PRG1_PRU0_GPO14/PRG1_PRU0_GPI14/PRG1_RGMII1_TD3/PRG1_PWM0_A1/RGMII1_TD3/MCAN5_RX/GPIO0_15/RGMII7_TD3/VOUT0_DATA19/VPFE0_DATA3/MCASP7_AXR1
PRG1_PRU0_GPO15/PRG1_PRU0_GPI15/PRG1_RGMII1_TX_CTL/PRG1_PWM0_B1/RGMII1_TX_CTL/MCAN6_TX/GPIO0_16/RGMII7_TX_CTL/VOUT0_DATA20/VPFE0_DATA4/MCASP7_AXR2/MCASP7_ACLKR
PRG1_PRU0_GPO16/PRG1_PRU0_GPI16/PRG1_RGMII1_TXC/PRG1_PWM0_A2/RGMII1_TXC/MCAN6_RX/GPIO0_17/RGMII7_TXC/VOUT0_DATA21/VPFE0_DATA5/MCASP7_AXR3/MCASP7_AFSR
PRG1_PRU0_GPO17/PRG1_PRU0_GPI17/PRG1_IEP0_EDC_SYNC_OUT1/PRG1_PWM0_B2/RMII5_TXD1/MCAN5_TX/GPIO0_18/VPFE0_DATA6/MCASP3_AXR3
PRG1_PRU0_GPO18/PRG1_PRU0_GPI18/PRG1_IEP0_EDC_LATCH_IN0/PRG1_PWM0_TZ_IN/RMII5_RX_ER/MCAN5_RX/GPIO0_19/VPFE0_DATA7/MCASP4_ACLKX
VDDSHV2
PRG1_PRU0_GPO19/PRG1_PRU0_GPI19/PRG1_IEP0_EDC_SYNC_OUT0/PRG1_PWM0_TZ_OUT/RMII5_TXD0/MCAN6_TX/GPIO0_20/VOUT0_EXTPCLKIN/VPFE0_PCLK/MCASP4_AFSX
PRG1_PRU1_GPO0/PRG1_PRU1_GPI0/PRG1_RGMII2_RD0/RGMII2_RD0/RMII2_RXD0/GPIO0_21/RGMII8_RD0/VOUT0_DATA0/VPFE0_HD/MCASP8_ACLKX
PRG1_PRU1_GPO1/PRG1_PRU1_GPI1/PRG1_RGMII2_RD1/RGMII2_RD1/RMII2_RXD1/GPIO0_22/RGMII8_RD1/VOUT0_DATA1/VPFE0_FIELD/MCASP8_AFSX
PRG1_PRU1_GPO2/PRG1_PRU1_GPI2/PRG1_RGMII2_RD2/PRG1_PWM2_A2/RGMII2_RD2/RMII2_CRS_DV/GPIO0_23/RGMII8_RD2/VOUT0_DATA2/VPFE0_VD/MCASP8_AXR0/MCASP3_ACLKR
PRG1_PRU1_GPO3/PRG1_PRU1_GPI3/PRG1_RGMII2_RD3/RGMII2_RD3/RMII2_RX_ER/GPIO0_24/RGMII8_RD3/EQEP1_A/VOUT0_DATA3/VPFE0_WEN/MCASP8_AXR1/MCASP3_AFSR/TIMER_IO2
PRG1_PRU1_GPO4/PRG1_PRU1_GPI4/PRG1_RGMII2_RX_CTL/PRG1_PWM2_B2/RGMII2_RX_CTL/RMII2_TXD0/GPIO0_25/RGMII8_RX_CTL/EQEP1_B/VOUT0_DATA4/VPFE0_DATA13/MCASP8_AXR2/MCASP8_ACLKR/TIMER_IO3
PRG1_PRU1_GPO5/PRG1_PRU1_GPI5/RMII5_TX_EN/MCAN6_RX/GPIO0_26/GPMC0_WP_N/EQEP1_S/VOUT0_DATA5/MCASP4_AXR0/TIMER_IO4
PRG1_PRU1_GPO6/PRG1_PRU1_GPI6/PRG1_RGMII2_TXC/RGMII2_TXC/RMII2_TXD1/GPIO0_27/RGMII8_RXC/VOUT0_DATA6/VPFE0_DATA14/MCASP8_AXR3/MCASP8_AFSR/TIMER_IO5
PRG1_PRU1_GPO7/PRG1_PRU1_GPI7/PRG1_IEP1_EDC_LATCH_IN1/SPI6_CS0/RMII6_RX_ER/MCAN7_TX/GPIO0_28/VOUT0_DATA7/VPFE0_DATA15/MCASP4_AXR1/UART3_TXD
PRG1_PRU1_GPO8/PRG1_PRU1_GPI8/PRG1_PWM2_TZ_OUT/RMII6_RXD0/MCAN7_RX/GPIO0_29/GPMC0_CS_N1/VOUT0_DATA8/MCASP4_AXR2/UART3_RXD
PRG1_PRU1_GPO9/PRG1_PRU1_GPI9/PRG1_UART0_RXD/SPI6_CS3/RMII6_RXD1/MCAN8_TX/GPIO0_30/GPMC0_CS_N0/PRG1_IEP0_EDIO_DATA_IN_OUT30/VOUT0_DATA9/MCASP4_AXR3
PRG1_PRU1_GPO10/PRG1_PRU1_GPI10/PRG1_UART0_TXD/PRG1_PWM2_TZ_IN/RMII6_CRS_DV/MCAN8_RX/GPIO0_31/GPMC0_CLKOUT/PRG1_IEP0_EDIO_DATA_IN_OUT31/VOUT0_DATA10/GPMC0_FCLK_MUX/MCASP5_ACLKX
PRG1_PRU1_GPO11/PRG1_PRU1_GPI11/PRG1_RGMII2_TD0/RGMII2_TD0/RMII2_TX_EN/GPIO0_32/RGMII8_TD0/EQEP1_I/VOUT0_DATA11/MCASP9_ACLKX
PRG1_PRU1_GPO12/PRG1_PRU1_GPI12/PRG1_RGMII2_TD1/PRG1_PWM1_A0/RGMII2_TD1/MCAN7_TX/GPIO0_33/RGMII8_TD1/VOUT0_DATA12/MCASP9_AFSX
PRG1_PRU1_GPO13/PRG1_PRU1_GPI13/PRG1_RGMII2_TD2/PRG1_PWM1_B0/RGMII2_TD2/MCAN7_RX/GPIO0_34/RGMII8_TD2/VOUT0_DATA13/VPFE0_DATA8/MCASP9_AXR0/MCASP4_ACLKR
PRG1_PRU1_GPO14/PRG1_PRU1_GPI14/PRG1_RGMII2_TD3/PRG1_PWM1_A1/RGMII2_TD3/MCAN8_TX/GPIO0_35/RGMII8_TD3/VOUT0_DATA14/MCASP9_AXR1/MCASP4_AFSR
PRG1_PRU1_GPO15/PRG1_PRU1_GPI15/PRG1_RGMII2_TX_CTL/PRG1_PWM1_B1/RGMII2_TX_CTL/MCAN8_RX/GPIO0_36/RGMII8_TX_CTL/VOUT0_DATA15/VPFE0_DATA9/MCASP9_AXR2/MCASP9_ACLKR
PRG1_PRU1_GPO16/PRG1_PRU1_GPI16/PRG1_RGMII2_TXC/PRG1_PWM1_A2/RGMII2_TXC/GPIO0_37/RGMII8_TXC/VOUT0_VP2_HSYNC/VOUT0_HSYNC/MCASP9_AXR3/MCASP9_AFSR/VOUT0_VP0_HSYNC
PRG1_PRU1_GPO17/PRG1_PRU1_GPI17/PRG1_IEP1_EDC_SYNC_OUT1/PRG1_PWM1_B2/SPI6_CLK/RMII6_TX_EN/PRG1_ECAP0_SYNC_OUT/GPIO0_38/VOUT0_VP2_DE/VOUT0_DE/VPFE0_DATA10/MCASP5_AFSX/VOUT0_VP0_DE/BOOTMODE1
PRG1_PRU1_GPO18/PRG1_PRU1_GPI18/PRG1_IEP1_EDC_LATCH_IN0/PRG1_PWM1_TZ_IN/SPI6_D0/RMII6_TXD0/PRG1_ECAP0_SYNC_IN/GPIO0_39/VOUT0_VP2_VSYNC/VOUT0_VSYNC/MCASP5_AXR0/VOUT0_VP0_VSYNC
PRG1_PRU1_GPO19/PRG1_PRU1_GPI19/PRG1_IEP1_EDC_SYNC_OUT0/PRG1_PWM1_TZ_OUT/SPI6_D1/RMII6_TXD1/PRG1_ECAP0_IN_APWM_OUT/GPIO0_40/VOUT0_PCLK/MCASP5_AXR1
EXTINT_N/GPIO0_0
RESERVED/NC
XTDA4VMXXXGALF
AD18
AD19
AC23
AC22
AF22
AJ23
AH23
AD20
AD22
AE20
AJ20
AG20
AD21
AF24
AJ24
AC24
AD24
AC24
AE24
AJ21
AE21
AH21
AE22
AG23
AF23
AD23
AH24
AC21
AE23
AC21
Y24
AF21
AB23
AJ25
AH25
AG25
AH26
AJ27
AJ26
AC23
AJ22
AH22
AC18
AA23
APHY2_LINKLED_P0_42 {1^,25}
APHY3_LINKLED_P0_41 {1^,26}
APHY1_INTB_N_P0_1 {1^,24}
APHY2_INTB_N_P0_2 {1^,25}
APHY4_LINKLED_P0_3 {1^,27}
DESER2_PWDN_N_P0_4 {1^,31}
DESER2_FSYNC_P0_5 {1^,31}
SYS_BOOTMODE0 (5)
DESER2_LOCK_P0_7 {1^,31}
DESER2_ERRB_N_P0_8 {1^,31}
DESER1_PWDN_N_P0_9 {1^,30}
DESER1_FSYNC_P0_10 {1^,30}
DESER1_ERRB_P0_11 {1^,30}
INTERNAL_SOC_MCAN4_TX {1^,34}
INTERNAL_SOC_MCAN4_RX {1^,34}
MCAN5_TX {1^,35}
MCAN5_RX {1^,35}
MCAN6_TX {1^,33}
MCAN6_RX {1^,33}
DESER1_LOCK_P0_18 {1^,30}
LS_PPS_IN_P0_19 {1^,46}
MCAN5_EN_P0_20 {1^,35}
3V3 IO LEVEL
RGMII2_RXD[0..3] {1^,26}
RGMII2_RXD0
RGMII2_RXD1
RGMII2_RXD2
RGMII2_RXD3
RGMII2_RX_CTL
RGMII2_RX_CTL {1^,26}
SER1_PWDN_N_P0_26 {1^,32}
RGMII2_RXCLK
RGMII2_RXCLK {1^,26}
MCAN7_TX {1^,34}
MCAN7_RX {1^,34}
APHY1_LINKLED_P0_30 {1^,24}
RGMII2_TXD0
RGMII2_TXD1
RGMII2_TXD2
RGMII2_TXD3
RGMII2_TXD[0..3] {1^,26}
RGMII2_TX_CTL
RGMII2_TX_CTL {1^,26}
RGMII2_TXCLK
RGMII2_TXCLK {1^,26}
SYS_BOOTMODE1 (5)
TDA_MCU_SYNC_P0_39 {1^,39}
SD_DV_SW_P0_40 {1^,23}
MCU_CAM4_EN_P0_39 {1^,29}
TP1719
TP1720
TP1721
TP1722
TP1703
TP1707
TP1711
TP1713
TP1708
TP1704
TP1701
TP1702
R1700 1K
R1712 0R
R1713 0R
R1715
R1716
R1717 470R 5%
R1706 22R
R1709 22R
R1707 22R
R1704 22R
R1706 22R
R1705 22R
R1701 4.7K
R1703 0R
R1714 0R
C1700 NA NC
VCC3V3_IO_SW
GND
470R 5%不焊接，PDCU焊接
ADCU不焊接，PDCU焊接
845501926 PDCU HZ
恒润科技 HIRAIN TECHNOLOGIES
Design NO. 825501036_ADAS_SCH
Rev V1.1
Sheet Name GMAC2_CAN
Size A3
Designer / Date ZEHUILI
Check / Date mingyu.gong
Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022
Sheet 17 of 51



845501926 PDCU HZ

恒润科技 HIRAIN TECHNOLOGIES

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825501036_ADAS_SCH	V1.1	TDA4_PWR1

Size	Designer / Date	Check / Date	Confirm / Date
Custom	ZEHUI.LI	mingyu.gong	jianmin.yang

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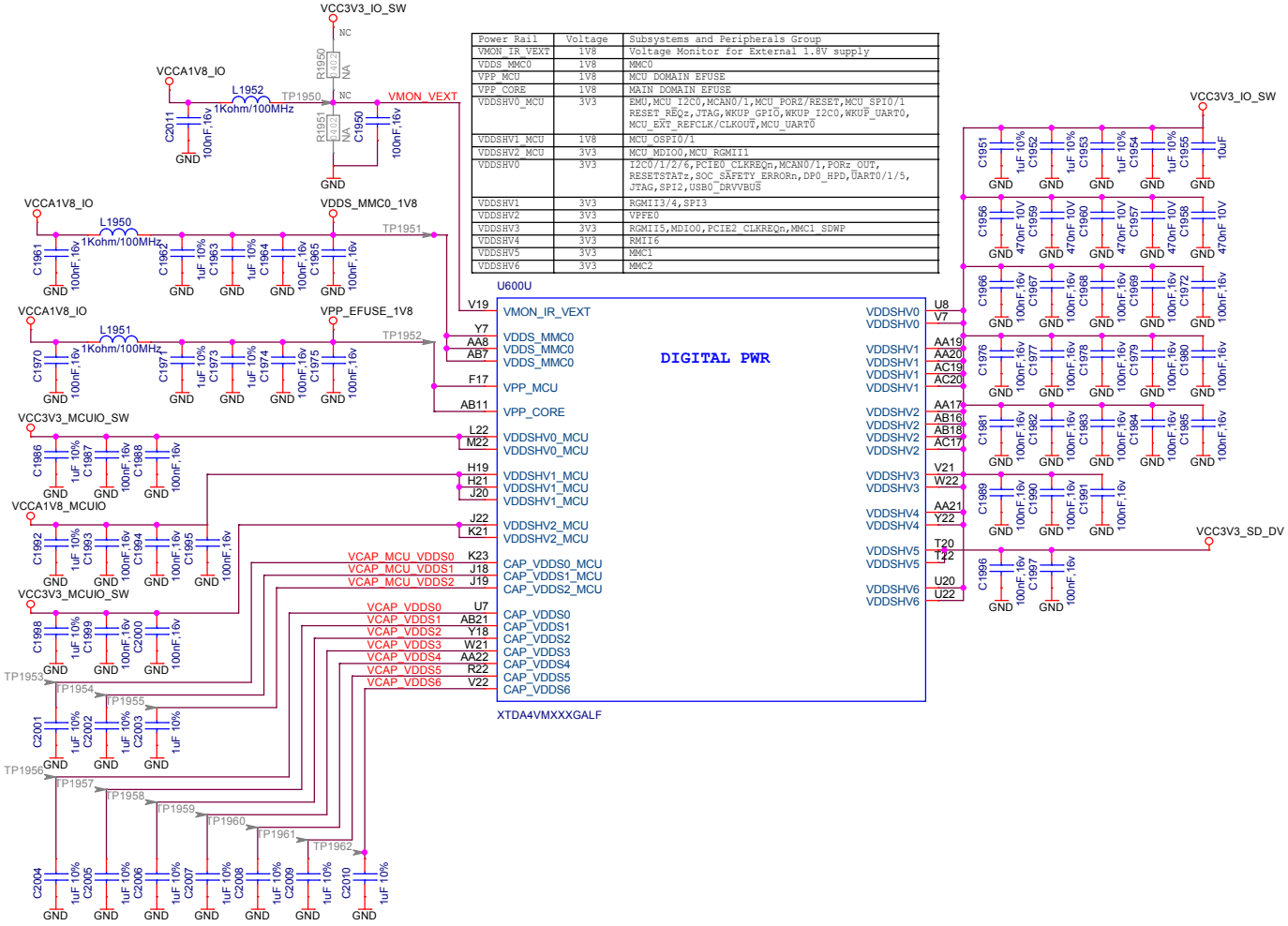

Power Rail	Voltage	Subsystems and Peripherals Group
VMON_IR_VEXT	1V8	Voltage Monitor for External 1.8V supply
VDDS_MMC0	1V8	MMC0
VPP_MCU	1V8	MCU_DOMAIN_EFUSE
VPP_CORE	1V8	MAIN_DOMAIN_EFUSE
VDDSHV0_MCU	3V3	EMU,MCU_I2C0,MCAN0/1,MCU_PORZ/RESET,MCU_SPI0/1 RESET_REQz,JTAG,WKUP_GPIO,WKUP_I2C0,WKUP_UART0, MCU_EXT_REFCLK/CLKOUT,MCU_UART0
VDDSHV1_MCU	1V8	MCU_OSPI0/1
VDDSHV2_MCU	3V3	MCU_MDIO0,MCU_RGMII1
VDDSHV0	3V3	I2C0/1/2/6,PCIE0_CLKREQn,MCAN0/1,PORz_OUT, RESETSTATz,SOC_SAFETY_ERRORn,DP0_HPD,UART0/1/5, JTAG,SPI2,USB0_DRVVBUS
VDDSHV1	3V3	RGMII3/4,SPI3
VDDSHV2	3V3	VPFE0
VDDSHV3	3V3	RGMII5,MDIO0,PCIE2_CLKREQn,MMC1_SDWP
VDDSHV4	3V3	RMII6
VDDSHV5	3V3	MMC1
VDDSHV6	3V3	MMC2

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恒润科技 HIRAIN TECHNOLOGIES

Design NO.	Rev	Sheet Name
825501036_ADAS_SCH	V1.1	TDA4_PWR2

Size	Designer / Date	Check / Date	Confirm / Date
Custom	ZEHUI.LI	mingyu.gong	jianmin.yang

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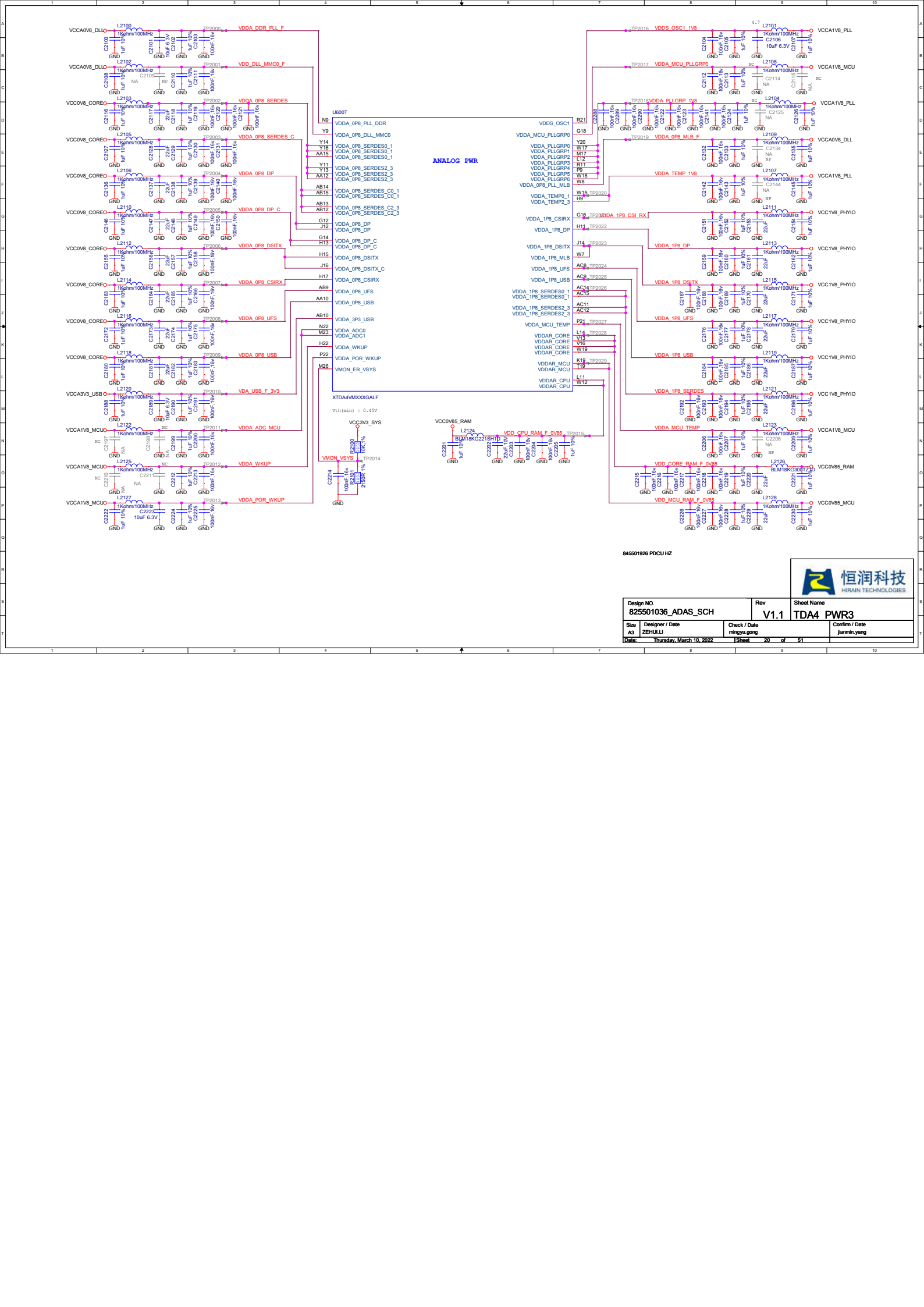
ANALOG PWR
U600T
XTDA4VMXXXGALF
Vth(min) = 0.45V
VDDA_0P8_PLL_DDR
VDDA_0P8_DLL_MMC0
VDDA_0P8_SERDES0_1
VDDA_0P8_SERDES0_1
VDDA_0P8_SERDES0_1
VDDA_0P8_SERDES2_3
VDDA_0P8_SERDES2_3
VDDA_0P8_SERDES2_3
VDDA_0P8_SERDES_C0_1
VDDA_0P8_SERDES_C0_1
VDDA_0P8_SERDES_C2_3
VDDA_0P8_SERDES_C2_3
VDDA_0P8_DP
VDDA_0P8_DP
VDDA_0P8_DP_C
VDDA_0P8_DP_C
VDDA_0P8_DSITX
VDDA_0P8_DSITX_C
VDDA_0P8_CSIRX
VDDA_0P8_UFS
VDDA_0P8_USB
VDDA_3P3_USB
VDDA_ADC0
VDDA_ADC1
VDDA_WKUP
VDDA_POR_WKUP
VMON_ERR_VSYS
VDDS_OSC1
VDDA_MCU_PLLGRP0
VDDA_PLLGRP0
VDDA_PLLGRP1
VDDA_PLLGRP2
VDDA_PLLGRP3
VDDA_PLLGRP4
VDDA_PLLGRP5
VDDA_PLLGRP6
VDDA_0P8_PLL_MLB
VDDA_TEMP0_1
VDDA_TEMP2_3
VDDA_1P8_CSIRX
VDDA_1P8_DP
VDDA_1P8_DSITX
VDDA_1P8_MLB
VDDA_1P8_UFS
VDDA_1P8_USB
VDDA_1P8_SERDES0_1
VDDA_1P8_SERDES0_1
VDDA_1P8_SERDES2_3
VDDA_1P8_SERDES2_3
VDDA_MCU_TEMP
VDDAR_CORE
VDDAR_CORE
VDDAR_CORE
VDDAR_CORE
VDDAR_MCU
VDDAR_MCU
VDDAR_CPU
VDDAR_CPU
VCC3V3_SYS
VMON_VSYS
VCC0V85_RAM
VDD_CPU_RAM_F_0V85
VDD_CORE_RAM_F_0V85
VDD_MCU_RAM_F_0V85
VCCA0V8_DLL
VCC0V8_CORE
VCCA3V3_USB
VCCA1V8_MCU
VDDA_DDR_PLL_F
VDD_DLL_MMC0_F
VDDA_0P8_SERDES
VDDA_0P8_SERDES_C
VDDA_0P8_DP
VDDA_0P8_DP_C
VDDA_0P8_DSITX
VDDA_0P8_CSIRX
VDDA_0P8_UFS
VDDA_0P8_USB
VDA_USB_F_3V3
VDDA_ADC_MCU
VDDA_WKUP
VDDA_POR_WKUP
VDDS_OSC1_1V8
VDDA_MCU_PLLGRP0
VDDA_0P8_MLB_F
VDDA_TEMP_1V8
VDDA_1P8_CSI_RX
VDDA_1P8_DP
VDDA_1P8_DSITX
VDDA_1P8_UFS
VDDA_1P8_USB
VDDA_1P8_SERDES
VDDA_MCU_TEMP
VDD_CORE_RAM_F_0V85
VDD_MCU_RAM_F_0V85
VCCA1V8_PLL
VCCA1V8_MCU
VCCA0V8_DLL
VCC1V8_PHYIO
VCC0V85_RAM
VCC0V85_MCU
845501926 PDCU HZ
恒润科技
HIRAIN TECHNOLOGIES
Design NO.
825501036_ADAS_SCH
Rev
V1.1
Sheet Name
TDA4 PWR3
Size
A3
Designer / Date
ZEHUI.LI
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jianmin.yang
Date:
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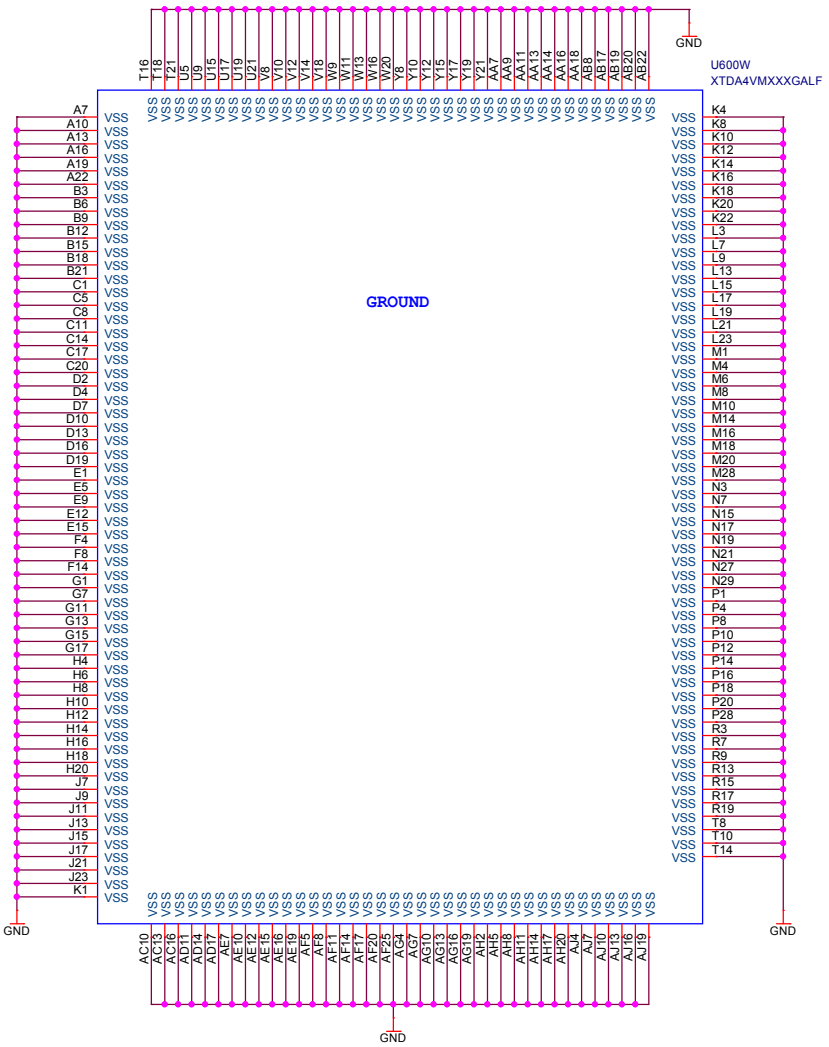

845501926 PDCU HZ

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HIRAIN TECHNOLOGIES

Design NO.	Rev	Sheet Name
825501036_ADAS_SCH	V1.1	TDA4_GND

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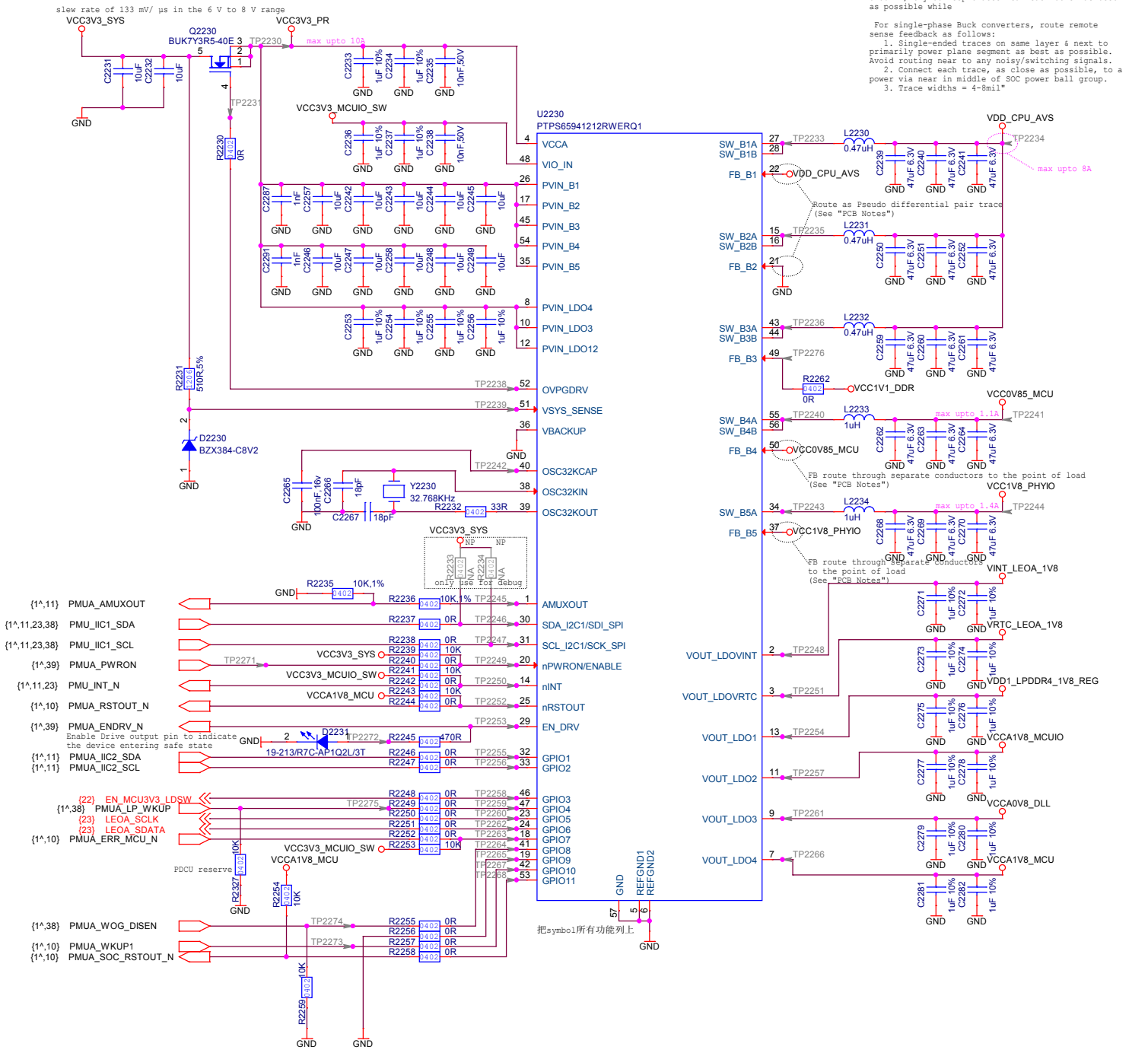
"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

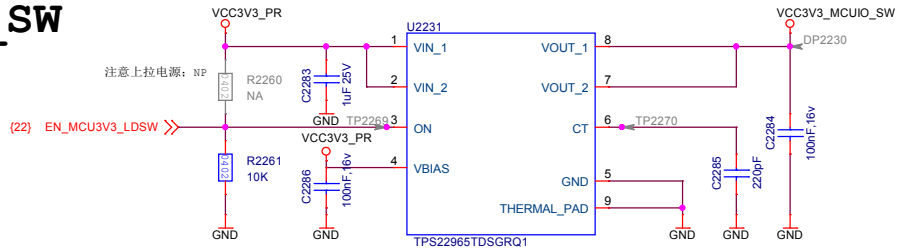
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMUA

slew rate of 133 mV/ µs in the 6 V to 8 V range



VCC3V3_SW



845501926 PDCU HZ

Design NO. 825501036_ADAS_SCH		Rev V1.1	Sheet Name PMIC1 CONTROL
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
Date: Thursday, March 10, 2022	Sheet 22 of 51		

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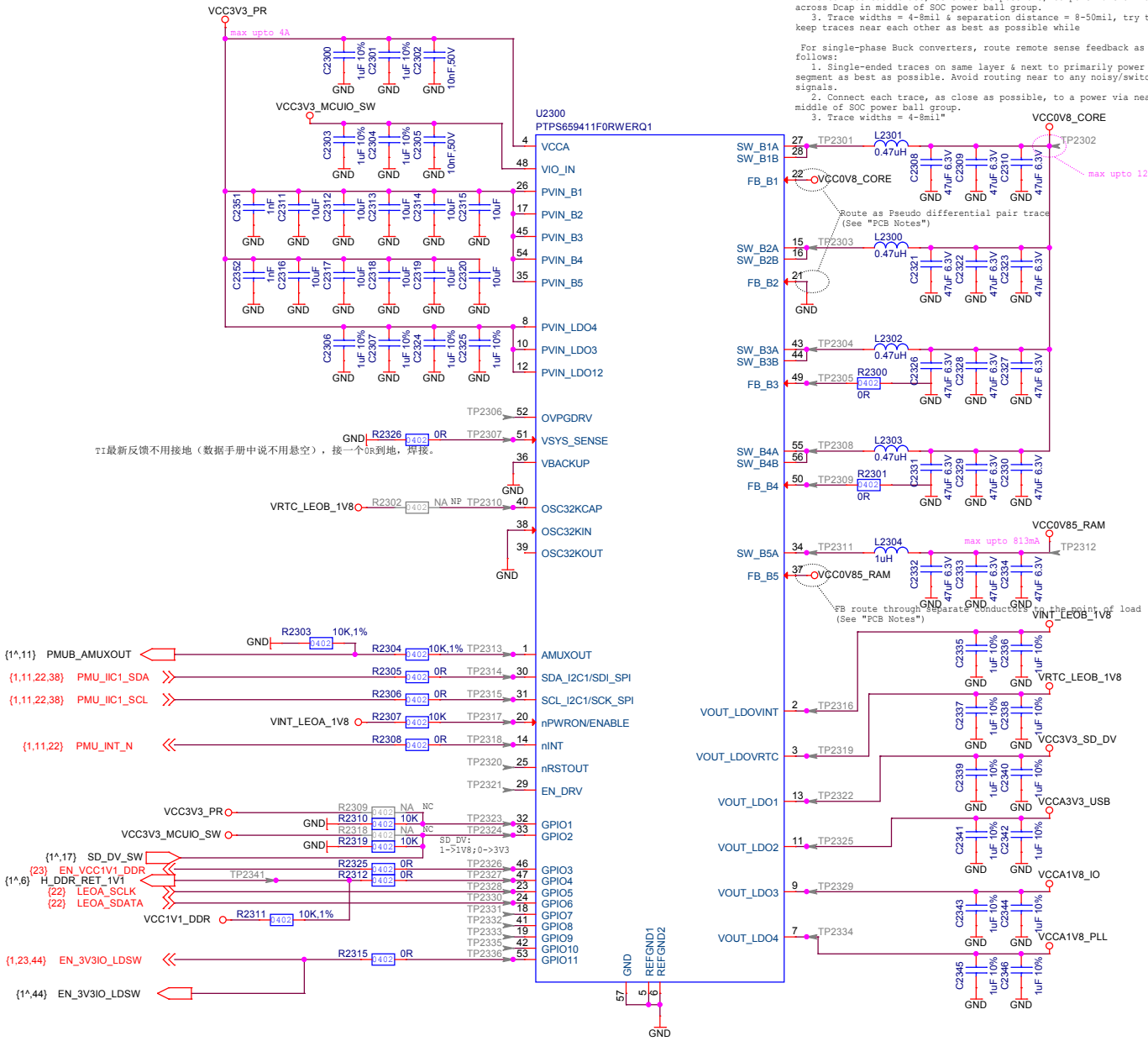
PMUB

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



845501926 PDCU HZ

Design NO. 825501036_ADAS_SCH	Rev V1.1	Sheet Name PMIC2_SMPS	
Size Custom	Designer / Date ZEHUI.LI	Check / Date mingyu.gong	Confirm / Date jianmin.yang
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