UCC28950 Design Calc

This spreadsheet guides the User through the desig

1. The Macros must be ENABLED.

2. The Analysis ToolPak Add-In must be checked.
   - This feature can be found in the Tools Menu
   - Select Add-Ins
   - Check the box next to Analysis ToolPak

3. Enter the desired design parameters in the YELL

4. The spreadsheet will calculate the ideal values a

5. Actual standard values must be entered for the s

6. Note this design tool was generated to accompar
SLUA560

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gn process for a

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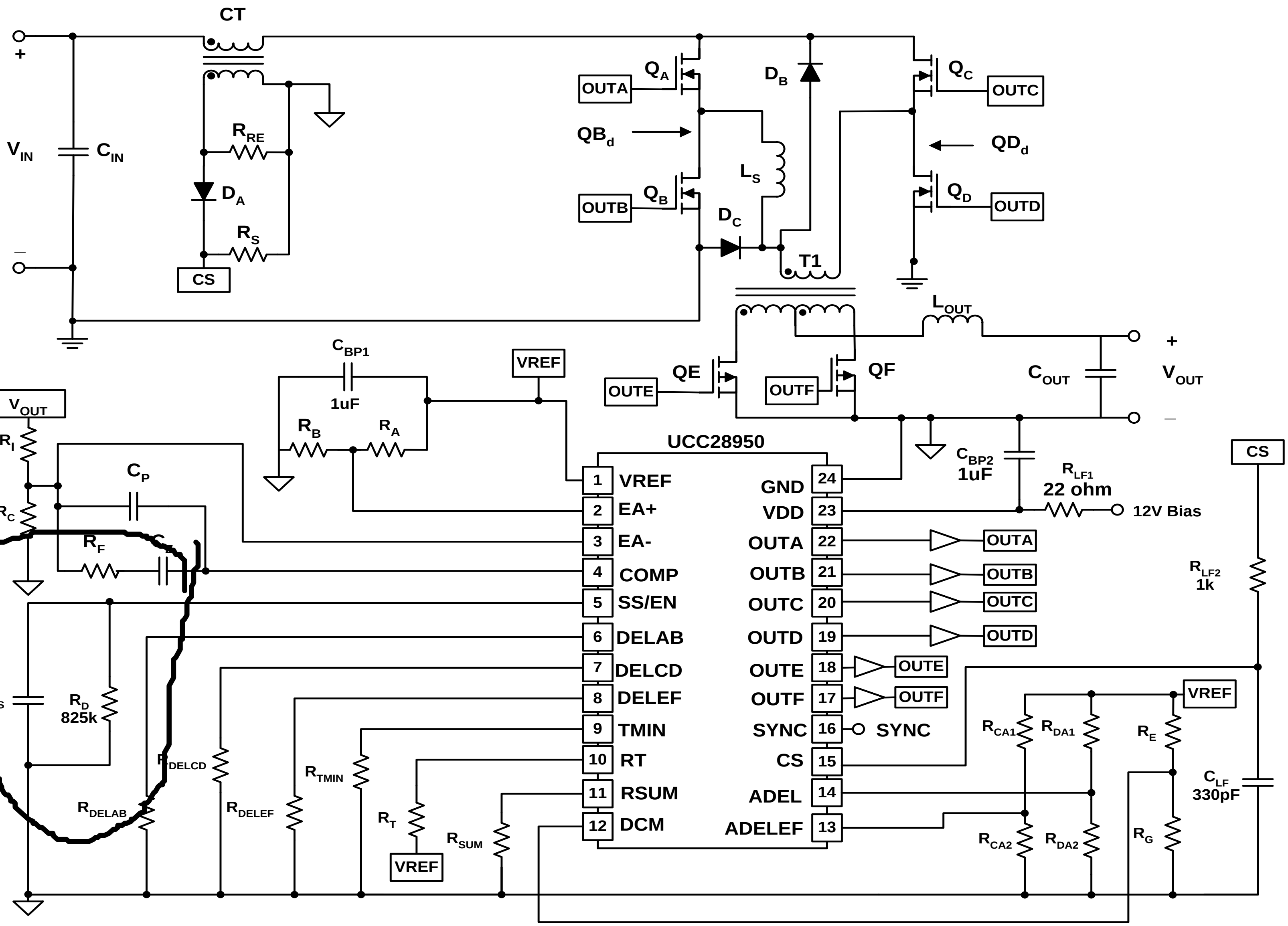
LOW shaded boxes

and display the results in red

spreadsheet to calculate the

ny application report



CT
+
VIN
CIN
RRE
DA
RS
CS
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OUTA
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QB
OUTB
DB
LS
DC
T1
QC
OUTC
QDd
QD
OUTD
LOUT
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UCC28950
VOUT
RI
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825k
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RDELCD
RDELEF
RTMIN
RT
VREF
RSUM
1 VREF
2 EA+
3 EA-
4 COMP
5 SS/EN
6 DELAB
7 DELCD
8 DELEF
9 TMIN
10 RT
11 RSUM
12 DCM
24 GND
23 VDD
22 OUTA
21 OUTB
20 OUTC
19 OUTD
18 OUTE
17 OUTF
16 SYNC
15 CS
14 ADEL
13 ADELEF
CBP2
1uF
RLF1
22 ohm
12V Bias
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RLF2
1k
OUTA
OUTB
OUTC
OUTD
OUTE
OUTF
SYNC
VREF
RCA1
RDA1
RE
CLF
330pF
RCA2
RDA2
RG

UCC28950 Excel Design Tool: SLUC222D			
Revision: D	**7/27/2018**		
This design tool was generated based on the information in application report SLUA560			
It is recommended that you read this application note before using this design tool			
Enter Design Parameters and Chosen Component Values in Yellow Cells			
Warning Negative Numbers in Calculated Values Could Indicate			
> Efficiency goal with selected components may not be achievable			
> Invalid parameters entered in yellow cells			
> Design cannot calculate realistic values for your design parameters			
Design Specifications			
Description	**Minimum**	**Typical**	**Maximum**
Input Voltage	**140**	**150.00**	**160**
Output Voltage	**24**	**27.00**	**28**
Allowable Output Voltage Transients (90% Load Step)			**2**
Output Power (P_{OUT})			**600**
Full Load Efficiency	**85%**		
Inductor (L_{OUT}) Switching Frequency		**200.00**	
Selecting Power Transformer (T1)			
Description	**Variable**		**Unit**
Set Initial Power Budget	**P_{BUDGET}**	**105.88**	**W**
Estimated FET Voltage Drop	**V_{RDSON}**	**0.30**	**V**
Maximum Duty Cycle Nominal	**D_{MAX}**	**0.66**	
T1 Transformer Turns Ratio=N_P/N_S	**a1**	**3.37**	

Select Transformer Turns Ratio	**a1**	**4.000**	
Typical Duty Cycle	**D_{TYP}**	**0.73**	
Inductor Ripple Current	**ΔI_{LOUT}**	**4.44**	**A**
T1 Primary Magnetizing Inductance > or =	**L_{MAG}**	**0.36**	**mH**
Please Refer to Figure of T1 Current	**I_{PS}**	**24.44**	**A**
Please Refer to Figure of T1 Current	**I_{MS}**	**20.00**	**A**
Please Refer to Figure of T1 Current	**I_{MS2}**	**22.22**	**A**
Partial RMS Current	**I_{SRMS1}**	**12.79**	**A**
Partial RMS Current	**I_{SRMS2}**	**9.62**	**A**
Partial RMS Current	**I_{SRMS3}**	**0.53**	**A**
Calculate T1 Secondary RMS Current (I_{SRMS})	**I_{SRMS}**	**16.01**	**A**
Primary Magnetizing Current Based on L_{MAG}	**ΔI_{LMAG}**	**1.27**	**A**
Please Refer to Figure of T1 Current	**I_{PP}**	**8.36**	**A**
Please Refer to Figure of T1 Current	**I_{MP}**	**7.25**	**A**
Please Refer to Figure of T1 Current	**I_{MP2}**	**7.70**	**A**
Partial RMS Current	**I_{PRMS1}**	**6.35**	**A**
Partial RMS Current	**I_{PRMS2}**	**4.69**	**A**
Calculate T1 Primary RMS Current (I_{PRMS})	**I_{PRMS}**	**7.89**	**A**
Primary Magnetizing Inductance	**L_{MAG}**	**0.41**	**mH**
Transformer Primary DC Resistance	**DCR_P**	**0.50**	**mΩ**
Transformer Secondary DC Resistance	**DCR_S**	**0.50**	**mΩ**
Measured Transformer Primary Leakage Inductance	**L_{LK}**	**14.22**	**uH**
Estimated transform loss, 2X Copper Losses	**P_{T1}**	**0.58**	**W**

Recalculate Power Budget	P_{BUDGET}	105.31	W
QA, QB, QC, QD FET selection:			
Voltage Applied to FET Gate ≈ VDD	V_g	10.00	V
FET drain to source on resistance	$R_{ds(on)QA}$	144.00	mΩ
FET Specified Coss	$C_{OSS\_QA\_SPEC}$	22.00	pF
QA FET Gate Charge	QA_g	28.00	nC
Voltage Across Drain to Source Where C_{OSS} was Measured, Data Sheet Parameter	V_{dsQA}	400.00	V
Calculate average C_{OSS}	$C_{OSS\_QA\_AVG}$	34.79	pF
Calculate QA losses	P_{QA}	9.02	W
Recalculate Power Budget	P_{BUDGET}	69.22	W
Select Shim Inductor (L_S)			
Calculated Shim Inductance	L_S	-14.09	uH
Shim Inductance Used	L_S	26.00	uH
L_S DC Resistance	DCR_{LS}	4.00	mΩ
Estimate L_S power loss (P_{LS})	P_{LS}	0.50	W
Recalculate Power Budget	P_{BUDGET}	68.72	W
Selecting Output Inductor (L_{OUT})			
Calculate Output Inductance	L_{OUT}	8.17	uH
Calculate L_{OUT} RMS Current	I_{LOUT_RMS}	22.37	A
Output Inductance Used	L_{OUT}	40.00	uH
L_{OUT} equivalent series resistance	DCR_{LOUT}	0.75	mΩ
Estimate L_{OUT} power loss	P_{LOUT}	0.75	W

Recalculate Power Budget	P_{BUDGET}	67.97	W
Selecting Output Capacitance (C_{OUT})			
Time it takes L_{OUT} to change 90% of its full load current	t_{HU}	29.63	us
Output Capacitance ESR ≤	ESR_{COUT}	90.00	mΩ
Output Capacitance Cout ≥	C_{OUT}	2962.96	uF
Output Capacitance RMS Current	I_{COUT_RMS}	2.57	A
Number of Output Capacitors Used	n	5.00	
Single Capacitor Capacitance		3000.00	uF
Single Capacitor ESR		31.00	mΩ
Total Output Capacitance	C_{OUT}	15000.00	uF
Total Equivalent Series Resistance	ESR_{COUT}	6.20	mΩ
Calculate Output Capacitance Loss	P_{COUT}	0.04	W
Recalculate Power Budget	P_{BUDGET}	67.93	W
Select FETs QE and QF:			
Maximum Voltage Across QE and QF	V_{dsQE}	80.00	V
QE and QF Gate Charge	QE_g	78.00	nC
QE and QF on Resistance	$R_{ds(on)QE}$	51.00	mΩ
Voltage Specified at C_{OSS} Specified in the Data Sheet	V_{dsQE_SPEC}	480.00	V
Specified QE and QF C_{OSS} From the Data Sheet	C_{OSS_SPEC}	780.00	pF
Average QE and QF C_{OSS}	$C_{OSS\_QE\_AVG}$	318.43	pF
QE and QF RMS Current	I_{QE_RMS}	16.01	A
Maximum Gate Charge at the end of the Miller Plateau	QE_{MILLER_MAX}	70.00	nC
Minimum Gate Charge at the beginning of the Miller Plateau	QE_{MILLER_MIN}	15.00	nC
Peak Current Gate of QE and QF is Driven with	I_P	6.00	A

Approximate QE and QF V_{ds} Rise and Fall Times	$t_r \approx t_f$	18.33	ns
Estimate QE FET Losses	P_{QE}	20.16	W
Recalculate Power Budget	P_{BUDGET}	27.61	W
Input Capacitance Calculations (C_{IN})			
Possible Delay That will Be Required for ZVS	t_{DELAY}	146.97	ns
t_{DELAY} will act as a duty cycle clamp	D_{CLAMP}	0.97	
Minimum Input During Line Dropout	V_{DROP}	113.11	V
Calculate Minimum Input Capacitance	C_{IN}	2060.42	uF
High Frequency C_{IN} RMS Current	I_{CINRMS}	3.86	A
Input Capacitance Used	C_{IN}	2500.00	uF
Equivalent Series Resistance	ESR_{CIN}	10.00	mΩ
Estimate C_{IN} Power Dissipation	P_{CIN}	0.15	W
Recalculate Power Budget This is the remaining power left for the CT network, IC and IC sensing resistors	P_{BUDGET}	27.47	W
Setting up the current sense network (CT, R_S, $R_{RE,}$ D_A):			
Select CT and Enter Turns Ratio a2 = I_P/I_S	a2	100.00	
Calculate nominal peak current (I_{P1}) at V_{INMIN}	I_{P1}	8.32	A
Calculate Current Sense Resistor	R_S	19.66	Ω
Closest Standard Resistor Value (E48)	R_S	19.60	Ω
Select Current Sense Resistor for Your Design	R_S	19.60	Ω
Estimate Rs Power Loss	P_{RS}	0.08	W
Maximum Diode D_A Reverse Voltage	V_{DA}	66.04	V

Estimate D_A Losses	P_{DA}	0.03	W
Setting up Voltage Amplifier Reference $G_C(f)$			
Programmed Voltage Reference, Needs to be < 5V	V1	2.50	V
Select Standard Resistor	R_B	2.37	kΩ
Calculated Resistance	R_A	2.37	kΩ
Closest Standard Resistor Value (E48)	R_A	2.37	kΩ
Select Standard Resistor Value	R_A	2.37	kΩ
Select Standard Resistor	R_C	2.37	kΩ
Calculated Resistance	R_I	23.23	kΩ
Closest Standard Resistor Value (E48)	R_I	23.70	kΩ
Select Standard Resistor Value	R_I	23.70	kΩ
Double pole of $G_{CO}(f)$	f_{PP}	50.00	kHz
Voltage Loop Crossover Frequency	f_C	5.00	kHz
Load Impedance at 10% Load	R_{LOAD}	12.15	Ω
Calculate Feedback Resistor	R_F	209.29	kΩ
Closest Standard Resistor Value (E48)	R_F	205.00	kΩ
Select Standard Resistor Value	R_F	205.00	kΩ
Calculate Zero Capacitor	C_Z	0.78	nF
Closest Standard Capacitor Value	Cz	0.82	nF
Select Standard Capacitor Value	C_Z	0.82	nF
Calculate Pole Capacitor	C_P	77.64	pF
Closest Standard Capacitor Value	C_P	82.00	pF
Select Standard Capacitor Value	C_P	82.00	pF

Select Soft Start Capacitor (C_{SS})			
Soft Start Time	t_{SS}	**55.00**	**ms**
Calculate Soft Start Capacitor	C_{SS}	**450.82**	**nF**
Closest Standard Capacitor Value	C_{SS}	**470.00**	**nF**
Select Standard Capacitor Value	C_{SS}	**470.00**	**nF**

Setting AB Initial Turn-on Delay (t_{ABSET})			
Calculate 1/4 LC Tank Frequency and set AB Initial Delay	t_{ABSET}	146.97	ns
Enter/Fine Tune t_{ABSET} Based on Valley Switching/ZVS	t_{ABSET}	146.97	ns
Select Standard Resistor for R_{DA1} for t_{ABSET} Delay Range	R_{DA1}	10.00	kΩ
Calculate Voltage at ADEL pin to Meet Delay Range	V_{ADEL}	1.80	V
Calculate R_{DA2}	R_{DA2}	5.63	kΩ
Closest Standard Resistor Value (E48)	R_{DA2}	5.62	kΩ
Select Standard Resistor for R_{DA2} for t_{ABSET} Delay Range	R_{DA2}	5.62	kΩ
Recalculate V_{ADEL} Based on R_{DA1} and R_{DA2} Selection	V_{ADEL}	1.80	V
Calculate AB timing resistor	R_{DELAB}	78.84	kΩ
Closest Standard Resistor Value (E48)	R_{DELAB}	78.70	kΩ
Select Standard Resistor Value (Between 13K and 90K ohm)	R_{DELAB}	26.10	kΩ
Setting CD Initial Turn-on Delay (t_{CDSET})			
Set Initial CD delay to AB Delay $t_{ABSET} = t_{CDSET}$	t_{CDSET}	146.97	ns
Enter/Fine Tune t_{ABSET} Based on Valley Switching/ZVS	t_{CDSET}	146.97	ns
Calculate AB timing resistor	R_{DELCD}	78.84	kΩ
Closest Standard Resistor Value (E48)	R_{DELCD}	78.70	kΩ
Select Standard Resistor Value (Between 13K and 90K ohm)	R_{DELCD}	78.70	kΩ
Setting AF and BE turnoff delay (t_{AFSET}, t_{BESET})			
Set to half of t_{ABSET}	$t_{AFSET} = t_{BESET}$	73.49	ns
Enter/Fine Tune t_{AFSET} and t_{AFSET}	$t_{AFSET} = t_{BESET}$	73.49	ns
Select Standard Resistor for R_{CA1} for t_{AFSET} Delay Range	R_{CA1}	27.80	kΩ
Calculate Voltage at ADELEF pin to Meet Delay Range	V_{ADELEF}	0.20	V

Calculate R_{CA2}	R_{CA2}	1.16	kΩ
Closest Standard Resistor Value (E48)	R_{CA2}	1.15	kΩ
Select Standard Resistor Value	R_{CA2}	1.15	kΩ
Calculate Voltage at ADELEF pin to Meet Delay Range	V_{ADELEF}	0.20	V
Calculate AB timing resistor	R_{DELEF}	33.19	kΩ
Closest Standard Resistor Value (E48)	R_{DELEF}	33.20	kΩ
Select Standard Resistor Value(Between 13K and 90K ohm)	R_{DELEF}	33.20	kΩ
Setting Minimum on Time			
Minimum on Time	t_{MIN}	125.00	ns
Calculate R_{TMIN}	R_{TMIN}	16.67	kΩ
Closest Standard Resistor Value (E48)	R_{TMIN}	16.90	kΩ
Select Standard Resistor Value	R_{TMIN}	16.90	kΩ
Setup PWM Switching Frequency			
Calculate R_T Value	R_T	60.00	kΩ
Closest Standard Resistor Value (E48)	R_T	59.00	kΩ
Select Standard Resistor Value	R_T	59.00	kΩ
Setup Slope Compensation			
Calculate Magnetizing Current during I_{LOUT} down slope	dIL_{MAG}	0.49	A
Calculate V_{SLOPE1}	V_{SLOPE1}	0.04	V/us
Calculate V_{SLOPE2}	V_{SLOPE2}	0.00	V/us
Calculate V_{SLOPE}	V_{SLOPE}	0.04	V/us
Calculate R_{SUM}	R_{SUM}	125.00	kΩ
Closest Standard Resistor Value (E48)	R_{SUM}	127.00	kΩ
Select Standard Resistor Value	R_{SUM}	127.00	kΩ

Setup DCM Comparator			
Voltage across R_S at 15% load	V_{RS}	0.32	V
Select Standard Resistor	R_G	1.00	kΩ
Calculate R_E	R_E	14.47	kΩ
Closest Standard Resistor Value (E48)	R_E	14.70	kΩ
Select Standard Resistor Value	R_E	16.90	kΩ

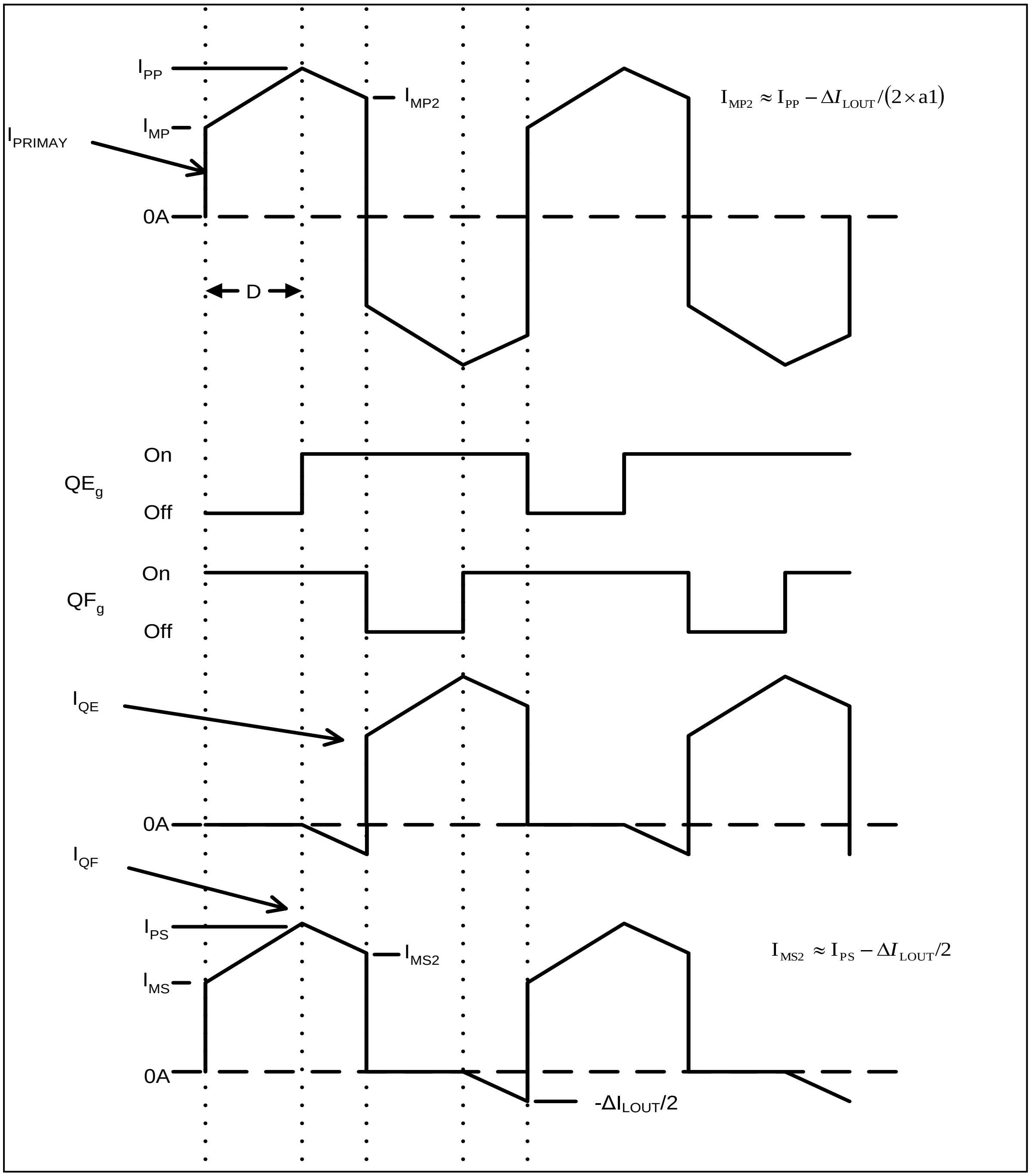
Unit										
V										
V										
V										
W										
kHz										

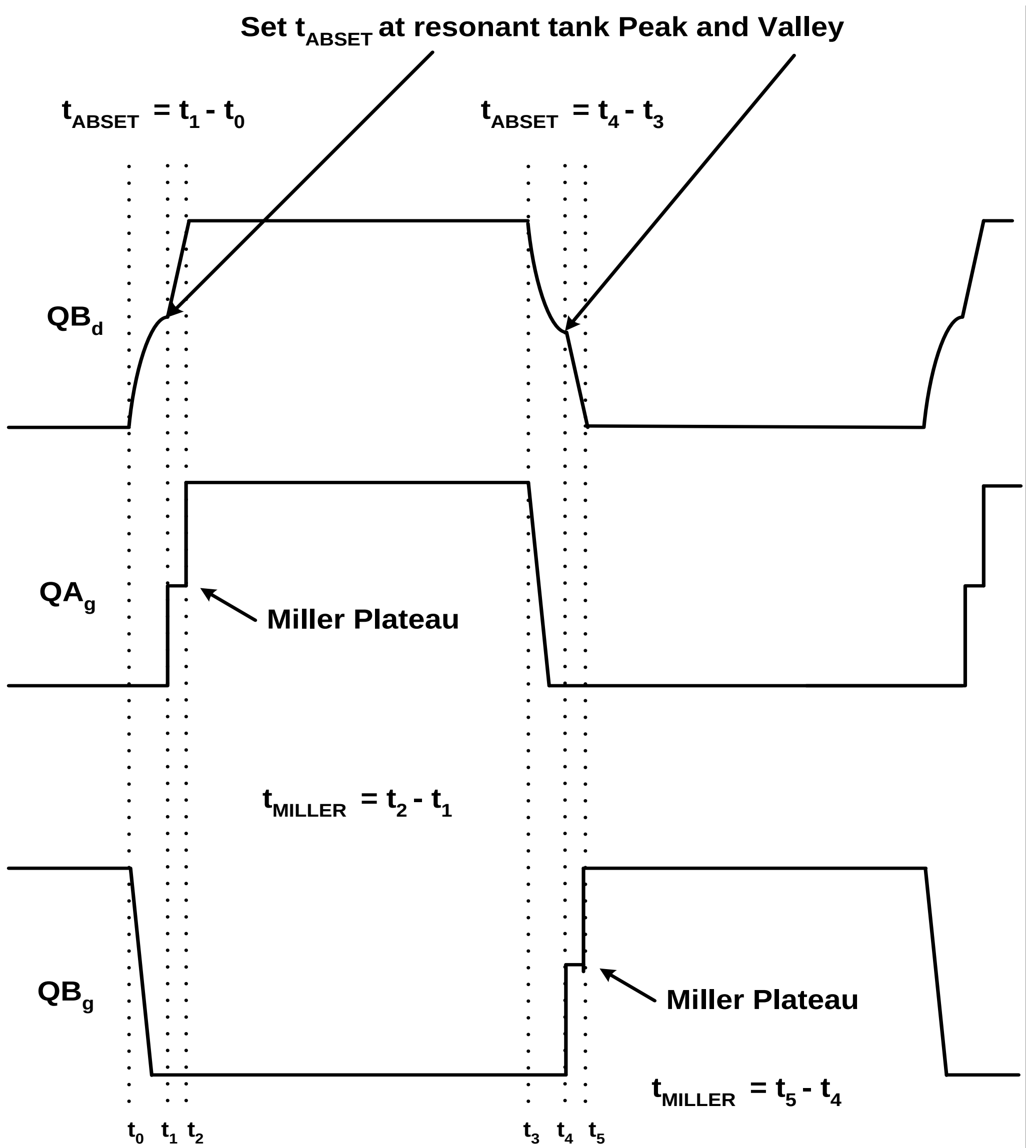
Calculated Ls is Negative and Ls Might Not be Needed, However, Leave a Place Holder for Ls Just in Case										

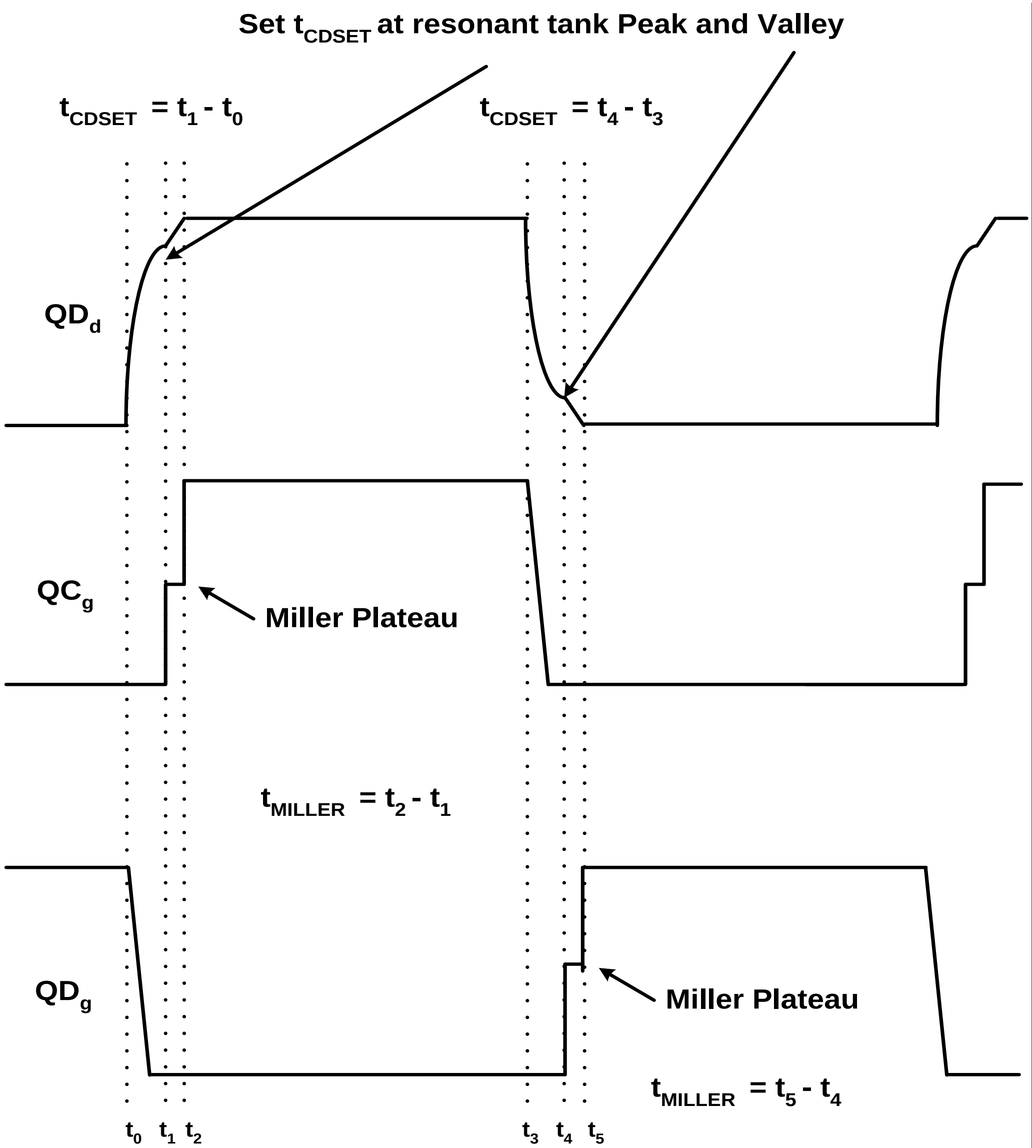
Assumes the centre tapped secondary - as per Functional Schematic										

		7.66								
Non-PFC Cin Capacitance Cannot Be Calculated, Use Other Method										

Figure shows T1 primary current ($I_{PRIMARY}$) and synchronous rectifiers QE (I_{QE}) and QF (I_{QF}) currents with respect to the synchronous rectifier gate drive currents. Note that I_{QE} and I_{QF} are also T1's secondary winding currents as well. Variable D is the converters duty cycle.




Set t_{ABSET} at resonant tank Peak and Valley
$t_{ABSET} = t_1 - t_0$
$t_{ABSET} = t_4 - t_3$
QB_d
QA_g
Miller Plateau
$t_{MILLER} = t_2 - t_1$
QB_g
Miller Plateau
$t_{MILLER} = t_5 - t_4$
t_0 t_1 t_2 t_3 t_4 t_5



Set tCDSET at resonant tank Peak and Valley
tCDSET = t1 - t0
tCDSET = t4 - t3
QDd
QCg
Miller Plateau
tMILLER = t2 - t1
QDg
Miller Plateau
tMILLER = t5 - t4
t0 t1 t2
t3 t4 t5

Compatibility Report for SLUC222D.xls
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