## **Code Details**

Part Number: Gate Driver( UCC587- Q1)

Issue: We are sending the 16-bit commands through the MOSI line of the SPI channel, but we are not receiving any data back from the gate driver.

Clock Frequency: 1MHz

The data is transmitted on the rising edge of the clock.

Chip Select 5 is used for this instance.

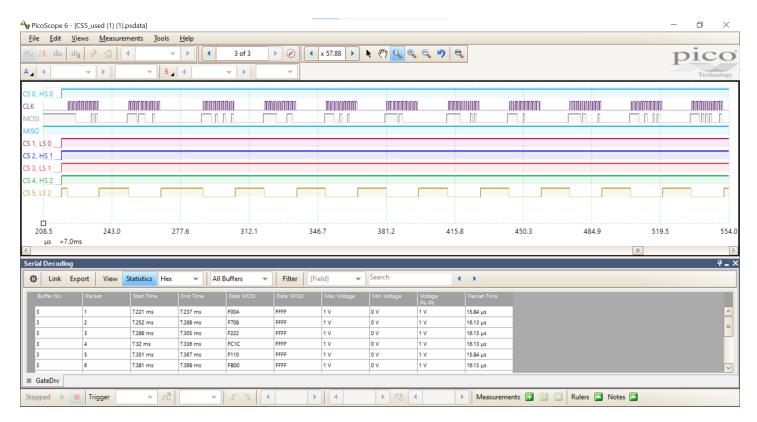


Figure 1

## Code:

We are sending the following commands from MCU and trying to write and read 0x0002 to the gate driver's SPITEST register (Offset = 0x14).

```
All signals broadcasting

*/
UCC5870_DRVDIS (BROADCAST_SIGNAL); // F00A
UCC5870_SWRESET (BROADCAST_SIGNAL); //F708
UCC5870_CFGIN(BROADCAST_SIGNAL); /* to move from cfgl to cfg2 */ // F222
UCC5870_WrReg(BROADCAST_SIGNAL,0x1C,0x1000); //FC1C F110 FB00
UCC5870_SPITEST(BROADCAST_SIGNAL,0x0002); //
```

Figure 2

Figure 3

Figure 4

Figure 5

```
void UCC5870_WrReg(uint16 chipAddress, uint16 regAddress, uint16 data)

{

| Comparison | Compar
```

## Figure 6

```
void UCC5870_setReg (uintl6 chipAddress, uintl6 regAddress) (
                  * add chip address to 12-15 bits
* and '110000' for bits 11-5
79
80
81
82
83
84
85
                   * and regAddress from 0-4 bits
                  Std_ReturnType ReadStatus ;
                   SpiWrite_Data_Buffer[lu] = (uint8)(0x0C + chipAddress);
SpiWrite_Data_Buffer[0u] = (uint8)(0x00 + regAddress);
// SpiWrite_Data_Buffer[0] = ((chipAddress << 12) | (0x0c00 + regAddress));
86
87
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91
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95
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99
100
101
102
                   Spi_SeqResultType setRg_Spi_stat = Spi_GetSequenceResult (SEQ_UCC5870_WRITE_DRV5);
                   if(Spi_stat == SPI_SEQ_OK)
                           /* Prepare for SPI transfer */
ReadStatus = Spi_SetupEB(CH_UCC5870_WRITE_DRV5 , &SpiWrite_Data_Buffer[0u] ,&SpiRead_Data_Buffer[0u] ,DataLengthl);
                           // ReadStatus = Spi_WriteIB (4, &SpiWrite_Data_Buffer[Ou] );
if ( ReadStatus == E OK ) {
                                    * Send data over SPI
                            ReadStatus = Spi_SyncTransmit(SEQ_UCC5870_WRITE_DRV5);
while (Spi_GetStatus() == SPI_BUSY)
                                 Spi MainFunction Handling();
                                 ReadStatus = E_NOT_OK ;
                      else
                           ReadStatus = E NOT OK;
```

Figure 7

Figure 8

```
void UCC5870_WRDHcmd (uintl6 chipAddress, uintl6 data) {
        ₽ /*
             * add chip address to 12-15 bits
124
             * and '1010' for bits 8-11
126
             * and data from 0-7 bits
             Std_ReturnType ReadStatus ;
129
               SpiWrite_Data_Buffer[lu] = (uint8) (0x01 +chipAddress);
               SpiWrite_Data_Buffer[Ou] = (uint8)(0x00 + data);
             // SpiWrite_Data_Buffer[2u] = ((chipAddress << 12) | (0x0a00 + ( data / 256 )));
             Spi_SeqResultType Spi_stat = Spi_GetSequenceResult (SEQ_UCC5870_WRITE_DRV5);
134
             if (Spi_stat == SPI_SEQ_OK)
135
         136
                    /* Prepare for SPI transfer */
                   ReadStatus = Spi_SetupEB(CH_UCC5870_WRITE_DRV5 , &SpiWrite_Data_Buffer[0u] ,&SpiRead_Data_Buffer[0u],DataLengthl);
                   // ReadStatus = Spi_WriteIB (4, &SpiWrite_Data_Buffer[lu] );
                   if ( ReadStatus == E_OK ) {
                        /* Send data over SPI */
140
                       ReadStatus = Spi_SyncTransmit(SEQ_UCC5870_WRITE_DRV5);
141
142
143
                   else {
144
                       ReadStatus = E_NOT_OK ;
145
               else
149
                   ReadStatus = E NOT OK;
150
```

Figure 9

Figure 10

```
117
        void UCC5870_SPITEST( uintl6 chipAddress , uintl6 Data){
118
119
        /* Spi_Init(Spi_Config);
120
          -Std_ReturnType Init_chk = Spi_InitCheck(Spi_Config); */
           //uint16 TEST Reg Addr = ;
123
           UCC5870_WrReg(chipAddress, 0x14, Data);
124
           UCC5870_RdReg(chipAddress, 0x14) ; /* For reading the status reg for cfg mode */
           UCC5870 NOP(BROADCAST SIGNAL);
126
           Spi_stat = Spi_GetSequenceResult( SEQ_UCC5870_READ_DRV5 ) ;
128
```

Figure 11

#define SEQ_UCC58	70_WRITE_DRV5	(14)
#define SEQ UCC58	70 READ DRV5	(17)
#define CH_UCC587(	D_READ_DRV5	(15)
#define CH_UCC587	WRITE DRV5	(9)

Figure 12

#define	BROADCAST_SIGNAL	((uint8)0xF0)
#define	CA0	(0x10)
#define	DataLength1	(1)

Figure 13