I have designed a flyback DC-DC converter with the UCC28700-Q1 recently. It all performs well apart from a problem that was noticed when the outputs were monitored at a reasonably big time scale on the oscilloscope (500us per division). There appears to be a 1.5-2kHz triangular/sawtooth wave on both of the outputs and feedback winding. This introduces further ripple voltage on the original output capacitor ripple voltage, which is undesirable, of course. Moreover, it brings into question the operation of the device as it leaves unanswered questions.

A few examples of the IC operation have been provided below (the green trace in all is the 15Vout):

|  |  |
| --- | --- |
| P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\2kHz Frequency.JPG  Fig.1 – Two outputs at 7.5V and 15V average | P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\Vdd.JPG  Fig.2 –IC supply rail at 12.5V average |
| P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\DRV.JPG  Fig.3 – DRV pulses on MOSFET Gate | P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\Vcs.JPG  Fig.4 – Current Sense voltage |
| P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\Vfb.JPG  Fig.5 – MOSFET Drain-Source voltage | P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 9.12.2015\Very Zoomed in Vfb.JPG  Fig.6 MOSFET Drain-Source voltage prior to FM |

A further interest has been taken in the auxiliary and the voltage sense as they control in CV:

|  |  |
| --- | --- |
| P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 10.12.2015\TEK0075.JPG  Fig.7 – Auxiliary voltage prior to FM | P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 10.12.2015\TEK0077.JPG  Fig.8 – Auxiliary voltage zoomed in |
| P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 10.12.2015\TEK0079.JPG  Fig.9 – Voltage Sense prior to FM | P:\R&T_Programmes\SILOET II P16\WP16.5 Electrical Power Demonstrator\02_Electronics\Design\Sub Circuit Design\DC-DC Converter\Testing 10.12.2015\TEK0086.JPG  Fig.10 – Overview of Voltage Sense |

The IC seems to work on maximum frequency for about 10 cycles so it builds up the outputs then it decides to slow down and skip 8 valleys on average for about 3 to 4 cycles. Afterwards the process repeats. My question is why does it not fix itself at say 2 valleys skipped and 100kHz for a given set line and load conditions? Basically instead of running a marathon it sprints, then slows down and repeats, thus, creating the undesired 2kHz ripple on both outputs that is observed in Fig.1.