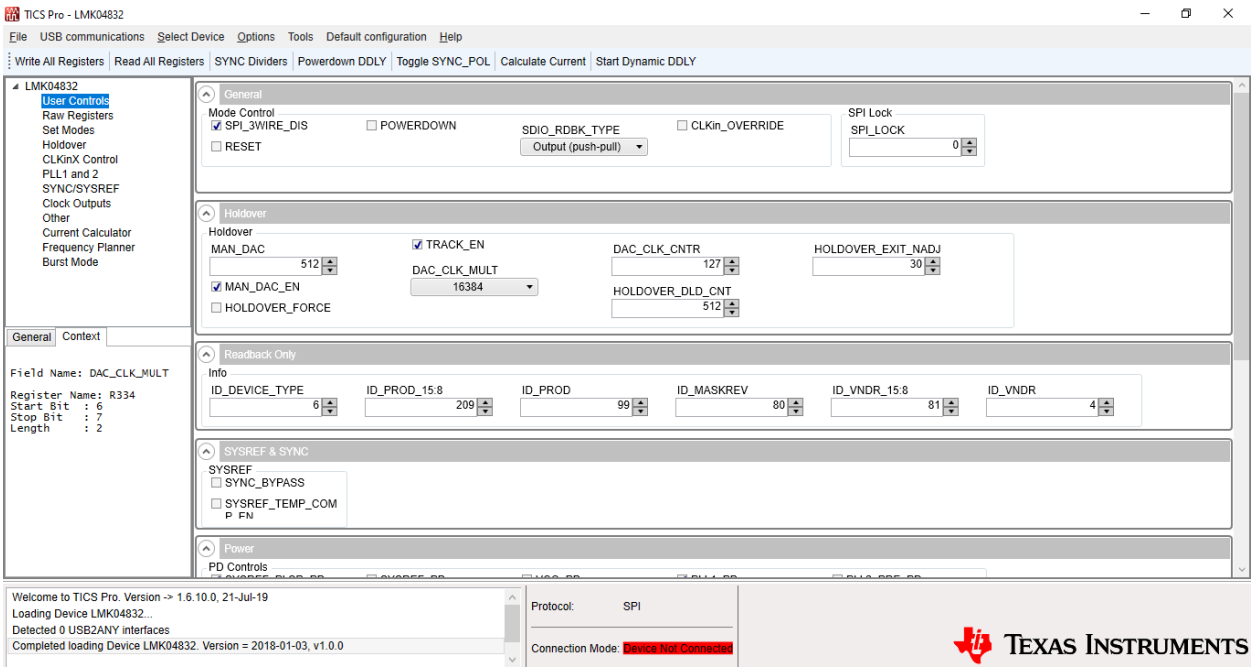
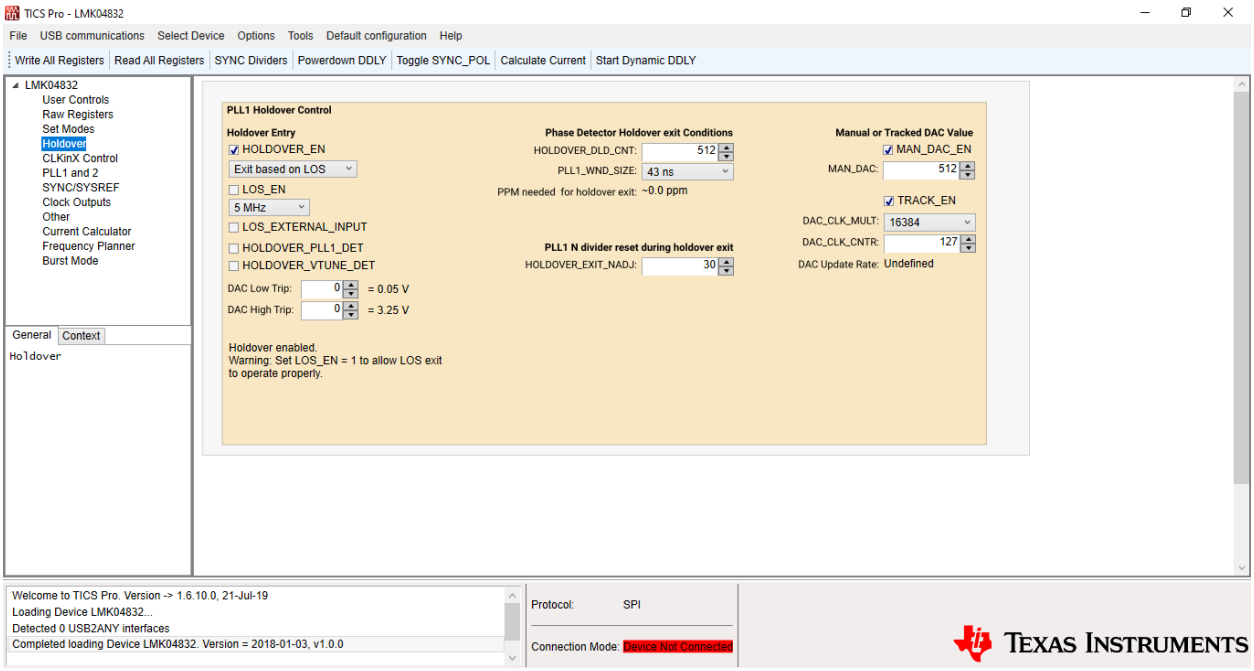
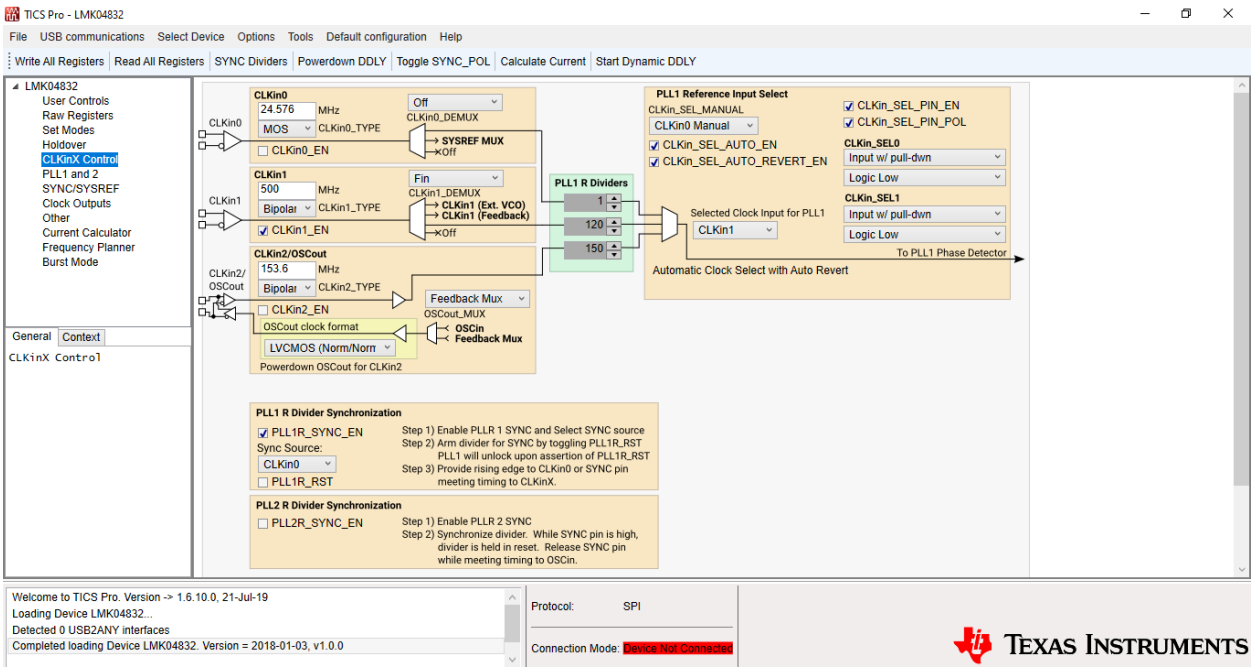
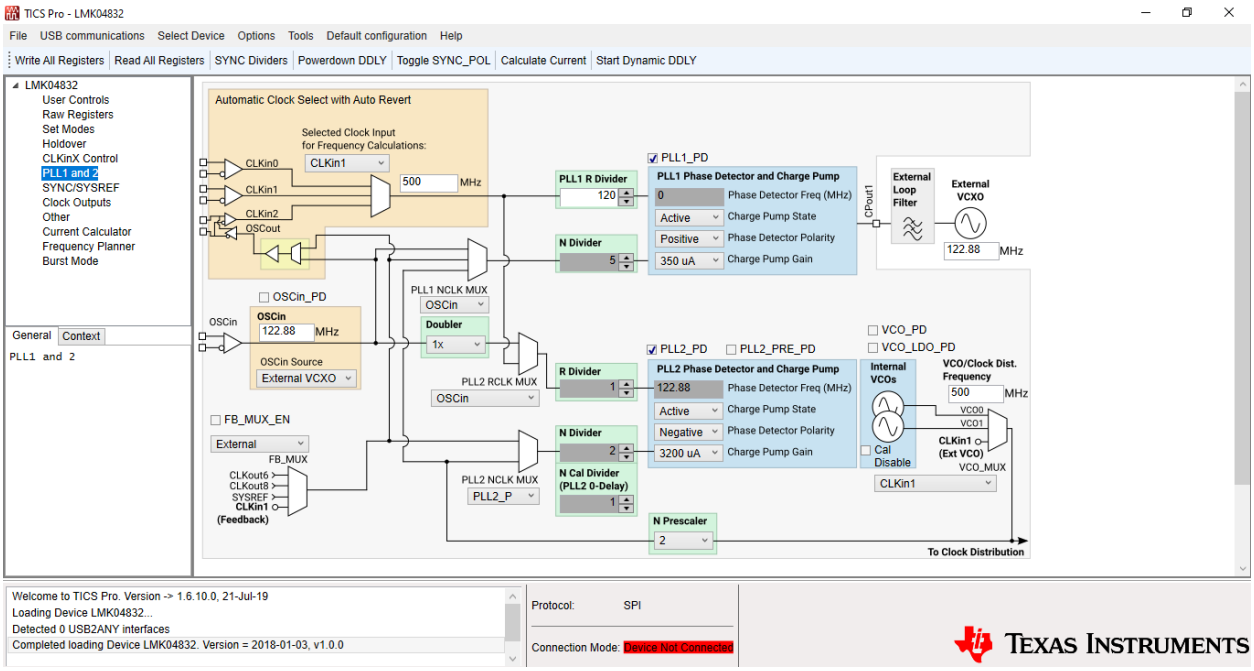
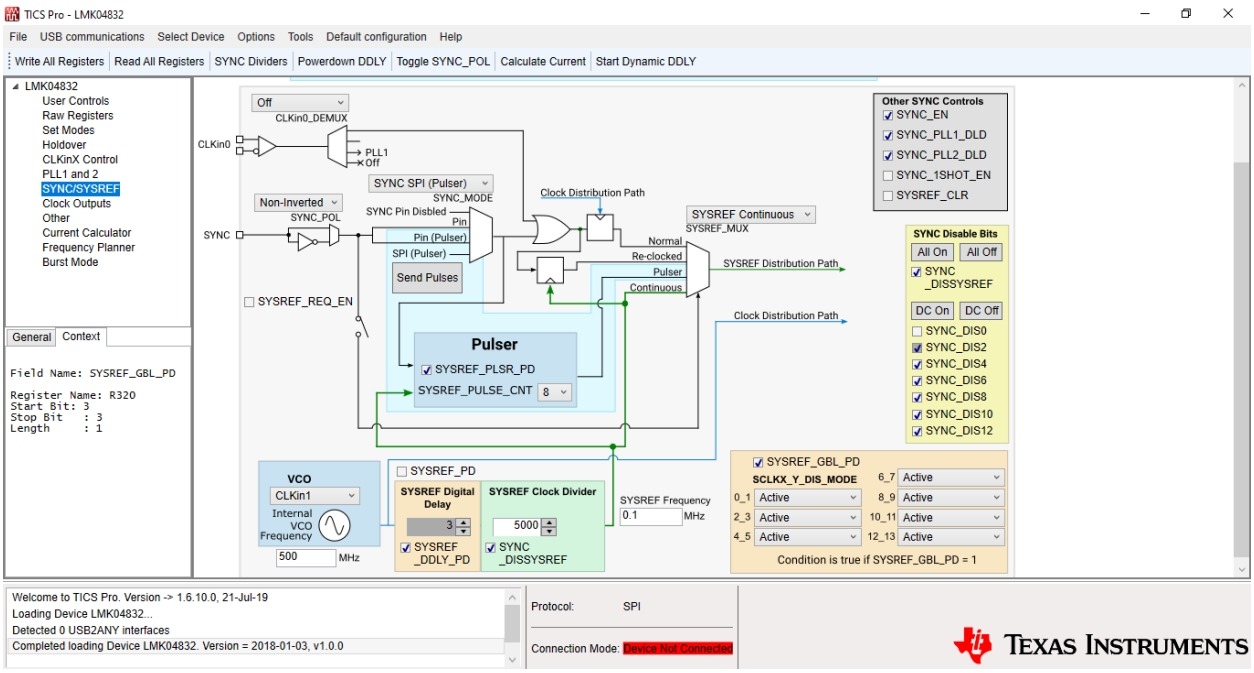
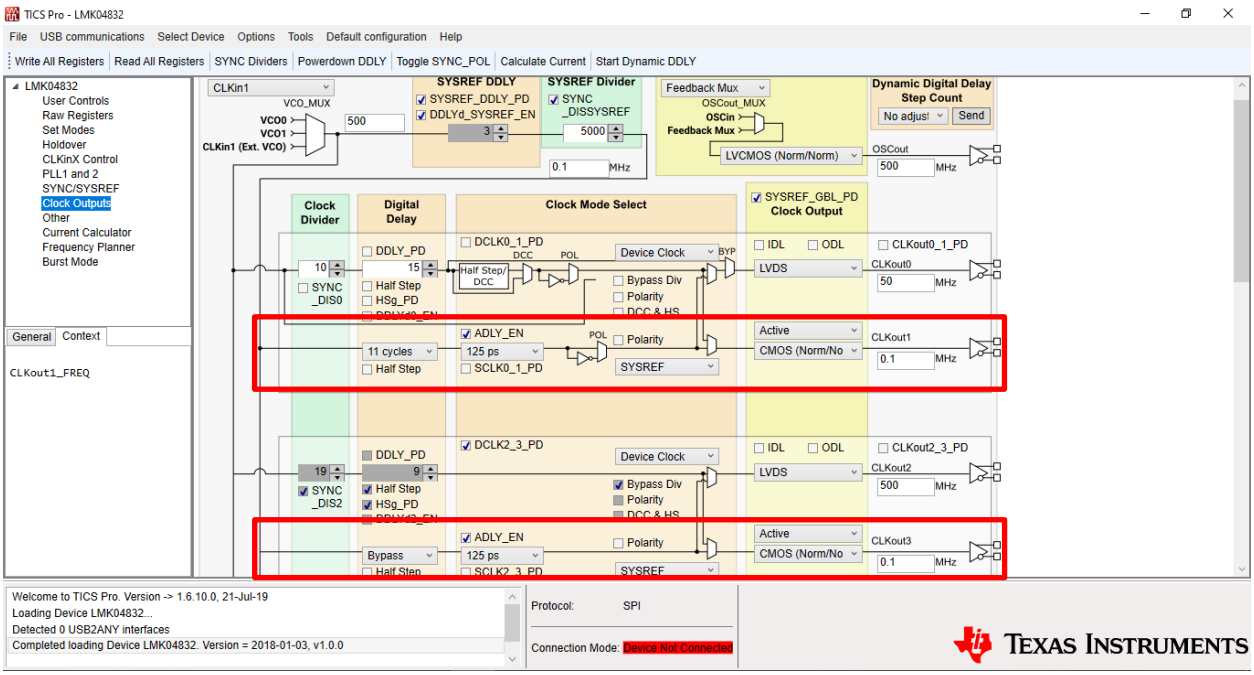

TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General
Mode Control
SPI_3WIRE_DIS
POWERDOWN
SDIO_RDBK_TYPE
Output (push-pull)
CLKin_OVERRIDE
RESET
SPI Lock
SPI_LOCK
Holdover
MAN_DAC
TRACK_EN
DAC_CLK_MULT
DAC_CLK_CNTR
HOLDOVER_EXIT_NADJ
MAN_DAC_EN
HOLDOVER_FORCE
HOLDOVER_DLD_CNT
General Context
Field Name: DAC_CLK_MULT
Register Name: R334
Start Bit : 6
Stop Bit : 7
Length : 2
Readback Only
Info
ID_DEVICE_TYPE
ID_PROD_15:8
ID_PROD
ID_MASKREV
ID_VNDR_15:8
ID_VNDR
SYSREF & SYNC
SYSREF
SYNC_BYPASS
SYSREF_TEMP_COMP_EN
Power
PD Controls
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments

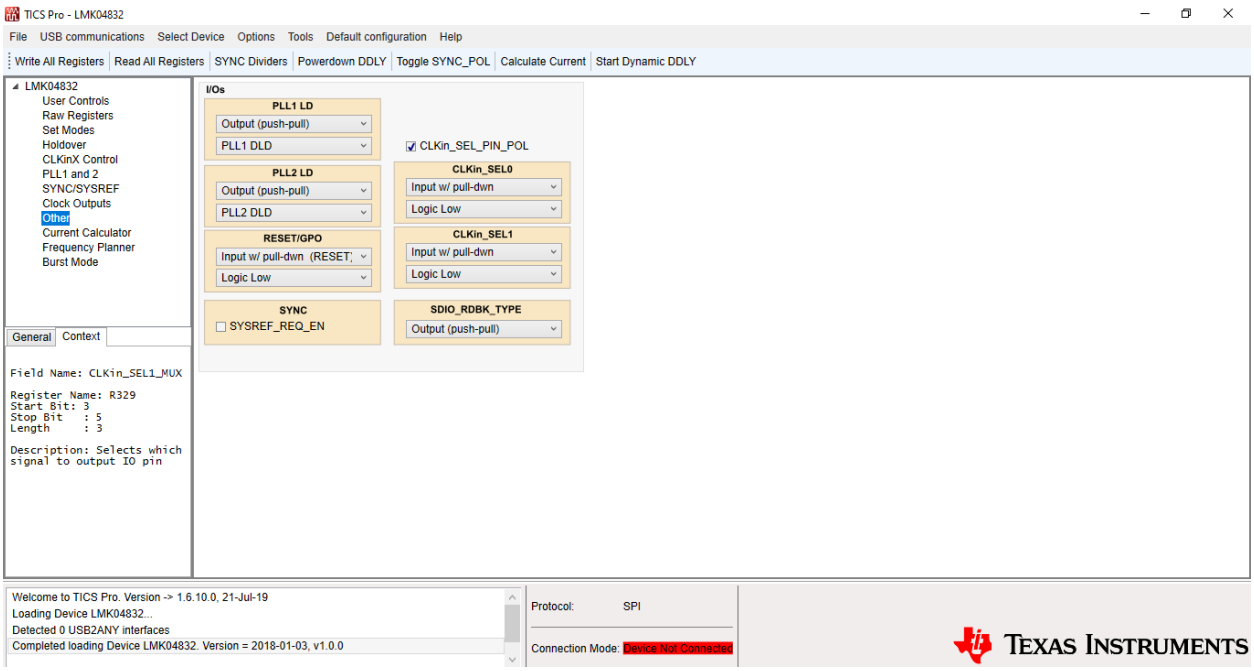

TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
PLL1 Holdover Control
Holdover Entry
HOLDOVER_EN
Exit based on LOS
LOS_EN
5 MHz
LOS_EXTERNAL_INPUT
HOLDOVER_PLL1_DET
HOLDOVER_VTUNE_DET
DAC Low Trip:
= 0.05 V
DAC High Trip:
= 3.25 V
Holdover enabled.
Warning: Set LOS_EN = 1 to allow LOS exit to operate properly.
Phase Detector Holdover exit Conditions
HOLDOVER_DLD_CNT:
PLL1_WND_SIZE:
43 ns
PPM needed for holdover exit:
~0.0 ppm
PLL1 N divider reset during holdover exit
HOLDOVER_EXIT_NADJ:
Manual or Tracked DAC Value
MAN_DAC_EN
MAN_DAC:
TRACK_EN
DAC_CLK_MULT:
16384
DAC_CLK_CNTR:
DAC Update Rate:
Undefined
General Context
Holdover
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments

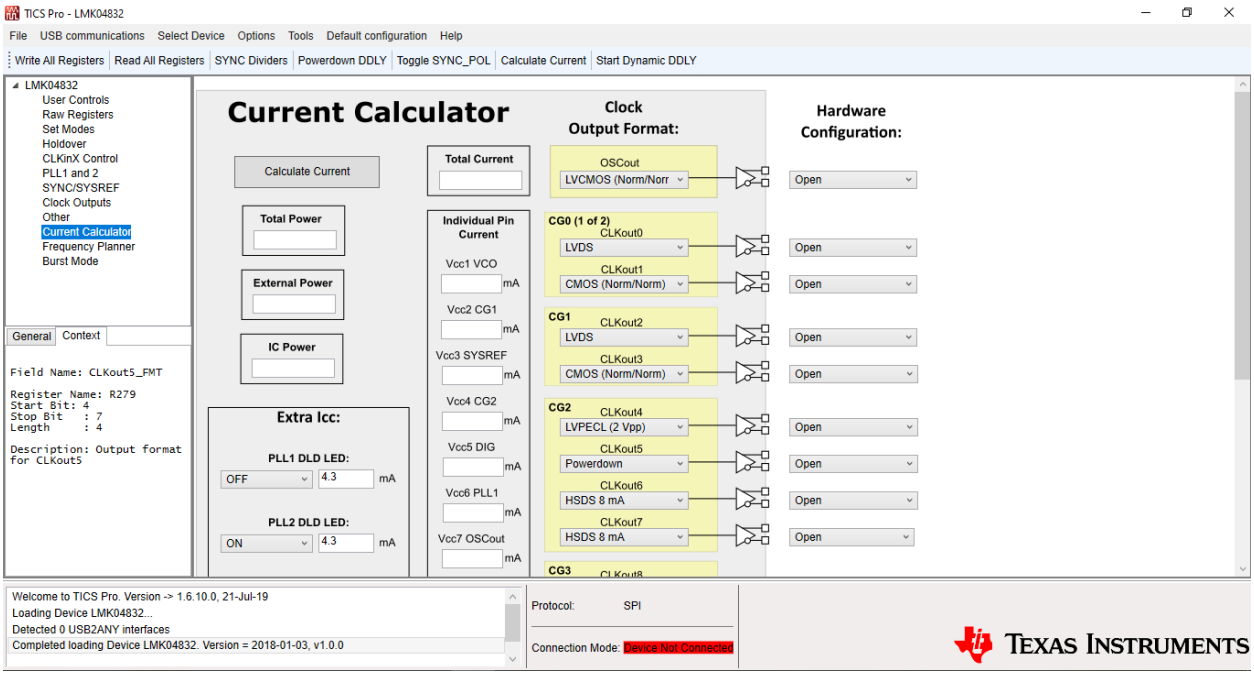

TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
CLKinX Control
CLKin0
24.576 MHz
MOS CLKin0_TYPE
CLKin0_EN
Off
CLKin0_DEMUX
SYSREF MUX
Off
CLKin1
500 MHz
Bipolar CLKin1_TYPE
CLKin1_EN
Fin
CLKin1_DEMUX
CLKin1 (Ext. VCO)
CLKin1 (Feedback)
Off
CLKin2/OSCout
153.6 MHz
Bipolar CLKin2_TYPE
CLKin2_EN
Feedback Mux
OSCout_MUX
OSCout clock format
LVCMOS (Norm/Norm
OSCin Feedback Mux
Powerdown OSCout for CLKin2
PLL1 R Dividers
1
120
150
PLL1 Reference Input Select
CLKin_SEL_MANUAL
CLKin0 Manual
CLKin_SEL_AUTO_EN
CLKin_SEL_AUTO_REVERT_EN
CLKin_SEL_PIN_EN
CLKin_SEL_PIN_POL
CLKin_SEL0
Input w/ pull-dwn
Logic Low
CLKin_SEL1
Input w/ pull-dwn
Logic Low
Selected Clock Input for PLL1
CLKin1
To PLL1 Phase Detector
Automatic Clock Select with Auto Revert
PLL1 R Divider Synchronization
PLL1R_SYNC_EN
Sync Source:
CLKin0
PLL1R_RST
Step 1) Enable PLLR 1 SYNC and Select SYNC source
Step 2) Arm divider for SYNC by toggling PLL1R_RST
PLL1 will unlock upon assertion of PLL1R_RST
Step 3) Provide rising edge to CLKin0 or SYNC pin
meeting timing to CLKinX.
PLL2 R Divider Synchronization
PLL2R_SYNC_EN
Step 1) Enable PLLR 2 SYNC
Step 2) Synchronize divider. While SYNC pin is high,
divider is held in reset. Release SYNC pin
while meeting timing to OSCin.
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
TEXAS INSTRUMENTS

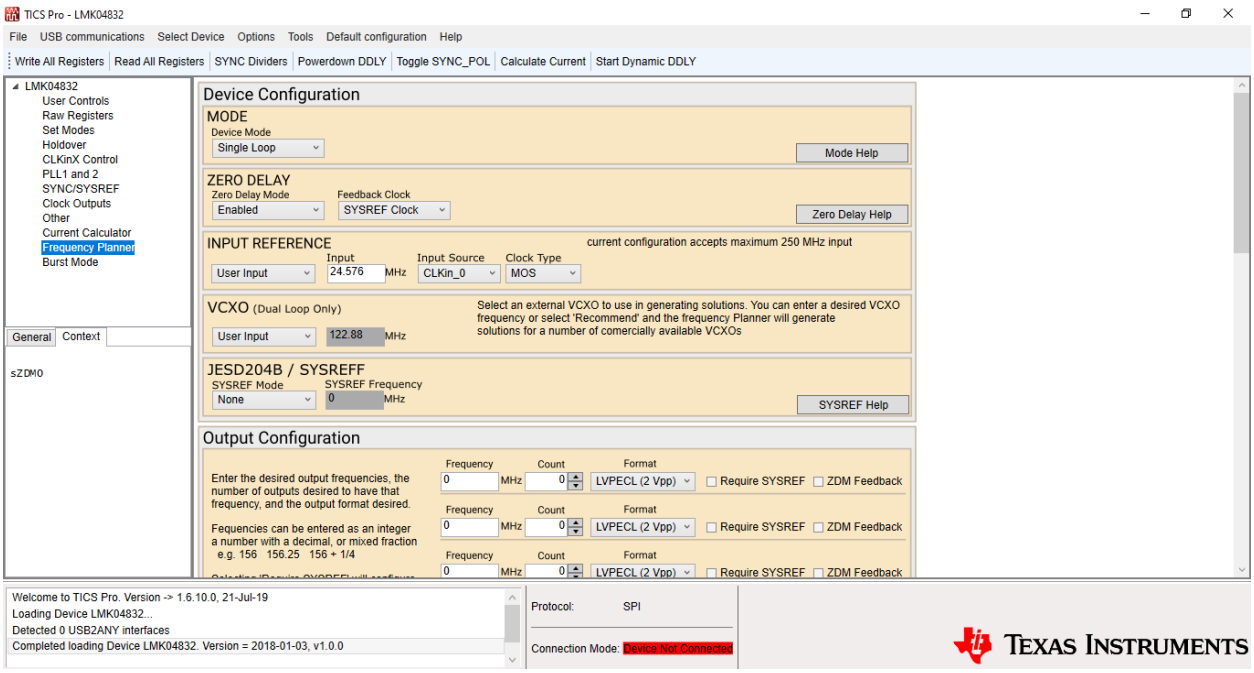

TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
PLL1 and 2
Automatic Clock Select with Auto Revert
Selected Clock Input for Frequency Calculations:
CLKin1
500 MHz
CLKin0
CLKin1
CLKin2
OSCout
OSCin_PD
OSCin
122.88 MHz
OSCin Source
External VCXO
FB_MUX_EN
External
FB_MUX
CLKout6
CLKout8
SYSREF
CLKin1 (Feedback)
PLL1 NCLK MUX
OSCin
Doubler
1x
PLL2 RCLK MUX
OSCin
PLL2 NCLK MUX
PLL2_P
PLL1_PD
PLL1 R Divider
120
N Divider
5
PLL1 Phase Detector and Charge Pump
0 Phase Detector Freq (MHz)
Active Charge Pump State
Positive Phase Detector Polarity
350 uA Charge Pump Gain
CPout1
External Loop Filter
External VCXO
122.88 MHz
PLL2_PD
PLL2_PRE_PD
R Divider
1
N Divider
2
N Cal Divider (PLL2 0-Delay)
1
PLL2 Phase Detector and Charge Pump
122.88 Phase Detector Freq (MHz)
Active Charge Pump State
Negative Phase Detector Polarity
3200 uA Charge Pump Gain
VCO_PD
VCO_LDO_PD
Internal VCOs
Cal Disable
VCO/Clock Dist. Frequency
500 MHz
VCO0
VCO1
CLKin1 (Ext VCO)
VCO_MUX
CLKin1
N Prescaler
2
To Clock Distribution
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
TEXAS INSTRUMENTS

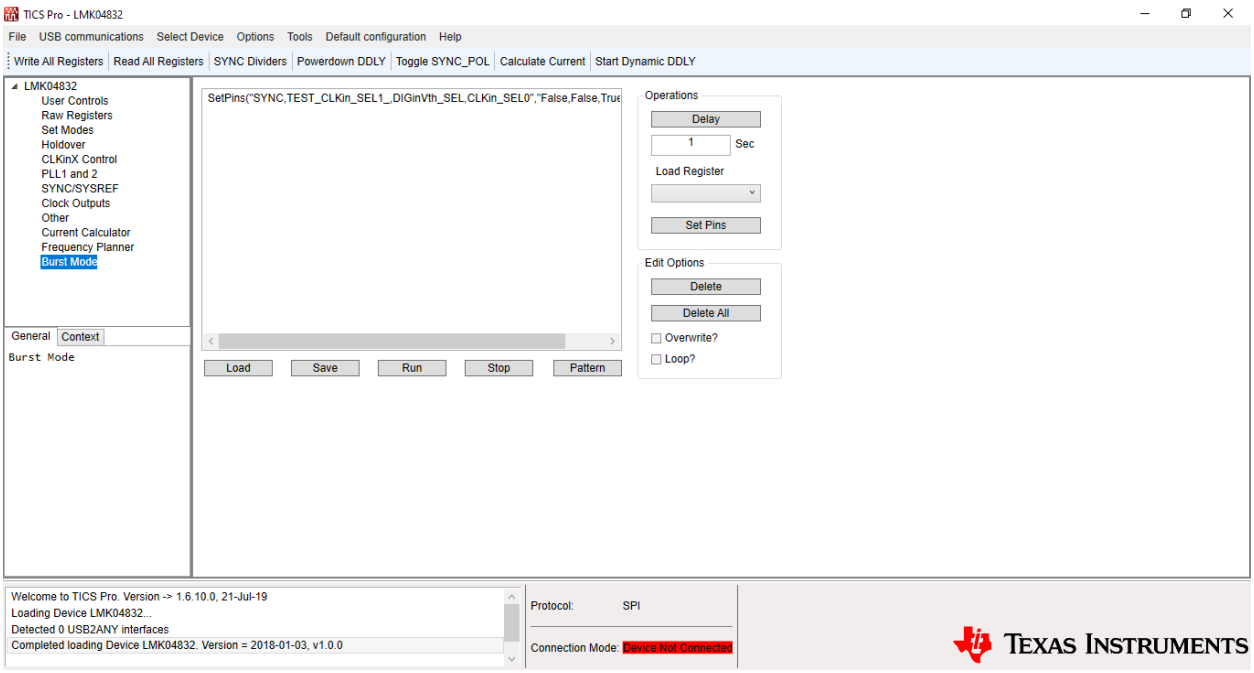

TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
Field Name: SYSREF_GBL_PD
Register Name: R320
Start Bit: 3
Stop Bit : 3
Length : 1
Off
CLKin0_DEMUX
CLKin0
PLL1
Off
SYNC SPI (Pulser)
SYNC_MODE
Non-Inverted
SYNC_POL
SYNC
SYNC Pin Disbled
Pin
Pin (Pulser)
SPI (Pulser)
Send Pulses
SYSREF_REQ_EN
Clock Distribution Path
SYSREF Continuous
SYSREF_MUX
Normal
Re-clocked
Pulser
Continuous
SYSREF Distribution Path
Clock Distribution Path
Pulser
SYSREF_PLSR_PD
SYSREF_PULSE_CNT 8
Other SYNC Controls
SYNC_EN
SYNC_PLL1_DLD
SYNC_PLL2_DLD
SYNC_1SHOT_EN
SYSREF_CLR
SYNC Disable Bits
All On All Off
SYNC _DISSYSREF
DC On DC Off
SYNC_DIS0
SYNC_DIS2
SYNC_DIS4
SYNC_DIS6
SYNC_DIS8
SYNC_DIS10
SYNC_DIS12
VCO
CLKin1
Internal VCO Frequency
500 MHz
SYSREF_PD
SYSREF Digital Delay
3
SYSREF _DDLY_PD
SYSREF Clock Divider
5000
SYNC _DISSYSREF
SYSREF Frequency
0.1 MHz
SYSREF_GBL_PD
SCLKX_Y_DIS_MODE
0_1 Active
2_3 Active
4_5 Active
6_7 Active
8_9 Active
10_11 Active
12_13 Active
Condition is true if SYSREF_GBL_PD = 1
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments


TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
CLKout1_FREQ
CLKin1
VCO_MUX
VCO0
VCO1
CLKin1 (Ext. VCO)
500
SYSREF DDLY
SYSREF_DDLY_PD
DDLYd_SYSREF_EN
3
SYSREF Divider
SYNC _DISSYSREF
5000
0.1 MHz
Feedback Mux
OSCout_MUX
OSCin
Feedback Mux
LVCMOS (Norm/Norm)
Dynamic Digital Delay Step Count
No adjus
Send
OSCout
500 MHz
Clock Divider
Digital Delay
Clock Mode Select
SYSREF_GBL_PD
Clock Output
DCLK0_1_PD
DDLY_PD
10
SYNC _DIS0
15
Half Step
HSg_PD
Half Step/ DCC
DCC
POL
Device Clock
BYP
Bypass Div
Polarity
DCC & HS
IDL
ODL
CLKout0_1_PD
LVDS
CLKout0
50 MHz
ADLY_EN
11 cycles
Half Step
125 ps
SCLK0_1_PD
Polarity
SYSREF
Active
CMOS (Norm/No
CLKout1
0.1 MHz
DCLK2_3_PD
DDLY_PD
19
SYNC _DIS2
9
Half Step
HSg_PD
Device Clock
Bypass Div
Polarity
DCC & HS
IDL
ODL
CLKout2_3_PD
LVDS
CLKout2
500 MHz
ADLY_EN
Bypass
Half Step
125 ps
SCLK2_3_PD
Polarity
SYSREF
Active
CMOS (Norm/No
CLKout3
0.1 MHz
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments


TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
I/Os
PLL1 LD
Output (push-pull)
PLL1 DLD
CLKin_SEL_PIN_POL
PLL2 LD
Output (push-pull)
PLL2 DLD
CLKin_SEL0
Input w/ pull-dwn
Logic Low
RESET/GPO
Input w/ pull-dwn (RESET)
Logic Low
CLKin_SEL1
Input w/ pull-dwn
Logic Low
SYNC
SYSREF_REQ_EN
SDIO_RDBK_TYPE
Output (push-pull)
General Context
Field Name: CLKin_SEL1_MUX
Register Name: R329
Start Bit: 3
Stop Bit : 5
Length : 3
Description: Selects which signal to output IO pin
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments


TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
Current Calculator
Calculate Current
Total Current
Total Power
External Power
IC Power
Extra Icc:
PLL1 DLD LED:
OFF
4.3
mA
PLL2 DLD LED:
ON
4.3
mA
Individual Pin Current
Vcc1 VCO
Vcc2 CG1
Vcc3 SYSREF
Vcc4 CG2
Vcc5 DIG
Vcc6 PLL1
Vcc7 OSCout
Clock Output Format:
OSCout
LVCMOS (Norm/Norr
CG0 (1 of 2)
CLKout0
LVDS
CLKout1
CMOS (Norm/Norm)
CG1
CLKout2
LVDS
CLKout3
CMOS (Norm/Norm)
CG2
CLKout4
LVPECL (2 Vpp)
CLKout5
Powerdown
CLKout6
HSDS 8 mA
CLKout7
HSDS 8 mA
CG3
Hardware Configuration:
Open
General Context
Field Name: CLKout5_FMT
Register Name: R279
Start Bit: 4
Stop Bit : 7
Length : 4
Description: Output format for CLKout5
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments


TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
sZDM0
Device Configuration
MODE
Device Mode
Single Loop
Mode Help
ZERO DELAY
Zero Delay Mode
Enabled
Feedback Clock
SYSREF Clock
Zero Delay Help
INPUT REFERENCE
current configuration accepts maximum 250 MHz input
Input
Input Source
Clock Type
User Input
24.576
MHz
CLKin_0
MOS
VCXO (Dual Loop Only)
Select an external VCXO to use in generating solutions. You can enter a desired VCXO frequency or select 'Recommend' and the frequency Planner will generate solutions for a number of comercially available VCXOs
User Input
122.88
MHz
JESD204B / SYSREFF
SYSREF Mode
SYSREF Frequency
None
0
MHz
SYSREF Help
Output Configuration
Enter the desired output frequencies, the number of outputs desired to have that frequency, and the output format desired.
Fequencies can be entered as an integer a number with a decimal, or mixed fraction
e.g. 156 156.25 156 + 1/4
Frequency
Count
Format
LVPECL (2 Vpp)
Require SYSREF
ZDM Feedback
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments


TICS Pro - LMK04832
File USB communications Select Device Options Tools Default configuration Help
Write All Registers Read All Registers SYNC Dividers Powerdown DDLY Toggle SYNC_POL Calculate Current Start Dynamic DDLY
LMK04832
User Controls
Raw Registers
Set Modes
Holdover
CLKinX Control
PLL1 and 2
SYNC/SYSREF
Clock Outputs
Other
Current Calculator
Frequency Planner
Burst Mode
General Context
Burst Mode
SetPins("SYNC,TEST_CLKin_SEL1_,DIGinVth_SEL,CLKin_SEL0","False,False,True
Operations
Delay
1
Sec
Load Register
Set Pins
Edit Options
Delete
Delete All
Overwrite?
Loop?
Load
Save
Run
Stop
Pattern
Welcome to TICS Pro. Version -> 1.6.10.0, 21-Jul-19
Loading Device LMK04832...
Detected 0 USB2ANY interfaces
Completed loading Device LMK04832. Version = 2018-01-03, v1.0.0
Protocol: SPI
Connection Mode: Device Not Connected
Texas Instruments