Time at which the falling bulk cap voltage equals the rectified line votlage at the overload power threshold.	Applies to UCC28630 only	ωt2_pol	7.57	ms		
Minimum bulk voltage at P_{OL}		Vbulkmin_OL	76.89	V	Ok	If this cell is Red, the bulk capacitance is too low to supply the speicifed overload power
Time at which the falling bulk cap voltage equals the rectified line votlage at the maximum power.		ωt2_surge	7.52	ms		
Minimum bulk voltage when load is stepped from Pnominal to Pmax for time Tmax		Vbulkmin_surge	75.43	V	Ok	If this cell is Red, the bulk voltage is too low to keep the output voltage in constant voltage regulation, the output will be in constant current regulation. Note that when Vbulk < Vbulkmin_nom the output may enter constant current regulation depending on the load power. This calculation assumes that the max load is applied at the peak of line. To calculate the Vbulkmin_surge when the max load is applied at an arbitrary phase angle, please use the accompaying mathcad design file.
Parameter Entry						
Boundary mode Vbulk voltage @ Pnom		$V_{boundary}$ (=Vbulkmin_nom by default, enter an override value in cell D33 if desired)		81.27 V		This is the voltage at which the unit operates in boundary mode. The inductance calculation is based on this voltage. By default this is equal to Vbulkmin_nom on line 27. For more continuous operation, increase this voltage
Target Vdd Voltage		Vdd	18	V		
Bias Diode Forward Voltage Drop		Vbias_diode	0.7	V		
Output Capacitor		Cout	1300	uF		
Secondary Side Reflected Voltage		$V_{reflected}$	95	V		- Recommended reflected output voltage = 120V, reflected output voltages of ~140V < Vreflected < 115V may result in the design violating inductance to current sense resistance ratios required. In this case the inductance and or current sense resistance may have to be manually adjusted in the User Override column provided below. Increasing the boundary mode point will allow a greater range of reflected voltage.
Output Rectifier Forward Voltage Drop		V_{rect}	0.45	V		
Rectifier Derating		$V_{Rect\_Derating}$	85%	%		
Transformer Core Maximum Flux density		Bpk	325	mT		
Transformer Core Cross Sectional area		Ae	96.6	mm^2		
Secondary to Bias Leakage inductance (as a percentage of the secondary inductance)		$\%L_{lk\_sb}$	6%	%		Approximate value on EVM transformer.
MosFET total Gate Charge		Qg_tot	30	nC		
LED Diode Drop			1.8	V		
Input X-capacitor value		$C_{X\text{-}cap}$	330	nF		
Component and paramter calculation						
			Suggested	User Override	Used	Units
Target Turns Ratio		N	3.89		3.89	
Primary Inductance (for boundary mode operation at Vbulkmin_nom)		Lmag	309		220	uH
Current Sense Resistance calculation (for boundary mode operation at Vbulkmin_nom)			229	200	200	mΩ
Standard E24 E-series value for Rcs		Rcs	200.00		200	mΩ
Maximum Primary Current		Ipk_max	4.00		4.00	A
Number of Primary Turns		Npri	28		34	
Number of Secondary Turns		Nsec	7		9	
Number of Bias Turns		Nbias	7		7	
Transformer Al		Al	190		190	nH
Rectifier Reverse Voltage Rating		V_{Rect_Rating}	145		145	V
Vdd Capacitor Calculation (Minimum)			17		17	uF
Next Highest Standard E-series value for CVdd (E6)		C_{VDD}	22		22	uF
Startup Delay		Tstart_delay	1027		1027	ms
Ra Calculation			39.54		39.54	kΩ
Standard E-series value for Ra (E96)		Ra	39.20		39.20	kΩ
Rb Calculation		Rb	28.28		28.28	kΩ
R_{TH} Value		Rth	16.43		16.43	kΩ
Minimum load power to maintain regulation			16.27		16.27	mW
Maximum load resistance to maintain regultaion			16.37		16.37	kΩ
Next lowest standard E-series value for $R_{preload}$		$R_{preload}$	16.00		16.00	kΩ
Output Constant Current Limit (default 100% value)	Applies to UCC28630 only	I_{out_limit}	5.16		5.16	A
Output Capacitor Ripple Current @ Pnom		$I_{ripple(nom)}$	4.39		4.39	A
Maximum X-capacitance value that cap be discharged using the current value of CVdd	Applies to UCC28630 & UCC28633 only	Xcap_max	454		454	nF
$R_{TH} = \frac{R_A \times R_B}{R_A + R_B}$ $10\ k\Omega < R_{TH} < 20\ k\Omega$			Ok			Is the thevenin equivalent resistance of the Ra,Rb resistor divider between 10kΩ and 20kΩ. ***If Rth is outside this range it will trigger a pin fault on startup and the IC will not start!!!***
$C_{VDD} \geq C_X \times \left(\frac{V_{AC(pk)} - V_{SELV}}{V_{DD(start\_min)} - V_{DD(reset\_max)}} \right)$	Applies to UCC28630 & UCC28633 only		Ok			Is the Vdd capacitor large enough to discharge the X-cap beow the SELV voltage level of 60V, without it's voltage rising about the IC start threshold.
$C_{BULK} \leq \frac{2\left(\frac{P_{NOM} \times P_{LL\%}}{\eta}\right) \times t_{XCAP(dis)}}{\left(V_{AC(pk)}{}^2 - V_{SELV}{}^2\right)}$	Applies to UCC28630 & UCC28633 only		Ok			Is the bulk capacitor below the level at which it will discharge the X-cap to the SELV level in 1 second when the power is above the threshold at which X-cap discharge is disabled.
$\frac{R_{CS}}{L_{PRI}} \leq \frac{V_{CS(min)}}{t_{OUT(smp)}} \times \frac{N_S}{N_P} \times \frac{1}{(V_{OUT} + V_{RECT})}$			True			Does the Rcs, Lpri ratio satisfy the Volt second contraint required for output sampling
$\frac{R_{CS}}{L_{PRI}} \leq \frac{1}{V_{IN(pk\_max)}} \times \frac{V_{CS(min)}}{t_{ON(min)}}$			FALSE, Increase Lpri or reduce Rcs			Does the Rcs, Lpri ratio satisfy the Volt second contraint required for tonmin