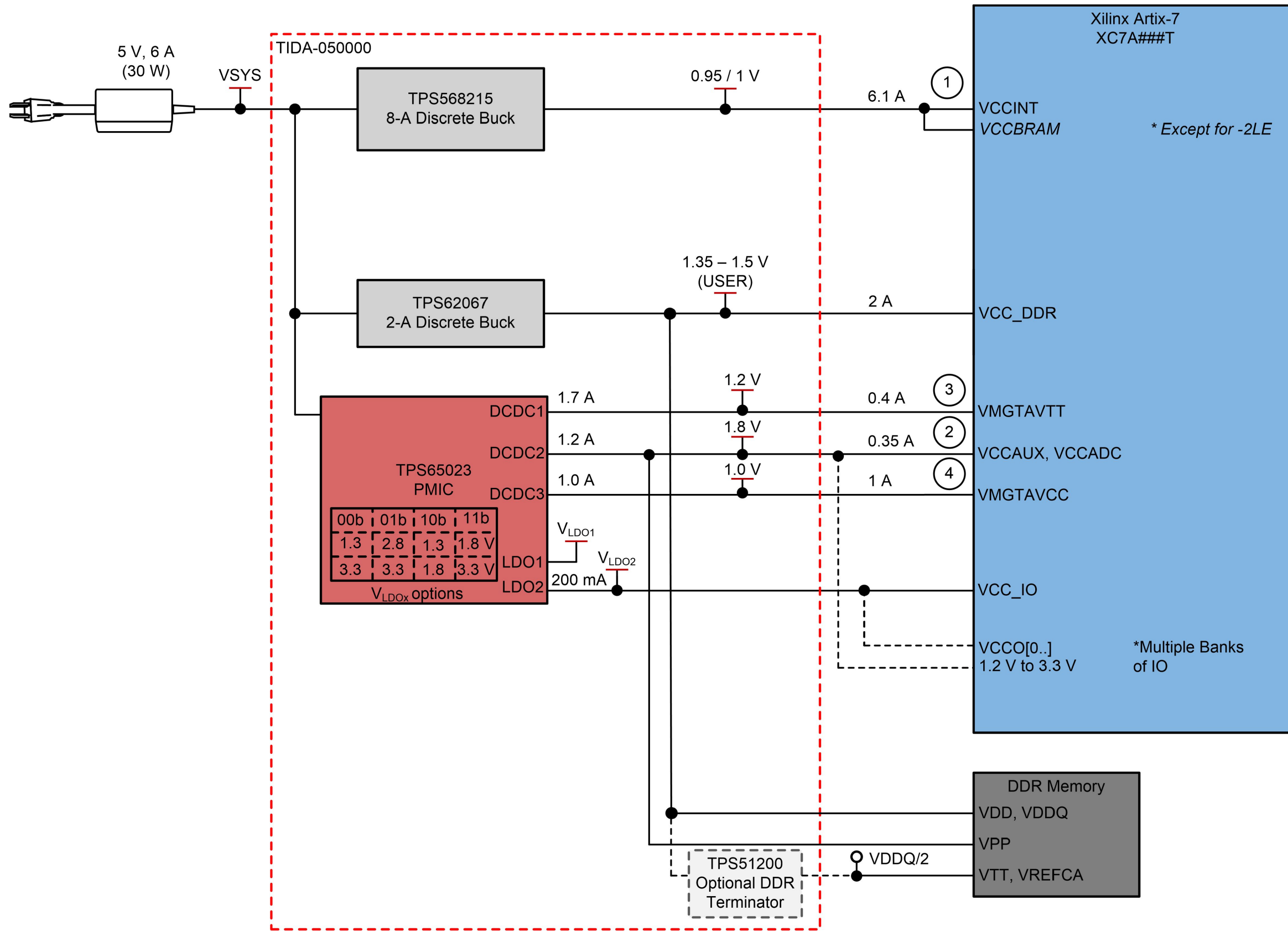


Variant 006 (Artix-7) shown. For block diagrams of other Variants, refer to the TIDA-050000 Design Guide (TIDUE63)

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	2017-11-14	Brian Berner	1st Build
E2	N/A	2017-12-06	Brian Berner	1st Web Release



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TID #: TIDA-050000	Project Title: Xilinx-A7-S7-Z7k Scalable PMIC Power Design	
Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 1 of 7
Drawn By:	File: TIDA050000_pg1_Cover.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	



IOs_and_LEDs
TIDA01480_pg6_MiscSignals.SchDoc

Discrete_Rails
TIDA01480_pg4_DscrRls.SchDoc

Connector_to_FPGA
TIDA01480_pg5_OutPwrRails.SchDoc

PMICs
TIDA01480_pg3_Main.SchDoc

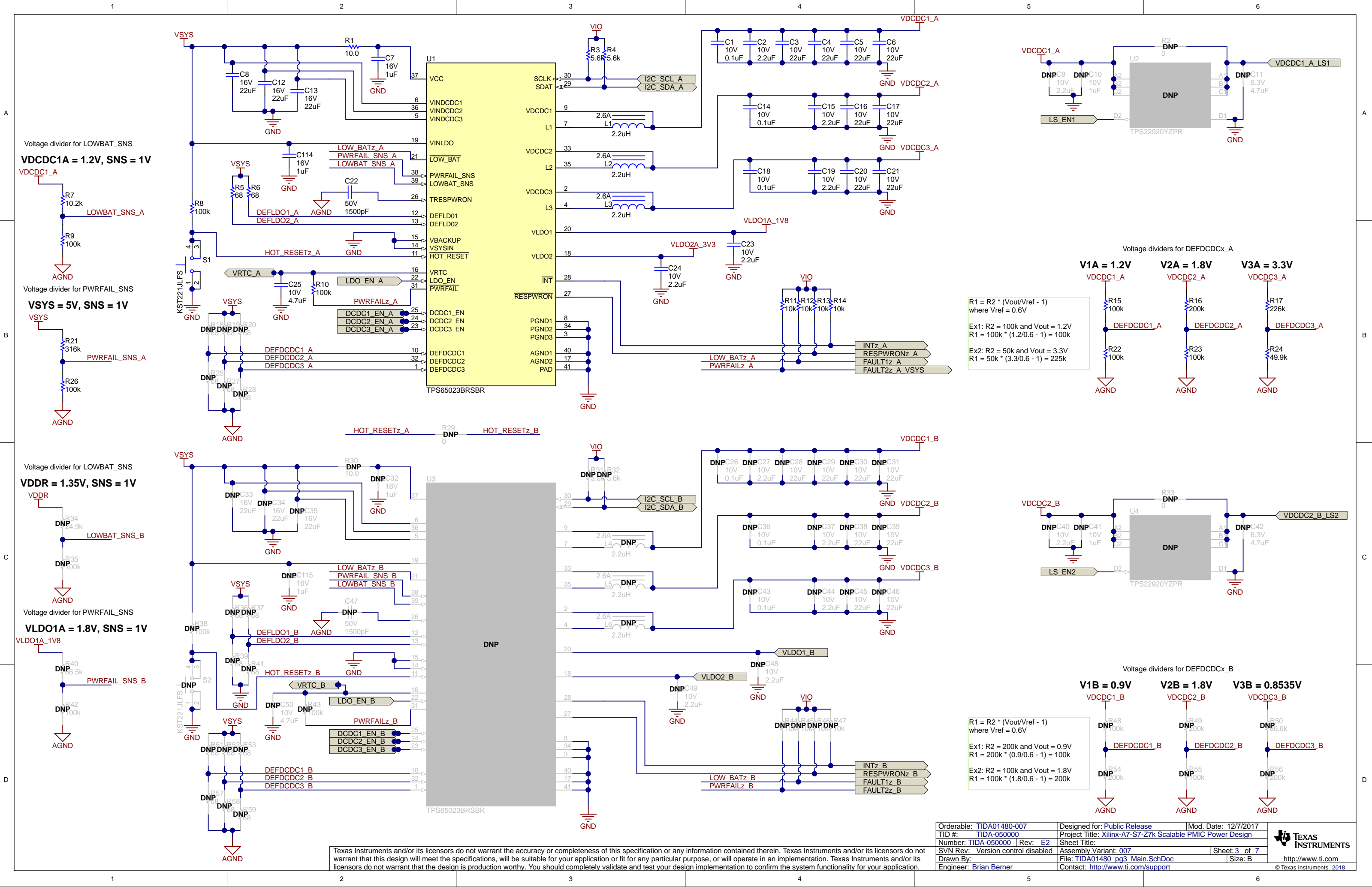
CoverSheet_Drawing
TIDA050000_pg1_Cover.SchDoc

Hardware
TIDA01480_pg7_Hardware.SchDoc

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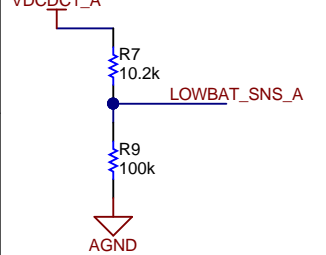
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Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 2 of 7
Drawn By:	File: TIDA050000_pg2_TopLvl.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	





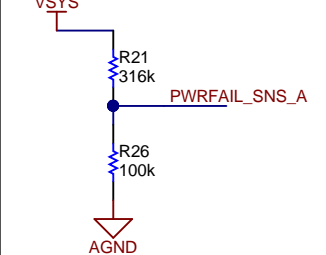
Voltage divider for LOWBAT_SNS

VDCDC1A = 1.2V, SNS = 1V



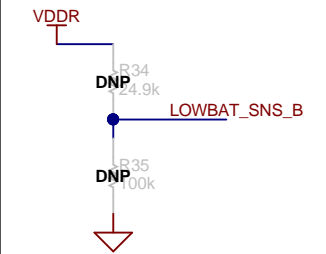
Voltage divider for PWRFAIL_SNS

VSYS = 5V, SNS = 1V



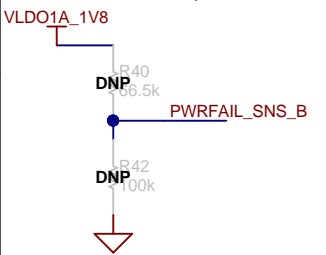
Voltage divider for LOWBAT_SNS

VDDR = 1.35V, SNS = 1V



Voltage divider for PWRFAIL_SNS

VLDO1A = 1.8V, SNS = 1V



$R1 = R2 * (Vout/Vref - 1)$
where $Vref = 0.6V$

Ex1: $R2 = 100k$ and $Vout = 1.2V$
 $R1 = 100k * (1.2/0.6 - 1) = 100k$

Ex2: $R2 = 50k$ and $Vout = 3.3V$
 $R1 = 50k * (3.3/0.6 - 1) = 225k$

$R1 = R2 * (Vout/Vref - 1)$
where $Vref = 0.6V$

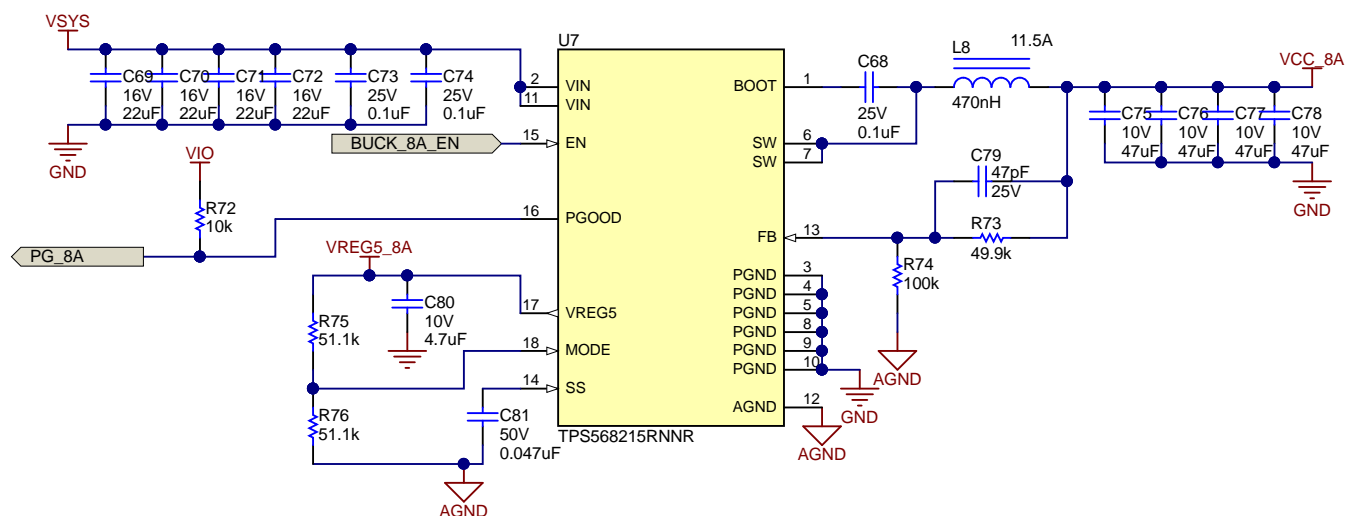
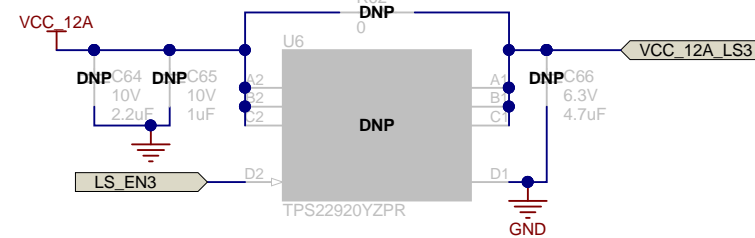
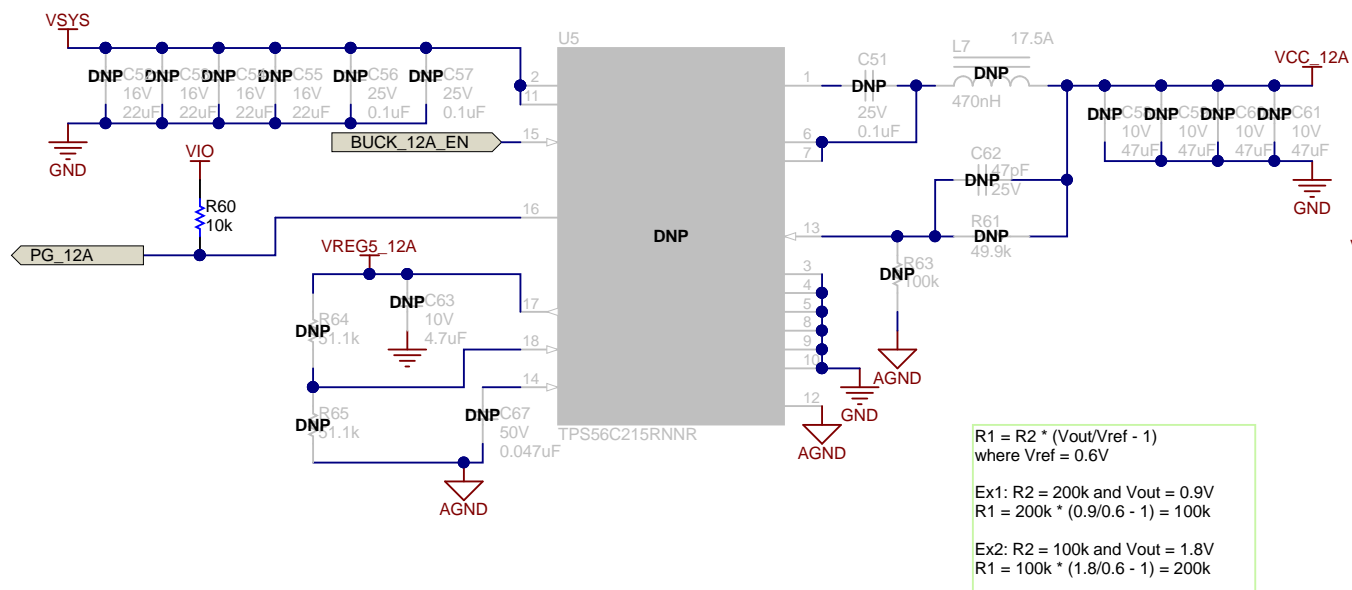
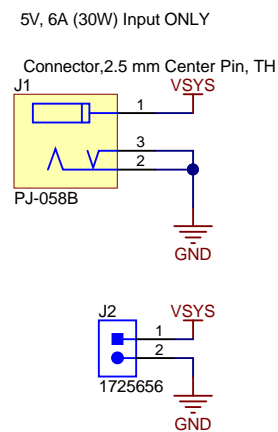
Ex1: $R2 = 200k$ and $Vout = 0.9V$
 $R1 = 200k * (0.9/0.6 - 1) = 100k$

Ex2: $R2 = 100k$ and $Vout = 1.8V$
 $R1 = 100k * (1.8/0.6 - 1) = 200k$

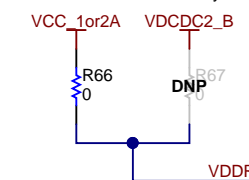
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Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 3 of 7
Drawn By:	File: TIDA01480_pg3_Main.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	

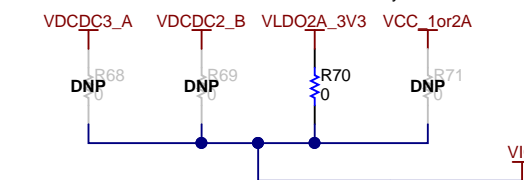




Connected to Discrete TPS62067 by default

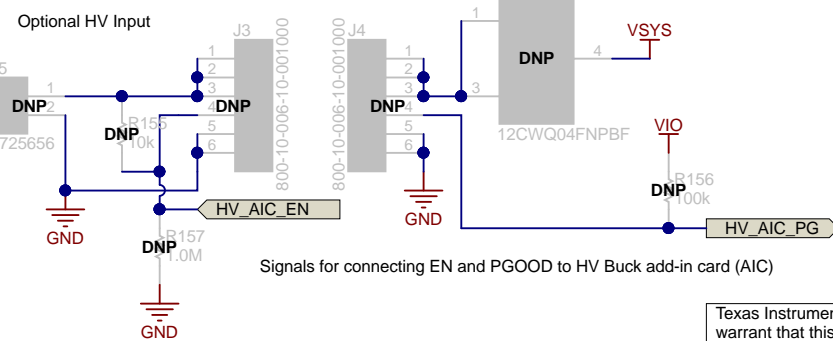
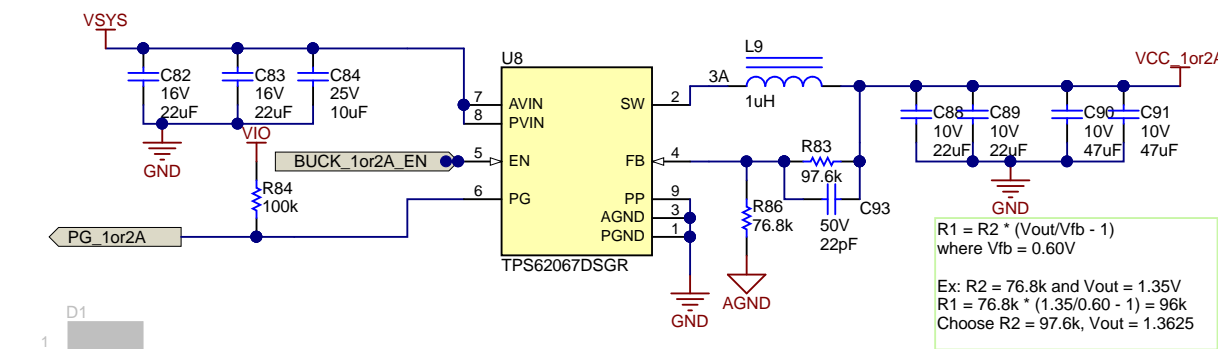
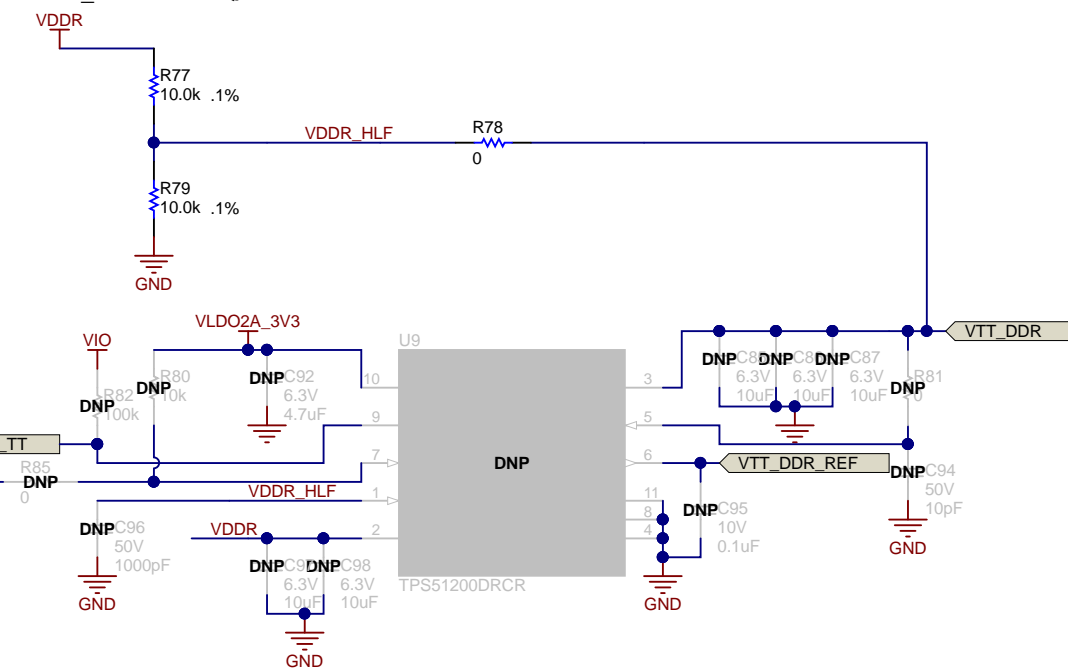


Connected to LDO2A of TPS65023 fixed at 3.3V by default



Voltage divider for DDR Ref (VDDQ/2)

VDDR_REF = VDDQ/2



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Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 4 of 7
Drawn By:	File: TIDA01480_pg4_DscrRIs.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	

A

B

C

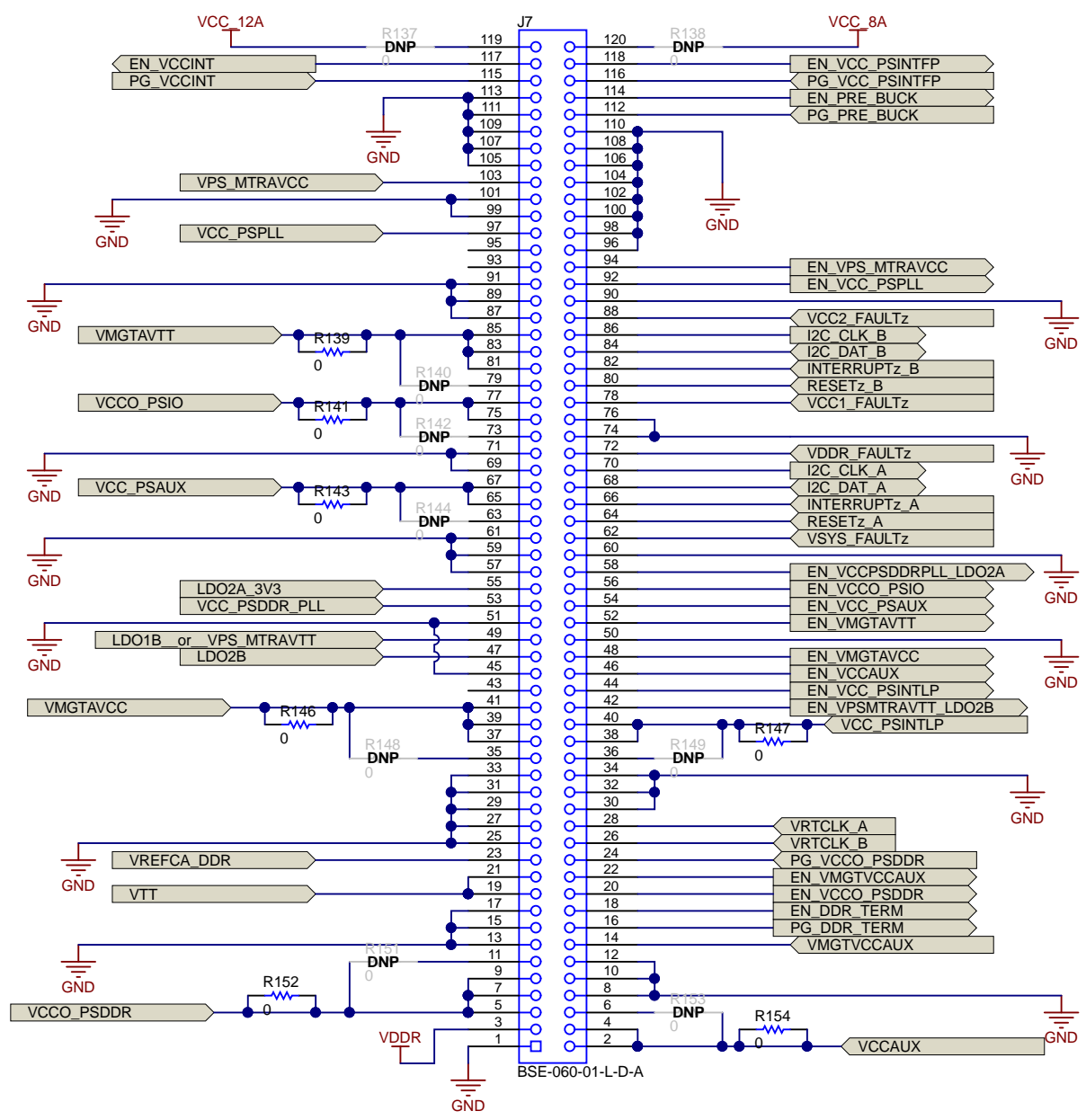
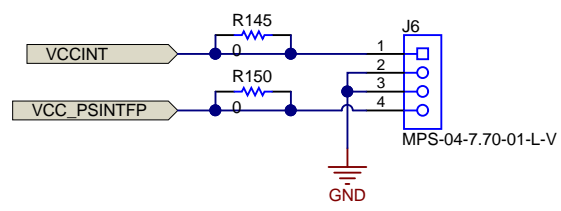
D

A

B

C

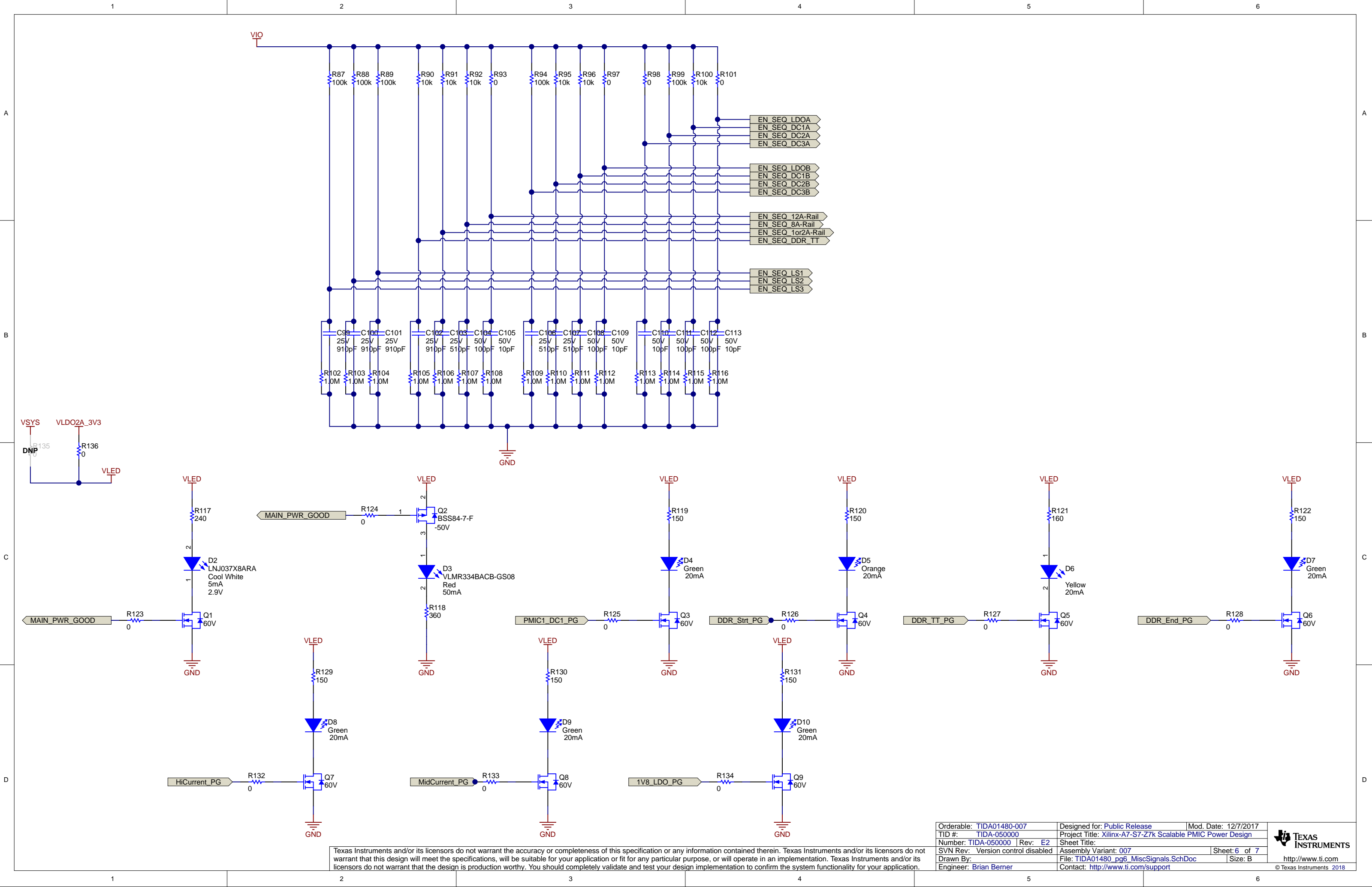
D



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Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 5 of 7
Drawn By:	File: TIDA01480_pg5_OutPwrRails.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	



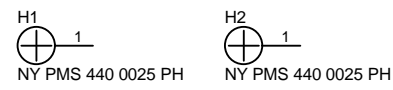


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Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 6 of 7
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PCB Number: TIDA-050000
PCB Rev: E2

PCB LOGO

PCB LOGO

PCB LOGO

Variant/Label Table	
Variant	Description
001	Zynq ZU2CG-ZU5EV Variant 001
002	Zynq ZU2CG-ZU5EV Variant 002
003	Zynq ZU2CG-ZU5EV Variant 003
004	Zynq ZU2CG-ZU5EV Variant 004
005	Zynq ZU2CG-ZU5EV Variant 005
006	Artix-7 FPGA

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

*NOTE: Physical label not on PCB. For documentation purposes only

ZZ2
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ3
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ4
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

Orderable: TIDA01480-007	Designed for: Public Release	Mod. Date: 12/7/2017
TID #: TIDA-050000	Project Title: Xilinx-A7-S7-Z7k Scalable PMIC Power Design	
Number: TIDA-050000	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 007	Sheet: 7 of 7
Drawn By:	File: TIDA01480_pg7_Hardware.SchDoc	Size: B
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