TISP8200M, BUFFERED P-GATE SCR DUAL
TISP8201M, BUFFERED N-GATE SCR DUAL
COMPLEMENTARY BUFFERED-GATE SCRS FOR OVERVOLTAGE PROTECTION

MAY 1998 - APRIL 2001

HIGH PERFORMANCE PROTECTION FOR SLICS WITH +VE & -VE BATTERY SUPPLIES

- **TISP8200M, Negative Overvoltage Protector**
  - **Wide 0 to -90 V Programming Range**
  - **Low 5 mA max. Gate Triggering Current**
  - **High -150 mA min. Holding Current**
- **TISP8201M, Positive Overvoltage Protector**
  - **Wide 0 to +90 V Programming Range**
  - **Low -5 mA max. Gate Triggering Current**
  - **20 mA min. Holding Current**
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	Telcordia GR-1089-CORE	210
10/700 µs	ITU-T K20, K21 & K.45	70
10/1000 µs	Telcordia GR-1089-CORE	45

- **Surface Mount Small-Outline Package**

description

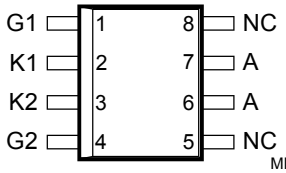
The TISP8200M/TISP8201M combination has been designed to protect dual polarity supply rail monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. Protection against negative overvoltages is given by the TISP8200M. Protection against positive overvoltages is given by the TISP8201M. Both parts are in 8-pin small-outline surface mount packages.

The TISP8200M has an array of two buffered P-gate SCRs with a common anode connection. Each SCR cathode and gate has a separate terminal connection. The NPN buffer transistors reduce the gate supply current.

In use, the cathodes of the TISP8200M SCRs are connected to the two conductors of the POTS line (see applications information). The gates are connected to the appropriate negative voltage battery feed of the SLIC driving the line conductor pair. This ensures that the TISP8200M protection voltage tracks the SLIC negative supply voltage. The anode of the TISP8200M is connected to the SLIC common.

TISP8200M

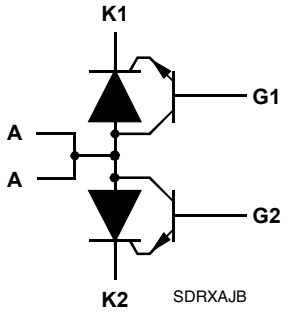
D PACKAGE
(TOP VIEW)



MDRXAKB

NC - No internal connection

device symbol



SDRXAJB

TISP8201M

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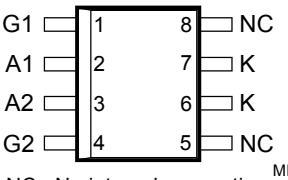
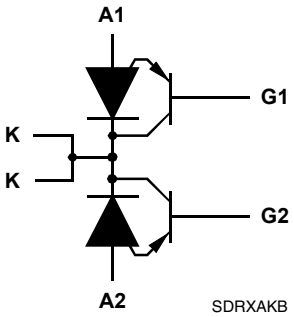
(TOP VIEW)



MDRXALB

NC - No internal connection

device symbol



SDRXAKB

HOW TO ORDER

DEVICE	PACKAGE	CARRIER	ORDER AS
TISP8200M	D (8-pin Small-Outline)	Embossed Tape Reeled	TISP8200MDR
TISP8201M	D (8-pin Small-Outline)	Embossed Tape Reeled	TISP8201MDR

TEXAS INSTRUMENTS

Designed and manufactured by Power Innovations, A Bourns Complany, under private label for Texas Instruments.

Negative overvoltages are initially clipped close to the SLIC negative supply by emitter follower action of the NPN buffer transistor. If sufficient clipping current flows the SCR will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of the SCR prevents d.c. latchup.

The TISP8201M has an array of two buffered N-gate SCRs with a common cathode connection. Each SCR anode and gate has a separate terminal connection. The PNP buffer transistors reduce the gate supply current.

In use, the anodes of the TISP8201M SCRs are connected to the two conductors of the POTS line (see applications information). The gates are connected to the appropriate positive voltage battery feed of the SLIC driving that line pair. This ensures that the TISP8201M protection voltage tracks the SLIC positive supply voltage. The cathode of the TISP8201M is connected to the SLIC common.

Positive overvoltages are initially clipped close to the SLIC positive supply by emitter follower action of the PNP buffer transistor. If sufficient clipping current flows the SCR will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides the SLIC pulls the conductor voltage down to its normal negative value and this commutates the conducting SCR into a reverse biassed condition.

absolute maximum ratings for TISP8200M, T_A = 25 °C (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, TISP8200M V_{GK} = 0	V_{DRM}	-120	V
Repetitive peak reverse voltage, V_{GA} = -70 V	V_{RRM}	120	V
Non-repetitive peak on-state pulse current, (see Notes 1 and 2)			
10/1000 µs (Telcordia/Bellcore GR-1089-CORE, Issue 2, February 1999, Section 4)	I_{TSP}	-45	A
5/310 µs (ITU-T K.20, K.21& K.45, K.44 open-circuit voltage wave shape 10/700 µs)		-70	
2/10 µs (Telcordia/Bellcore GR-1089-CORE, Issue 2, February 1999, Section 4)		-210	
Non-repetitive peak on-state current, 50/60 Hz (see Notes 1, 2 and 3)			
100 ms	I_{TSM}	-11	A
1 s		-6.5	
5 s		-3.4	
300 s		-1.4	
900 s		-1.3	
Non-repetitive peak gate current, 2/10 µs pulse, cathode commoned (see Note 1)	I_{GSM}	10	A
Junction temperature	T_J	-55 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values. The rated current values may be applied to any cathode-anode terminal pair. Above 85 °C, derate linearly to zero at 150 °C lead temperature.
3. These non-repetitive rated terminal currents are for the TISP8200M and TISP8201M together. Device (A) terminal positive current values are conducted by the TISP8201M and (K) terminal negative current values by the TISP8200M.

absolute maximum ratings for TISP8201M, T_A = 25 °C (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, V_{GA} = 0	V_{DRM}	120	V
Repetitive peak reverse voltage, V_{GK} = 70 V	V_{RRM}	-120	V
Non-repetitive peak on-state pulse current, (see Notes 1 and 2)			
10/1000 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)	I_{TSP}	45	A
5/310 µs (ITU-T K.20, K.21& K.45, K.44 open-circuit voltage wave shape 10/700 µs)		70	
2/10 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)		210	
Non-repetitive peak on-state current, 50/60 Hz (see Notes 1, 2 and 3)			
100 ms	I_{TSM}	11	A
1 s		6.5	
5 s		3.4	
300 s		1.4	
900 s		1.3	
Non-repetitive peak gate current, 2/10 µs pulse, cathode commoned (see Note 1)	I_{GSM}	-10	A
Junction temperature	T_J	-55 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values. The rated current values may be applied to any cathode-anode terminal pair. Above 85 °C, derate linearly to zero at 150 °C lead temperature.
3. These non-repetitive rated terminal currents are for the TISP8200M and TISP8201M together. Device (A) terminal positive current values are conducted by the TISP8201M and (K) terminal negative current values by the TISP8200M.

recommended operating conditions

See Figure 10		MIN	TYP	MAX	UNIT
C1, C2	Gate decoupling capacitor	100	220		nF
R1, R2	Series resistance for Telcordia GR-1089-CORE first-level and second-level surge survival	15	20		Ω
	Series resistance for ITU-T K.20, K.21 and K.45 coordination with a 400 V primary protector	10	20		

electrical characteristics for TISP8200M, T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 0 °C			-5	µA
			T_J = 85 °C			-50	µA
I_R	Reverse current	$V_R = V_{RRM}$, V_{GA} = -70 V	T_J = 0 °C			5	µA
			T_J = 85 °C			50	µA
$V_{(BO)}$	Breakover voltage	dv/dt = -250 V/ms, Source Resistance = 300 Ω, V_{GA} = -80 V				-82	V
$V_{(BO)}$	Breakover voltage	2/10 waveshape, (I_K) I_T = -100 A, $di/dt_{max.}$ = -58 A/µs, V_{GA} = -80 V				-95	V
I_H	Holding current	(I_K) I_T = -1 A, di/dt = 1 A/ms, V_{GA} = -80 V		-150			mA

electrical characteristics for TISP8200M, T_A = 25 °C (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GT}	Gate trigger current	(I_K) I_T = -5 A, $t_{p(g)} \geq$ 20 µs, V_{GA} = -80 V				5	mA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V, V_{GA} = -80 V, (see Note 4)	V_D = 0			35	pF
			V_D = -5 V			20	
			V_D = -50 V			10	

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

electrical characteristics for TISP8201M, T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, V_{GA} = 0	T_J = 0 °C			5	µA
			T_J = 85 °C			50	µA
I_R	Reverse current	$V_R = V_{RRM}$, V_{GK} = 70 V	T_J = 0 °C			-5	µA
			T_J = 85 °C			-50	µA
$V_{(BO)}$	Breakover voltage	dv/dt = 250 V/ms, Source Resistance = 300 Ω, V_{GK} = 80 V				82	V
$V_{(BO)}$	Breakover voltage	2/10 waveshape, (I_A) I_T = 100 A, $di/dt_{max.}$ = 58 A/µs, V_{GK} = 80 V				95	V
I_H	Holding current	(I_A) I_T = 1 A, di/dt = -1 A/ms, V_{GK} = 80 V		+20			mA
I_{GT}	Gate trigger current	(I_A) I_T = 5 A, $t_{p(g)} \geq$ 20 µs, V_{GK} = 80 V				-5	mA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V, V_{GK} = 80 V, (see Note 4)	V_D = 0			35	pF
			V_D = 5 V			20	
			V_D = 50 V			10	

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.52 W, T_A = 70°C, 5 cm^2, FR4 PCB			160	°C/W

PARAMETER MEASUREMENT INFORMATION

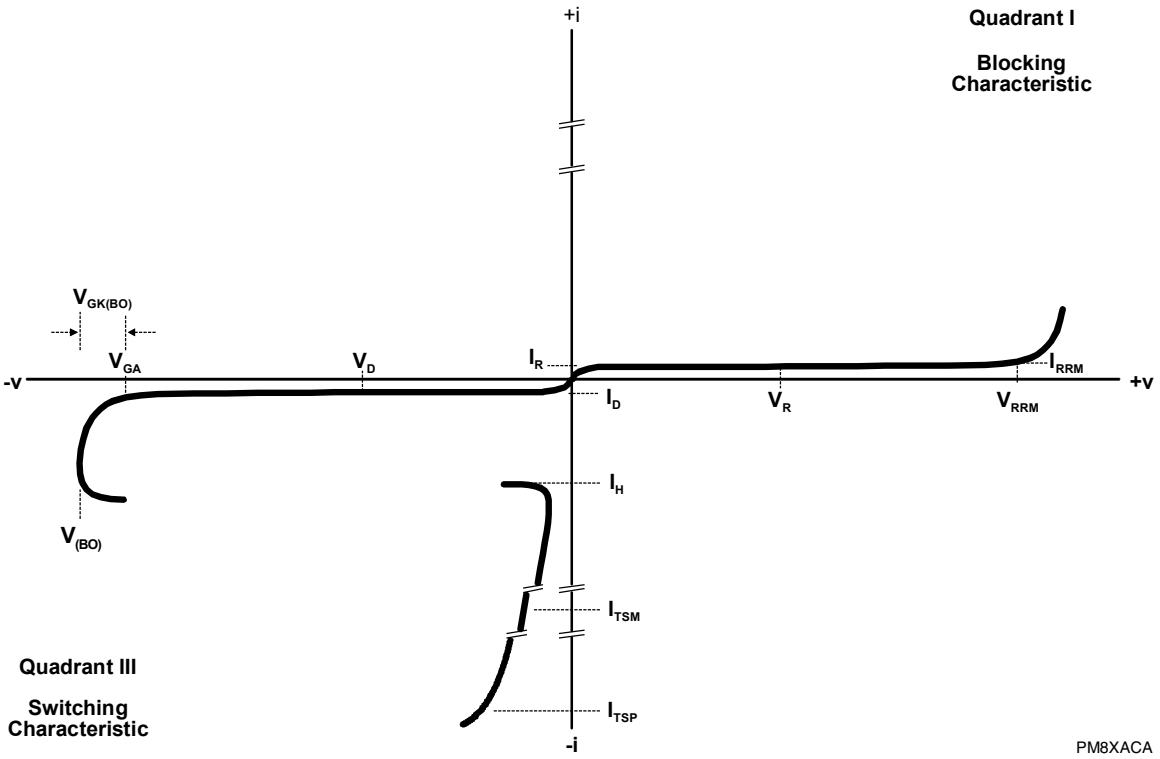


Figure 1. TISP8200M KA TERMINAL CHARACTERISTIC

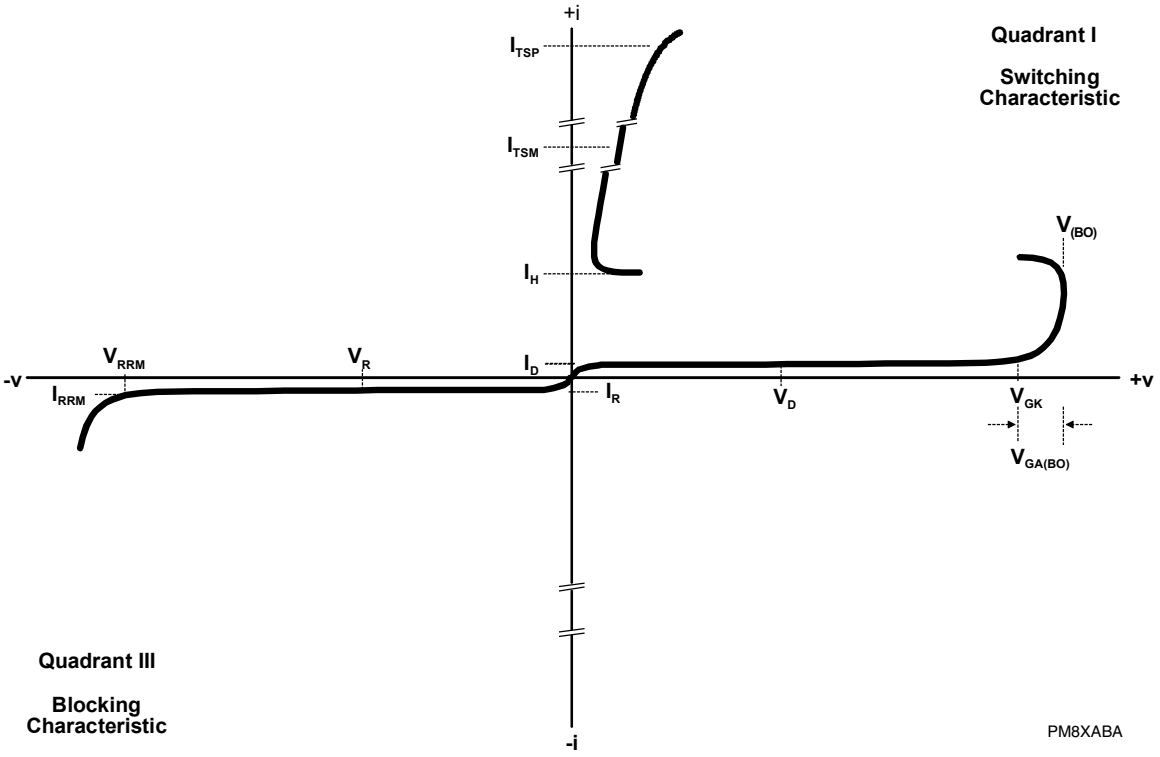


Figure 2. TISP8201M AK TERMINAL CHARACTERISTIC

APPLICATIONS INFORMATION

operation of SLICs using positive and negative voltage supply rails

Figure 3 shows a typical powering arrangement for a multi-supply rail SLIC. V_{BATR} is a positive supply and V_{BATL} and V_{BATH} are negative supplies. V_{BATH} is more negative than V_{BATL}. With the positive and negative supply switches, S2 and S1, in the positions shown, the line driver amplifiers are powered between 0 V and V_{BATL}. This mode minimises the power consumption for short loop transmission. For long loops, the driver voltage is increased by operating S1 to connect V_{BATH}. To generate ringing, S2 is operated to apply V_{BATR}, powering the drivers from a total supply voltage of V_{BATR} - V_{BATH}. These conditions are shown in Figure 4.

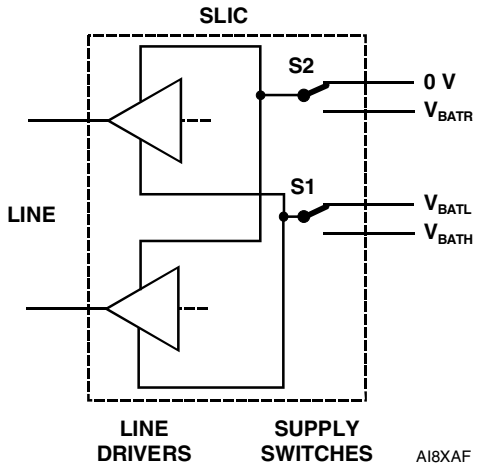


Figure 3. SLIC WITH VOLTAGE SUPPLY SWITCHING

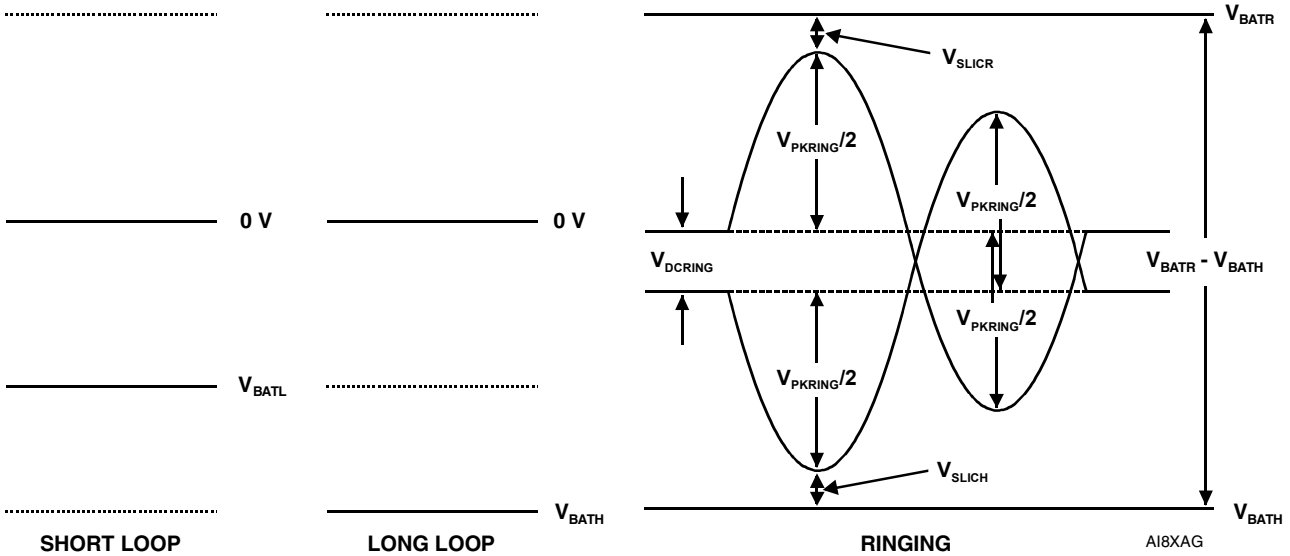


Figure 4. DRIVER SUPPLY VOLTAGE LEVELS

Conventional ringing is typically unbalanced ground or battery backed. To minimise the supply voltage required, most multi-rail SLICs use balanced ringing as shown in Figure 4. The ringing has d.c., V_{DCRING}, and a.c., V_{PKRING}, components. A 70 V rms a.c. ring signal has a peak value, V_{PKRING}, of 99 V. If the d.c. component was 20 V, then the total voltage swing needed would be 99 + 20 = 119 V. There are internal losses in the SLIC from the positive supply, V_{SLICR}, and the negative supply, V_{SLICH}. The sum of these two

losses generally amounts to a total of 10 V. This makes a total supply rail value of 119 + 10 = 129 V. In practice, the voltage might be distributed as V_{BATR} = +60 V and V_{BATH} = -70 V. These values are nominal and some extra voltage should be provided to cover power supply voltage tolerance.

SLIC parameter values

The table below shows some details of currently available SLICs using positive and negative supply rails.

MANUFACTURER	INFINEON‡				LEGERITY™‡		UNIT
SLIC SERIES	SLIC-S‡		SLIC-E‡		ISLIC™‡		
SLIC #	PEB4264		PEB 4265		79R251		
Data Sheet Issue	14/07/2000		14/07/2000		-/08/2000		
Short Circuit Current	±130		±130		±150		mA
V_{BATH} max.	-70		-90		-85		V
V_{BATR} max.	+50		+90		+85		V
V_{BATR}-V_{BATH} max.	90		160		150		V
AC Ringing for:	45		85		65		V rms
V_{BATH}	-54		-70		-68		V
V_{BATR}	+36		+80		+52		V
V_{BATR}-V_{BATH}	90		150		120		V
R or T Power Max. < 10 ms	TBA		10				W
R or T Overshoot < 10 ms					-5	5	V
R or T Overshoot < 1 ms	-10	+10	-10	+10			V
R or T Overshoot < 10 µs	-10	+30	-10	+30			V
R or T Overshoot < 1 µs					-10	10	V
R or T Overshoot < 250 ns					-15	15	V
Line Feed Resistance	20 + 30		20 + 30		50		Ω

‡ Legerity, the Legerity logo and ISLIC are the trademarks of Legerity, Inc., formally AMD's Communication Division. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

The maximum total voltage, V_{BATR} - V_{BATH}, is normally about 10 % less than the sum of the maximum V_{BATR} and maximum V_{BATH} values. In terms of voltage overshoot, ±10 V is needed for 1 µs and ±15 V for 250 ns. It is important to define the protector overshoot under actual circuit conditions. For example, if the series line feed resistor was 20 Ω, R1 in Figure 10, and Telcordia GR-1089-CORE 2/10 and 10/1000 first level impulses were applied, the peak protector currents would be 100 A and 33 A. Therefore, the protector voltage overshoot should be measured at 100 A, 2/10 and 33 A, 10/1000.

Using the table values for maximum battery voltage and minimum overshoot gives a requirement of ±105 V from the output to ground and ±175 V between outputs. There needs to be temperature guard banding for the change in protector characteristics with temperature. To cover down to -40 °C the 25 °C protector minimum values become; ±120 V referenced to ground, ±190 V between outputs and 100 V or -100 V on the gate.

operation of gated protectors

Figure 5 shows how the TISP8200M and TISP8201M limit overvoltages. The TISP8200M SCR sections limit negative overvoltages and the TISP8201M SCR sections limit positive overvoltages.

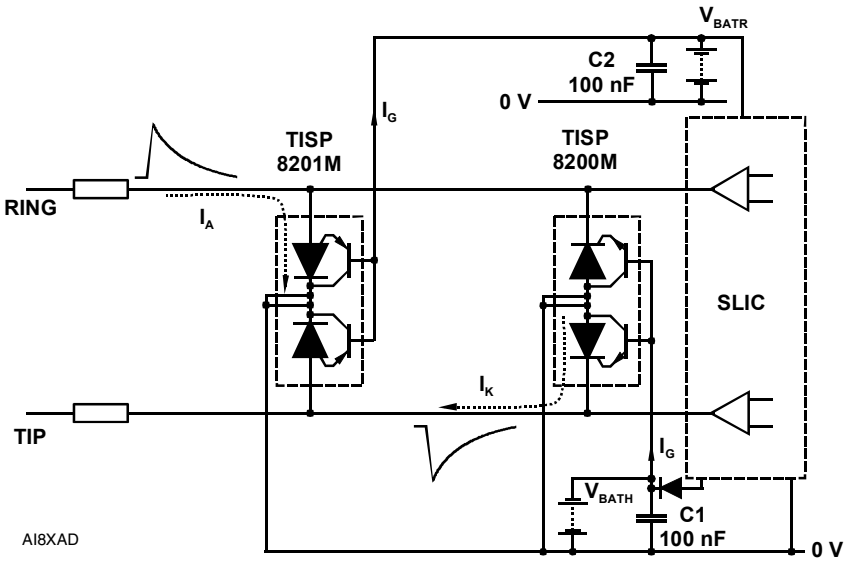


Figure 5. OVERVOLTAGE CONDITIONS

The TISP8200M (buffered) gate is connected to the negative SLIC battery feed voltage (V_{BATH}) to provide the protection reference voltage. Negative overvoltages are initially clipped close to the SLIC negative supply rail value (V_{BATH}) by the conduction of the TISP8200M transistor base-emitter and the SCR gate-cathode junctions. If sufficient current is available from the overvoltage, then the SCR will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the high holding current of the SCR prevents d.c. latchup with the SLIC output current.

The negative protection voltage, $V_{(BO)}$, will be the sum of the gate supply (V_{BATH}) and the TISP8200M peak gate(terminal)-cathode voltage (V_{GT}). Under a.c. overvoltage conditions V_{GT} will be less than 2.0 V. The integrated transistor buffer in the TISP8200M greatly reduces protectors source and sink current loading on the V_{BATH} supply. Without the transistor, the SCR gate current would charge the V_{BATH} supply. An electronic power supply is not usually designed to be charged like a battery. As a result, the electronic supply would switch off and the SCR gate current would provide the SLIC supply current. Normally the SLIC current would be less than the gate current, which would cause the supply voltage to increase and destroy the SLIC by a supply overvoltage. Older designs using just SCRs, needed to incorporate a sacrificial zener diode across the supply line to go short if the supply voltage increased too much. The integrated transistor buffer removes the charging problem and the need for a safety zener.

Fast rising impulses will cause short term overshoots in gate-cathode voltage. The negative protection voltage under impulse conditions will also be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 60 A/µs can cause inductive voltages of 0.6 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised.

The TISP8201M (buffered) gate is connected to the positive SLIC battery feed voltage (V_{BATR}) to provide the protection reference voltage. Positive overvoltages are initially clipped close to the SLIC positive supply rail value (V_{BATR}) by the conduction of the TISP8201M transistor base-emitter and the SCR gate-anode

junctions. If sufficient current is available from the overvoltage, then the SCR will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the SLIC pulls the conductor voltage down to its normal negative value and this commutates the conducting SCR into a reverse biassed condition.

voltage stress levels on the TISP8200M and TISP8201M

Figure 6 shows the protector electrodes. The package terminal designated gate, G, is the transistor base, B, electrode connection and so is marked as B (G). The following junctions are subject to voltage stress: Transistor EB and CB, SCR AK (reverse and off state). This clause covers the necessary testing to ensure the junctions are good.

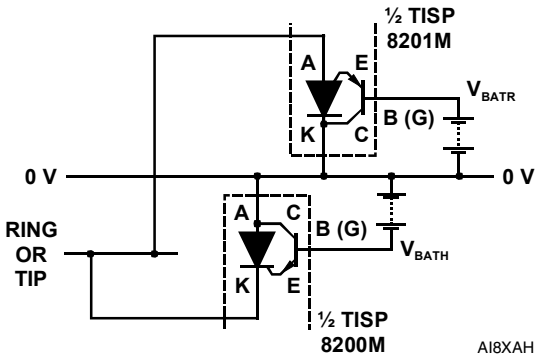


Figure 6. PROTECTOR ELECTRODES

Testing transistor EB and SCR AK reverse: The highest reverse EB voltage and reverse AK voltage occurs during the overshoot period of the other protector. For the TISP8200M, the SCR has V_{BATR} plus the TISP8201M overshoot above V_{BATR}. The transistor EB has an additional V_{BATH} voltage applied (see Figure 7). The reverse current, I_R, flowing into the K terminal will be the sum of the transistor I_{EB} and the actual internal SCR I_R. The reverse voltage applied to the K terminal is the TISP8201M protection voltage, $V_{(BO)}$ (V_{BATR} plus overshoot), and the G terminal has V_{BATH}. Similarly for the TISP8201M, I_R is measured with the TISP8200M $V_{(BO)}$ applied and it is the sum of the transistor I_{EB} and the actual internal SCR I_R. V_{BATR} is applied to the G terminal.

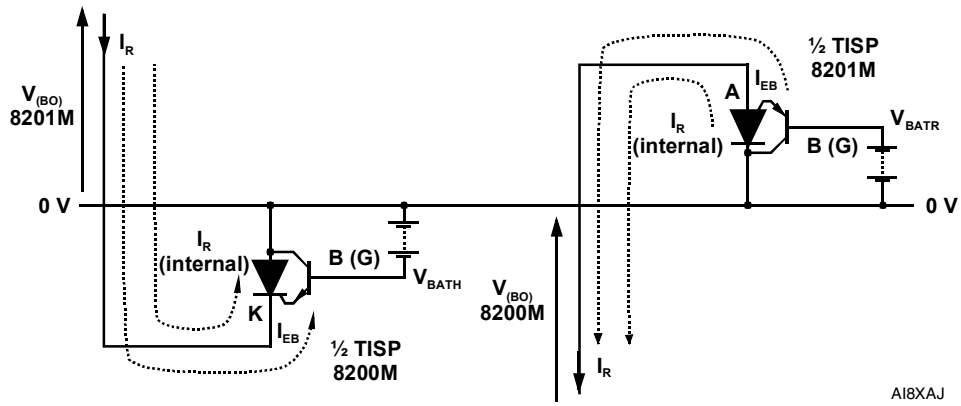


Figure 7. REVERSE CURRENT VERIFICATION

Testing transistor CB and SCR AK off state: The highest AK voltage occurs during the overshoot period of the protector. To make sure that the SCR blocking junction does not break down during this period, a d.c. test for off-state current can be applied at the overshoot voltage value. To avoid transistor CB current amplification by the transistor gain, the transistor base-emitter is shorted during this test (see Figure 8).

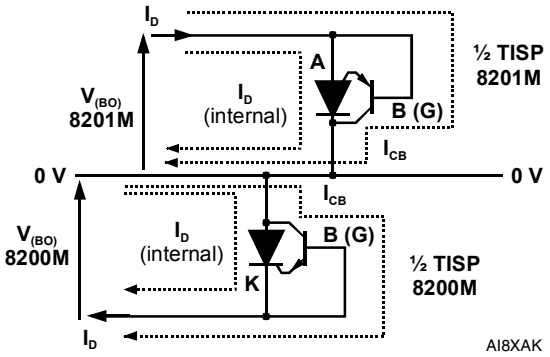


Figure 8. OFF-STATE CURRENT VERIFICATION

Summary: Two tests are need to verify the protector junctions. Maximum current values for I_R and I_D are required.

TISP8200M and TISP8201M voltage overshoot

Figure 9 shows typical overshoots on a 100 A 2/10 waveshape. Both devices are under 10 V peak, which meets the needs of the SLICs listed earlier.

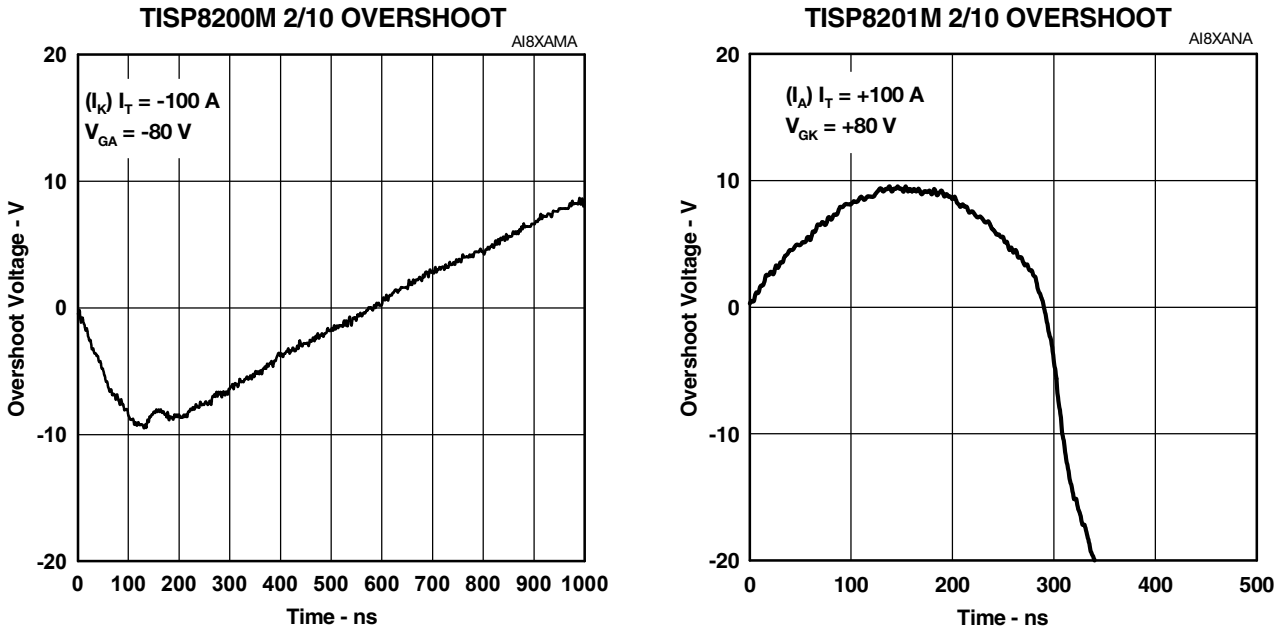


Figure 9. VOLTAGE OVERSHOOT REFERENCED TO GATE BIAS VOLTAGE

line protection with TISP8200M and TISP8201M

Figure 10 shows a typical circuit for single line protection using one TISP8200M and one TISP8201M. The series resistor values limit the test impulse currents to within the protector ratings.

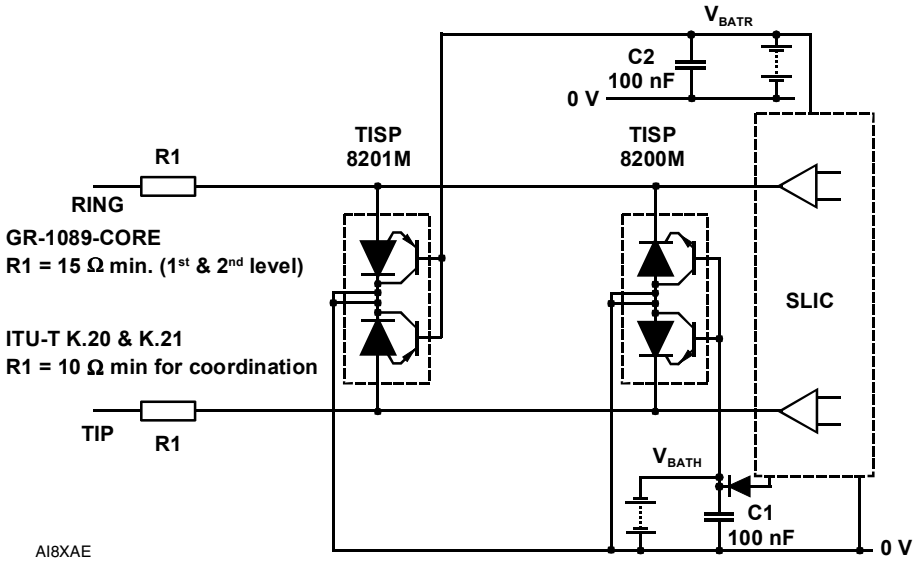


Figure 10. LINE PROTECTION WITH TISP8200M AND TISP8201M

MECHANICAL DATA

device symbolization code

Devices are coded as below

DEVICE	SYMBOLIZATION
TISP8200M	8200M
TISP8201M	8201M

carrier information

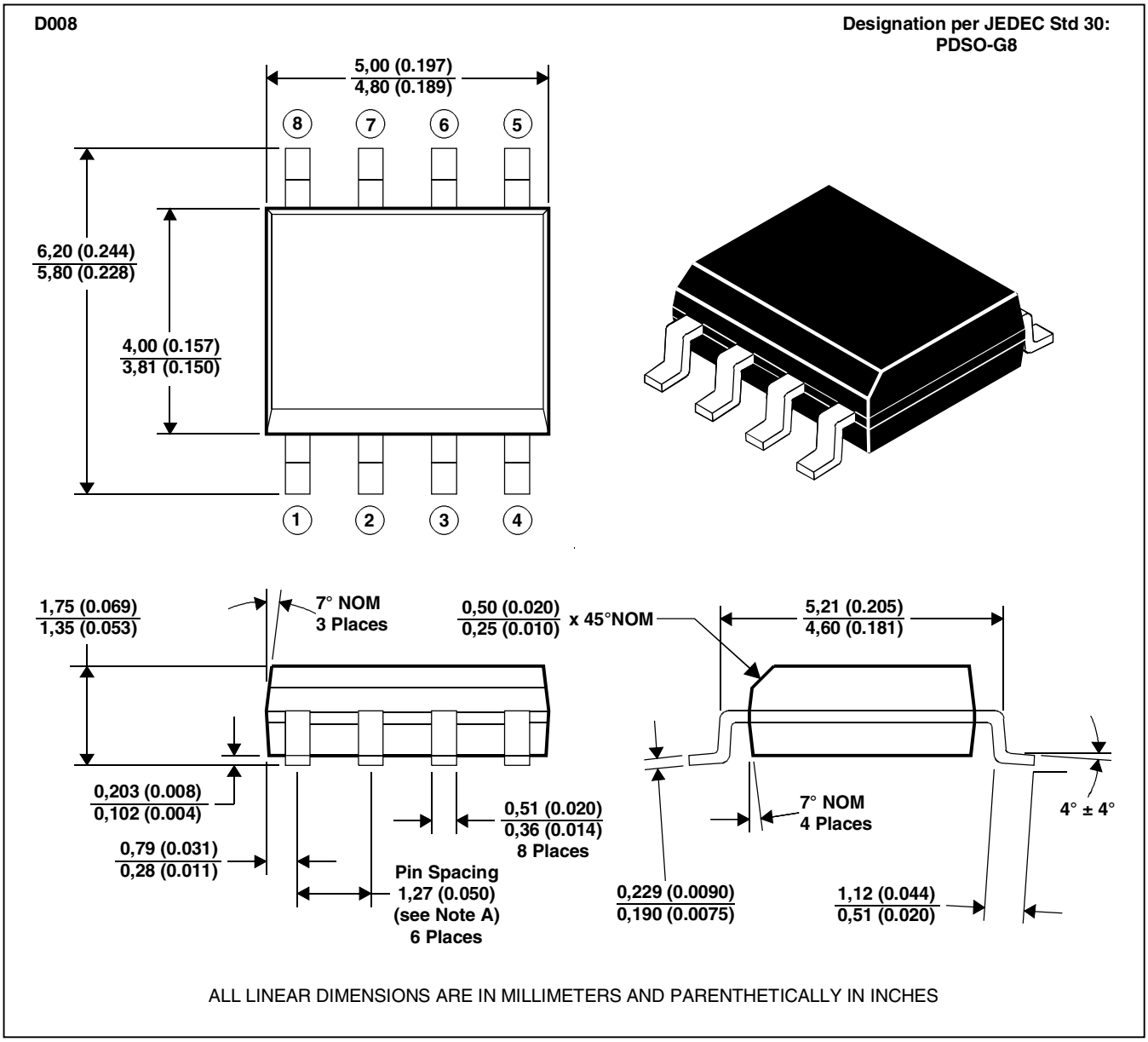
Evaluation quantities will be shipped in the most practical carrier.

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



MDXXAA

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

IMPORTANT NOTICE

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