

Orderable Part Number ^{(1) (2)}	Output Current	Output Voltage	External Sync	F _{sw}	Internal Capacitors	Spread Spectrum
LMQ66430MC3RXBRQ1	3 A	3.3-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes
LMQ66430MC5RXBRQ1 ⁽³⁾	3 A	5-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes
LMQ66420MC3RXBRQ1 ⁽³⁾	2 A	3.3-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes
LMQ66420MC5RXBRQ1 ⁽³⁾	2 A	5-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes
LMQ66420MA3RXBRQ1	2 A	3.3-V Fixed / Adjustable	(PFM / FPWM Selectable)	Fixed 400 kHz	Yes	Yes
LMQ66410MC3RXBRQ1 ⁽³⁾	1 A	3.3-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes
LMQ66410MC5RXBRQ1	1 A	5-V Fixed / Adjustable	Yes (PFM / FPWM Selectable)	Fixed 2.2 MHz	Yes	Yes

(1) For more information on device orderable part numbers, see [Device Nomenclature](#).

(2) For other variant options, please contact TI.

(3) Preview.

Table 8-1. Pulse-Dependent Mode Selection Settings

Mode/Sync Input	Mode
> V _{MODE_H}	FPWM with spread spectrum factory setting
< V _{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

V _{MODE_L}	SYNC/MODE input voltage low level threshold	1 V
V _{MODE_H}	SYNC/MODE input voltage high level threshold	1.6 V

ENABLE (EN PIN)			
V _{EN-WAKE}	EN wakeup threshold	0.5	0.7
V _{EN-VOUT}	Precision enable rising threshold for V _{OUT}	1.16	1.23
V _{EN-HYST}	Enable hysteresis below V _{EN-VOUT}	0.3	0.4
I _{KLG-EN}	Enable pin input leakage current	V _{EN} = V _{IN} = 13.5 V	10 nA

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in [Figure 9-2](#). The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then Equation 9 and Equation 10 are used to calculate R_{ENT} and V_{OFF}, respectively.

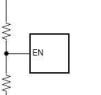
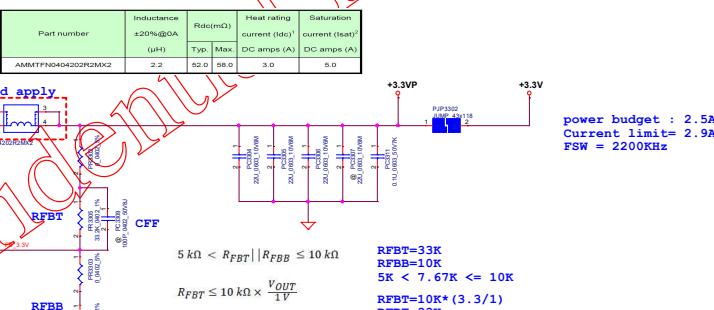


Figure 9-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN} - V_{OUT}} - 1 \right) \times R_{ENB}$$

(9)



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