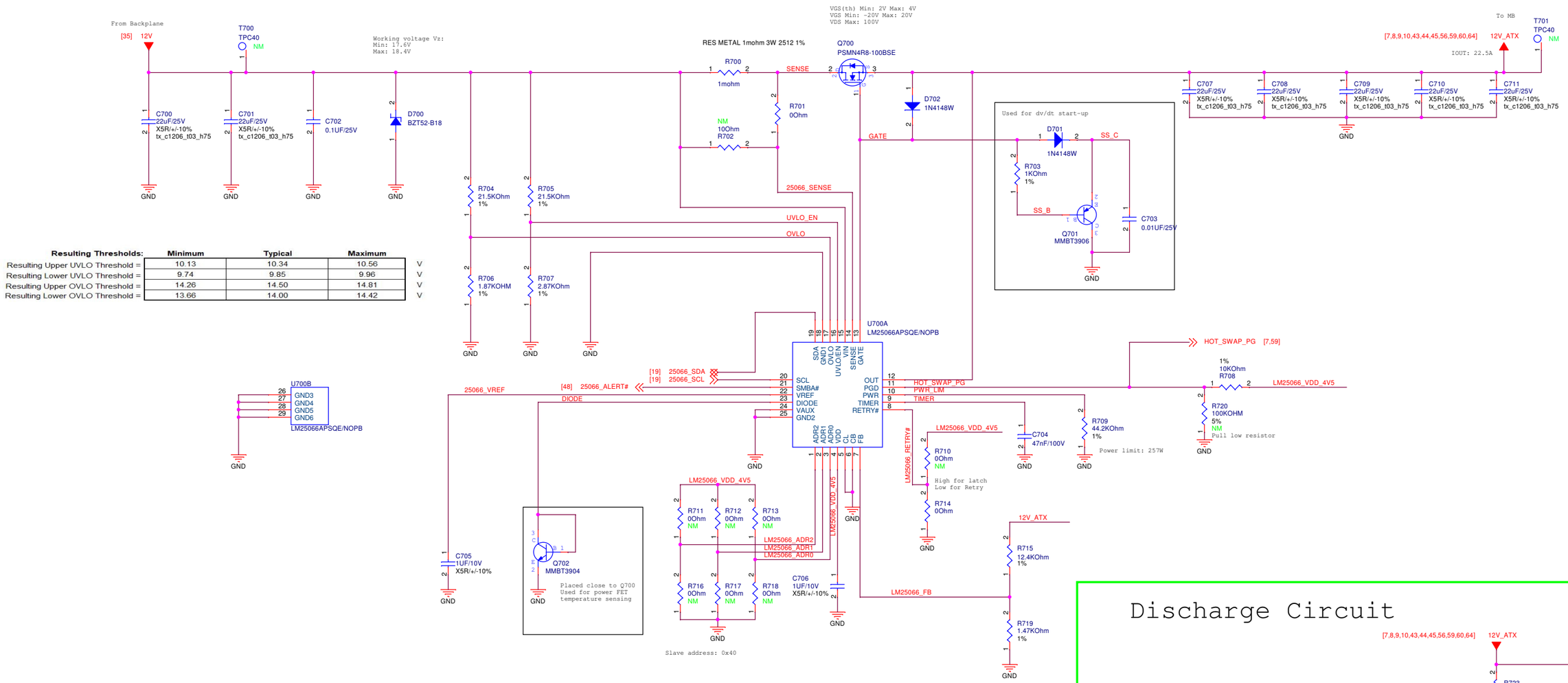
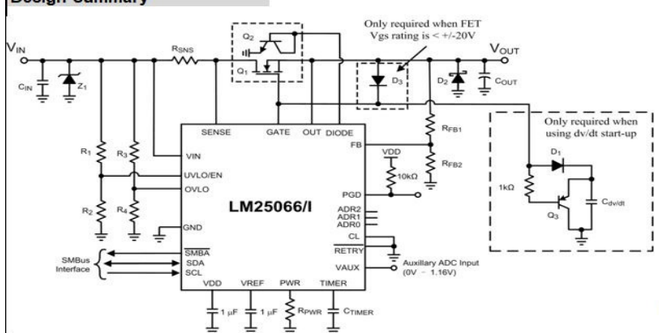
# PWR HOT SWAP PROTECTION




| Resulting Thresholds: | Minimum | Typical | Maximum | |
|---|---|---|---|---|
| Resulting Upper UVLO Threshold = | 10.13 | 10.34 | 10.56 | V |
| Resulting Lower UVLO Threshold = | 9.74 | 9.85 | 9.96 | V |
| Resulting Upper OVLO Threshold = | 14.26 | 14.50 | 14.81 | V |
| Resulting Lower OVLO Threshold = | 13.66 | 14.00 | 14.42 | V |

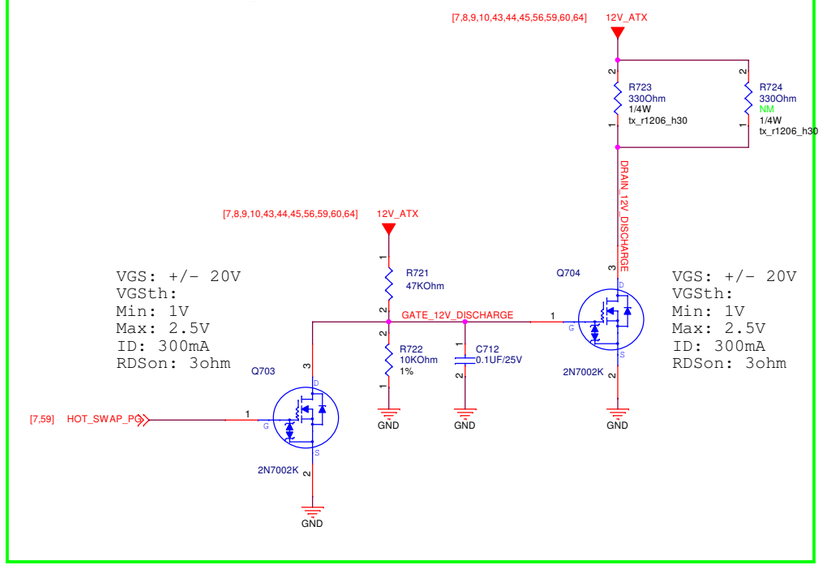
## Design Summary




| | | |
|---|---|---|
| $R_S$ = | 1 | mΩ |
| $R_{CL1}$ = | Open | Ω |
| $R_{CL2}$ = | 0 | Ω |
| $R_{PWR}$ = | 44.2 | kΩ |
| $C_T$ = | 47.00 | nF |
| R1 = | 21.5 | kΩ |
| R2 = | 2.87 | kΩ |
| R3 = | 21.5 | kΩ |
| R4 = | 1.87 | kΩ |
| $R_{FB1}$ = | 12.4 | kΩ |
| $R_{FB2}$ = | 1.5 | kΩ |
| $R_{PG}$ = | 10 | kΩ |
| $C_{IN}$ = | 0.01 | µF |
| $C_{VDD}$ = | 1 | µF |
| $C_{VREF}$ = | 1 | µF |
| D1, D3 = | 1N4148W-7-F | |
| D2 = | SK153-TP | |
| $C_{dv/dt}$ = | 10 | nF |
| Connect CL Pin to | GND | µF |
| Connect CB Pin to | GND | µF |
| Connect /Retry to | GND | µF |
| Q1 = | PSMN4R8-100BSE | |
| Q2 = | MMBT3904 | |
| Q3 = | MMBT3906 | |
| Z1 = | 5.0SMDJXXX | |

| | Typical | Units |
|---|---|---|
| Current limit | 25.0 | A |
| Power Limit | 257 | W |
| Circuit Breaker Current | 45.0 | A |
| Startup Time | 6.36 | ms |
| Insertion Delay | 14.5 | ms |
| Fault Timeout | 0.888 | ms |
| Restart Time During Fault | 108.309 | ms |
| Upper UVLO Threshold | 10.344 | V |
| Lower UVLO Threshold | 9.850 | V |
| Upper OVLO Threshold | 14.497 | V |
| Lower OVLO Threshold | 14.002 | V |
| PGD Threshold | 11.0110816 | V |
| | | |
| PGD Hystersis | 297.6 | mV |

## Discharge Circuit




<Core Design>

PEGATRON CORP.

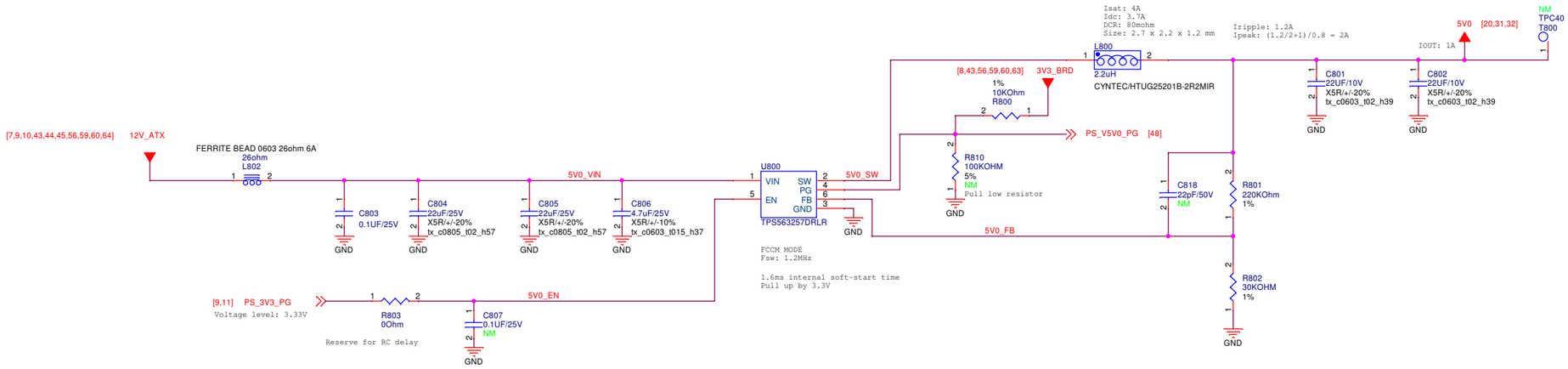
Title : PWR HOT SWAP PROTECTION

Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| A2 | Endeavor | 2.0 |

Date: Wednesday, July 31, 2024 Sheet 7 of 64

# 5V Regulator




| LOGIC THRESHOLD | | | | | | |
|---|---|---|---|---|---|---|
| $V_{ENH}$ | EN threshold high level | Rising enable threshold | 1.15 | 1.19 | 1.25 | V |
| $V_{ENL}$ | EN threshold low level | Falling disable threshold | 0.90 | 1.00 | 1.10 | V |
| $V_{ENHYS}$ | EN hystersis | Hysteresis | | 190 | | mV |
| $R_{EN}$ | EN pulldown resistor | | | 2 | | MΩ |

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pin voltage | VIN | 3 | | 17 | V |
| | FB, EN, PG | –0.1 | | 5.5 | |
| | GND | –0.1 | | 0.1 | |
| | SW | –1 | | 17 | |
| | SW (transient < 20 ns) | –5 | | 18 | |
| Output current | $I_{OUT}$ | 0 | | 3 | A |



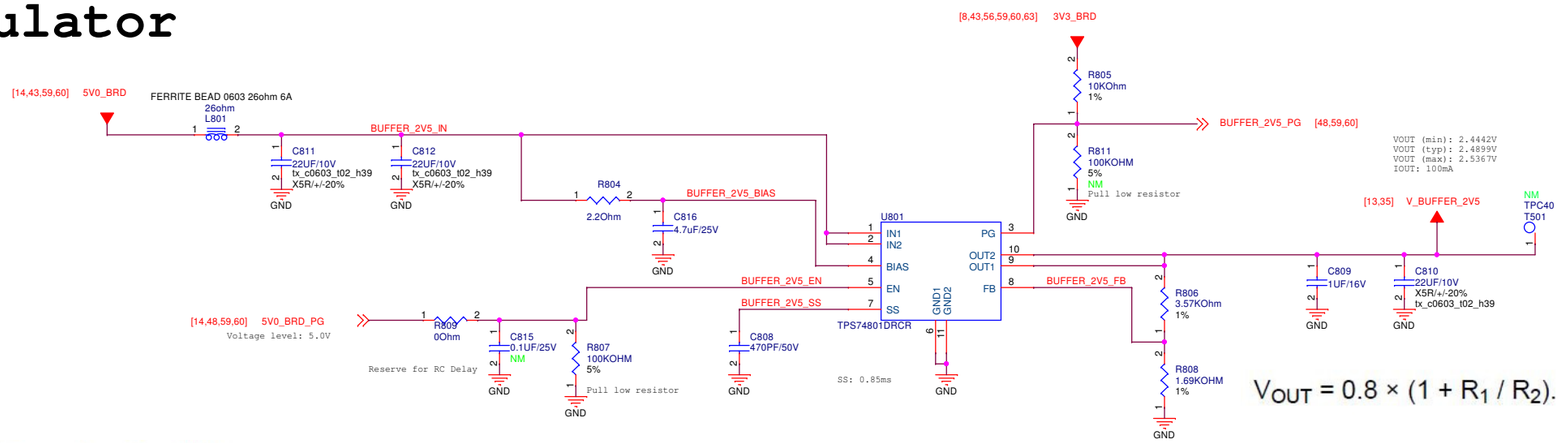
**Table 8-2. Recommended Component Values (continued)**

| Output Voltage (V) | R4 (kΩ) | R5 (kΩ) | Typical L1 (µH) | Typical $C_{OUT}$ (µF) | Typical $C_{OUT}$ (µF) Norminal Value Range | Typical $C_{OUT}$ Category | Typical C6 (pF) |
|---|---|---|---|---|---|---|---|
| 3.3 | 135.0 | 30.0 | 2.2 | 22 | 22-88 | MLCC, 0805, 10V | 33 |
| 5 | 220.0 | 30.0 | 2.2 | 22 | 22-88 | MLCC, 0805, 10V | 22 |
| 10 | 470.0 | 30.0 | 4.7 | 44 | 44-88 | MLCC, 0805, 16V | 47 |

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}}$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2}$$

# 2V5 Regulator




$$V_{OUT} = 0.8 \times (1 + R_1 / R_2).$$

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | $V_{OUT} + V_{DO}$ ($V_{IN}$) | $V_{OUT}$ + 0.3 | 5.5 | V |
| $V_{EN}$ | Enable supply voltage | | $V_{IN}$ | 5.5 | V |
| $V_{BIAS}$ ((1)) | BIAS supply voltage | $V_{OUT} + V_{DO}$ ($V_{BIAS}$)((2)) | $V_{OUT}$ + 1.6(2) | 5.5 | V |

| | | | | | |
|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference (Adj.) | $T_J$ = +25°C | 0.796 | 0.8 | 0.804 | V |
| $V_{OUT}$ | Output voltage range | $V_{IN}$ = 5V, $I_{OUT}$ = 1.5A | $V_{REF}$ | | 3.6 | V |
| | Accuracy(1) | 2.97V ≤ $V_{BIAS}$ ≤ 5.5V, 50mA ≤ $I_{OUT}$ ≤ 1.5A | –2 | ±0.5 | 2 | % |

| | | | | | |
|---|---|---|---|---|---|
| $V_{EN(hi)}$ | Enable input high level | | 1.1 | 5.5 | V |
| $V_{EN(lo)}$ | Enable input low level | | 0 | 0.4 | V |

<Core Design>

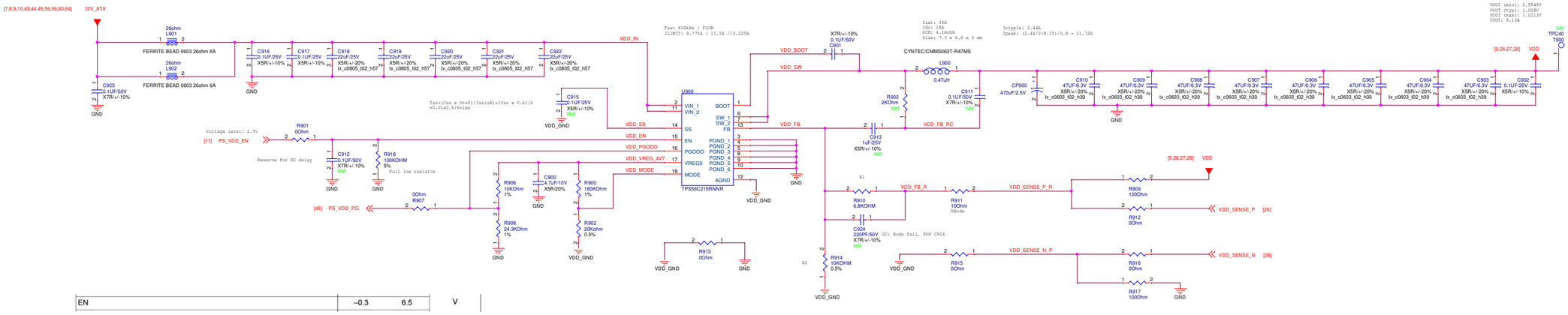
PEGATRON Title : 5V0 2V5 Regulator

PEGATRON CORP. Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| A2 | Endeavor | 2.0 |

Date: Wednesday, July 31, 2024 Sheet 8 of 64

# 12V to 1V for LS1028A



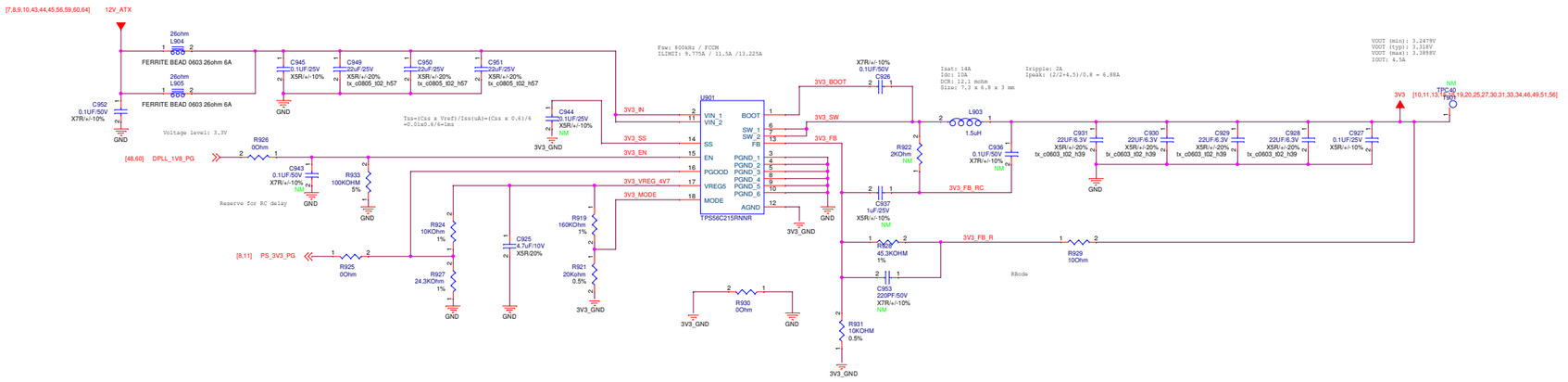

| | | | | |
|---|---|---|---|---|
| EN | –0.3 | 6.5 | V | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{ENH}$ | EN H-level threshold voltage | | 1.175 | 1.225 | 1.3 | V |
| $V_{ENL}$ | EN L-level threshold voltage | | 1.025 | 1.104 | 1.15 | V |

**Table 7-3. MODE Pin Resistor Settings**

| $R_{M\_L}$ (kΩ) | $R_{M\_H}$ (kΩ) | LIGHT LOAD OPERATION | CURRENT LIMIT | FREQUENCY (kHz) |
|---|---|---|---|---|
| 5.1 | 300 | FCCM | ILIM-1 | 400 |
| 10 | 200 | FCCM | ILIM | 400 |
| 20 | 160 | FCCM | ILIM-1 | 800 |
| 20 | 120 | FCCM | ILIM | 800 |
| 51 | 200 | FCCM | ILIM-1 | 1200 |
| 51 | 180 | FCCM | ILIM | 1200 |
| 51 | 150 | DCM | ILIM-1 | 400 |
| 51 | 120 | DCM | ILIM | 400 |
| 51 | 91 | DCM | ILIM-1 | 800 |
| 51 | 82 | DCM | ILIM | 800 |
| 51 | 62 | DCM | ILIM-1 | 1200 |
| 51 | 51 | DCM | ILIM | 1200 |

# 12V to 3.3V for System



# META 1V8 AVD POWER

TPS53355 Layout notes:
1. C177 should be placed near the device and R213 and C178 can be placed near the power stage.

2. Place resistors connected to TRIP and MODE pins as close to the device as possible. Use common GND via to connect them to ground

3. Place the VDD and VREG decoupling capacitors as close as possible to the device. Make sure GND vias are provided for each decoupling capacitor and make the loop as small as possible.

4. Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop

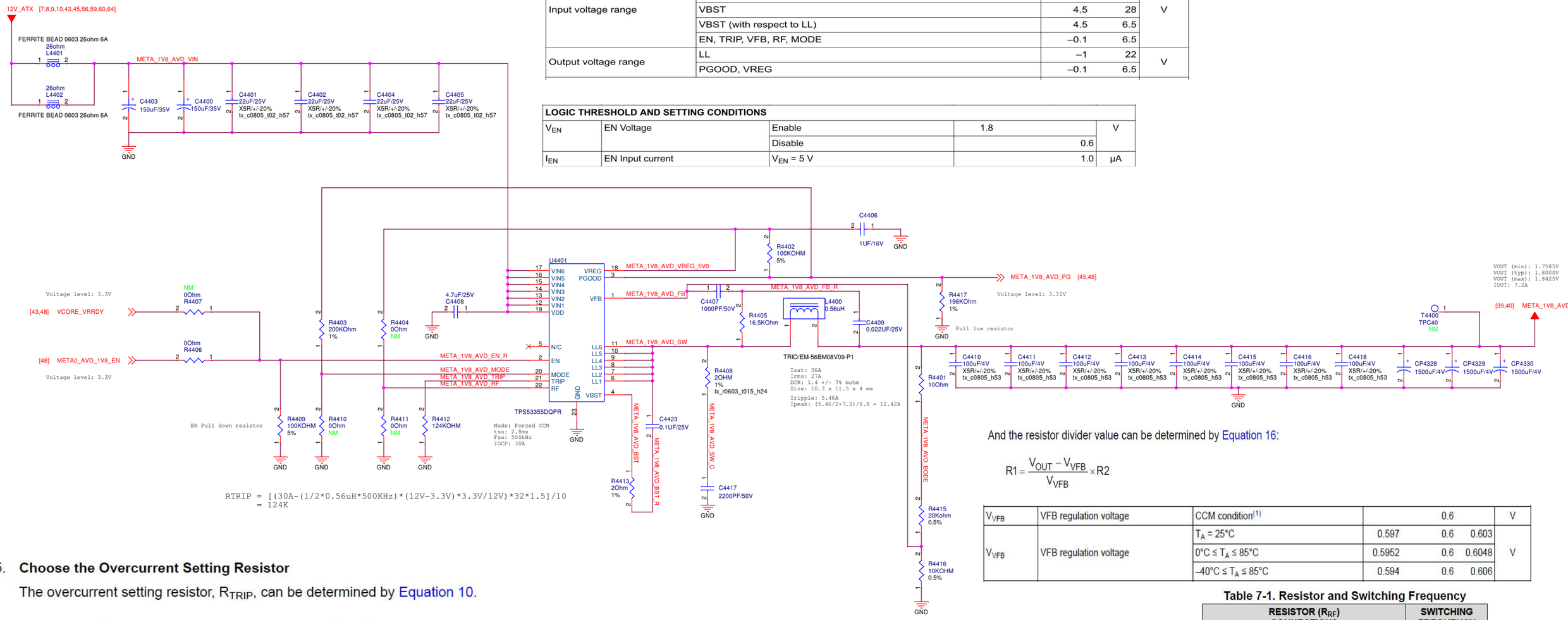
5. All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LLx, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.

6. The power components (including input/output capacitors, inductor and TPS53355) must be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.

7. The trace from these resistors to the VFB pin should be short and thin.

8. The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor should be as short and wide as possible.

9. Use separate vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.




RTRIP = [(30A-(1/2*0.56uH*500KHz)*(12V-3.3V)*3.3V/12V)*32*1.5]/10
= 124K

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage range | VIN (main supply) | 1.5 | 15 | V |
| | VDD | 4.5 | 25 | |
| | VBST | 4.5 | 28 | |
| | VBST (with respect to LL) | 4.5 | 6.5 | |
| | EN, TRIP, VFB, RF, MODE | –0.1 | 6.5 | |
| Output voltage range | LL | –1 | 22 | V |
| | PGOOD, VREG | –0.1 | 6.5 | |

| LOGIC THRESHOLD AND SETTING CONDITIONS | | | | |
|---|---|---|---|---|
| $V_{EN}$ | EN Voltage | Enable | 1.8 | V |
| | | Disable | 0.6 | |
| $I_{EN}$ | EN Input current | $V_{EN}$ = 5 V | 1.0 | µA |

## 5. Choose the Overcurrent Setting Resistor

The overcurrent setting resistor, $R_{TRIP}$, can be determined by Equation 10.

$$R_{TRIP}(k\Omega) = \frac{\left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}}\right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}\right) \times 32 \times R_{DS(on)}(m\Omega)}{I_{TRIP}(\mu A)} \quad (10)$$

where

- $I_{TRIP}$ is the TRIP pin sourcing current (10 µA)
- $R_{DS(on)}$ is the thermally compensated on-time resistance value of the low-side MOSFET

Use an $R_{DS(on)}$ value of 1.5 mΩ for an overcurrent level of approximately 30 A. Use an $R_{DS(on)}$ value of 1.7 mΩ for overcurrent level of approximately 10 A.

And the resistor divider value can be determined by Equation 16:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2$$

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{VFB}$ | VFB regulation voltage | CCM condition(1) | | 0.6 | | V |
| $V_{VFB}$ | VFB regulation voltage | $T_A$ = 25°C | 0.597 | 0.6 | 0.603 | V |
| | | 0°C ≤ $T_A$ ≤ 85°C | 0.5952 | 0.6 | 0.6048 | |
| | | –40°C ≤ $T_A$ ≤ 85°C | 0.594 | 0.6 | 0.606 | |

**Table 7-1. Resistor and Switching Frequency**

| RESISTOR ($R_{RF}$) CONNECTIONS | | SWITCHING FREQUENCY ($f_{SW}$) (kHz) |
|---|---|---|
| VALUE (kΩ) | CONNECT TO | |
| 0 | GND | 250 |
| 187 | GND | 300 |
| 619 | GND | 400 |
| OPEN | n/a | 500 |
| 866 | VREG | 650 |
| 309 | VREG | 750 |
| 124 | VREG | 850 |
| 0 | VREG | 970 |

**Table 7-3. Soft-Start and MODE Settings**

| MODE SELECTION | ACTION | SOFT-START TIME (ms) | $R_{MODE}$ (kΩ) |
|---|---|---|---|
| Auto Skip | Pull down to GND | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |
| Forced CCM(1) | Connect to PGOOD | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor $R_{MODE}$.

<Core Design>

PEGATRON Title : META DX1 1V8 AVD POWER
PEGATRON CORP. Engineer: Timmy Chien
Size A2 | Project Name Endeavor | Rev X00
Date: Wednesday, July 31, 2024 Sheet 44 of 64

# META 0V8 AVD POWER

TPS53355 Layout notes:
1. C82 should be placed near the device and R79 and C81 can be placed near the power stage.

2. Place resistors connected to TRIP and MODE pins as close to the device as possible. Use common GND via to connect them to ground

3. Place the VDD and VREG decoupling capacitors as close as possible to the device. Make sure GND vias are provided for each decoupling capacitor and make the loop as small as possible.

4. Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop

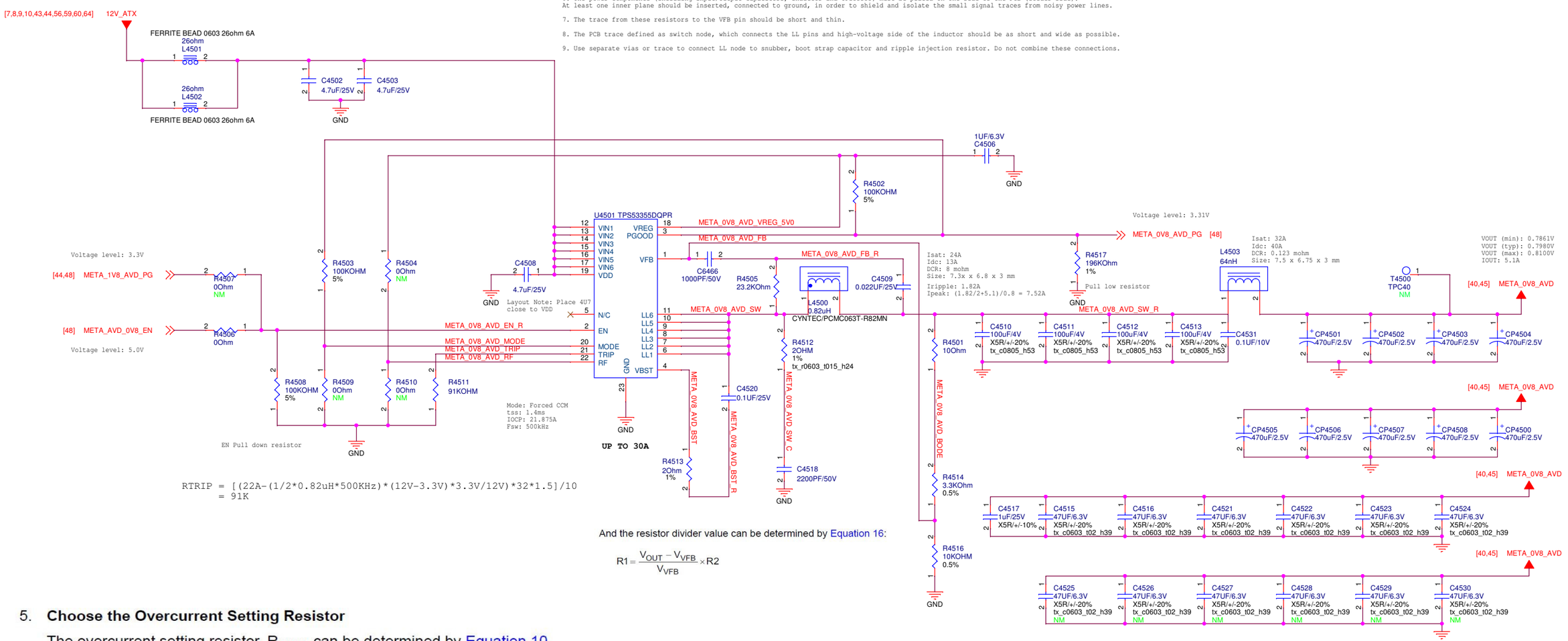
5. All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LLx, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.

6. The power components (including input/output capacitors, inductor and TPS53355) must be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.

7. The trace from these resistors to the VFB pin should be short and thin.

8. The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor should be as short and wide as possible.

9. Use separate vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.




RTRIP = [(22A-(1/2*0.82uH*500KHz)*(12V-3.3V)*3.3V/12V)*32*1.5]/10
= 91K

And the resistor divider value can be determined by Equation 16:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2$$

## 5. Choose the Overcurrent Setting Resistor

The overcurrent setting resistor, $R_{TRIP}$, can be determined by Equation 10.

$$R_{TRIP}(k\Omega) = \frac{\left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}}\right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}\right) \times 32 \times R_{DS(on)}(m\Omega)}{I_{TRIP}(\mu A)} \quad (10)$$

where

- $I_{TRIP}$ is the TRIP pin sourcing current (10 µA)
- $R_{DS(on)}$ is the thermally compensated on-time resistance value of the low-side MOSFET

Use an $R_{DS(on)}$ value of 1.5 mΩ for an overcurrent level of approximately 30 A. Use an $R_{DS(on)}$ value of 1.7 mΩ for overcurrent level of approximately 10 A.

**Table 7-3. Soft-Start and MODE Settings**

| MODE SELECTION | ACTION | SOFT-START TIME (ms) | $R_{MODE}$ (kΩ) |
|---|---|---|---|
| Auto Skip | Pull down to GND | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |
| Forced CCM(1) | Connect to PGOOD | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor $R_{MODE}$.

| LOGIC THRESHOLD AND SETTING CONDITIONS | | | | |
|---|---|---|---|---|
| $V_{EN}$ | EN Voltage | Enable | 1.8 | V |
| | | Disable | 0.6 | |
| $I_{EN}$ | EN Input current | $V_{EN}$ = 5 V | 1.0 | µA |

**6.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage range | VIN (main supply) | 1.5 | 15 | V |
| | VDD | 4.5 | 25 | |
| | VBST | 4.5 | 28 | |
| | VBST (with respect to LL) | 4.5 | 6.5 | |
| | EN, TRIP, VFB, RF, MODE | –0.1 | 6.5 | |
| Output voltage range | LL | –1 | 22 | V |
| | PGOOD, VREG | –0.1 | 6.5 | |

| | | | | | |
|---|---|---|---|---|---|
| $V_{VFB}$ | VFB regulation voltage | CCM condition(1) | | 0.6 | V |
| $V_{VFB}$ | VFB regulation voltage | $T_A$ = 25°C | 0.597 | 0.6 | 0.603 | V |
| | | 0°C ≤ $T_A$ ≤ 85°C | 0.5952 | 0.6 | 0.6048 | |
| | | –40°C ≤ $T_A$ ≤ 85°C | 0.594 | 0.6 | 0.606 | |

**Table 7-1. Resistor and Switching Frequency**

| RESISTOR ($R_{RF}$) CONNECTIONS | | SWITCHING FREQUENCY ($f_{SW}$) (kHz) |
|---|---|---|
| VALUE (kΩ) | CONNECT TO | |
| 0 | GND | 250 |
| 187 | GND | 300 |
| 619 | GND | 400 |
| OPEN | n/a | 500 |
| 866 | VREG | 650 |
| 309 | VREG | 750 |
| 124 | VREG | 850 |
| 0 | VREG | 970 |

<Core Design>

PEGATRON CORP. Title : META DX1 0V8 AVD POWER

Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| C | Endeavor | X00 |

Date: Wednesday, July 31, 2024 Sheet 45 of 64

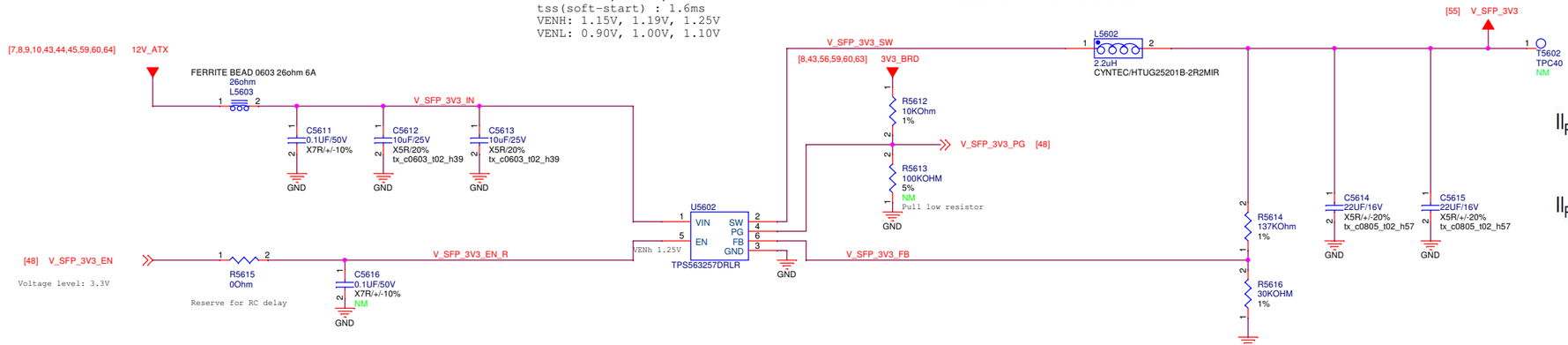
# SFP POWER

FCCM MODE
IMAX: 3A
FSW: 1.2MHz
VFB: 591mV, 600mV, 609mV
tss(soft-start) : 1.6ms
VENH: 1.15V, 1.19V, 1.25V
VENL: 0.90V, 1.00V, 1.10V

Isat: 3.7A
Idc: 3.3A
DCR: 80mohm
Size: 2.5 x 2.0 x 1.2 mm

Iripple: 0.91A
Ipeak: (0.91/2+1.3)/0.8 = 2.2A

VOUT (min): 3.2529V
VOUT (typ): 3.34V
VOUT (max): 3.429V
IOUT: 1.3A




$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}}$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2}$$

<Core Design>

PEGATRON Title : BLANK

PEGATRON CORP. Engineer: Max Chang

| Size | Project Name | Rev |
|---|---|---|
| A2 | Endeavor | 2.0 |

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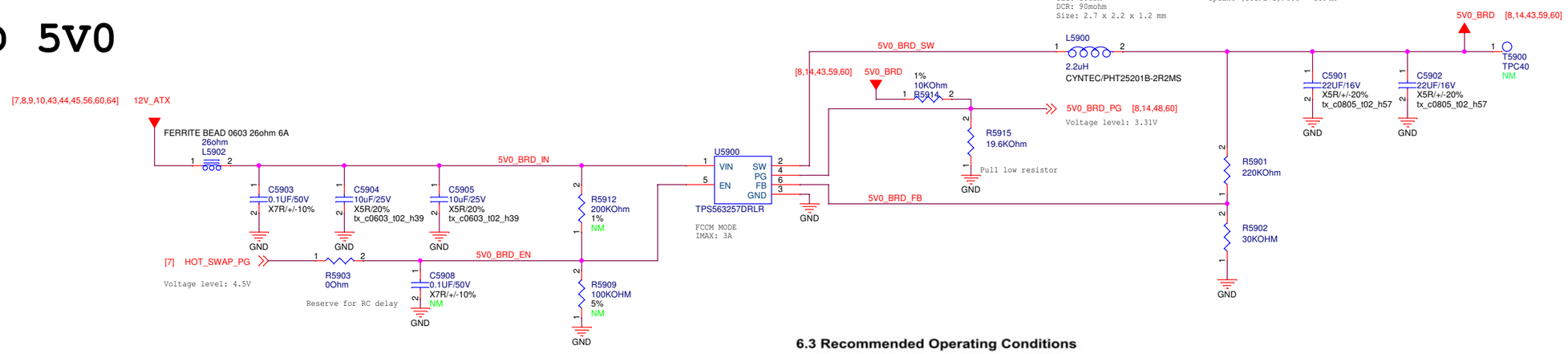
# POWER BOARD 5V0



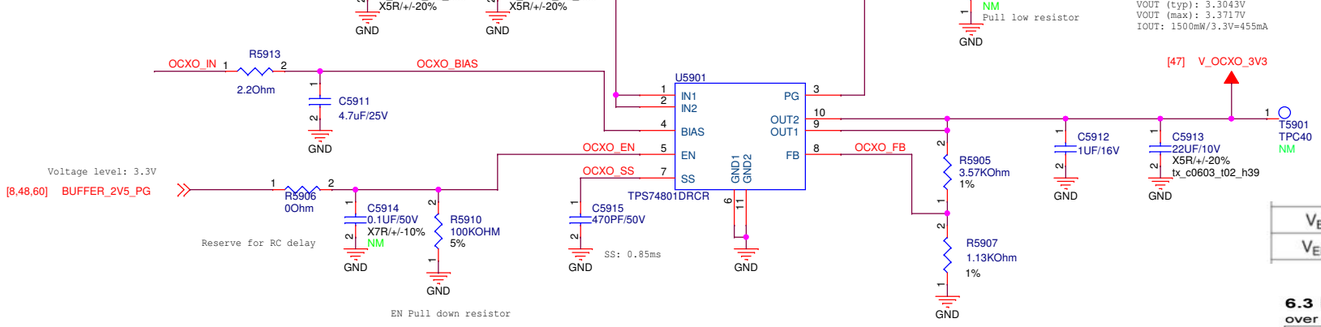

| LOGIC THRESHOLD | | | | | | |
|---|---|---|---|---|---|---|
| $V_{ENH}$ | EN threshold high level | Rising enable threshold | 1.15 | 1.19 | 1.25 | V |
| $V_{ENL}$ | EN threshold low level | Falling disable threshold | 0.90 | 1.00 | 1.10 | V |
| $V_{ENHYS}$ | EN hystersis | Hysteresis | | 190 | | mV |
| $R_{EN}$ | EN pulldown resistor | | | 2 | | MΩ |

**6.3 Recommended Operating Conditions**

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pin voltage | VIN | 3 | | 17 | V |
| | FB, EN, PG | –0.1 | | 5.5 | |
| | GND | –0.1 | | 0.1 | |
| | SW | –1 | | 17 | |
| | SW (transient < 20 ns) | –5 | | 18 | |
| Output current | $I_{OUT}$ | 0 | | 3 | A |

# OCXO POWER 3V3



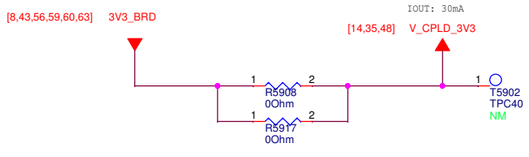

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{EN, HI}$ | Enable input high level | | 1.1 | | 5.5 | V |
| $V_{EN, LO}$ | Enable input low level | | 0 | | 0.4 | V |

**6.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | $V_{OUT} + V_{DO}$ ($V_{IN}$) | $V_{OUT}$ + 0.3 | 5.5 | V |
| $V_{EN}$ | Enable supply voltage | | $V_{IN}$ | 5.5 | V |
| $V_{BIAS}$ [(1)] | BIAS supply voltage | $V_{OUT} + V_{DO}$ ($V_{BIAS}$)[(2)] | $V_{OUT}$ + 1.6[(2)] | 5.5 | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 3.3 | V |

# CPLD POWER 3V3




| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference (Adj.) | $T_J$ = +25°C | 0.796 | 0.8 | 0.804 | V |
| $V_{OUT}$ | Output voltage range | $V_{IN}$ = 5V, $I_{OUT}$ = 1.5A | $V_{REF}$ | | 3.6 | V |
| | Accuracy[(1)] | 2.97V ≤ $V_{BIAS}$ ≤ 5.5V, 50mA ≤ $I_{OUT}$ ≤ 1.5A | –2 | ±0.5 | 2 | % |

<Core Design>

PEGATRON Title : BOARD 5V0/OCXO/CPLD

PEGATRON CORP. Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| C | Endeavor | 2.0 |

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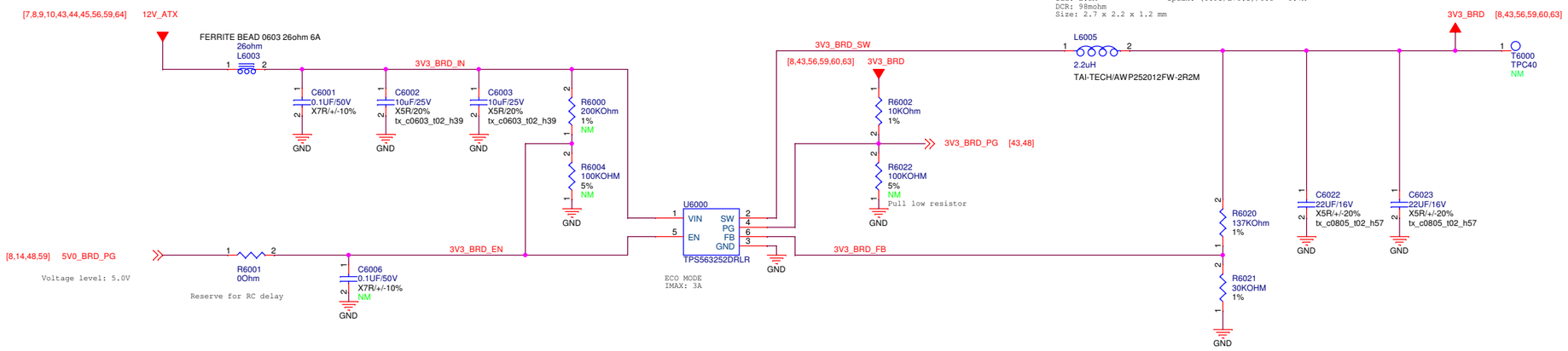
# BOARD 3V3



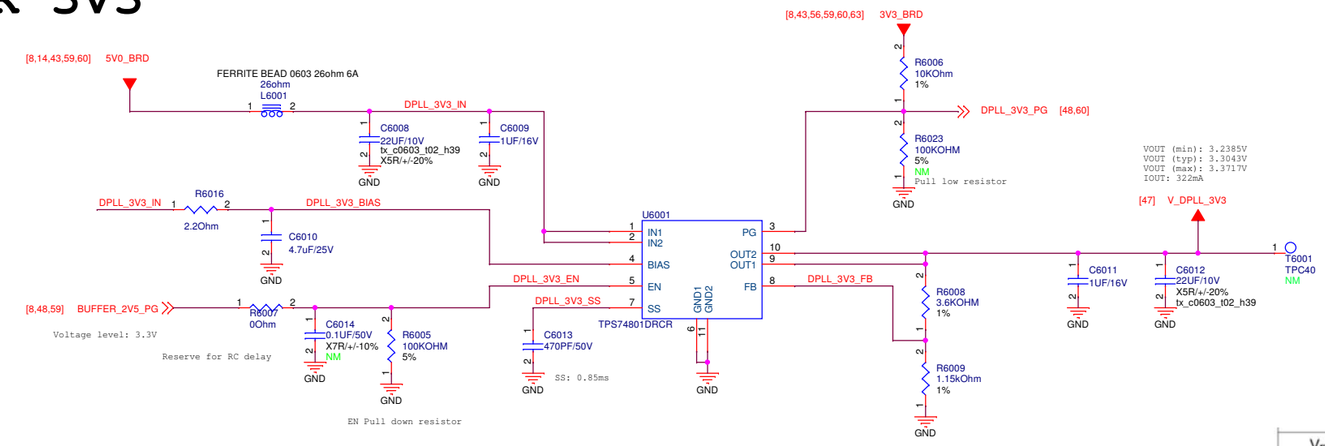

| LOGIC THRESHOLD | | | | | | |
|---|---|---|---|---|---|---|
| $V_{ENH}$ | EN threshold high level | Rising enable threshold | 1.15 | 1.19 | 1.25 | V |
| $V_{ENL}$ | EN threshold low level | Falling disable threshold | 0.90 | 1.00 | 1.10 | V |
| $V_{ENHYS}$ | EN hystersis | Hysteresis | | 190 | | mV |
| $R_{EN}$ | EN pulldown resistor | | | 2 | | MΩ |

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

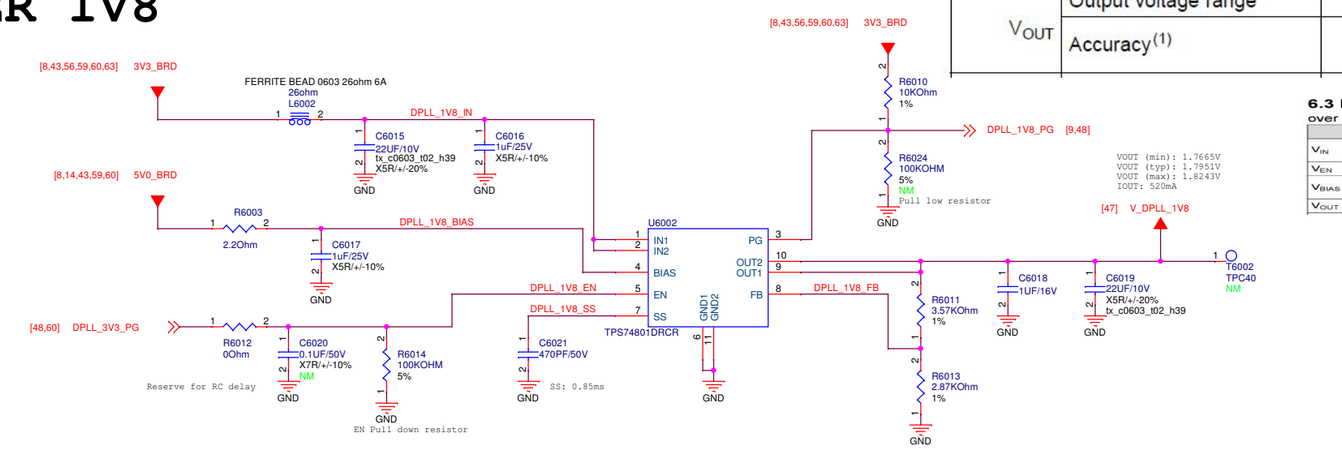
| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pin voltage | VIN | 3 | | 17 | V |
| | FB, EN, PG | –0.1 | | 5.5 | |
| | GND | –0.1 | | 0.1 | |
| | SW | –1 | | 17 | |
| | SW (transient < 20 ns) | –5 | | 18 | |
| Output current | $I_{OUT}$ | 0 | | 3 | A |

# DPLL POWER 3V3




| | | | | | |
|---|---|---|---|---|---|
| $V_{EN, HI}$ | Enable input high level | | 1.1 | | 5.5 | V |
| $V_{EN, LO}$ | Enable input low level | | 0 | | 0.4 | V |

# DPLL POWER 1V8




| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference (Adj.) | $T_J$ = +25°C | 0.796 | 0.8 | 0.804 | V |
| $V_{OUT}$ | Output voltage range | $V_{IN}$ = 5V, $I_{OUT}$ = 1.5A | $V_{REF}$ | | 3.6 | V |
| | Accuracy(1) | 2.97V ≤ $V_{BIAS}$ ≤ 5.5V, 50mA ≤ $I_{OUT}$ ≤ 1.5A | –2 | ±0.5 | 2 | % |

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | $V_{OUT}$ + $V_{DO}$ ($V_{IN}$) | $V_{OUT}$ + 0.3 | 5.5 | V |
| $V_{EN}$ | Enable supply voltage | | $V_{IN}$ | 5.5 | V |
| $V_{BIAS}$ (1)(3) | BIAS supply voltage | $V_{OUT}$ + $V_{DO}$ ($V_{BIAS}$)(2)(3) | $V_{OUT}$ + 1.6(2) | 5.5 | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 3.3 | V |

<Core Design>

PEGATRON Title : BOARD 3V3/DPLL

PEGATRON CORP. Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| A2 | Endeavor | 2.0 |

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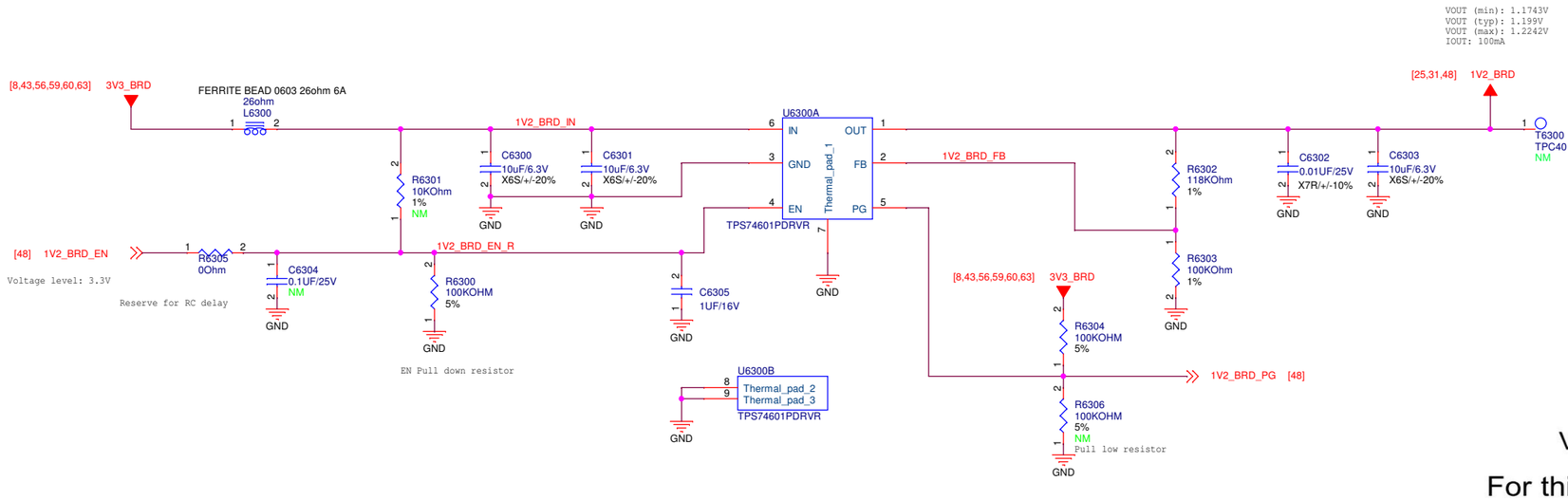
# BOARD 1V2 POWER (CFP2_Buffer_Power level shift)




$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$$

For this device, $V_{FB}$ = 0.55 V.

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{IN}$ | –0.3 | 6.5 | V |
| Enable voltage, $V_{EN}$ | –0.3 | 6.5 | V |
| Power-good, $V_{PG}$ | –0.3 | 6.0 | V |

## 6.5 Electrical Characteristics

at operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF, unless otherwise noted. All typical values at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback voltage | $T_J$ = 25°C | | 0.55 | | V |
| | Output accuracy(1) | $T_J$ = 25°C | –0.7% | | 0.7% | |
| | | –40°C ≤ $T_J$ ≤ +85°C | –1% | | 1% | |
| | | –40°C ≤ $T_J$ ≤ +125°C | –1.5% | | 1.5% | |

| | | | | |
|---|---|---|---|---|
| $V_{EN(HI)}$ | EN pin high voltage | | 1.0 | V |
| $V_{EN(LO)}$ | EN pin low voltage | | 0.3 | V |

<Core Design>

PEGATRON Title : Board 1V2

PEGATRON CORP. Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| C | Endeavor | 2.0 |

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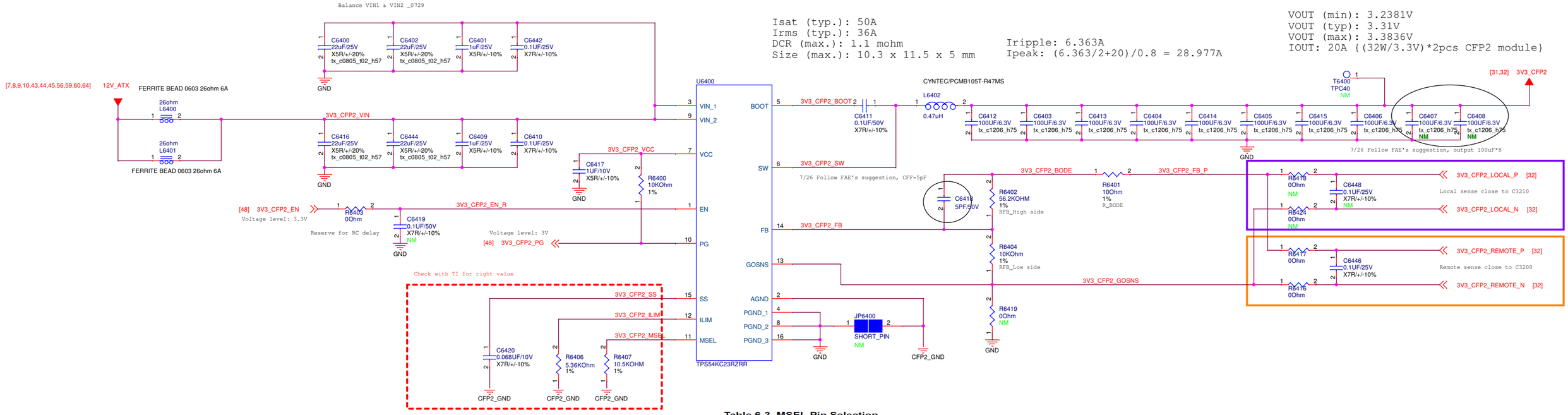
# CFP2 3V3 POWER



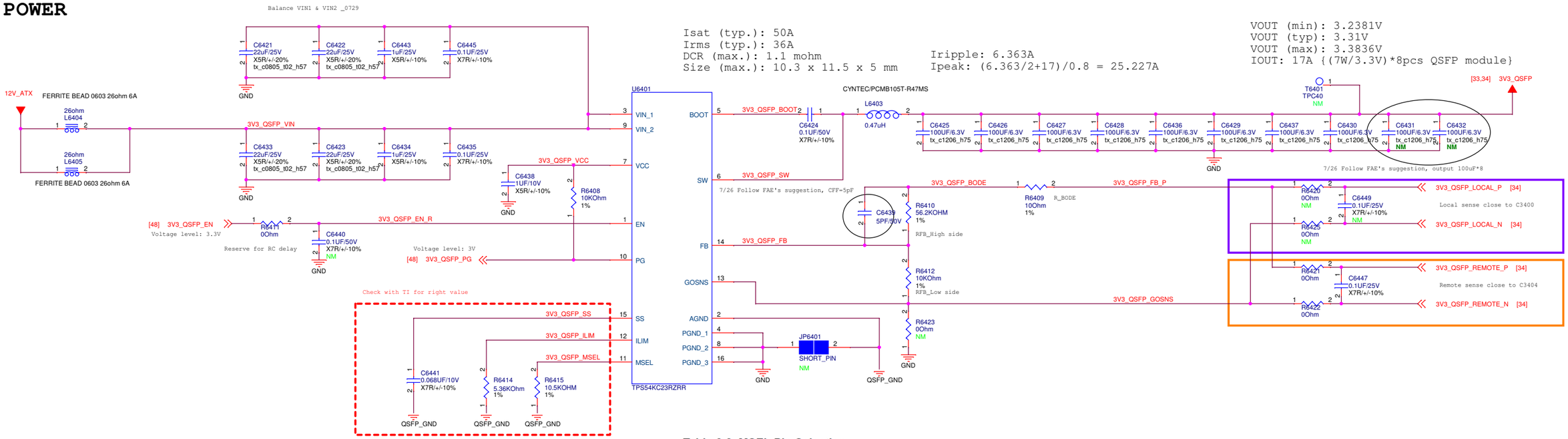

$$R_{ILIM} = \frac{134000}{I_{LIM\_VALLEY}}$$

ILIM_VALLEY (A): 25A
RILIM (KOHM): 5.36K

**Table 6-3. MSEL Pin Selection**

| MSEL PIN RESISTANCE TO AGND (kΩ) | OPERATION MODE UNDER LIGHT LOAD | SWITCHING FREQUENCY ($f_{SW}$) (kHz) (1) | RAMP |
|---|---|---|---|
| 0 (SHORT) | FCCM | 800 | RAMP4 |
| 4.99 | FCCM | 800 | RAMP3 |
| 7.50 | FCCM | 800 | RAMP2 |
| 10.5 | FCCM | 800 | RAMP1 |

# QSFP 3V3 POWER




$$R_{ILIM} = \frac{134000}{I_{LIM\_VALLEY}}$$

ILIM_VALLEY (A): 25A
RILIM (KOHM): 5.36K

**Table 6-3. MSEL Pin Selection**

| MSEL PIN RESISTANCE TO AGND (kΩ) | OPERATION MODE UNDER LIGHT LOAD | SWITCHING FREQUENCY ($f_{SW}$) (kHz) (1) | RAMP |
|---|---|---|---|
| 0 (SHORT) | FCCM | 800 | RAMP4 |
| 4.99 | FCCM | 800 | RAMP3 |
| 7.50 | FCCM | 800 | RAMP2 |
| 10.5 | FCCM | 800 | RAMP1 |

<Core Design>

PEGATRON Title : CFP2 / QSFP Power

PEGATRON CORP. Engineer: Timmy Chien

| Size | Project Name | Rev |
|---|---|---|
| A2 | Endeavor | X00 |

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