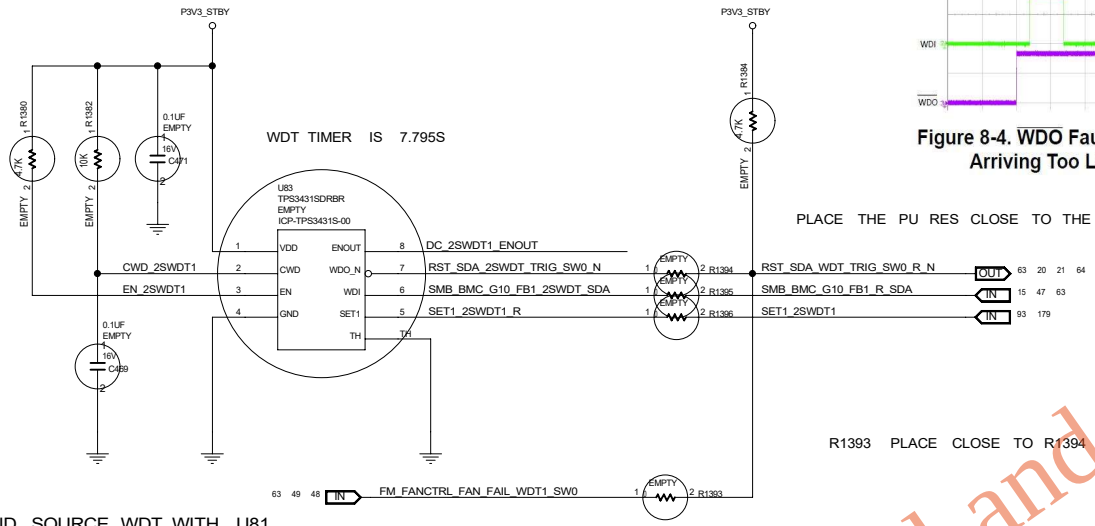
2S WATCHDOG

Figure 8-4. $\overline{WDO}$ Fault Caused by WDI Pulse Arriving Too Late (After $t_{WD(max)}$)

Figure 8-5. $\overline{WDO}$ Fault Caused by missing WDI Pulses Followed by Correct Timing WDI Pulses

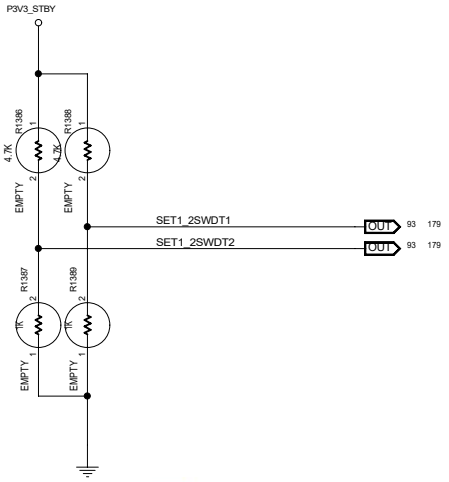


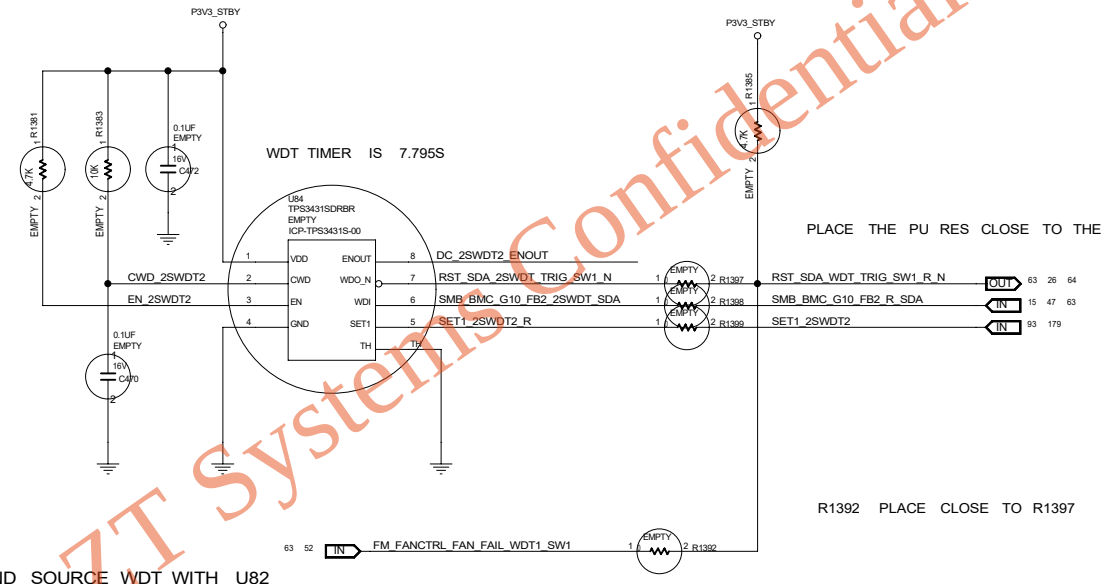
PLACE THE PU RES CLOSE TO THE WDO PIN AS POSSIBLE

R1393 PLACE CLOSE TO R1394

CO-LAYOUT 2ND SOURCE WDT WITH U81

FROM 2ND SOURCE FAN CONTROLLER U55





PLACE THE PU RES CLOSE TO THE WDO PIN AS POSSIBLE

R1392 PLACE CLOSE TO R1397

CO-LAYOUT 2ND SOURCE WDT WITH U82

FROM 2ND SOURCE FAN CONTROLLER U80

$$t_{WD}(ms) = 77.4 \times C_{CWD}(nF) + 55\ (ms)$$

Table 8-2. Programmable CWD Timing

INPUT		WATCHDOG TIMEOUT WDT (t_{WD})[1]			UNIT
CWD	SET1	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			
C_{CWD}	1	t_{WD} × 0.905	t_{WD} Equation 1	t_{WD} × 1.095	ms

(1) Calculated from Equation 1 using an ideal capacitor.

Table 8-3. t_{WD} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
	MIN[1]	TYP	MAX[1]	
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 µF	70096	77455	84814	ms

Table 8-1. Factory Programmed Watchdog Timing

INPUT		STANDARD WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
CWD	SET1	MIN	TYP	MAX	
NC	0	Watchdog disabled			
NC	1	1360	1600	1840	ms
10 kΩ to VDD	0	Watchdog disabled			
10 kΩ to VDD	1	170	200	230	ms